Mandatory Assignment (Handin 1)

1 Introduction

Mandatory assignment. You can see the deadline for timely hand-in on Itslearning.
You must hand in ***a single zipped file*** containing:

- A single document in PDF format (with answers for task A, C, E, F, G) – henceforth just called *the document*.
- Logisim files (with answers for task B, D)

You can only upload ONCE, even if you are working in a group. So, make sure that you:

- ***Write the names of all group members on the front/first page of the document you hand-in.***
- ***List all group members when you upload your hand-in on Itslearning.***

2 Boolean Arithmetic 1

The truth table of some combinational logic can be seen in Table 1

Table 1: Truth table

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

2.1 TASK A

Write down the Arithmetic equation for the logic described in Table 1 and reduce it as much as possible. Put the result in the document.

2.2 TASK B

Implement the circuit in Logisim using AND, OR and inverter gates. Create a Logisim file called ***task_b.circ*** with the designed circuit and insert it in the zip file.

3 Boolean Arithmetic 2

The truth table of some combinational logic can be seen in Table 2

Table 2: Truth table

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3.1 TASK C

Write down the Arithmetic equation for the logic described in Table 2 and reduce it as much as possible. Put the result in the document.

3.2 TASK D

Implement the circuit in Logisim using AND, OR and inverter gates. Create a Logisim file called ***task_d.circ*** with the designed circuit and insert it in the zip file.

4 Sequential Logic

4.1 Data Flip Flop

A high-level triggered latch can be seen on Figure 1.

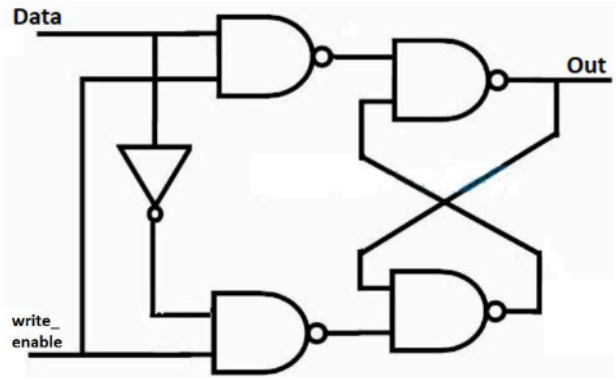

Figure 1 Data Flip Flop (DFF):

4.2 TASK E

Draw the output of the DFF in Figure 1 on Figure 2 below and insert the result in the document.

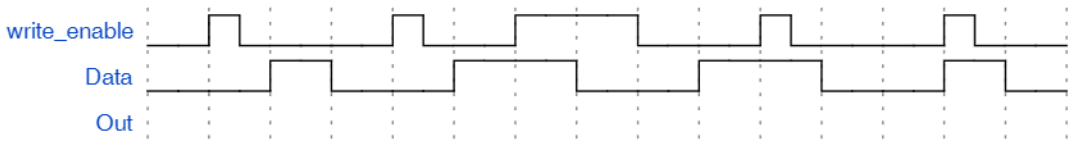

Figure 2: DFF timing diagram

5 CPU

The 8-bit AVR CPU is running a program stored in the memory. The first 3 instructions can be seen in Figure 3.

Address	Opcode	Hint	Explanation
0	1110 0001 0011 1111	Look at page 129 in the AVR instruction set manual	
1	0110 1100 0011 0100	Look at page 106	
2	0111 1010 0011 1100	Look at page 28	

Figure 3: Three instruction, that are fetched and executed by the CPU

The instruction set manual for the AVR processor can be found in the course pages in Itslearning.

5.1 TASK F

Explain what happens in each of the instructions above and write down the value of R19 after each of the instructions. Insert the answers in the document.
(HINT if done correctly register 19 (R19) should contain the value 140 in the end)

5.2 TASK G

Fill out the explanations in the table below. If done correctly R18 contains the value 19 in the end.

Address	Opcode	Hint	Explanation
0	1110 1111 0010 1111	Look at page 129 in the AVR instruction set manual	
1	1110 0001 0110 0100	Look at page 129	
2	0000 1111 0010 0110	Look at page 25	