Lab 3: Combinational Logic Design with Decoders and Multiplexers

Objectives

- To design a combinational circuit and implement it with decoders.
- To design a combinational circuit and implement it with multiplexers.

Apparatus

7404 HEX inverter
7430 8 input NAND gate (x2)
74151 8x1 multiplexer
74154 4-to-16 line decoder

PreLab Questions:

Q1. Design a parity generator by using a 74151 multiplexer. Parity (P) is an extra bit that is added to ensure that the number of bits with the value one in a set of bits is even or odd. For odd parity, the parity bit is set if number of ones in the code is even, otherwise it set to 0. Fill the parity bit (P) column in Table 1 for a 4-bit code (A, B, C, D). Assume odd parity method as it is explained before.

Table 1

Inputs				Parity Bit
A	B	C	D	P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

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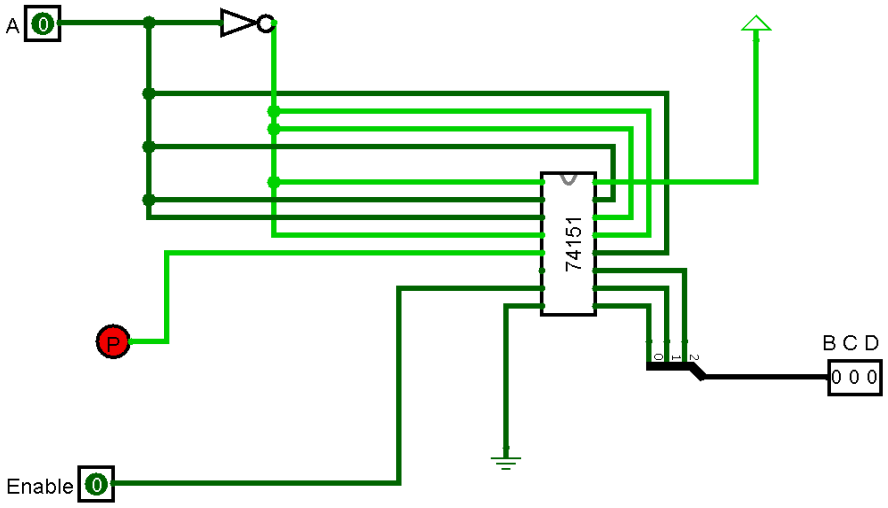

Devrede B C D seçim bit leri olarak belirlenip, sonuç A bit inin bir fonksiyonu şeklinde yazılmıştır. 2x8'lik bir tablo yardımıyla P değerinin 1 çıktığı yerler belirlenidiğinde, 74151 multiplexer ın 0-3-5-6 bağlantılarına A'nın değilinin; 1-2-4-7 bağlantılarına ise A'nın bağlanmasıyla "Odd Partiy Generator" tasarımı gerçekleştirilmiştir.

Q2. Design the parity bit generator circuit defined in Q1. The circuit has four inputs (A, B, C, D) and one output (P). Use one 4 line-to-1 line multiplexer and external gates (if required) in the design.

Hint: If you choose A and B as selection bits, then inputs of the multiplexer will be a function of C and D.

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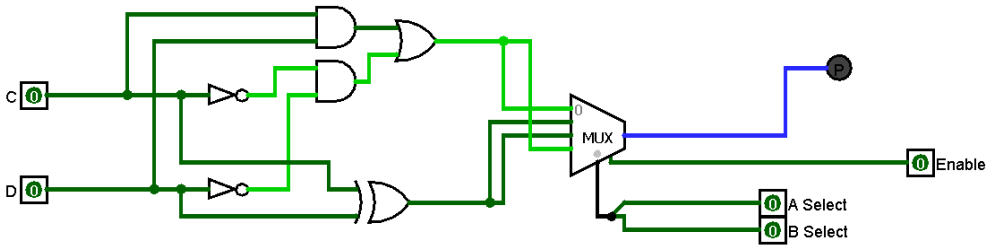

Q1 deki devre dizaynı 4 line-to-1 line multiplexer kullanılarak bu devrede gereçekleştirilmiştir. Devrede A ve B seçim bit i olarak seçilmiştir. Multiplexer daki inputlar ise C ve D'nin bir fonksiyonudur.

Multiplexer ın 0. Ve 3. Input değerleri = CD + $\bar{C}\bar{D}$

Multiplexer ın 1. Ve 2. Input değerleri = C$\bar{D}$ + $\bar{C}$D

Q3. Design a combinational logic circuit by using one 74154 decoder and only NAND gates. The circuit has 2-bit inputs, A and B, and two outputs Z1 and Z2. The circuit operates as follows:

- If A+B is EVEN, Z_1Z_2=01
- If A+B is ODD, Z_1Z_2=10

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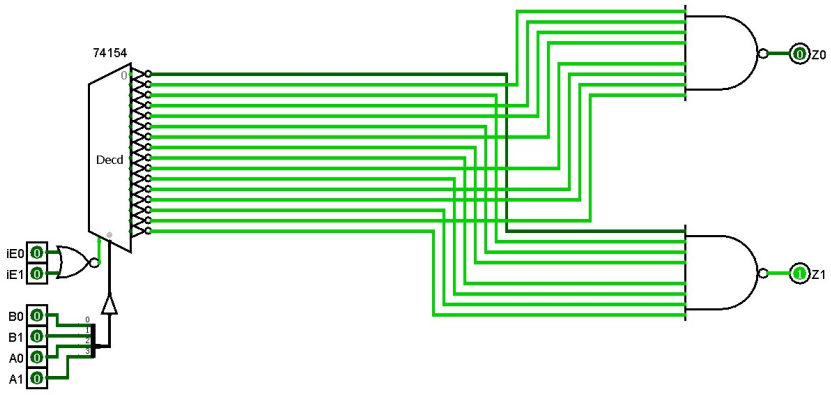
A_1	A_0	B_1	B_0	Z_1	Z_0
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	1



Seçim bit leri olan A_1A_0 ve B_1B_0 toplanarak çıkan sonuca göre Z_1Z_0 belirlenmiştir. Z_1 ve Z_0 için 1 çıkan değerler ayrı ayrı NAND kapısıyla gerçekleştirilip değerlerin doğruluğu devre tasarımıyla gösterilmiştir.

Q4. Design the logic circuit defined in Q3 by using 3-to-8 line decoders and external logic gates.

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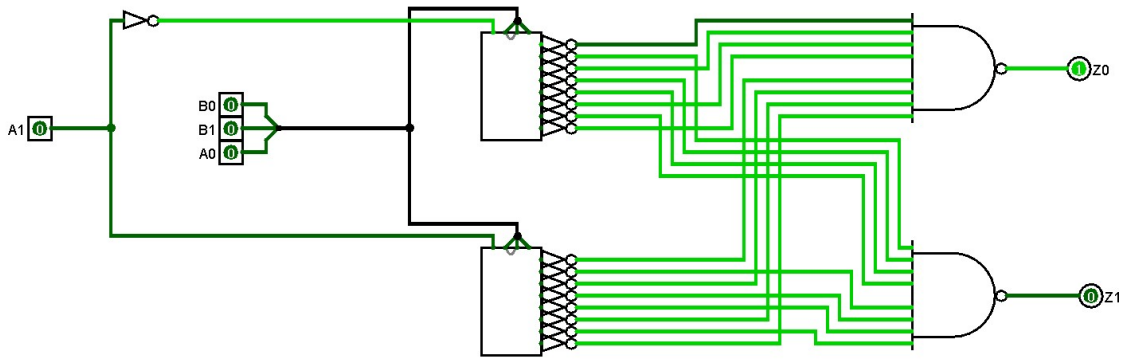

Devre, Q3'deki devrenin iki adet 3x8 decoder kullanılmasıyla tasarlanmıştır. Devrede A_1 enable olarak kullanılmıştır. Bu sayede 0 iken üst taraftaki deceoder 1 iken alt taraftaki decoder çalışmaktadır. B_0 B_1 A_0 bit leri ise seçim bit i olarak kullanılmıştır.

Q5. Test all the designs in Q1, Q2, Q3 and Q4 with the digital circuit simulator Proteus ISIS before lab session, and send the files to your lab assistant.

IC Description:

74151 is a 8 line-to-1 line multiplexer. It has the schematic representation shown in Fig 1. Selection lines A, B and C select the particular input and this input is directed to the output. Strobe S acts as an enable signal. If S =1, the 74151 is disabled and output Y = 0. If S = 0 then the 74151 is enabled and it functions as a multiplexer. Table 2 shows the multiplex function of 74151 in terms of select lines.

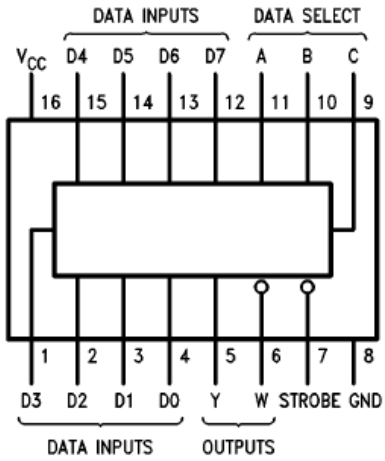

Figure 1

Table 2

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1 . . . D7 = the level of the respective D input

74154 is a 4 line-to-16 line decoder. Fig.2 shows the pin-out for the 74154. This IC decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The function table of IC 74154 is given Table 3.

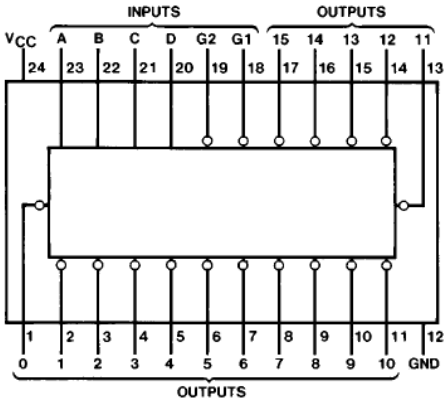

Figure 2

Table 3

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Procedure:

1. Connect the parity generator circuit that you designed in the prelab Q1 and verify the operation of the circuit. Connect an LED to the multiplexer output to observe the state of the parity bit for all possible input combinations.

2. Connect the logic circuit that you designed in the prelab Q3 and test the circuit by applying all possible input combinations.