

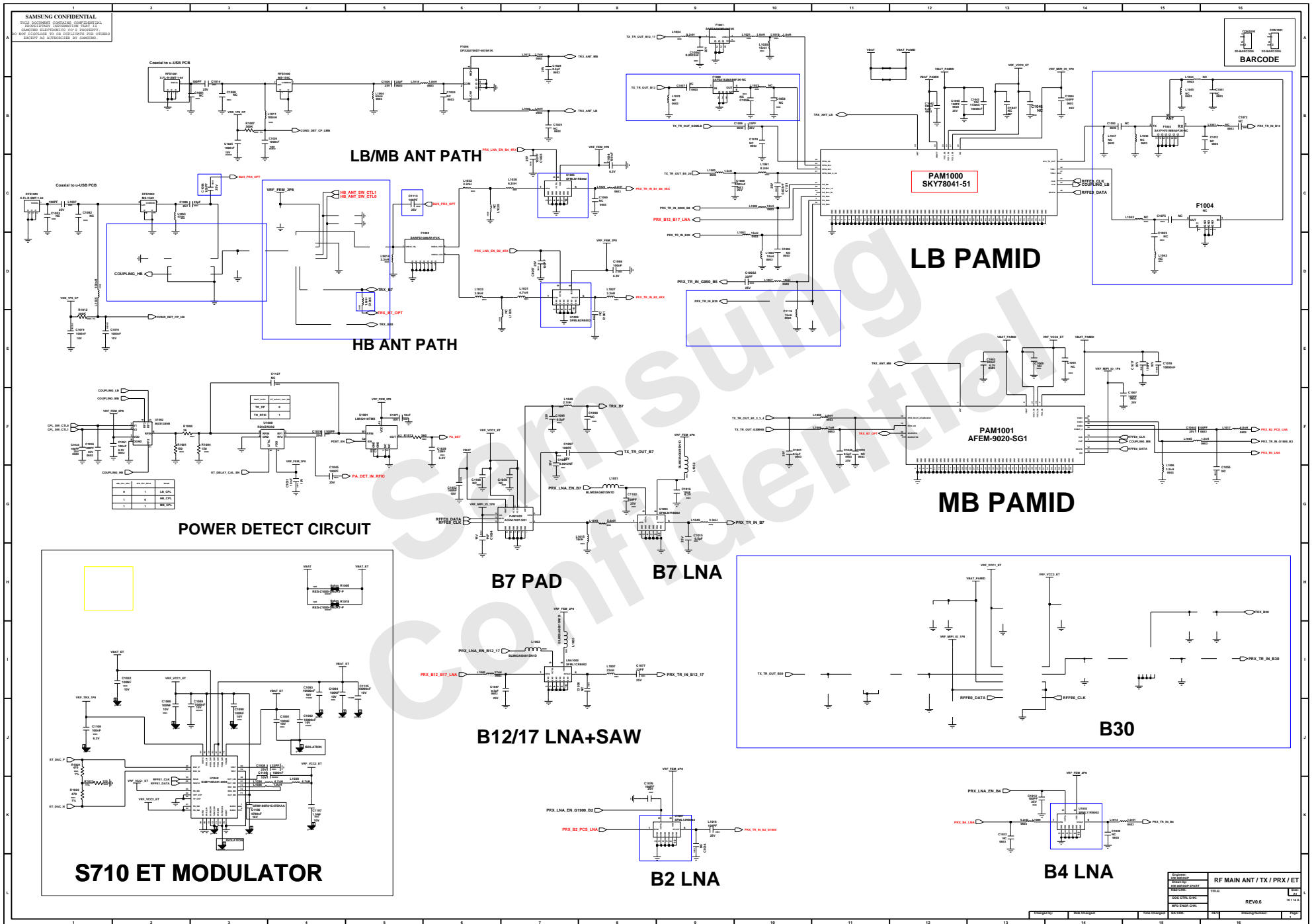


# SM-G928T\_REV0.6

2015.07.03

- sheet01 : GSM / WCDMA / LTE RF
- sheet02 : TRANCEIVER, DRX
- sheet03 : S333, CP\_PMIC
- sheet04 : SENSORS, HUB, GPS, BT/WIFI, NFC
- sheet05 : AP(ISTOR), SIM SOCKET
- sheet06 : AP(ISTOR) POWER PART
- sheet07 : AP PMIC, SUB PMIC, Wireless Charging, MST
- sheet08 : AUDIO, SUB PCB CON.
- sheet09 : CAMERA, DISPLAY, DCDC

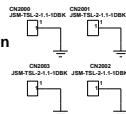
Project	
Sheet No.	
Rev. No.	
Rev. Date	
Rev. Description	
Rev. No.	MAIN_REV0.6
Rev. Date	
Rev. Description	



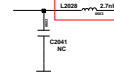
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# RF2

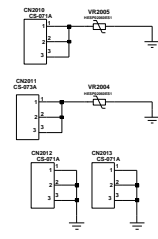
SMR Poron



Coupling pad

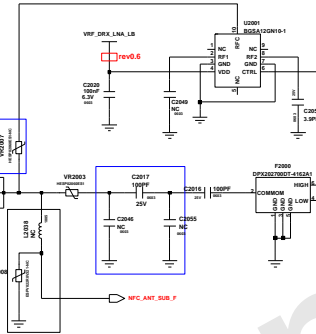


GND Contact



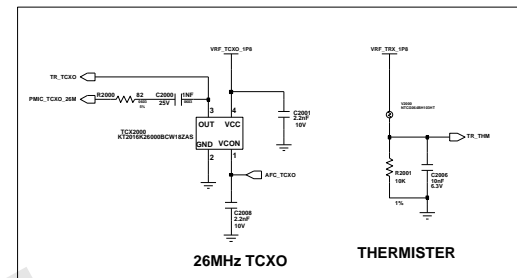
## SUB ANT

## SUB ANT S/W2

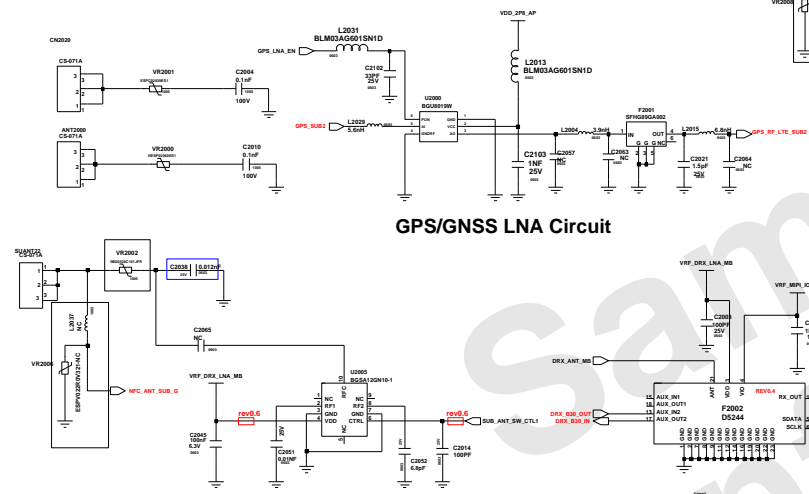


26MHz TCXO

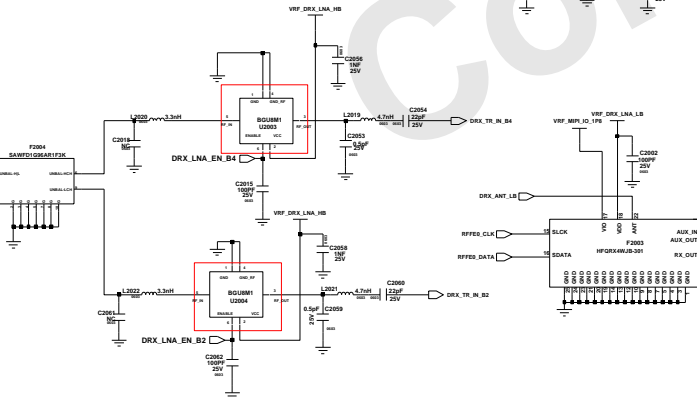
THERMISTOR



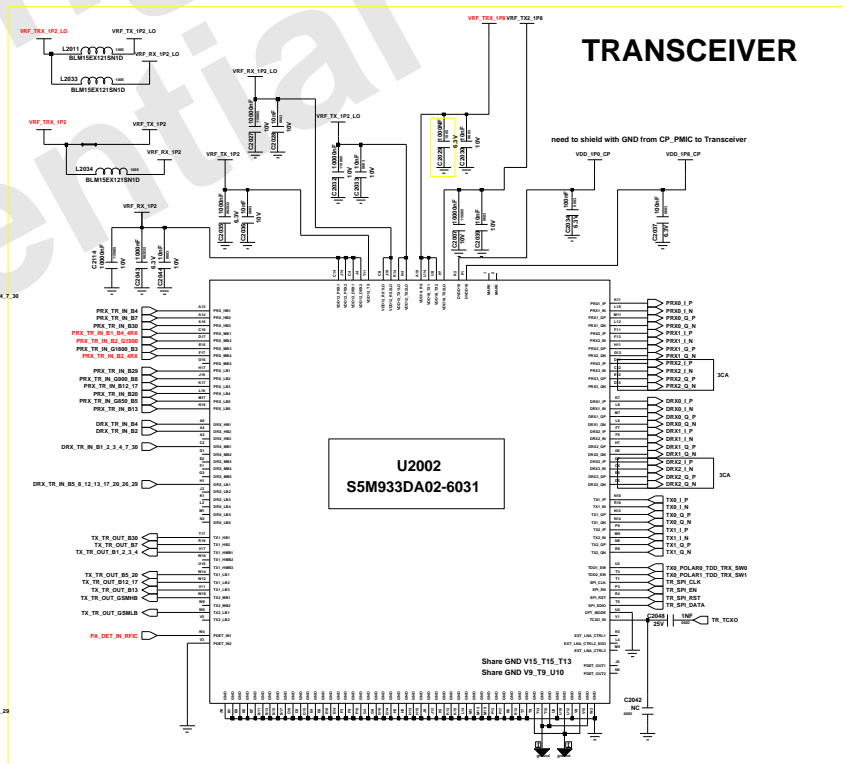
## GPS/GNSS LNA Circuit



## SUB ANT S/W2



## SUB ANT

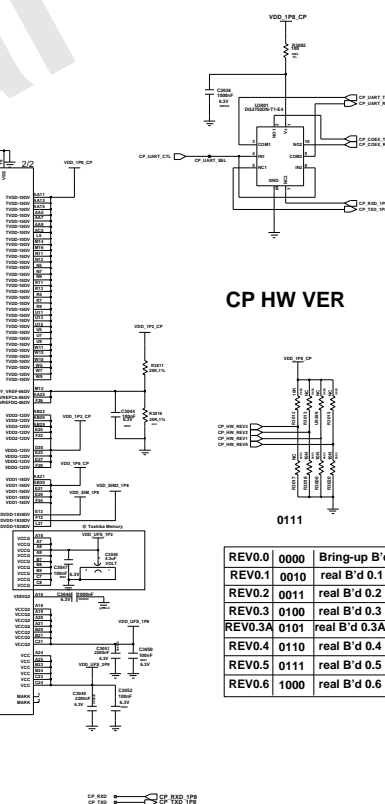
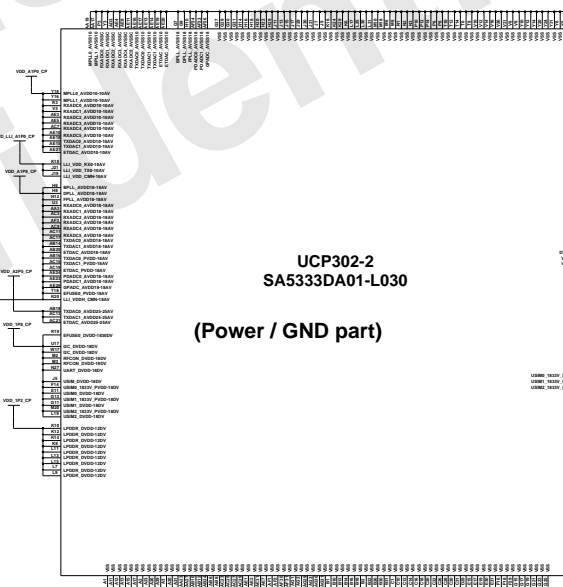
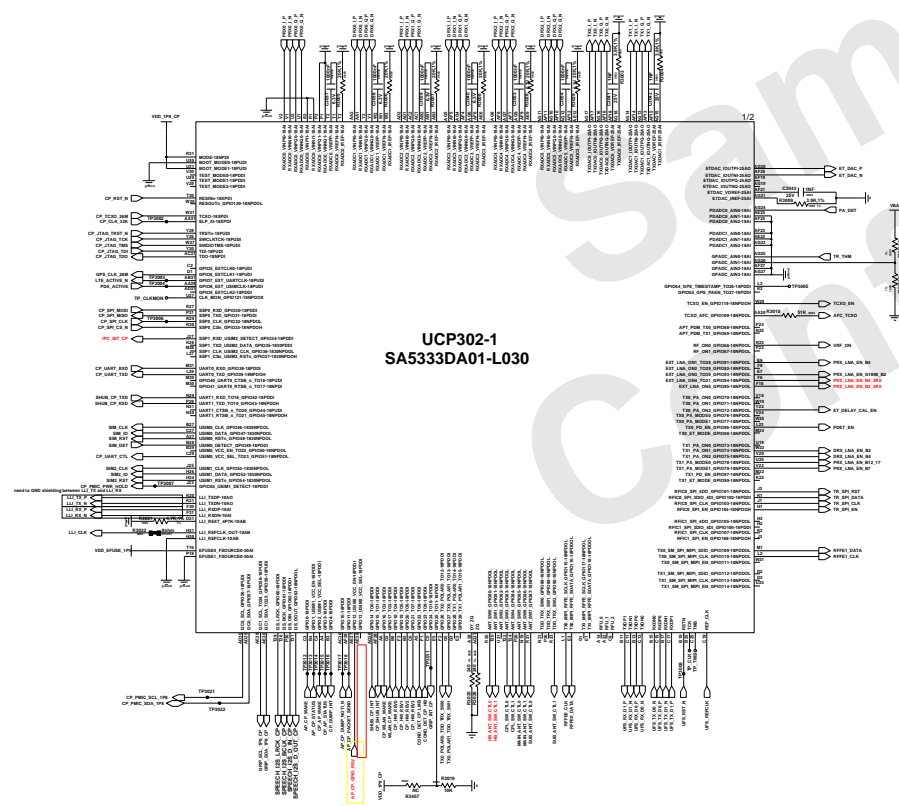
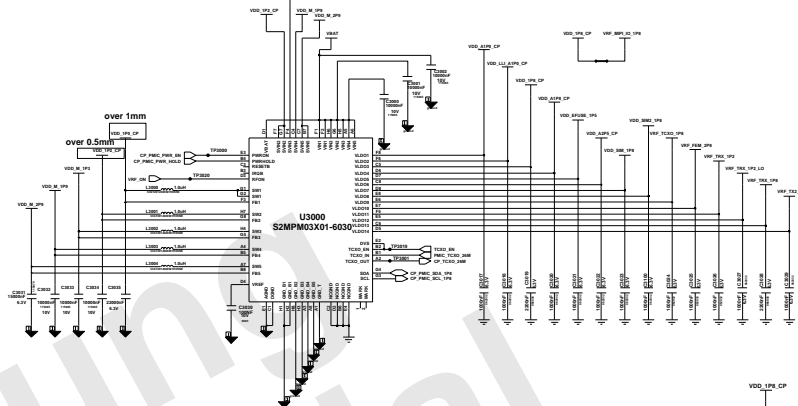


U2002  
S5M933DA02-6031

Engineer	RF DIVERSITY ANT / DRX / RFIC / GPS
Drawn by	
RAD CHK	
DOC CYCL CHK	
MFG ENGR CHK	
REV	REV.0
Drawing Number	
Sheet	

**CP PART (S333)**

### SHANNON333 Bypass capacitors



REV0.0	0000	Bring-up B'
REV0.1	0010	real B'd 0.1
REV0.2	0011	real B'd 0.2
REV0.3	0100	real B'd 0.3
REV0.3A	0101	real B'd 0.3A
REV0.4	0110	real B'd 0.4
REV0.5	0111	real B'd 0.5
REV0.6	1000	real B'd 0.6

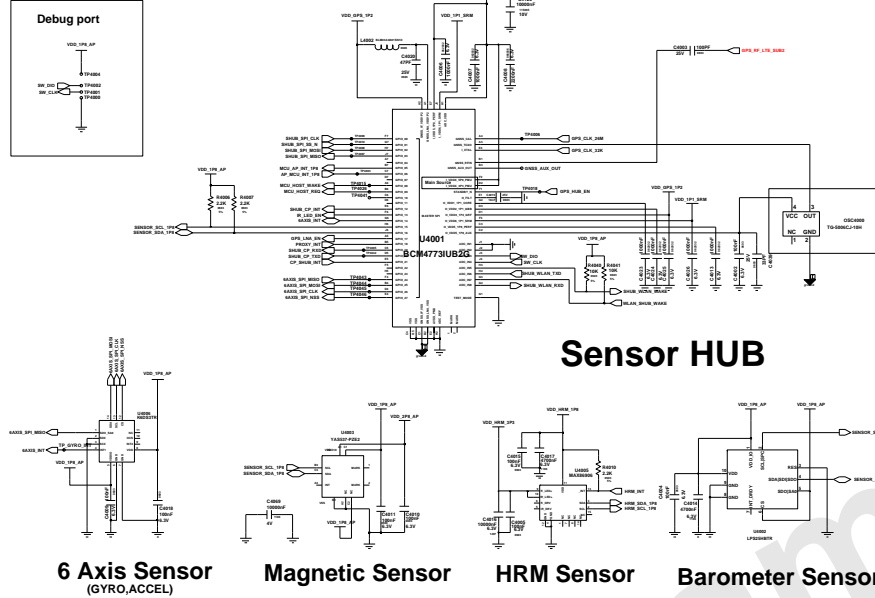
CP JTAG

Engineer:	CP, CP PMIC		
Drawn by:			
PAD CHK:			
DWG CTRL CHK:			
MFG ENG'G CHK:			
QA CHK:	REV:	Issuing Number:	

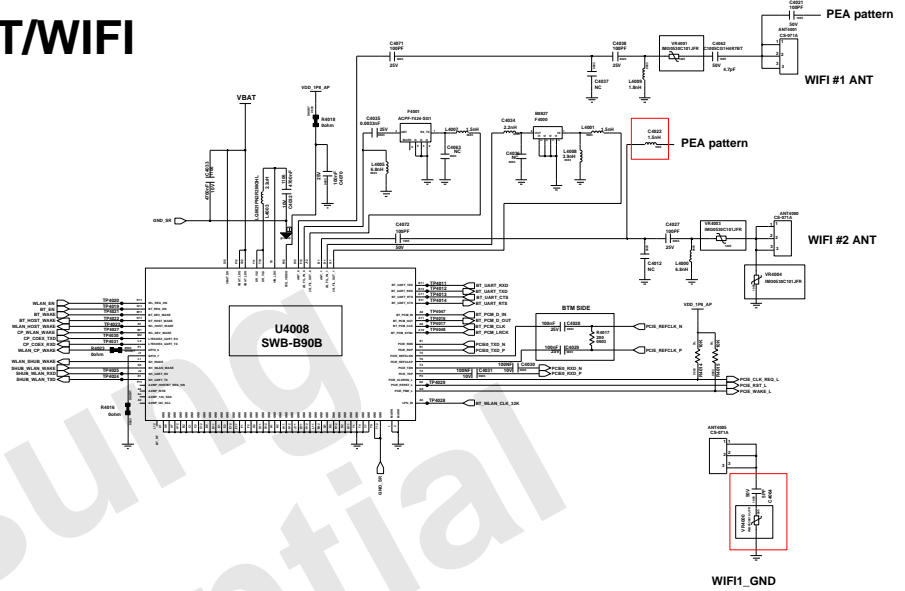
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## SENSORS

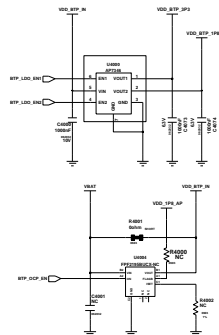
Debug port



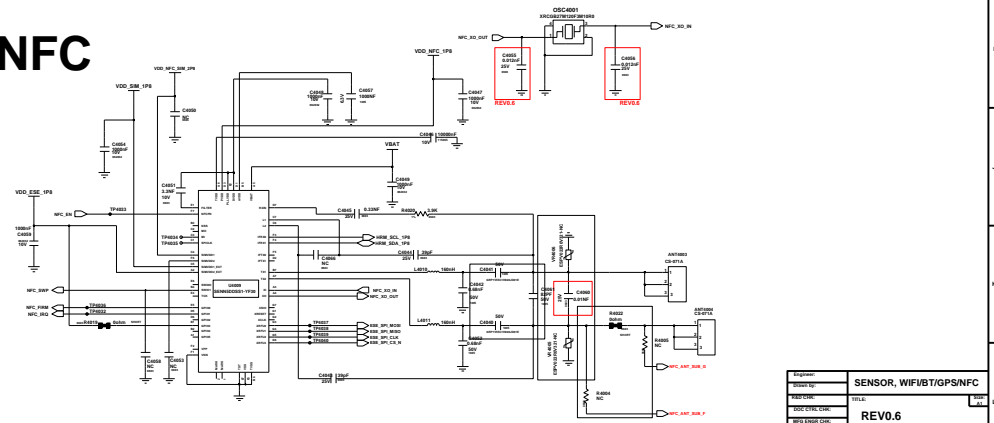
## BT/WIFI



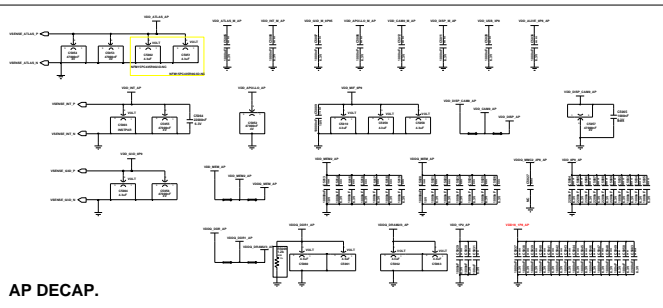
## BTP



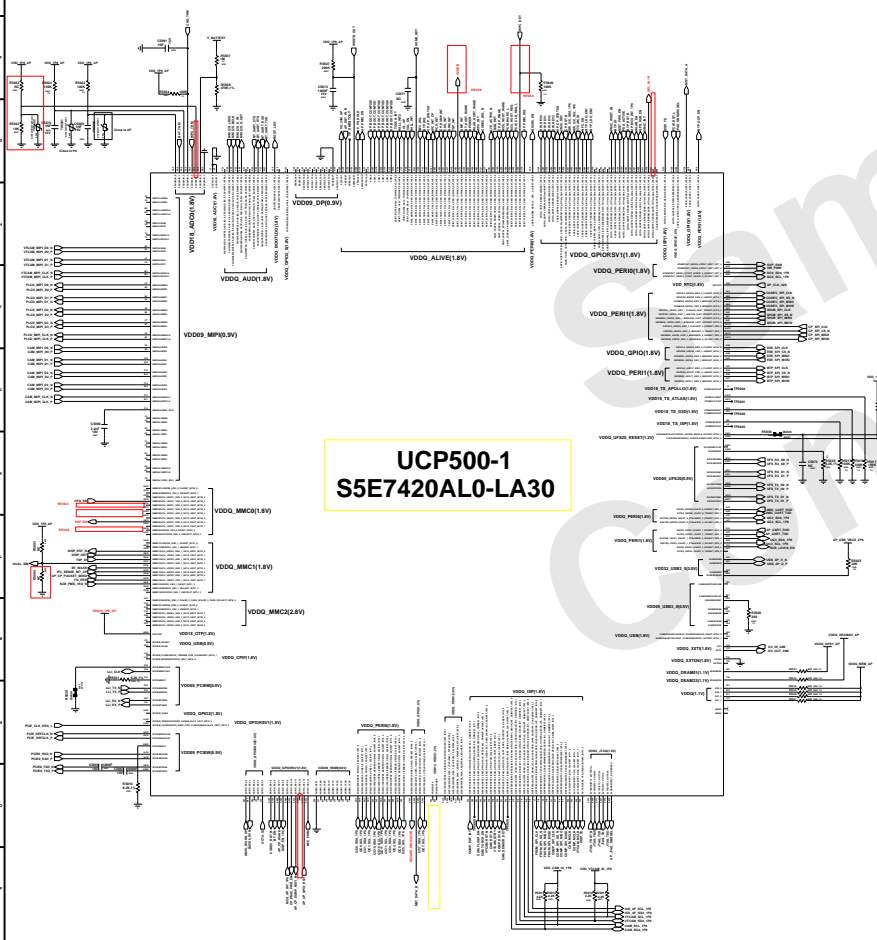
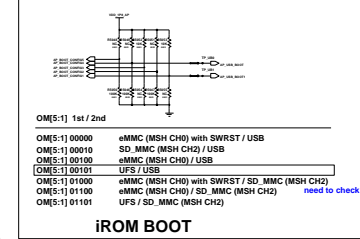
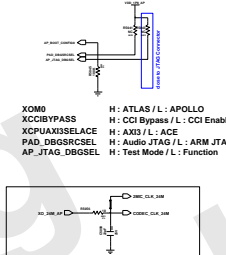
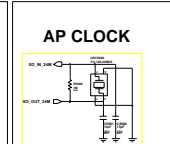
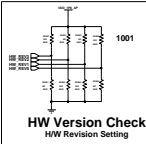
## NFC



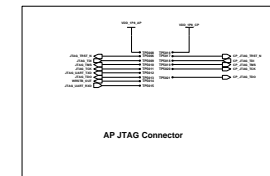
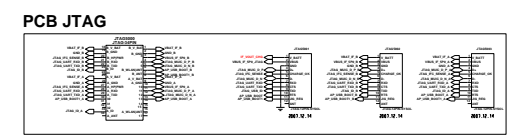
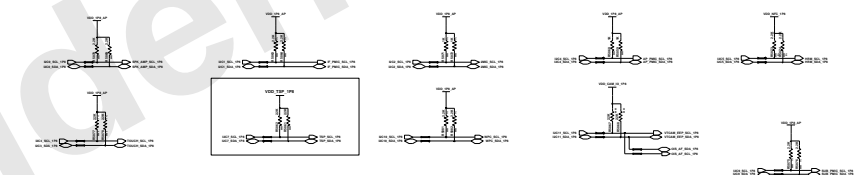
# 4. EXYNOS7420(ISTOR), eMMC



0000	MAIN_REV0.0, bringup
0001	MAIN_REV0.1, 0024
0010	MAIN_REV0.2, 0044
0011	MAIN_REV0.3, 0014
0100	MAIN_REV0.4, 0023
0101	
0110	MAIN_REV0.5, 0006
1001	MAIN_REV0.6, 0015

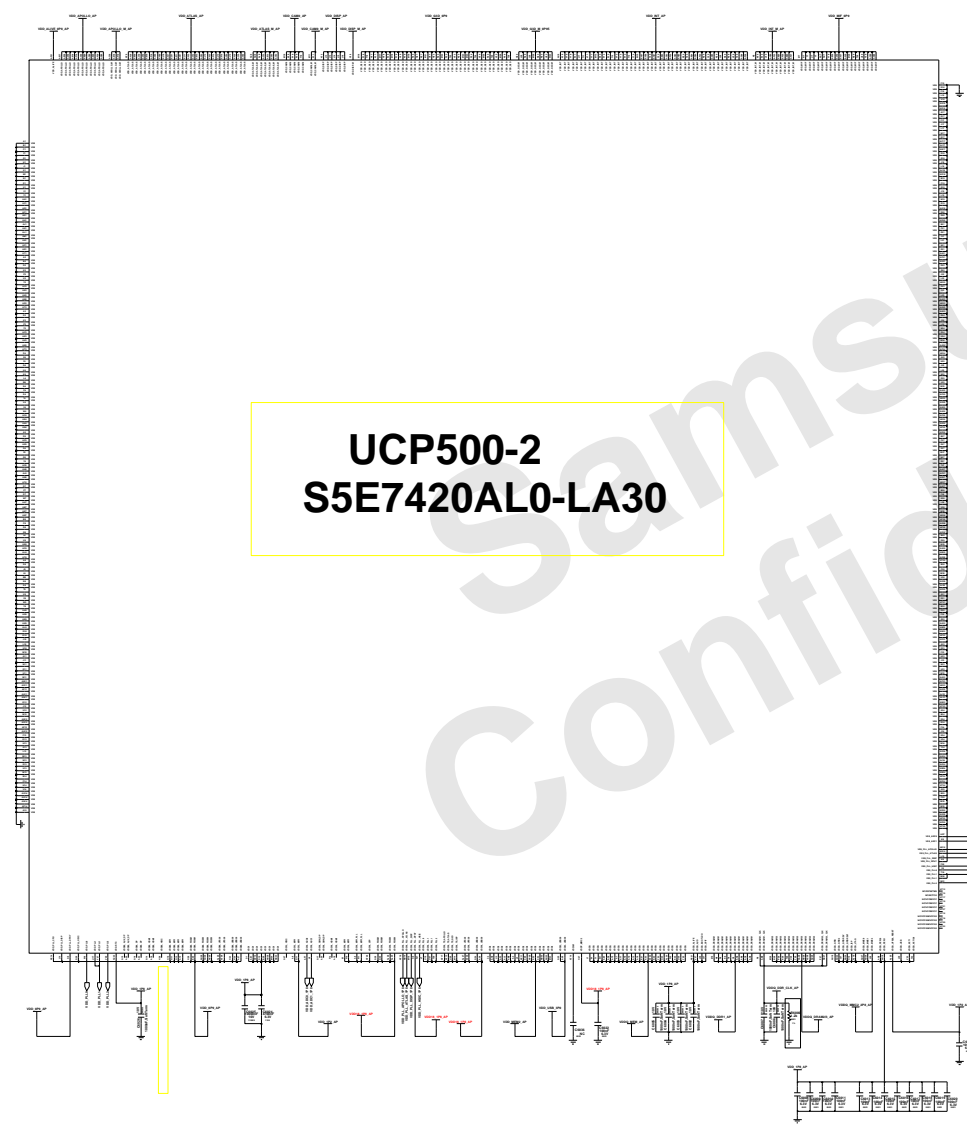


H/W I2C



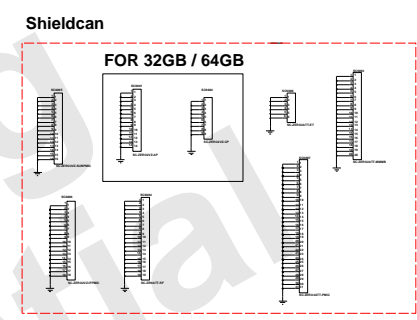
AP JTAG CONNECT
REV0.6

STANDARD CONFIDENTIAL



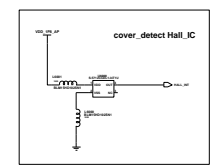
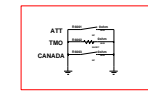
**UCP500-2  
S5E7420AL0-LA30**

32GB / 64 GB : USE SC6008 AND SC6009  
128 GB : USE SC6001

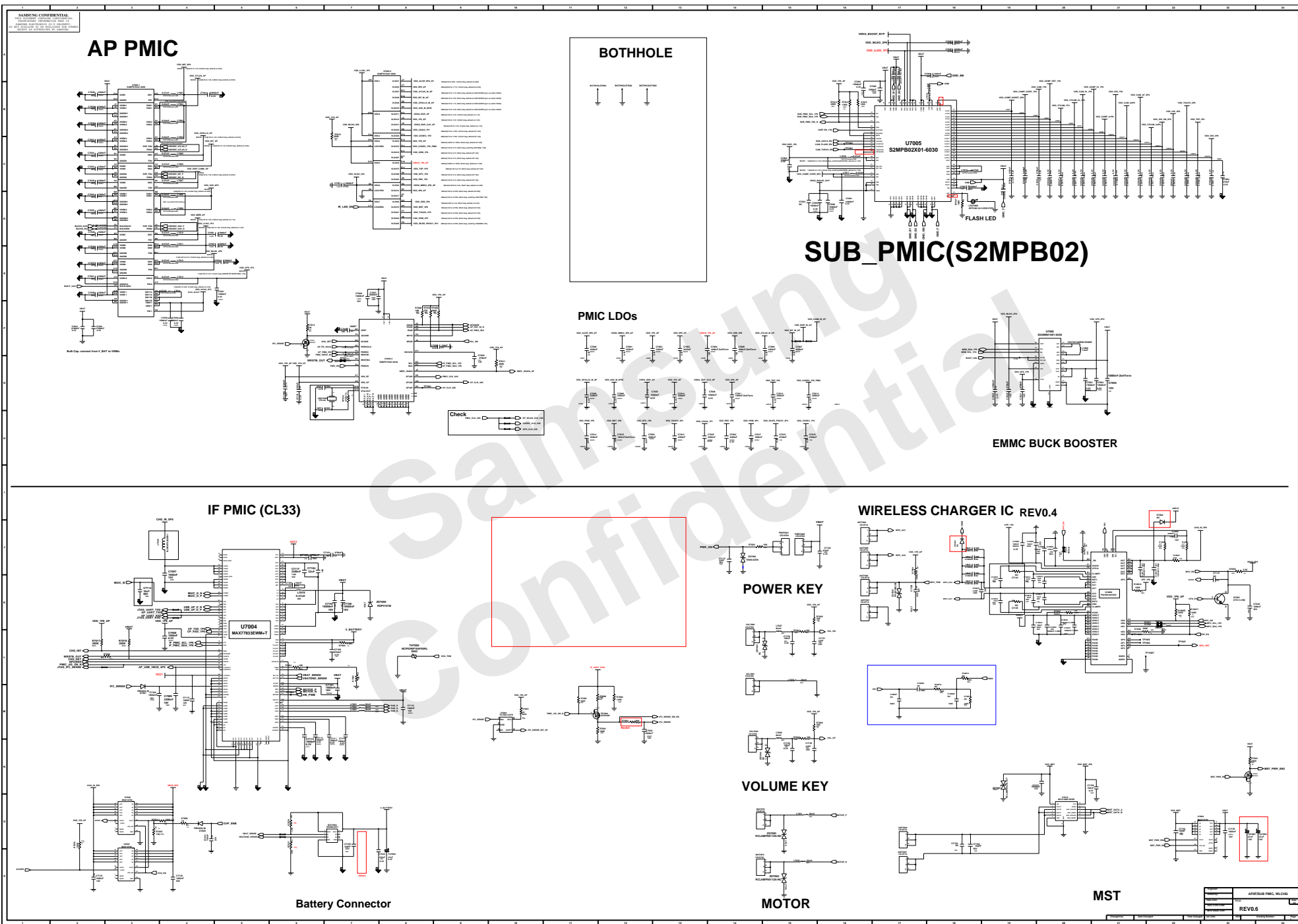


FOR 128GB

PIC-8002501-AP  
GH3-10007A



AP
REV0.6

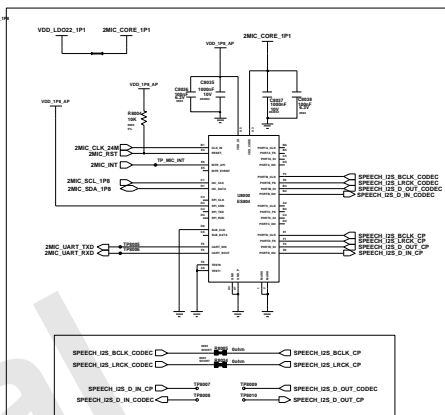




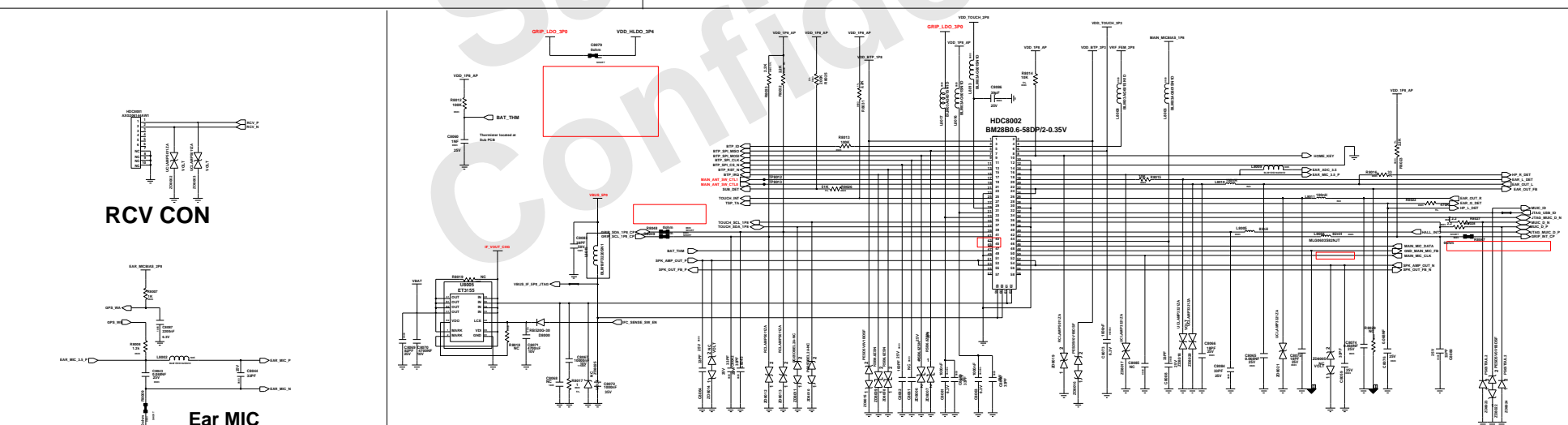
# AUDIO

[illegible]

**SPK AMP**



**2MIC NS(SMD ES804)**



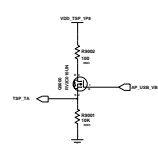
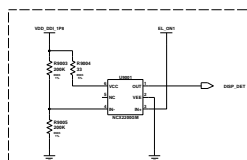
**SUB FPCB IF CONN.**  
(USB2.0 / Main ANT / MIC)

Engineer:	AUDIO, SUB PCB CON.		
DRAWN BY:			
READ CHECK:	TITLE:	Scale:	AS
DOC CTRL CHECK:	REV0.6		
MFG ENG CHG:			
Approved: QA CHECK:	REV	Drawing Number:	Page

# CAMERA

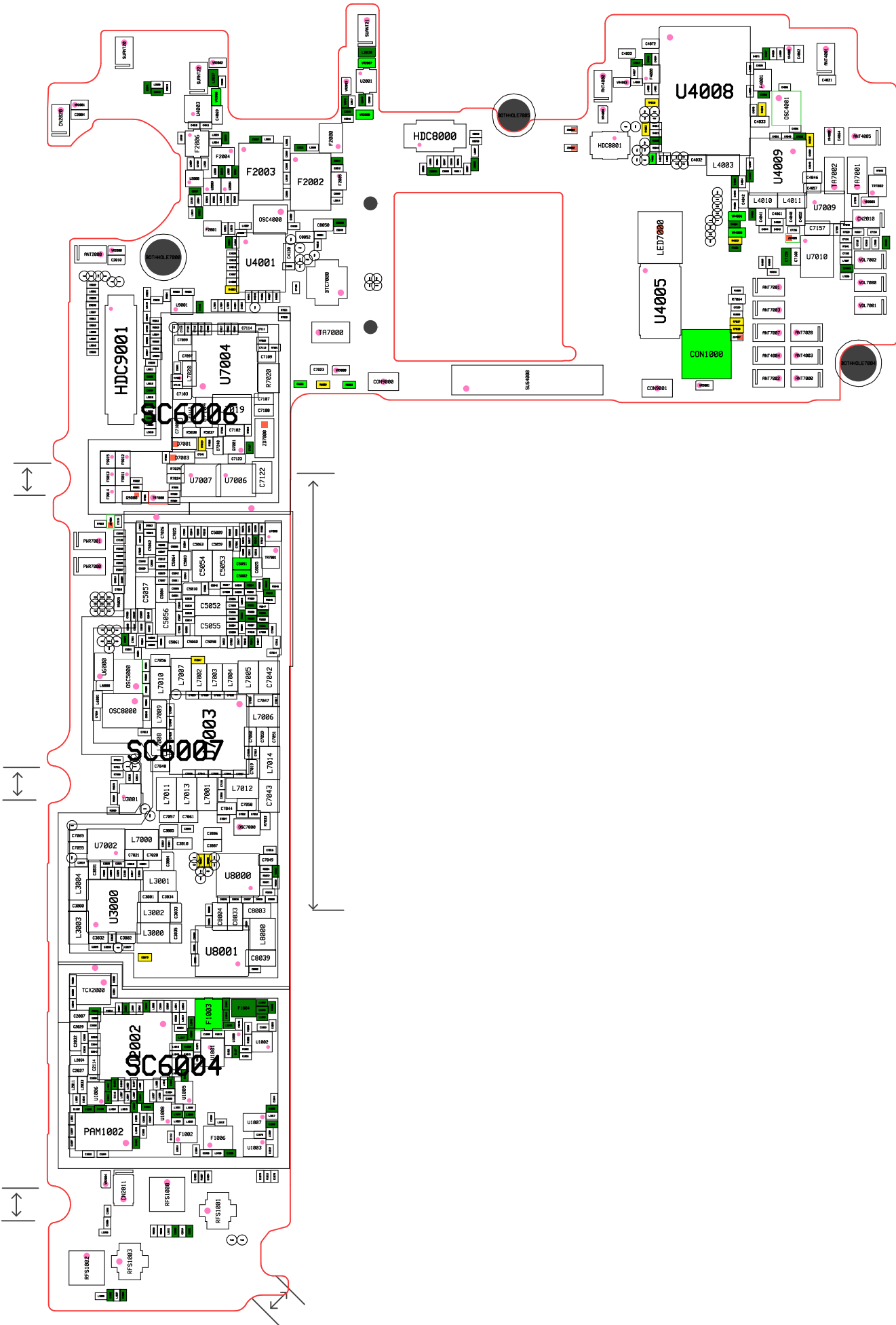


The figure contains three circuit diagrams, each implementing a 2-to-1 multiplexer using a 74VHC00 (NAND gate) and a 74VHC04 (inverter).  
 - The top diagram shows a 2-to-1 multiplexer with inputs Y0 and Y1, select input S, and output Y. It uses a 74VHC00 (NAND gate) and a 74VHC04 (inverter).  
 - The middle diagram shows a 2-to-1 multiplexer with inputs Y0 and Y1, select input S, and output Y. It uses a 74VHC00 (NAND gate) and a 74VHC04 (inverter).  
 - The bottom diagram shows a 2-to-1 multiplexer with inputs Y0 and Y1, select input S, and output Y. It uses a 74VHC00 (NAND gate) and a 74VHC04 (inverter).

user17|swcad17|10.253.45.194|20150703-155808

Model :  
Revision :  
Manufacture Count :  
Charge :  
Contact :  
Date :  
Routing :  
Resin :

# Setup(2015-05-20)\_HHP

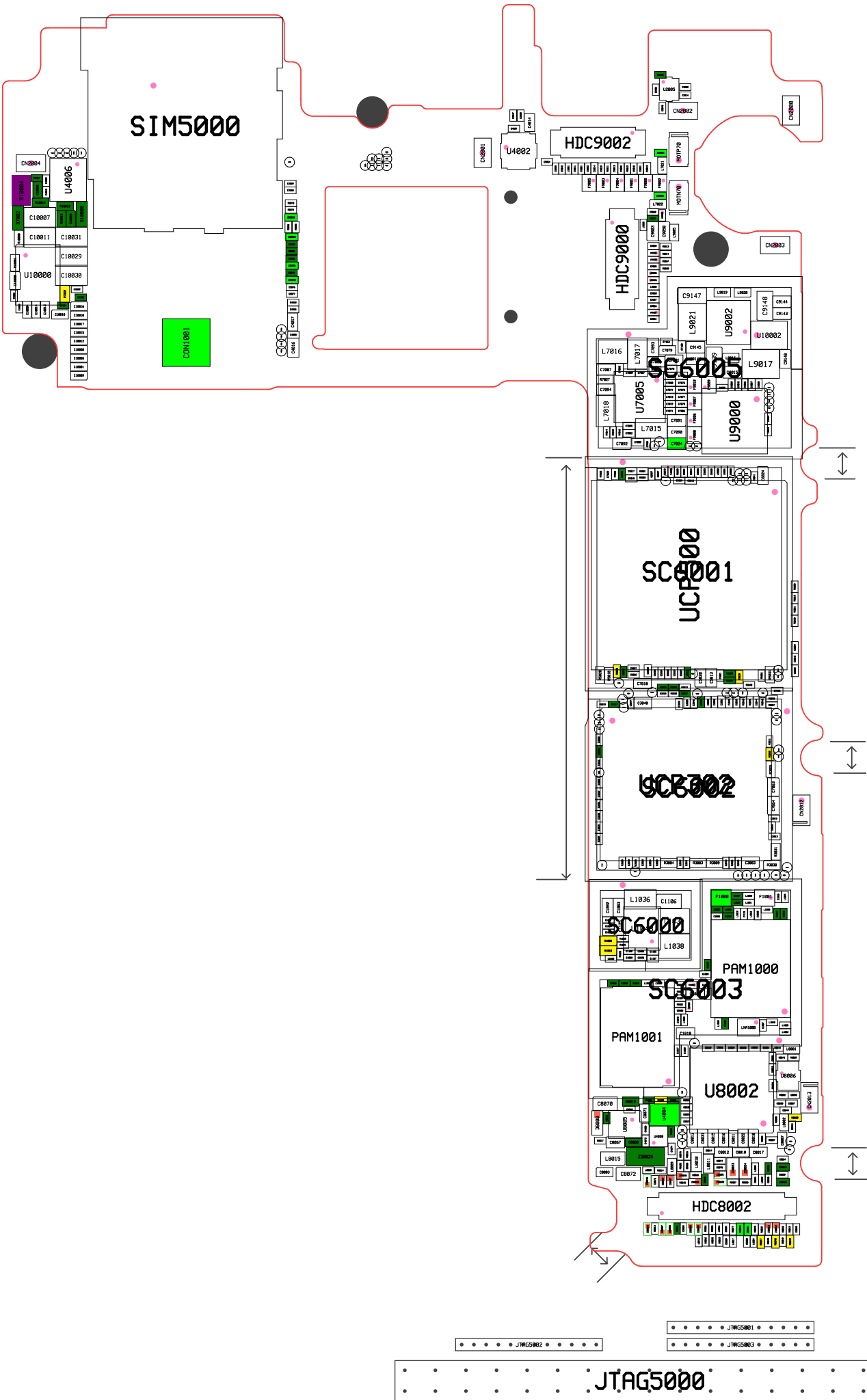


Number of books read	Number of students
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2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	9
11	8
12	7
13	6
14	5
15	4
16	3
17	2
18	1

AON1605(TR7000) : IT'S Wrong Polarity possibility. Check the Pin1  
2007-010848(R10004) : Check! Bottom Surface of Component

Model :  
Revision :  
Manufacture Count :  
Charge :  
Contact :  
Date :  
Routing :  
Resin :

Setup(2015-05-20)\_HHP



AON1605(TR7000) : IT'S Wrong Polarity possibility. Check the Pin1  
2007-010848(R10004) : Check! Bottom Surface of Component