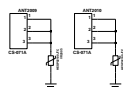


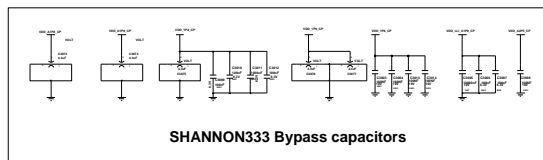
## B GND CONTACT



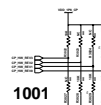
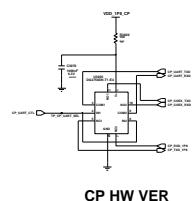
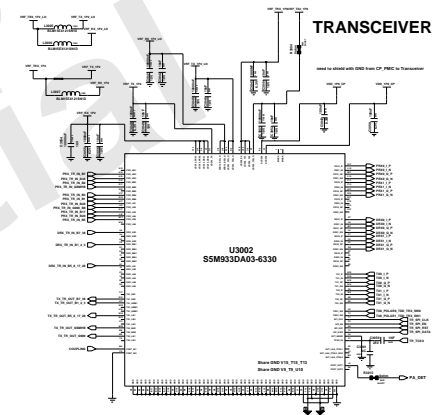
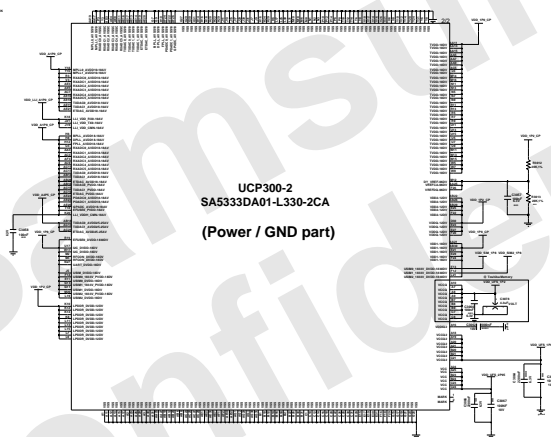
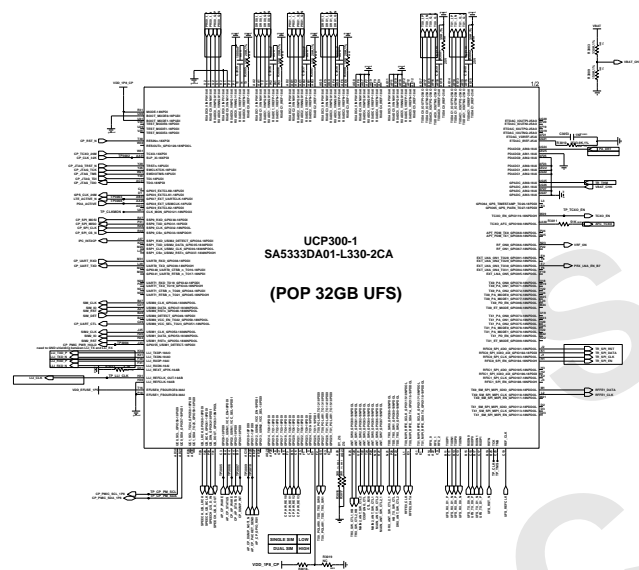
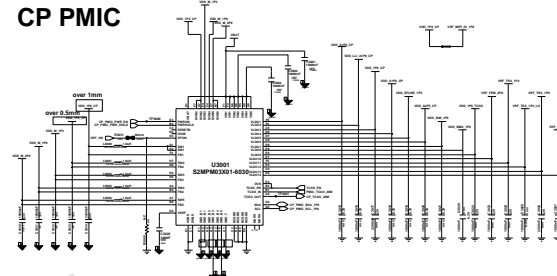
**R GND CONTACT**

Engineer:	RF DRX		
Drawn by:			
R&D CTR:			
DQC CTR, CTR:			
MFG & ASST CTR:	TITLE: A8_ISTOR		
Original	QA CTR:	REV	Issuing Number:

## CP PART (S333)

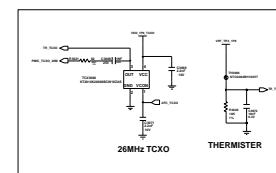


## CP PMIC



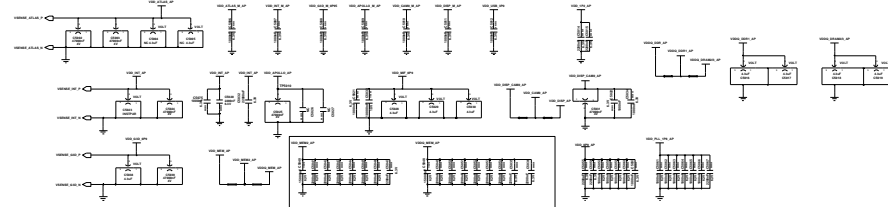
REV0.0	0000
REV0.1	0001
REV0.2	0010
REV1.0A	0011
REV0.3	0100
REV1.0A	0101
REV0.5	1001

## CP JTAG

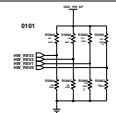




**AP DECAP.**



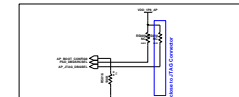
0000	REV0.0
0001	REV0.1
0010	REV0.2
0011	REV0.3
0100	REV0.4
0101	REV0.5



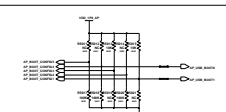
**HW Version Check**  
H/W Revision Setting



## AP CLOCK



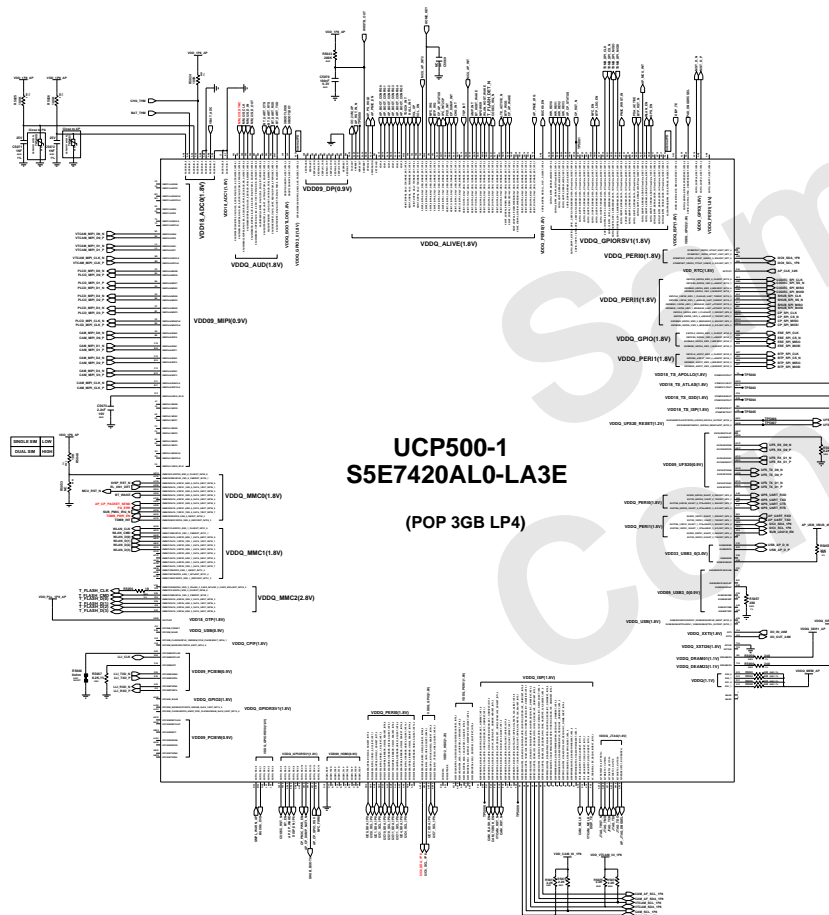
XOM0	H: ATLAS / L: APOLLO
XCCIBYPASS	H: CCI Bypass / L: CCI Enable
XCPUAXI3SELACE	H: AXI3 / L: ACE
PAD_DBGSRSEL	H: Audio JTAG / L: ARM JTAG
AP_JTAG_DBGSEL	H: Test Mode / L: Function



OM[5:1] 1st / 2nd

OM[5:1] 00000	eMMC (MSH CH0) with SWRST / USB
OM[5:1] 00010	SD_MMC (MSH CH2) / USB
OM[5:1] 00100	eMMC (MSH CH0) / USB
OM[5:1] 00101	UFS / USB
OM[5:1] 01000	eMMC (MSH CH0) with SWRST / SD_M
OM[5:1] 01100	eMMC (MSH CH0) / SD_MMC (MSH CH
OM[5:1] 01101	UFS / SD_MMC (MSH CH2)

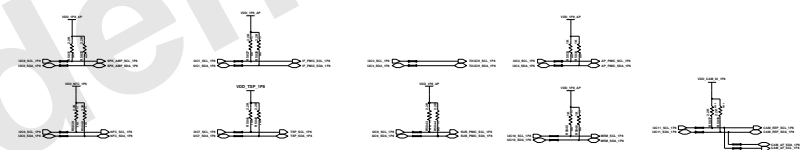
## iROM BOOT



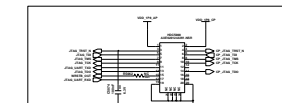
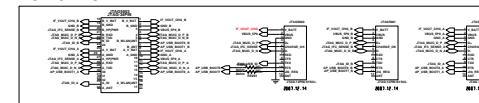
UCP500-1  
S5E7420AL0-LA3E

(POP 3GB LP4)

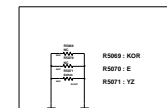
## H/W I2C



## PCB JTAG

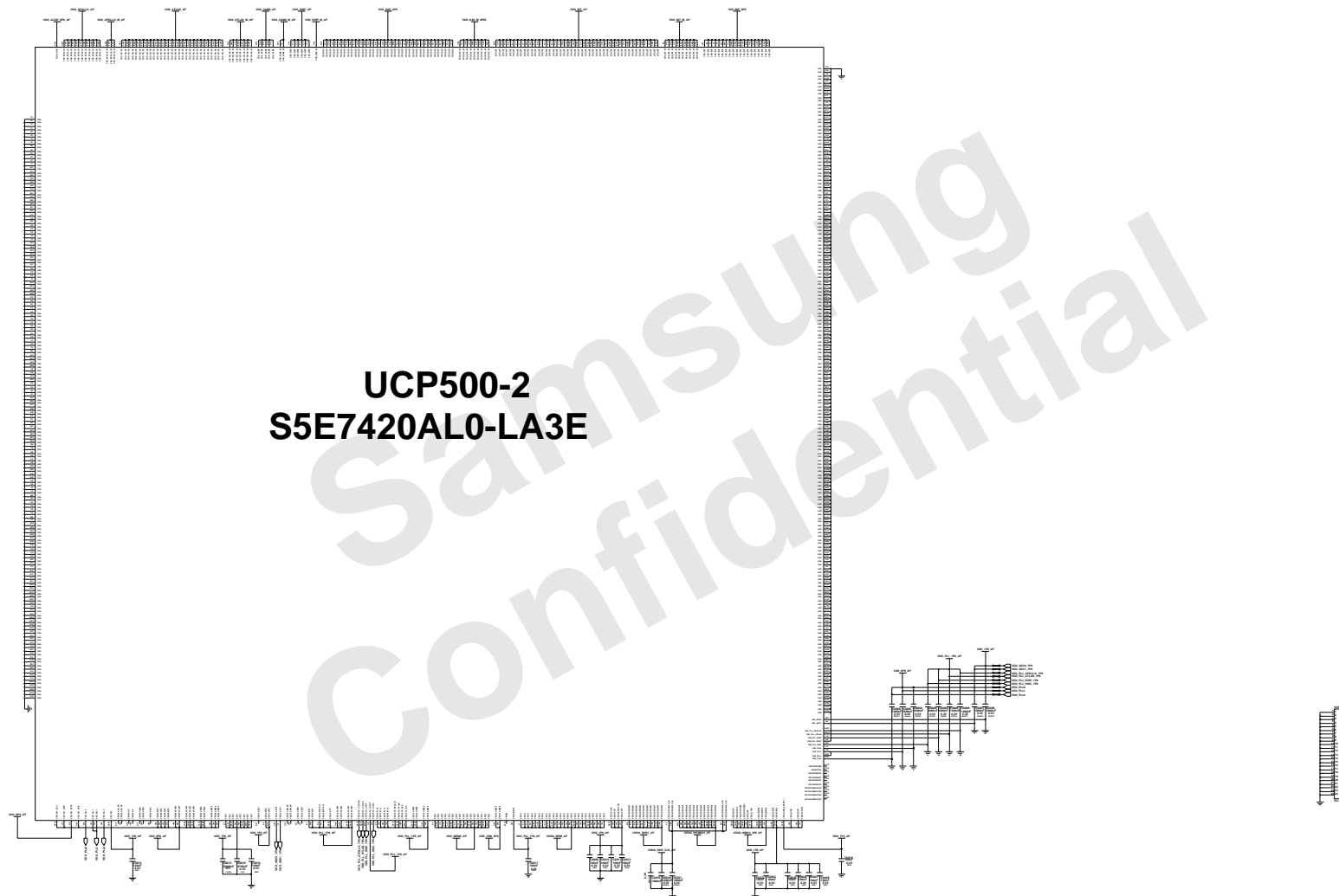


AP\_CP\_JTAG

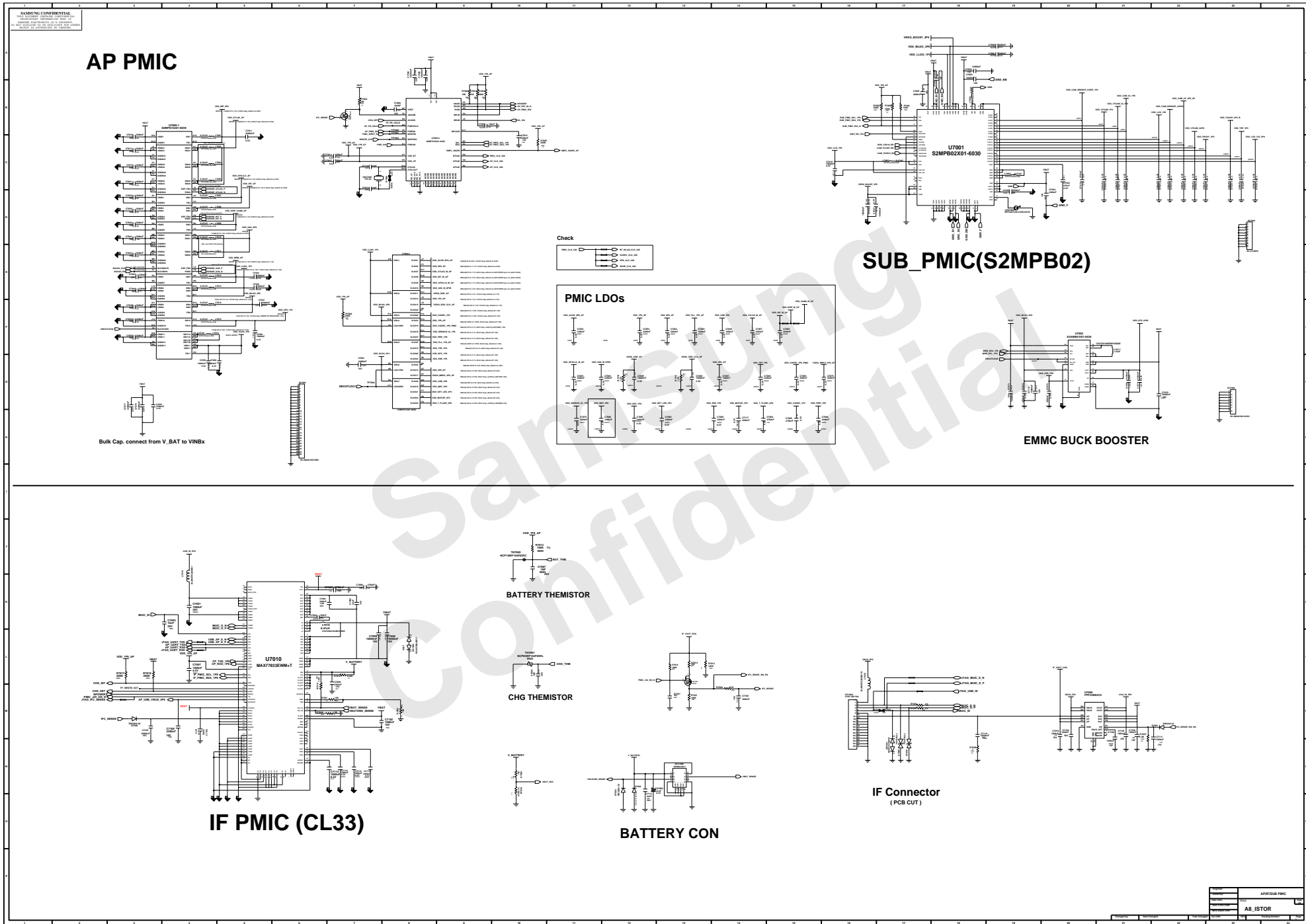


WARNING: CONFIDENTIAL

UCP500-2  
S5E7420AL0-LA3E

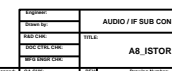
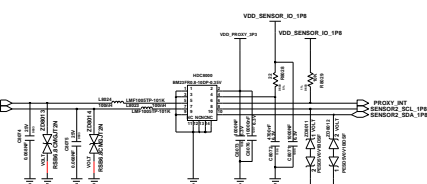
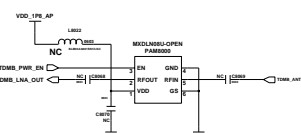
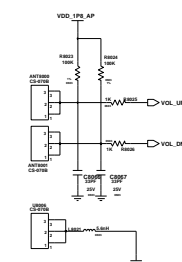
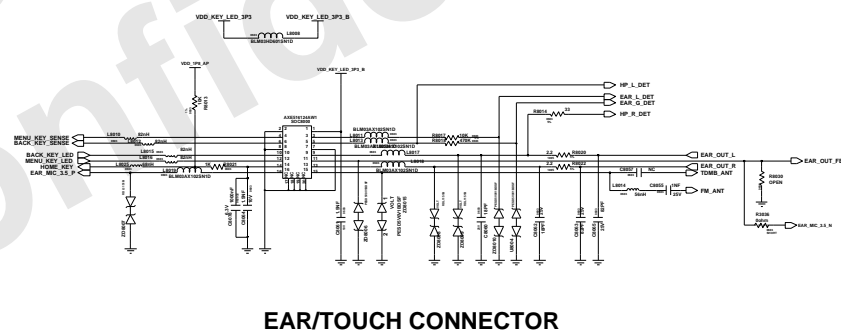
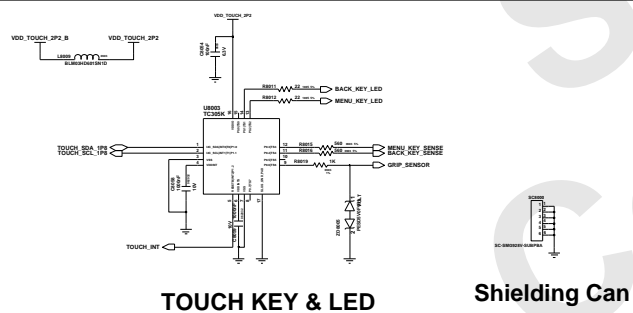
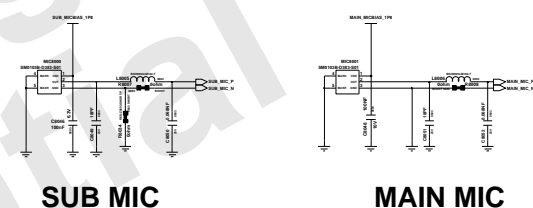


AP
SM-G920F

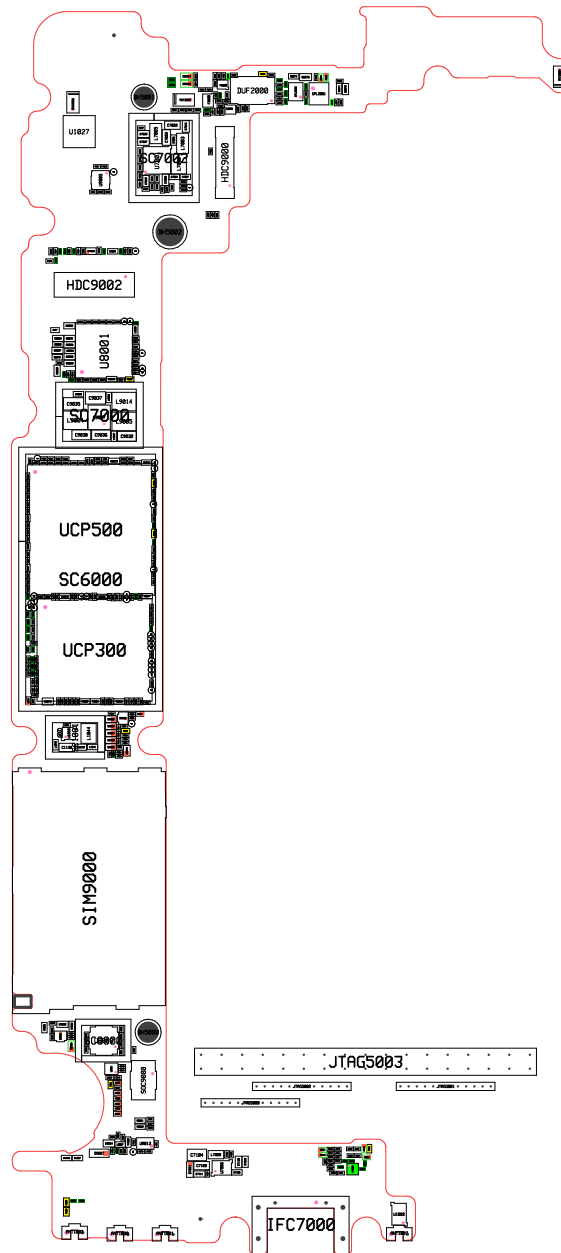




# AUDIO







AON1605(TR7001) : IT'S Wrong Polarity possibility. Check the Pin1

Model :  
Revision :  
Manufacture Count :  
Charge :  
Contact :  
Date :  
Routing :  
Resin :