CSCE 337: Digital Design II
Projects 2 (Static Timing Analysis)

Introduction

In this project you are required to develop (using any programming language of your choice; preferably JavaScript) a static timing analysis tool that gets (1) the Verilog gate level net list of a digital circuit, (2) the library of the cells used in the circuit, (3) the net capacitances file, (4) the clocks skew file and (5) timing constraints (the clock period, input delays and output delays). The tool checks all the timing paths and reports the violating timing paths, if any. For testing purpose, you need to generate gate level netlist for some designs using yosys synthesis tool.

Requirements

- Task 1: Define the formats for every input file (3, 4, and 5). [5%]
- Task 2: Reading the gate level net list (given as JSON), identifying the timing paths and creating a DAG. Output the identified timing paths (starting point, ending point and path type). [30%].
- Task 3: Read the library file (JSON), read the net capacitances file and apply the Critical Path Method (CPM) to find the critical path. Output the identified critical path (see fig. 1). [40%]
- Task 4: Read the clock skews file as well as the timing constrains file then check for timing violations (setup and hold). Output the identified violations. [25%]
- Task 5: Calculate the Arrival and Required times at each node of the DAG as well as the slacks. Output the slacks at all gates. [Bonus: 20%]

```
-------------------------------------------------------
Pin          type        Incr        Path delay
-------------------------------------------------------
A[0]         (in)        0.00        0.00              r
U10/A        (NAND2)     0.00        0.00              r
U10/Y        (NAND2)     1.00        1.00              r
U9/A         (NOT1)      0.00        1.00              f
U9/Y         (NOT1)      1.00        2.00              f
U2/B         (AND2)      0.00        2.00              f
U2/Y         (AND2)      1.00        3.00              f
U1/A         (AND2)      0.00        3.00              f
U1/Y         (AND2)      1.00        4.00              f
M[2]         (out)       0.00        4.00              f
-------------------------------------------------------
Data Arrival Time                     4.00
```

Fig. 1. Timing path output

Rules:

- The project should be demonstrated before the final exam. Each team is responsible for scheduling an appointment with Dr. Shalan for project demonstration (5-10 minutes per team).
- The deadlines are hard ones.
- All deliverables should be done through Google drive. Every team has to create a folder and share it with Dr. Shalan. A notification email must be sent for every deliverable.

Deliverables:

April 27th (11:59PM) 5%	• Group members • Input files definitions (task 1) • Specifying the Programming language and the libraries/middleware to be used • Workload distribution
May 4th (11:59PM) 30%	• Source code for Task 2 • Test designs (at least 8) as well as the reports
May 11th (11:59PM) 40%	• Source code for Task 2 • Input files and output reports for at least 8 designs
Before the final exam 25%	• Source code for Task 2 • Input files and output reports for at least 8 designs

Resources

Yosys synthesis tool:

- http://www.clifford.at/yosys/

Liberty Standard Cell Library Format:

- http://link.springer.com.library.aucegypt.edu:2048/chapter/10.1007/978-0-387-93820-2_3

Good Book for STA (You may read Chapter 8):

- http://link.springer.com.library.aucegypt.edu:2048/book/10.1007/978-90-481-9591-6/page/1

RapidJSON: C++ Library for reading JSON data

- http://rapidjson.org/md_doc_tutorial.html