8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
00h	nop	C	0
01h	soft_reset	C	0
04h	get_display_ID	R	3
05h	get_DSI_err	R	1
09h	read_display_status	R	4
0Ah	get_power_mode	R	1
0Bh	get_address_mode	R	1
0Ch	get_pixel_format	R	1
0Dh	get_display_mode	R	1
0Eh	get_signal_mode	R	1
0Fh	get_diagnostic_result	R	1
10h	enter_sleep_mode	C	0
11h	exit_sleep_mode	C	0
12h	enter_partial_mode	C	0
13h	enter_normal_mode	C	0
20h	exit_invert_mode	C	0
21h	enter_invert_mode	C	0
28h	set_display_off	C	0
29h	set_display_on	C	0
2Ah	set_column_address	W	4
2Bh	set_page_address	W	4
2Ch	write_memory_start	W	Variable
2Eh	read_memory_start	R	Variable
30h	set_partial_area	W	4
33h	set_scroll_area	W	6
34h	set_tear_off	C	0
35h	set_tear_on	W	1
36h	set_address_mode	W	1
38h	exit_idle_mode	C	0
39h	enter_idle_mode	C	0
3Ah	set_pixel_format	W	1
3Ch	write_memory_continue	W	Variable
3Eh	read_memory_continue	R	Variable
44h	set_tear_scanline	W	2
45h	get_scanline	R	2
51h	set_display_brightness	W	1
52h	get_display_brightness	R	1
53h	set_control_display	W	1

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
54h	get_control_display	R	1
55h	set_cabc_mode	W	1
56h	get_cabc_mode	R	1
5Eh	set_cabc_min_brightness	W	1
5Fh	get_cabc_min_brightness	R	1
AAh	read_first_checksum	R	1
AFh	read_continue_checksum	R	1
DAh	read_ID1	R	1
DBh	read_ID2	R	1
DCh	read_ID3	R	1
B0h	Interface_mode_control	W	1
B1h	frame_rate_control (in normal mode)	W	2
B2h	frame_rate_control (in idle mode/8 colors)	W	2
B3h	frame_rate_control (in partial mode)	W	2
B4h	display_inversion_control	W	1
B5h	blanking_porch_control	W	4
B6h	display_function_control	W	3
B7h	entry_mode_set	W	1
BFh	device_code_read	R	5
C0h	power_control_1	W	2
C1h	power_control_2	W	2
C2h	power_control_3	W	1
C4h	power_control_4	W	1
C5h	vcom_control_1	W	4
D0h	nv_memory_write	W	2
D1h	nv_memory_protection_key	W	3
D2h	nv_memory_status_read	R	3
D3h	read_ID4	R	3
E0h	Gamma_setting	W	15

8.2. Command Description

NOP (00h)

00H	NOP (No Operation)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart: None

SWRESET(01h) : Software Reset

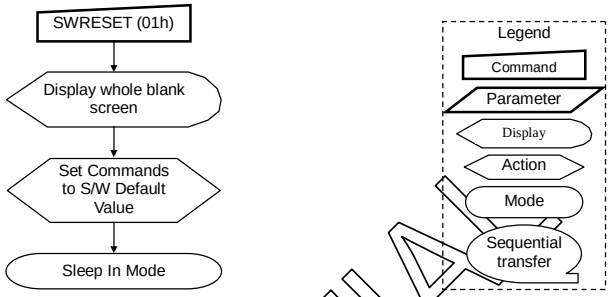
01H	SWRESET(Software Reset)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01
Parameter	No parameter												
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X = Don't care												
Restriction	The display module loads all display supplier's factory default values to the registers during 5ms. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120ms before sending Sleep Out command. Software Reset Command can not be sent during Sleep Out sequence.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart	

RDDIDIF(04h) : Read Display ID

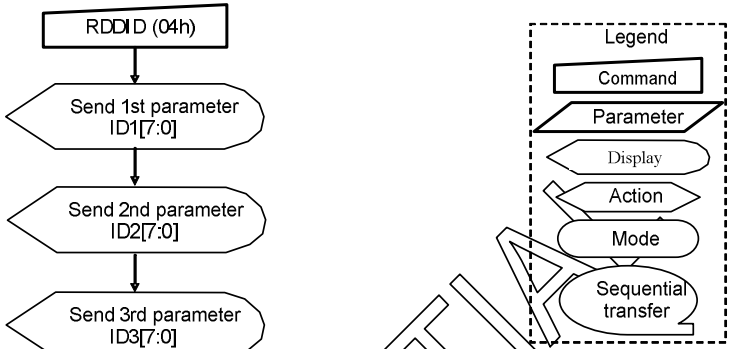
04H	RDDIDIF												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	00h	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	X
2nd parameter	1	↑	1	00h	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	54
3rd parameter	1	↑	1	00h	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	80
4th parameter	1	↑	1	00h	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	66
Parameter	-												
Description	The 1st parameter (ID1): dummy data. The 2nd parameter (ID2): the LCD module's manufacture ID The 3rd parameter (ID3): the LCD module/driver version ID The 4th parameter (ID4): the LCD module/driver ID												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID1=54h / ID2=80h / ID3=66h
SW Reset	ID1=54h / ID2=80h / ID3=66h
HW Reset	ID1=54h / ID2=80h / ID3=66h

Flow Chart	

RDNUMED(05h) : Read Number of Errors on DSI

05H	RDNUMED (Read Number of the Error on DSI)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	0	1	0	1	05
1st parameter	1	↑	1	x	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]	00
Parameter	NO PARAMETER												
Description	The second parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to “1” if there is overflow with P[6..0] bits. P[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the second parameter information (= The read function is completed). This command is used for MIPI DSI only. It is no function for others interface operation.												
Restriction	-												

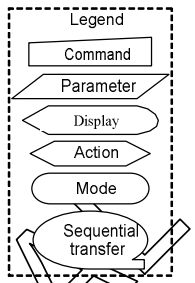
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDST (09h) : Read Display Status

09H	RDDST (Read Display Status)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	x	D31	D30	D29	D28	D27	D26	D25	0	xx
3rd parameter	1	↑	1	x	0	D22	D21	D20	D19	D18	D17	D16	xx
4th parameter	1	↑	1	x	D15	0	D13	0	0	D10	D9	D8	xx
5th parameter	1	↑	1	x	D7	D6	D5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Value	Status
D31	BSTON	Booster Voltage Status	0	Booster off
			1	Booster on
D30	MY	Row Address Order	0	Top to Bottom (36H- D7='0')
			1	Bottom to Top (36H-D7='1')
D29	MX	Column Address Order	0	Left to Right (MADCTL D6='0')
			1	Right to Left (MADCTL D6='1')
D28	MV	Row/Column Order (MV)	0	Normal (36H-D5='1')
			1	Row/column exchange(36H-D5='1')
D27	ML	Vertical Refresh Order	0	LCD Refresh Bottom to Top
			1	LCD Refresh Top to Bottom
D26	RGB	RGB/BGR Order	0	RGB
			1	BGR
D25	MH	Horizontal Refresh Order	0	LCD Refresh Left to Right
			1	LCD Refresh Right to Left
D22	IFPF[2:0]	DBI Pixel Format(Control Interface Color Format)	101	16-bits / pixel
D21			110	18-bits / pixel
D20			others	-
D19	IDMOD	Idle Mode On/Off	0	Idle Mode Off
			1	Idle Mode On
D18	PTLON	Partial Mode On/Off	0	Partial Mode Off
			1	Partial Mode On
D17	SLPOUT	Sleep In/Out	0	Sleep In
			1	Sleep Out
D16	NORON	Display Normal Mode On/Off	0	Partial Display
			1	Normal Display
D15	VSSON	Vertical scrolling status	0	Vertical scrolling is Off
			1	Vertical scrolling is On
D13	INVON	Inversion On/Off	0	Inversion is Off
			1	Inversion is On
D10	DISPON	Display On/Off	0	Display Off
			1	Display On

D9	TEON	Tearing Effect Line On/Off	0	Off
			1	on
D8	GAMMA C SEL	NOT USED	-	-
D7	GAMMA C SEL	NOT USED	-	-
D6	GAMMA C SEL	NOT USED	-	-
D5	TELOM	Tearing effect line mode	0	"0" = mode1
			1	"1" = mode2

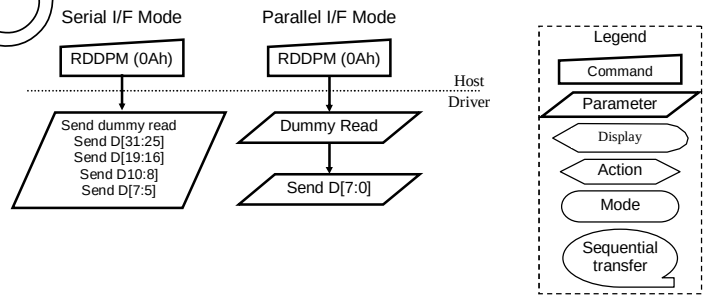
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDPM (0Ah) : Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	BSTON	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
D5	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
D4	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
D3	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
D2	DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Reserved	-	0
D0	Reserved	-	0

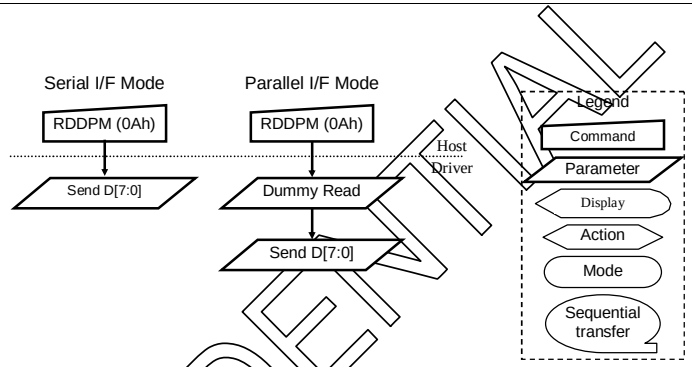
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDMADCTR (0Bh): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	00

Description

This command indicates the current status of the display as described in the table below:

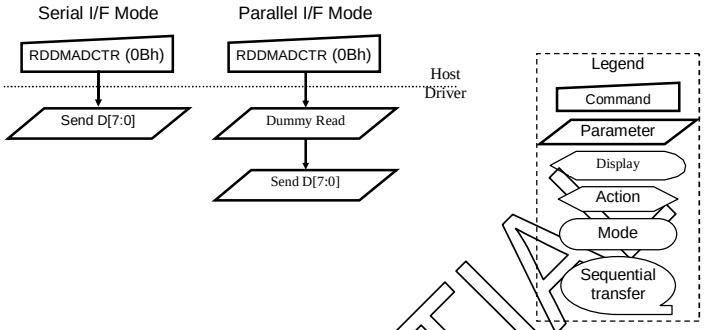
Bit	Symbol	Description	Comment
D7	MY	Row Address Order	'1' = Bottom to Top (36H-D7='1') '0' = Top to Bottom (36H- D7='0')
D6	MX	Column Address Order	'1' = Right to Left (MADCTL D6='1') '0' = Left to Right (MADCTL D6='0')
D5	MV	Row/Column Order (MV)	'1' = Row/column exchange (36H-D5='1') '0' = Normal (36H-D5='1')
D4	ML	Vertical Refresh Order	'1' =LCD Refresh Top to Bottom '0' =LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
D2	MH	Horizontal Refresh Order	'0' = LCD Refresh Left to Right '1' = LCD Refresh Right to Left
D1	Reserved		0
D0	Reserved		0

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow Chart	

RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	x	D7	D6	D5	D4	0	D2	D1	D0	66

Description

This command indicates the current status of the display as described in the table below:

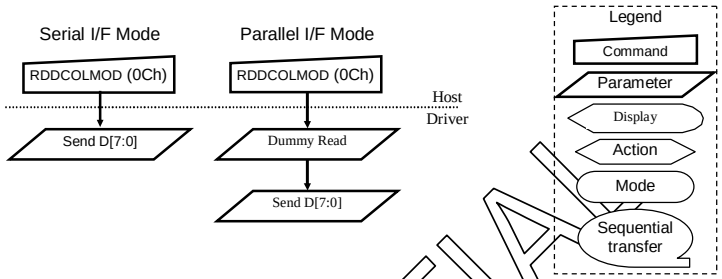
Bit	Symbol	Description	Comment
D7	VIPF[3]	DPI Pixel Format(RGB Interface Color Format)	'0101' = 16-bits / pixel, '0110' = 18-bits / pixel, others are reserved
D6	VIPF[2]		
D5	VIPF[1]		
D4	VIPF[0]		
D3	Reserved	-	'0'
D2	IFPF[2]	DBI Pixel Format(Control Interface Color Format)	'101' = 16-bits / pixel, '110' = 18-bits / pixel, others are reserved
D1	IFPF[1]		
D0	IFPF[0]		

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
SW Reset	No Change
HW Reset	66h

Flow Chart	

RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D
1st Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the display image mode status.

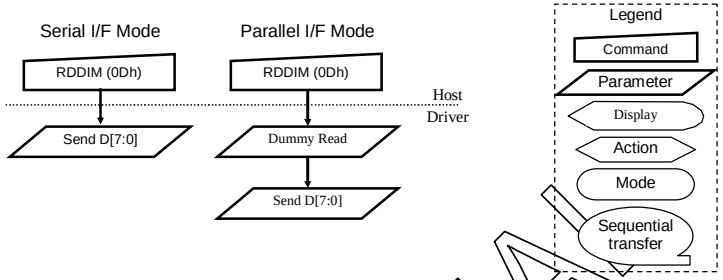
Bit	Symbol	Description	Comment
D7	VSSON	Vertical scrolling status	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Reserved		'0'
D5	INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	Reserved		'0'
D3	Reserved		'0'
D2~D0	Reserved		'0'

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the Display Signal Mode.

Bit	Symbol	Description	Comment
D7	TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2
D5	HS	Horizontal Sync On/Off	'0' = HSYNC is Off '1' = HSYNC is On
D4	VS	Vertical Sync On/Off	'0' = VSYNC is Off '1' = VSYNC is On
D3	PCLK	Pixel Clock On/Off	'0' = PCLK is Off '1' = PCLK is On
D2	DE	Data Enable On/Off	'0' = DE is Off '1' = DE is On
D1	Reserved	-	'0'
D0	DSI ERROR	Error on DSI	'0' = No Error '1' = Error

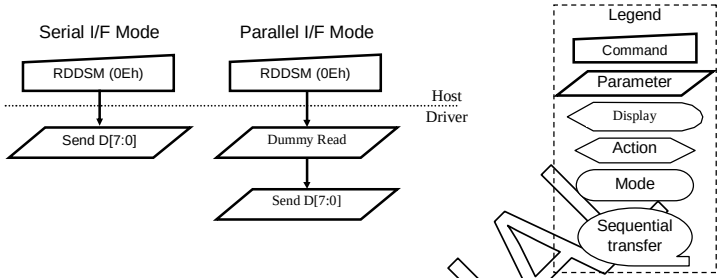
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F
1st Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	D0	00

Description

The display module returns the self-diagnostic results following a Sleep Out command.

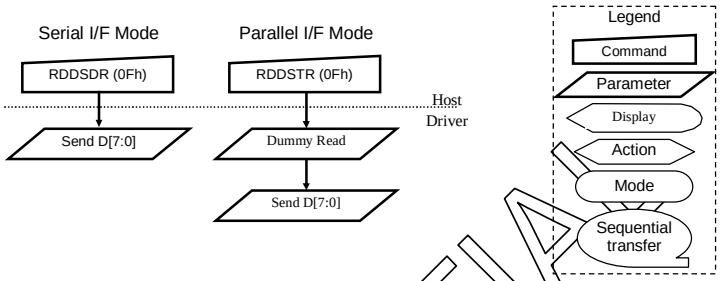
Bit	Symbol	Description	Comment
D7	SDR	Register Loading Detection	Invert the D7 if register values loading won't propedy
D6	FUNCD	Functionality Detection	Invert the D6 if the display is functionality
D5	Reserved		'0'
D4	Reserved		'0'
D3	Reserved		'0'
D2	Reserved		'0'
D1	Reserved		'0'
D0	CKSCMP	Checksums comparison	'0' = checksums are same '1' = checksums are not the same

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

SLPIN (10h): Sleep In

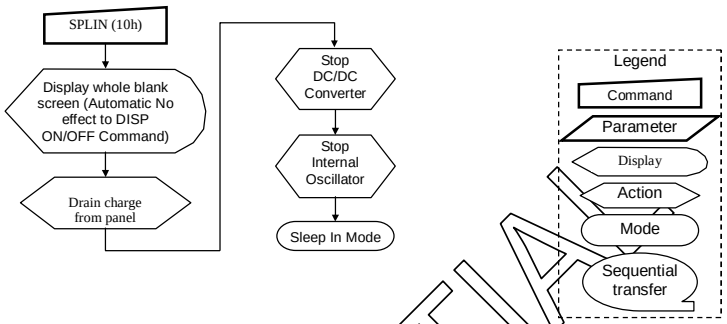
10H	SLPIN (Sleep In)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												
Description	This command causes the display module to enter the Sleep mode. This command causes the module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal mode.												
Restriction	This command has no effect when the display module is already in Sleep mode. The host processor must wait 5 milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending Sleep Out command before sending Sleep In command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart	

SLPOUT (11h): Sleep Out

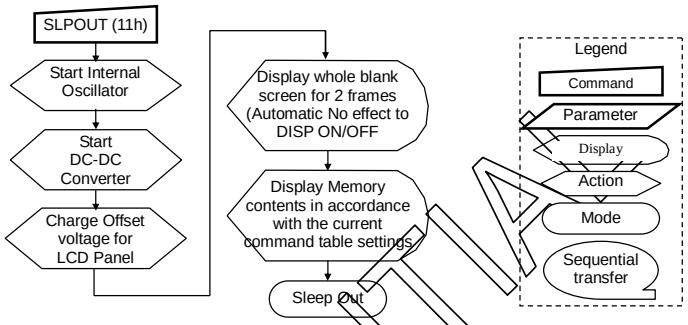
11H	SLPOUT (Sleep Out)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow chart	

PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12
Parameter	No Parameter												
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.												
Restriction	This command has no effect when Partial Display Mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal display mode On
SW Reset	Normal display mode On
HW Reset	Normal display mode On

Flow Chart	Refer to Partial Area (30h)

NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off.												
Restriction	This command has no effect when Normal Display mode is already active.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

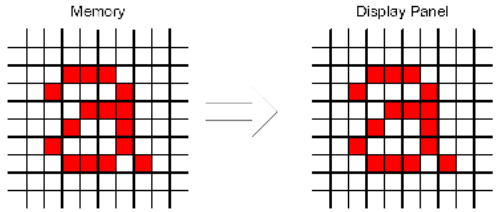
Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart: Refer to the description of Partial Area (30h)

INVOFF (20H): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.												



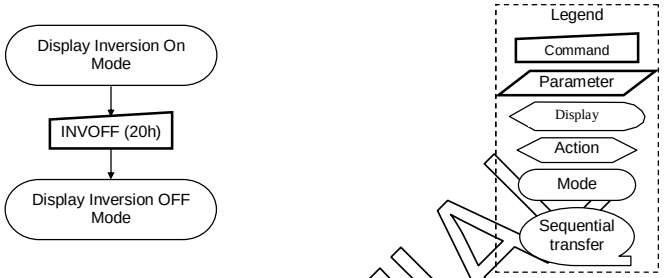
Restriction: This command has no effect when the display module is not inverting the display image.

Register Availability

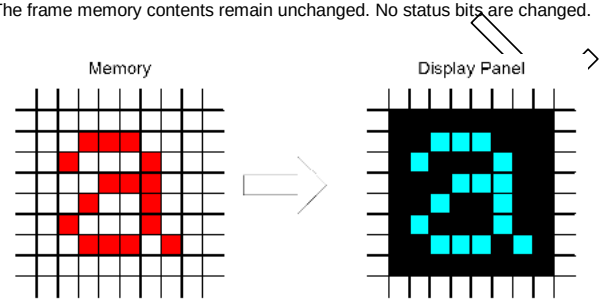
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

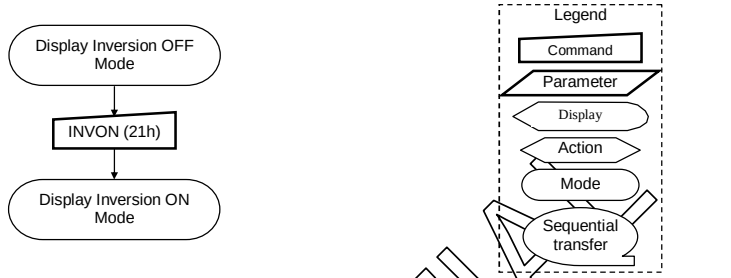
Flow Chart	

INVON (21H): Display Inversion On

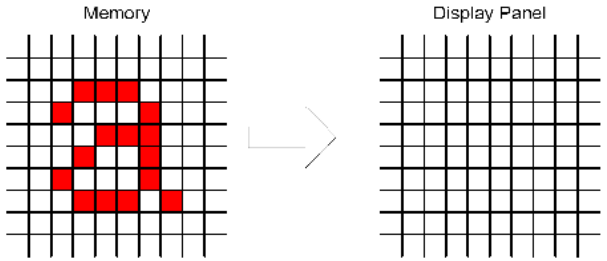
21H	INVON (Display Inversion On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

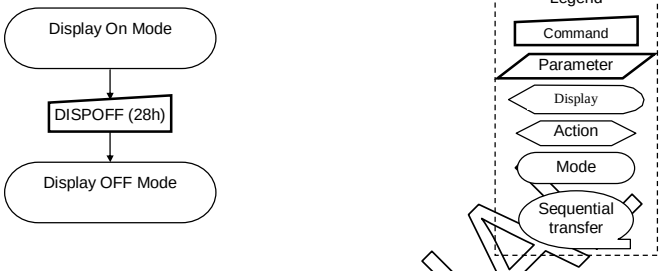
Flow Chart	

DISPOFF (28h): Display Off

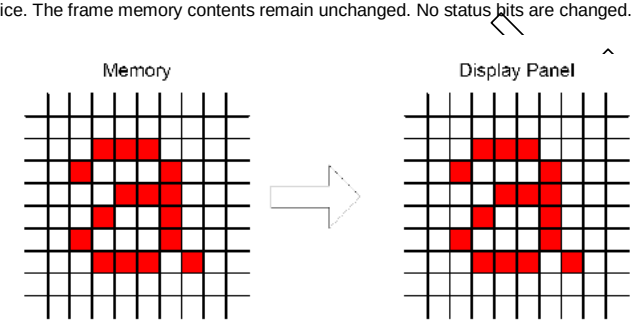
28H	DISPOFF (Display Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display off mode.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart	

DISPON (29h): Display On

29H	DISPON (Display On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display on mode.												

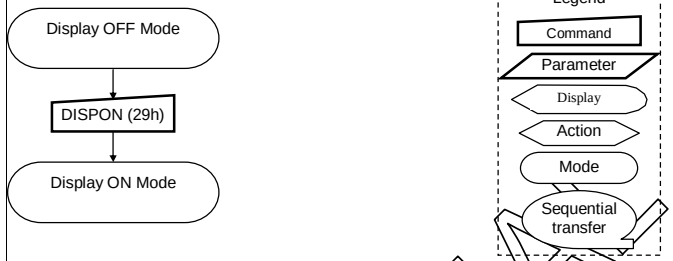
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

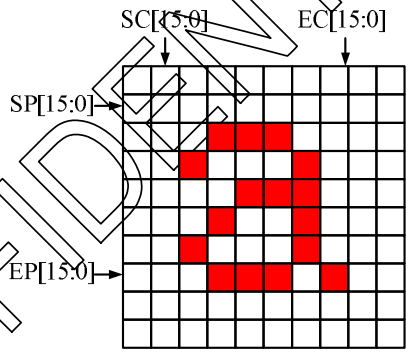
Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	x	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00
2nd parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
3rd parameter	1	1	↑	x	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	01
4th parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	DF
Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. 												
Restriction	SC[15:0] always must be equal to or less than EC[15:0]. Note 1: When SC[15:0] or EC[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh (When MADCTL's B5 = 1), data of out of range will be ignored												

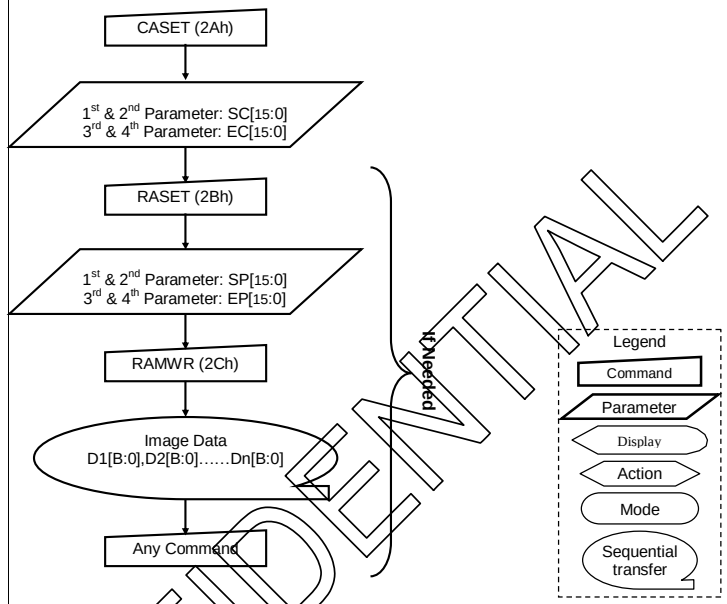
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

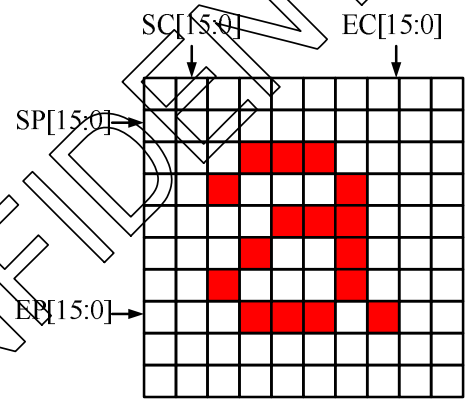
Status	Default Value	
	SC[15:0]	EC[15:0]
Power On Sequence	0000h	00EFh
SW Reset	0000h	013Fh (If MADCTL's B5=0) 01DFh (If MADCTL's B5=1)
HW Reset	0000h	013Fh

Flow chart



Note : B=23

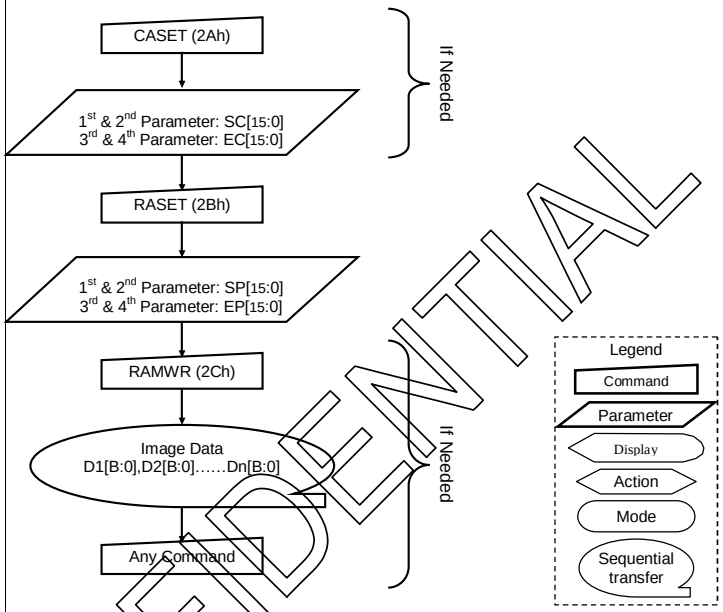
RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	x	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00
2nd parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
3rd parameter	1	1	↑	x	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	01
4th parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	3F
Description	This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory. 												
Restriction	SP[15:0] always must be equal to or less than EP[15:0] When SP[15:0] or EP[15:0] is greater than 01DFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data ofout of range will be ignored.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value	
		SP[15:0]	EP[15:0]
	Power On Sequence	0000h	013Fh
	SW Reset	0000h	01DFh (If MADCTL's B5=0) 013Fh (If MADCTL's B5=1)
	HW Reset	0000h	01EFh

Flow chart



Note : B=23

RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C
1st pixel data	1	1	↑	D1[15..8]	D17	D16	D15	D14	D13	D12	D11	D10	xx
:	1	1	↑	Dx[15..8]	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	xx
Nth pixel data	1	1	↑	Dn[15..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	xx
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												

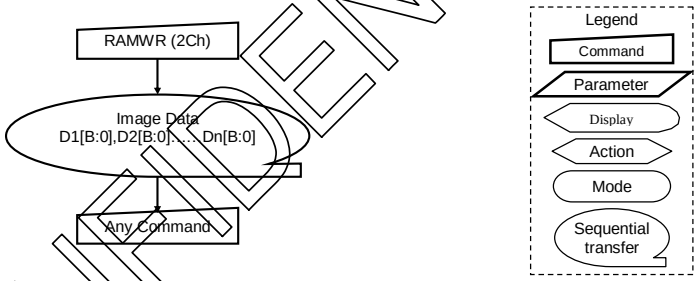
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



RAMRD (2Eh): Memory Read

2EH	RAMRD (Memory Read)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	D1[15..8]	D17	D16	D15	D14	D13	D12	D11	D10	
:	1	↑	1	Dx[15..8]	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	
(N+1)th parameter	1	↑	1	Dn[15..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	

Description

This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preseding CASET (2Ah) and RASET (2Bh) commands.

If MV(36h-B5) = 0:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If MV(36h-B5) = 1:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

There is no restriction on length of parameters.

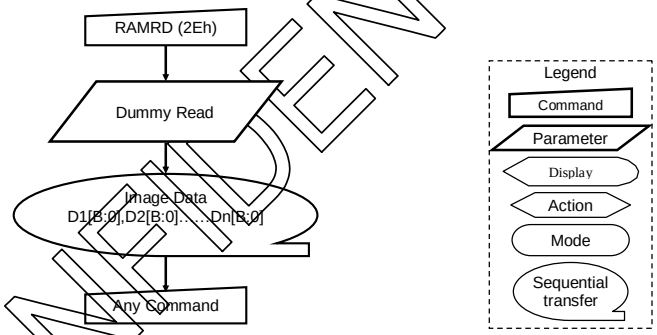
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



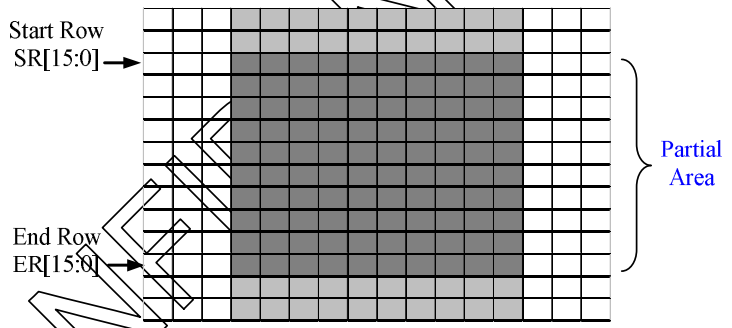
PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	x	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd parameter	1	1	↑	x	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	DF

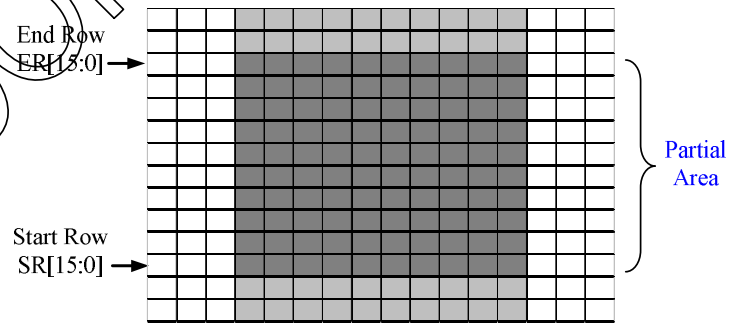
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory.

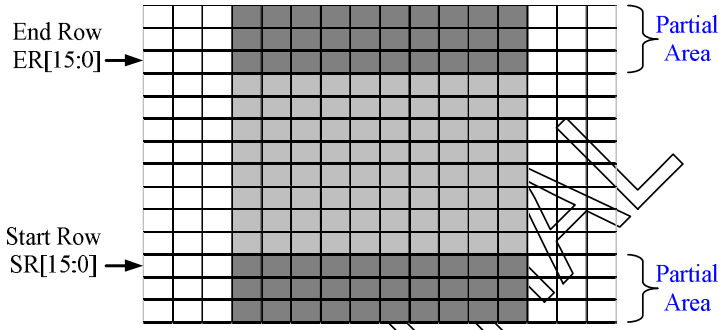
-If End Row > Start Row, when ML(36h-B4) ='0'



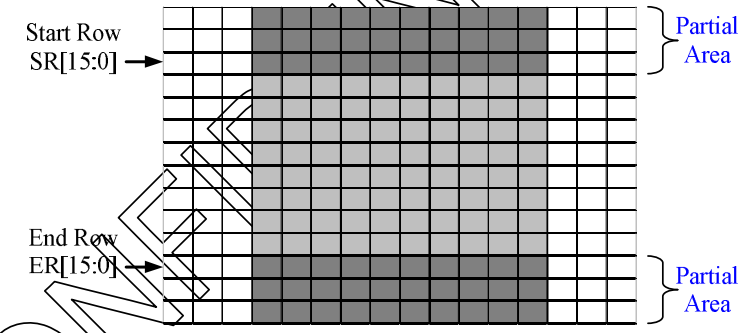
-If End Row > Start Row, when ML(36h-B4) ='1'



-If End Row < Start Row, when ML(36h-B4) ='0'



-If End Row < Start Row, when ML(36h-B4) ='1'



-If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).

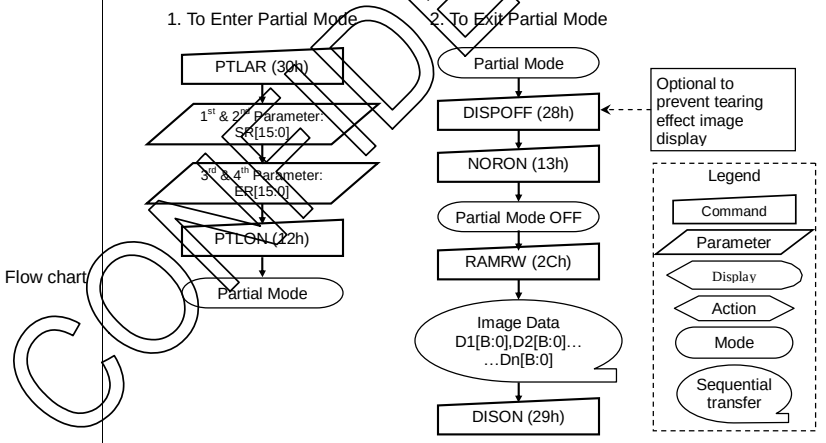
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SR[15:0]	ER[15:0]
Power On Sequence	0000h	01DFh
SW Reset	0000h	01DFh
HW Reset	0000h	01DFh

Flow chart



VSCRDEF (33h): Vertical Scrolling Definition

33H	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	x	TFA[15]	TFA[14]	TFA[13]	TFA[12]	TFA[11]	TFA[10]	TFA[9]	TFA[8]	xx
2nd parameter	1	1	↑	x	TFA[7]	TFA[6]	TFA[5]	TFA[4]	TFA[3]	TFA[2]	TFA[1]	TFA[0]	xx
3rd parameter	1	1	↑	x	VSA[15]	VSA[14]	VSA[13]	VSA[12]	VSA[11]	VSA[10]	VSA[9]	VSA[8]	xx
4th parameter	1	1	↑	x	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]	xx
5th parameter	1	1	↑	x	BFA[15]	BFA[14]	BFA[13]	BFA[12]	BFA[11]	BFA[10]	BFA[9]	BFA[8]	xx
6th parameter	1	1	↑	x	BFA[7]	BFA[6]	BFA[5]	BFA[4]	BFA[3]	BFA[2]	BFA[1]	BFA[0]	xx

Description

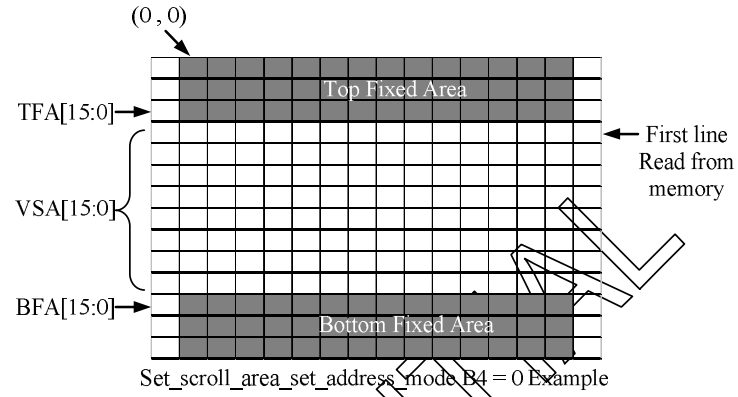
This command defines the display vertical scrolling area.

Memory Data Access Control (36h) B4 = 0:

The 1st & 2nd parameter, TFA[15:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[15:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Set_scroll_area_set_address_mode B4 = 0 Example

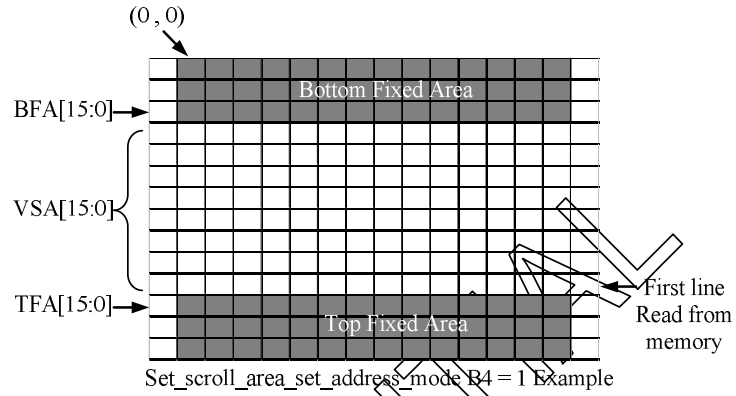
Memory Data Access Control (36h) B4 = 1:

The 1st & 2nd parameter, TFA[15:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[15:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory.
The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Set_scroll_area_set_address_mode B4 = 1 Example

Restriction

The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

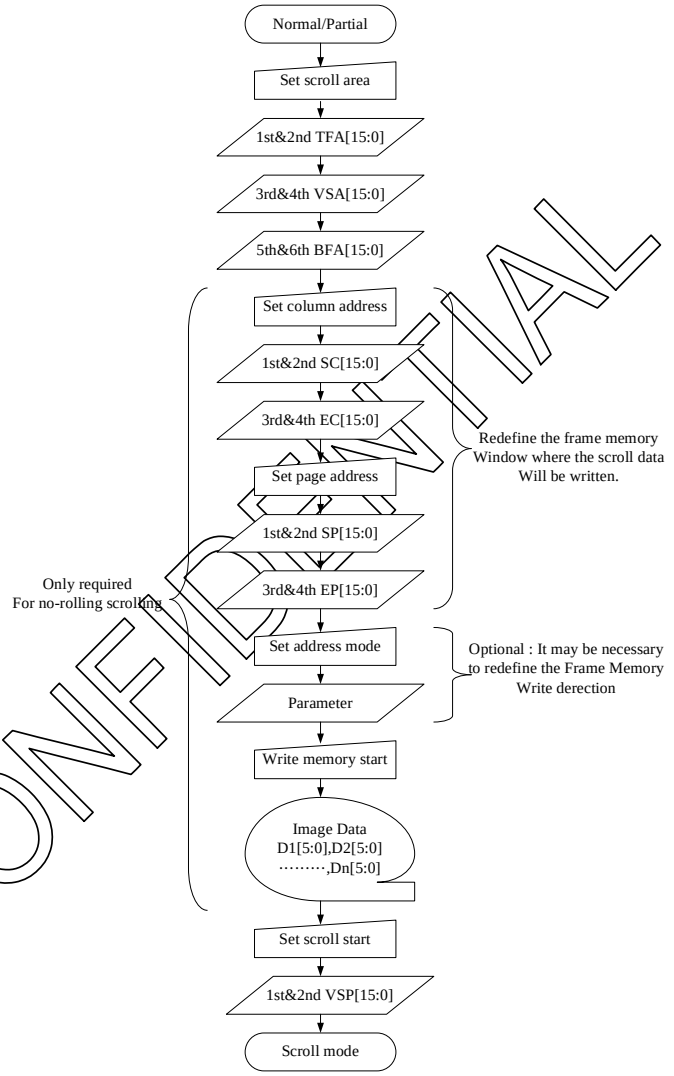
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000HEX	VSA[15:0]=01E0HEX	BFA[15:0]=0000HEX
SW Reset	TFA[15:0]=0000HEX	VSA[15:0]=01E0HEX	BFA[15:0]=0000HEX
HW Reset	TFA[15:0]=0000HEX	VSA[15:0]=01E0HEX	BFA[15:0]=0000HEX

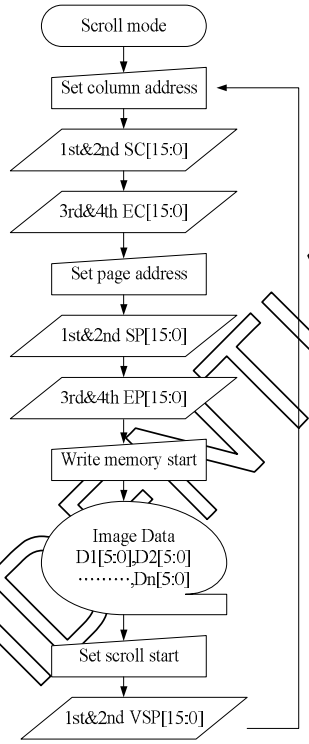
Flow chart

1. To enter vertical scroll mode:

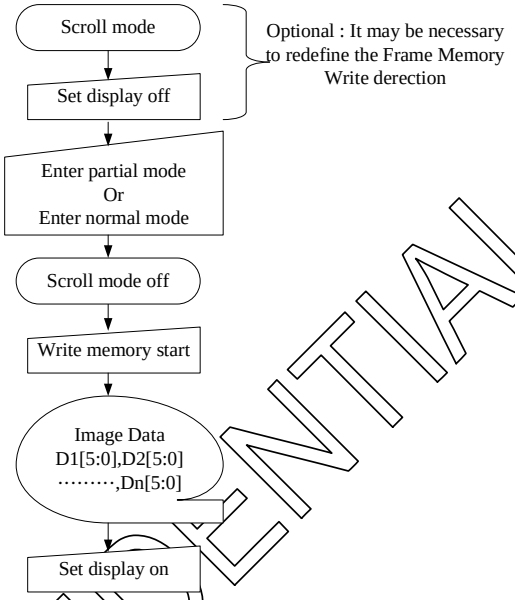


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

2. Continuous scroll:



3. To leave vertical scroll mode:



TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												

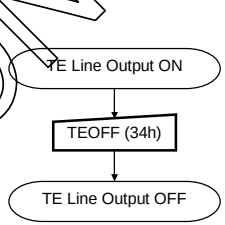
Register Availability

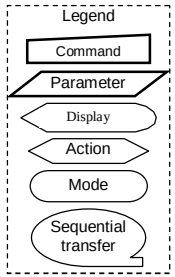
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

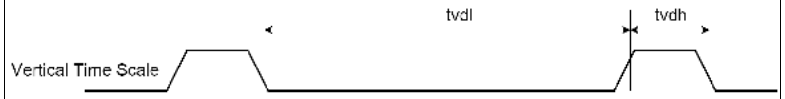
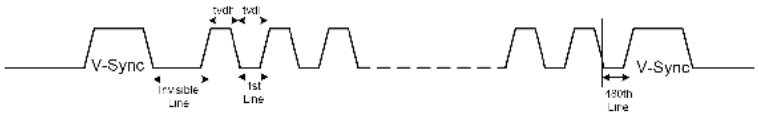
Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

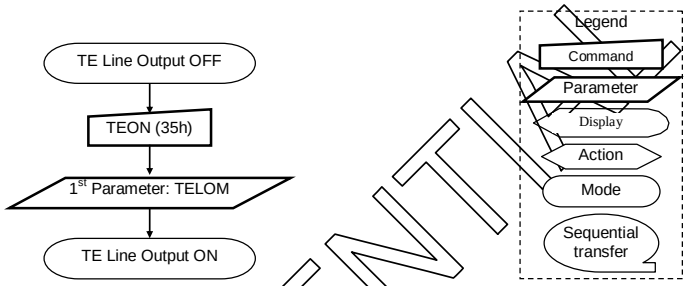
Flow Chart





TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	TELOM	00
Description	This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order). The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. If TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only.  If TELOM = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.  ***The Tearing Effect Output line shall be active low when the display module is in Sleep mode.***												
Restriction	This command has no effect when Tearing Effect output is already ON.												
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes												

Default	Status / Default Value: Power On Sequence — OFF SW Reset — OFF HW Reset — OFF
Flow Chart	

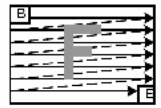
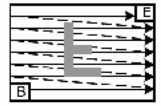
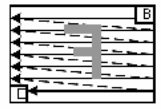
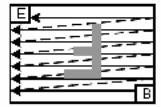
MADCTR (36h): Memory Data Access Control

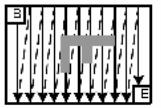
36H	MADCTR (Memory Data Access Control)												
	DCX	RDX	WRX	D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	x	B7	B6	B5	B4	B3	B2	B1	B0	00

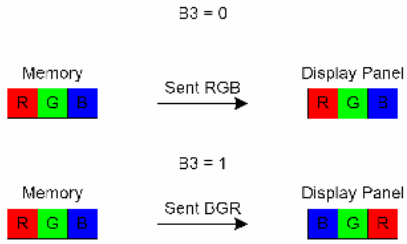
Description

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
B7	MY	Row Address Order	'1' = Bottom to Top '0' = Top to Bottom
B6	MX	Column Address Order	'1' = Right to Left '0' = Left to Right
B5	MV	Row/Column Order (MV)	'1' = Row/column exchange '0' = Normal
B4	ML	Vertical Refresh Order	'0' =LCD Refresh Top to Bottom '1' =LCD Refresh Bottom to Top
B3	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
B2	MH	Horizontal Refresh Order	'0' =LCD Refresh Left to Right '1' =LCD Refresh Right to Left
B1	H_FLIP	Horizontal Flip	'0' = Normal display '1' = Flipped display
B0	V_FLIP	Vertical Flip	'0' = Normal display '1' = Flipped display

B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	



Restriction

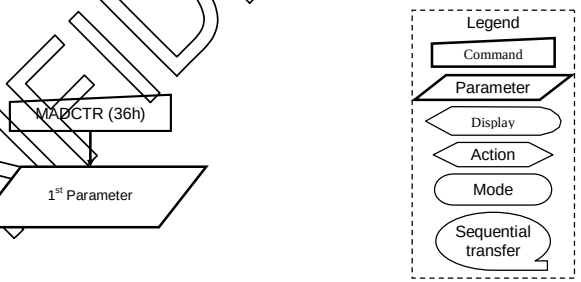
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow chart



VSCRSADD (37h): Vertical Scrolling Start Address

37H	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP8	xx
2nd parameter	1	1	↑	x	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	xx

Description

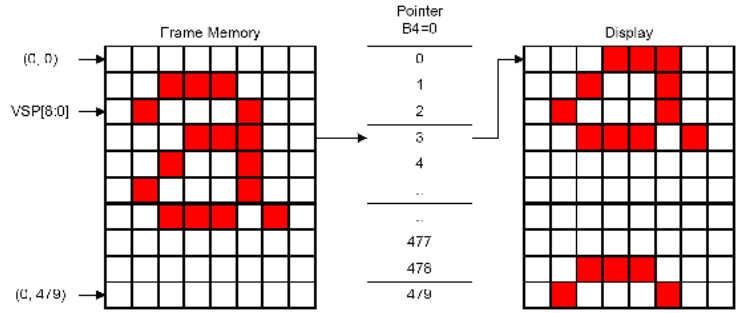
This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command

The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.

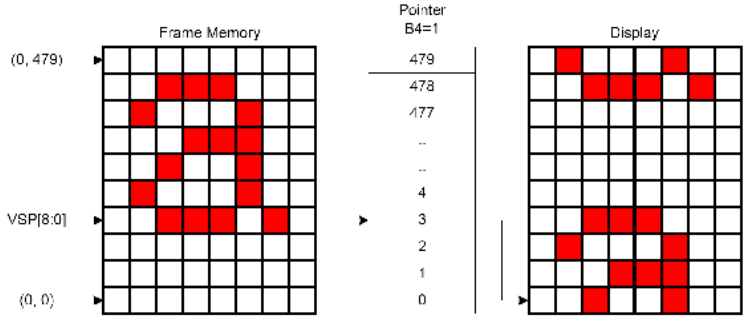
The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.

If set_address_mode (R36h) B4 = 0:
Example:

When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 480 and VSP = 3.



If set_address_mode (R36h) B4 = 1:
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.



Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000HEX
SW Reset	0000HEX
HW Reset	0000HEX

Flow chart	Refer to the description Vertical Scrolling Definition (33h)

IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart

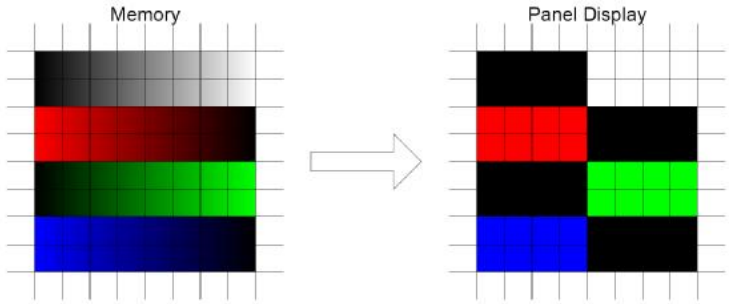
IDMON (39h): Idle Mode ON

39H	IDMON (Idle Mode ON)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command causes the display module to enter Idle Mode.

In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.



Color	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Restriction: This command has no effect when module is already in idle on mode.

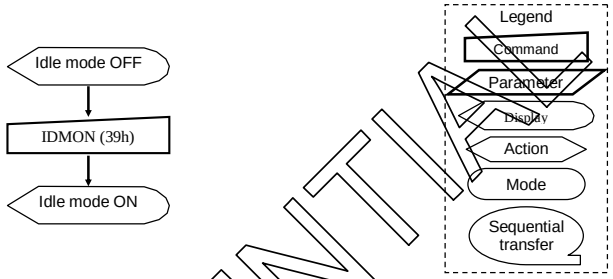
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	x	0	D6	D5	D4	0	D2	D1	D0	66

Description

This command sets the pixel format for the RGB image data used by the interface.

Bits D[6:4] – DPI Pixel Format Definition

Bits D[2:0] – DBI Pixel Format Definition

Bits D7 and D3 are not used.

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
Reserved	0	1	1
Reserved	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Reserved	1	1	1

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

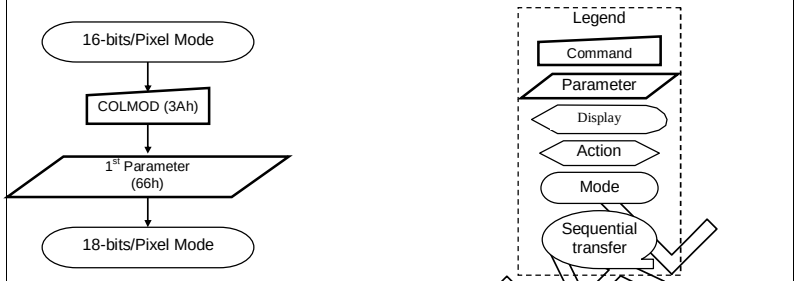
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
SW Reset	66h
HW Reset	66h

Flow chart

Example :



RAMWRC (3Ch) : Write_Memory_Continue

3CH	Write_Memory_Continue												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	D1[15..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	XX
Xst parameter	1	1	↑	Dx[15..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	XX
Nst parameter	1	1	↑	Dn[15..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	XX

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If MV(36h-B5) = 0:

Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If MV(36h-B5) = 1:

Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

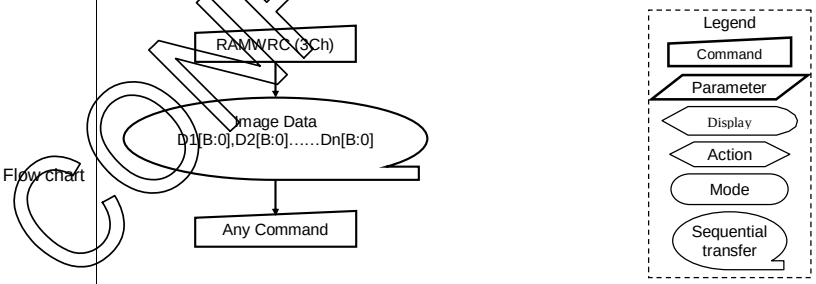
Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

	Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.
Register Availability	
Default	
Flow chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared



RAMRDC (3Eh) : Read_Memory_Continue

3EH	Read_Memory_Continue												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	D1[15..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	xx
Xst parameter	1	↑	1	Dx[15..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	xx
Nst parameter	1	↑	1	Dn[15..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	xx

Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If MV(36h-B5) = 0: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.
Restriction	A Memory Read should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMRD(2Eh) and any following RAMRDC(3Eh) commands is written to undefined locations.

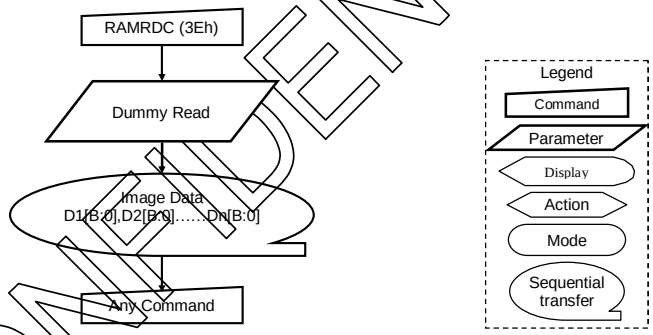
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart

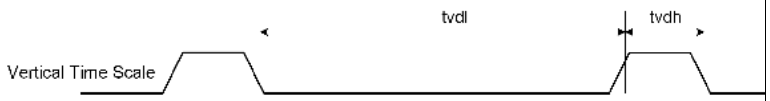


TESLWR (44h) : Write Tear Scan Line

44H	TESLWR (Write Tear Scan line)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS[8]	00
2nd parameter	1	1	↑	xx	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

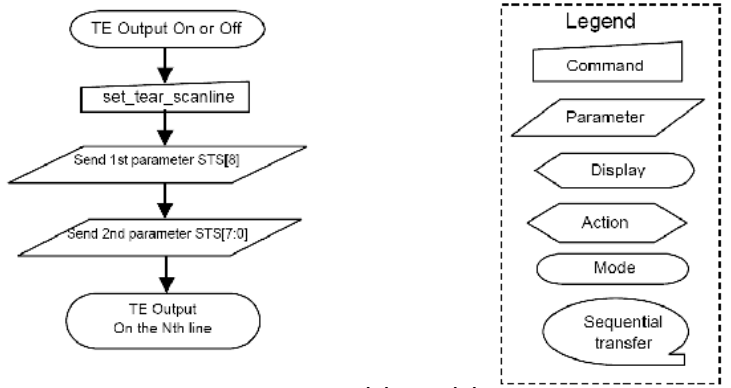
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS[8:0]=9'h000
SW Reset	No change
HW Reset	STS[8:0]=9'h000

Flow Chart	

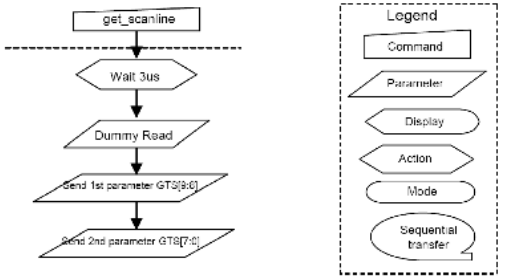
TESLRD (45h) : Read Tear Scan Line

45H	TESLRD (Read Tear Scan Line)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS[8]	0x
3rd parameter	1	↑	1	xx	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart



WRDISBV (51h): Write Display Brightness

51H	WRDISBV (Write Display Brightness)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	The display supplier cannot use this command for tuning												

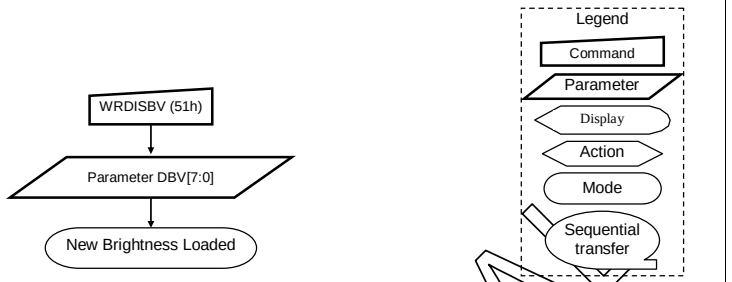
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	-												

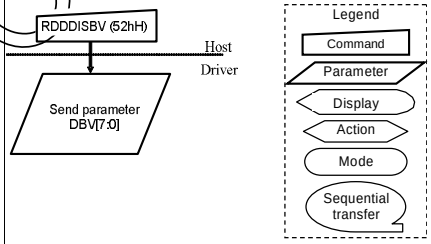
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRCTRLD (53h): Write CTRL Display

53H	WRCTRLD (White CTRL Display)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	x	0	0	BCTRL	x	DD	BL	x	x	00

Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION LEDPWM Pin	DESCRIPTION LEDPWMPin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%) LEDPWPOL="1": keep high (0%)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": keep low (non-lit) LEDPWPOL="1": keep high (non-lit)
1	On	LEDPWPOL="0": keep high (lit) LEDPWPOL="1": PWM output (lit)

The *dimming* function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

Restriction: The display supplier cannot use this command for tuning

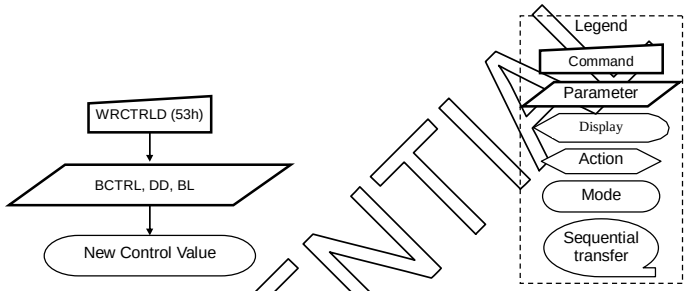
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDCTRLD (54h): Read CTRL Display Value

54H	RDCTRLD												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	0	0	54
1st parameter	1	↑	1	x	0	0	BCTRL	x	DD	BL	x	x	00

Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION LEDPWM Pin	DESCRIPTION LEDPWMPin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%) LEDPWPOL="1": keep high (0%)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": keep low (non-lit) LEDPWPOL="1": keep high (non-lit)
1	On	LEDPWPOL="0": keep high (lit) LEDPWPOL="1": PWM output (lit)

The *dimming* function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

Restriction

The display supplier cannot use this command for tuning

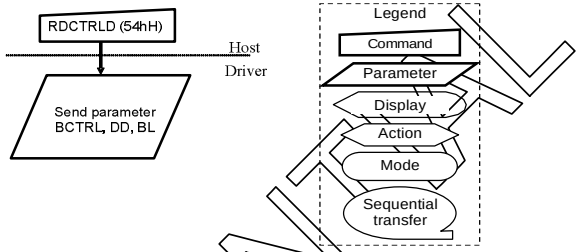
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRCABC (55h): Write Content Adaptive Brightness Control

55H	WRCABC (Write Content Adaptive Brightness Control)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	x	0	0	0	0	0	0	C1	C0	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	UI Mode
1	0	Still Mode
1	1	Moving Mode

Restriction

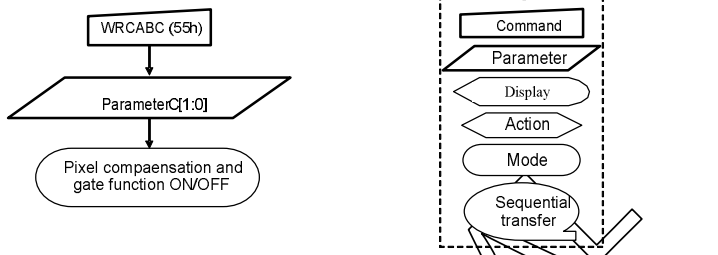
This register is synchronized with V-sync by internal circuit.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart	

RDCABC (56h): Read Content Adpative Brightness Control

56H	RDCABC (Read Content Adpative Brightness Control)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	x	0	0	0	0	0	0	C1	C0	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	UI Mode
1	0	Still Mode
1	1	Moving Mode

Restriction

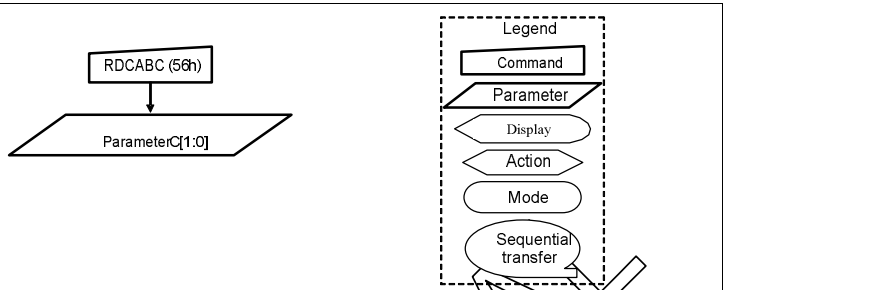
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

WRCABCMB (5Eh): Write CABC Minimum Brightness

5EH	WRCABCMB												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	↑	x	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00
Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Restriction	-												

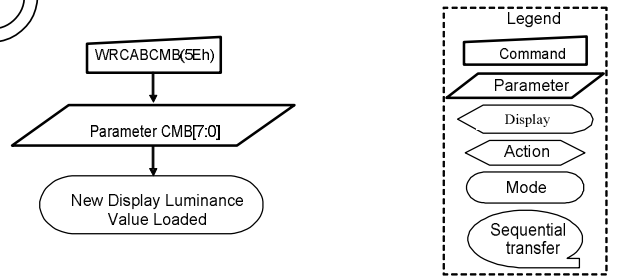
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDCABCMB (5Fh): Read CABC Minimum Brightness

5FH	RDCABCMB												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	1	1	1	1	5F
1st parameter	1	1	↑	x	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00
Description	This command return the minimum brightness value of CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. CMB[7:0] is minimum brightness forCABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.												
Restriction	-												

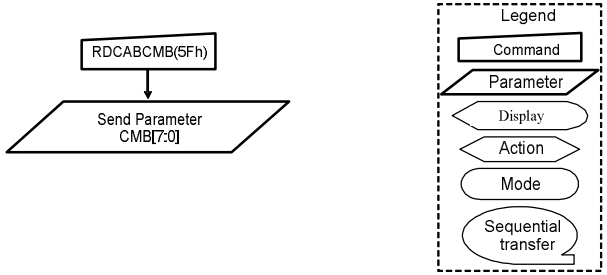
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDFCS (AAh) : Read First Checksum

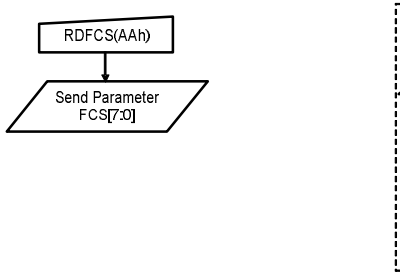
AAH	RDFCS (Read First Checksum)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	1	0	1	0	AA
1st parameter	1	↑	1	x	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	This command returns the first checksum what has been calculated from "User Command Set" area registers (not include "Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 150ms after there is the last write access on "User Command Set" area registers before there can read this checksum value.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

RDCFCS (AFh) : Read Continue Checksum

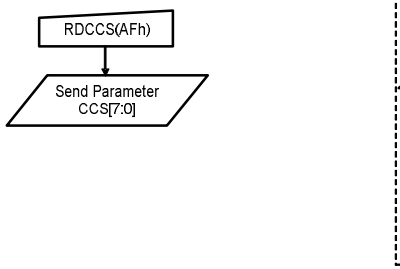
AFH	RDCFCS (Read Continue Checksum)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	1	1	1	1	AF
1st parameter	1	↑	1	x	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

RDID1 (DAh) : Read ID1

DAH	RDID1												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
Description	This read byte identifies the TFT LCD module's manufacture ID.												
Restriction	-												

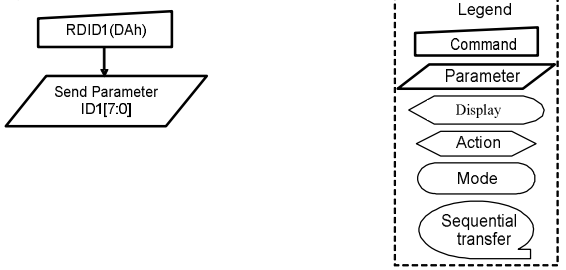
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDID2(DBh) : Read ID2

DBH	RDID2												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	0	1	1	DB
1st parameter	1	↑	1	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00
Description	This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 80h to FFh												
Restriction	-												

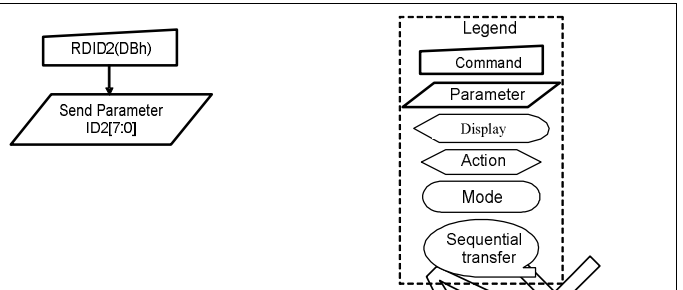
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	80h
SW Reset	MTP Value	80h
HW Reset	MTP Value	80h

Flow Chart



RDID3(DCh) : Read ID3

DCH	RDID3												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	This parameter read byte identifies the TFT LCD module/driver.												
Restriction	-												

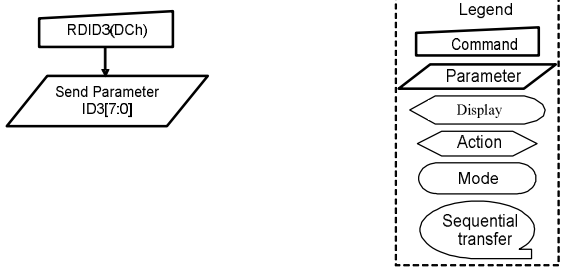
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h

Flow Chart



IFMODE (B0h): Interface Mode Control

B0H	IFMODE												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	1	x	SDA_EN	x	x	x	VSPL	HSPL	DPL	EPL	xx

Description

EPL: DE polarity (“0”= High enable for RGB interface, “1”=Low enable for RGB interface)

DPL: PCLK polarity set (“0”=data fetched at the rising time, “1”=data fetched at the falling time)

HSPL: HSYNC polarity (“0”=Low level sync clock, “1”=High level sync clock)

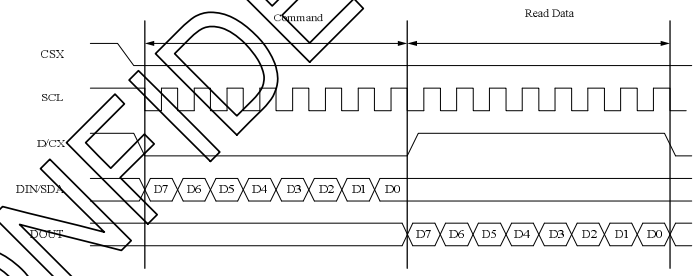
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)

SDA_EN: 3 or 4 wire serial interface selection.

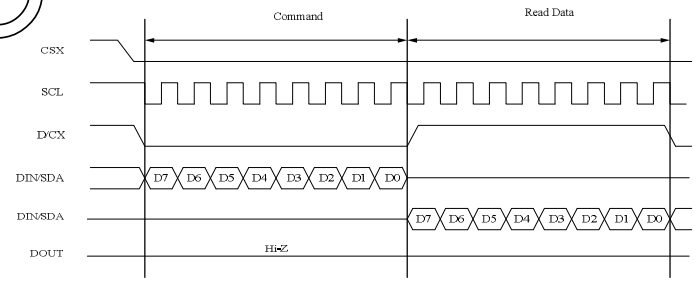
SDA_EN = “0”, DIN and DOUT pins are used for 3/4 wire serial interface.

SDA_EN = “1”, DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used.

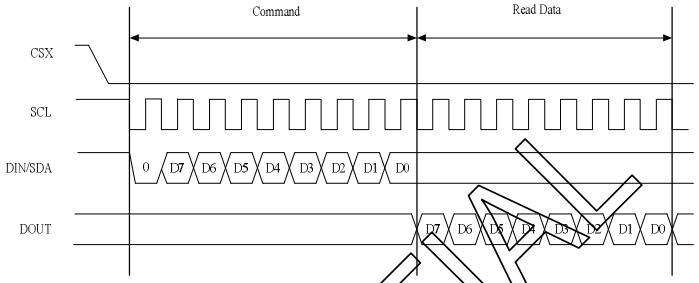
SDA_EN=0



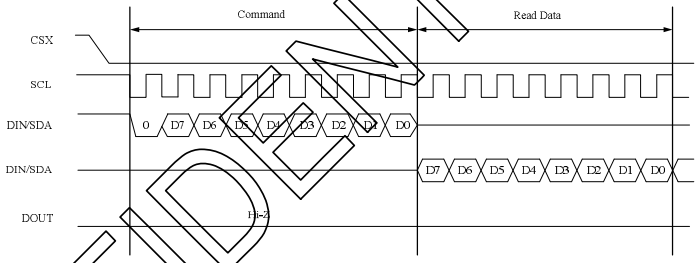
SDA_EN=1



SDA_EN=0



SDA_EN=1



Restriction: -

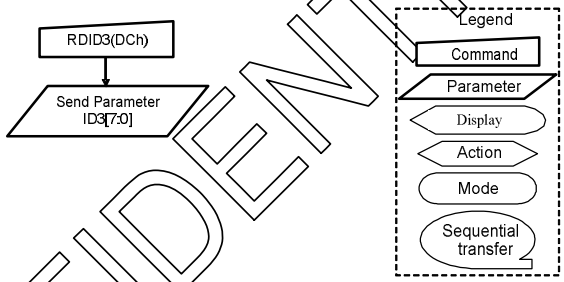
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h

Flow Chart



FRMCTR1 (B1h) : Frame Rate Control (In Normal Mode/Full Colors)

B1H	FRMCTR2 (Frame Rate Control (in Idle Mode/8 Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	0	1	B1
1st Parameter	1	1	↑	x	FRS3	FRS2	FRS1	FRS0	0	0	DIVA1	DIVA0	xx
2nd parameter	1	1	↑	x	0	0	0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0	Xx

Description

FRS[3:0]: Sets the frame frequency of full color normal mode.

RTNB[3:0]	Frame rate(Hz)
0000	28
0001	30
0010	32
0011	34
0100	36
0101	39
0110	42
0111	46

RTNB[4:0]	Frame rate(Hz)
1000	50
1001	56
1010	62
1011	70
1100	81
1101	96
1110	117
1111	117

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Idle mode at CPU interface.

RTNB[4:0]	Clock per Line
00000	Setting prohibited
00001	Setting prohibited
00010	Setting prohibited
00011	Setting prohibited
00100	Setting prohibited
00101	Setting prohibited
00110	Setting prohibited
00111	Setting prohibited
01000	Setting prohibited
01001	Setting prohibited
01010	Setting prohibited
01011	Setting prohibited
01100	Setting prohibited
01101	Setting prohibited
01110	Setting prohibited
01111	Setting prohibited

RTNB[4:0]	Clock per Line
10000	16 clocks
10001	17 clocks
10010	18 clocks
10011	19 clocks
10100	20 clocks
10101	21 clocks
10110	22 clocks
10111	23 clocks
11000	24 clocks
11001	25 clocks
11010	26 clocks
11011	27 clocks
11100	28 clocks
11101	29 clocks
11110	30 clocks
11111	31 clocks

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVA[1:0]	RTNA[4:0]
Power On Sequence	2'b00	5'b10001
HW Reset	2'b00	5'b10001

FRMCTR2 (B2h) : Frame Rate Control (In Idle Mode/8 Colors)

B2H	FRMCTR2 (Frame Rate Control (in Idle Mode/8 Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	1	0	B2
1st Parameter	1	1	↑	x	0	0	0	0	0	0	DIVB1	DIVB0	Xx
2nd parameter	1	1	↑	x	0	0	0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0	Xx

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface.

DIVB [1:0] : division ratio for internal clocks when Idle mode

DIVB[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNB [4:0] : RTNB[4:0] is used to set 1H (line) period of Idle mode at CPU interface.

RTNB[4:0]	Clock per Line	RTNB[4:0]	Clock per Line
00000	Setting prohibited	10000	16 clocks
00001	Setting prohibited	10001	17 clocks
00010	Setting prohibited	10010	18 clocks
00011	Setting prohibited	10011	19 clocks
00100	Setting prohibited	10100	20 clocks
00101	Setting prohibited	10101	21 clocks
00110	Setting prohibited	10110	22 clocks
00111	Setting prohibited	10111	23 clocks
01000	Setting prohibited	11000	24 clocks
01001	Setting prohibited	11001	25 clocks
01010	Setting prohibited	11010	26 clocks
01011	Setting prohibited	11011	27 clocks
01100	Setting prohibited	11100	28 clocks
01101	Setting prohibited	11101	29 clocks
01110	Setting prohibited	11110	30 clocks
01111	Setting prohibited	11111	31 clocks

Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVB[1:0]	RTNB[4:0]
Power On Sequence	2'b00	5'b10001
HW Reset	2'b00	5'b10001

FRMCTR3 (B3h) : Frame Rate Control (In Partial Mode/Full Colors)

B3H	FRMCTR3 (Frame Rate Control (in Partial Mode/Full Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	1	1	B3
1st Parameter	1	1	↑	x	0	0	0	0	0	0	DIVC1	DIVC0	xx
2nd parameter	1	1	↑	x	0	0	0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0	xx

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface.

DIVC [1:0] : division ratio for internal clocks when Partial mode.

DIVC[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNC [4:0] : RTNC[4:0] is used to set 1H (line) period of Partial mode at CPU interface.

RTNB[4:0]	Clock per Line	RTNB[4:0]	Clock per Line
00000	Setting prohibited	10000	16 clocks
00001	Setting prohibited	10001	17 clocks
00010	Setting prohibited	10010	18 clocks
00011	Setting prohibited	10011	19 clocks
00100	Setting prohibited	10100	20 clocks
00101	Setting prohibited	10101	21 clocks
00110	Setting prohibited	10110	22 clocks
00111	Setting prohibited	10111	23 clocks
01000	Setting prohibited	11000	24 clocks
01001	Setting prohibited	11001	25 clocks
01010	Setting prohibited	11010	26 clocks
01011	Setting prohibited	11011	27 clocks
01100	Setting prohibited	11100	28 clocks
01101	Setting prohibited	11101	29 clocks
01110	Setting prohibited	11110	30 clocks
01111	Setting prohibited	11111	31 clocks

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVC[1:0]	RTNC[4:0]
Power On Sequence	2'b00	5'b10001
HW Reset	2'b00	5'b10001

INVTR (B4h) : Display Invrsion Control

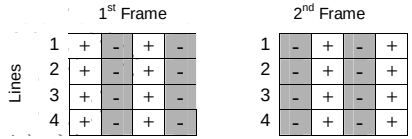
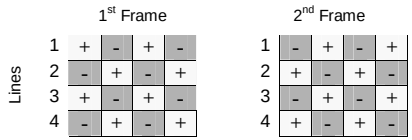
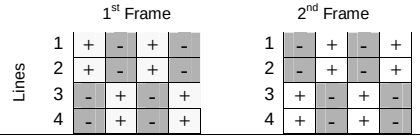
B4H	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	0	0	B4
Parameter	1	1	↑	x	0	0	0	ZINV	0	0	DINV1	DINV0	xx

Description

ZINV : Set Z-inversion mode.

ZINV	Status
0	Disable Z-inversion
0	Enable Z-inversion

DINV[1:0] : Set the inversion mode.

DINV[1:0]	Dot inversion mode	
2'b00	Column inversion	
2'b01	1-dot inversion	
2'b10	2-dot inversion	
2'b11	Setting prohibited	

Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ZINV	DINV[1:0]
Power On Sequence	1'b0	2'b00
HW Reset	1'b0	2'b00

PRCTR (B5h) : Blocking Porch Control

B5H	PRCTR (Blocking Porch Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	0	1	B5
1st Parameter	1	1	↑	x	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	xx
2nd parameter	1	1	↑	x	VBP7	VFB6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	Xx
3rd parameter	1	1	↑	x	0	0	0	HFP4	HFP3	HFP2	HFP1	HFP0	Xx
4nd parameter	1	1	↑	x	HBP7	HFB6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	Xx

Description

VFP [7:0] / VBP [7:0]: The VFP [7:0] and VBP [7:0] bits specify the line number of vertical front and back porch period respectively.

VFP[7:0]	Number of lines of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

VBP[7:0]	Number of lines of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

HFP [4:0] / HBP [7:0]: The HFP [4:0] and HBP [7:0] bits specify the dotclk number of horizontal back porch period.

HFP[4:0]	Number of dotclk of front porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
: :	: :
11100	28
11101	29
11110	30
11111	31

HBP[7:0]	Number of dotclk of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	VFP[7:0]	VBP[7:0]	HFP[7:0]	HBP[7:0]
Power On Sequence	8'b00000010	8'b00000010	8'b00001010	8'b00000100
HW Reset	8'b00000010	8'b00000010	8'b00001010	8'b00000100

DISCTRL (B6h): Display Function Control

B6H	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	1	0	B6
1st parameter	1	1	↑	x	BYPASS	RCM	RM	DM	PTG[1]	PTG[0]	PT[1]	PT[0]	x
2nd parameter	1	1	↑	x	0	GS	SS	SM	ISC[3]	ISC[2]	ISC[1]	ISC[0]	xx
3rd parameter	1	1	↑	x	0	0	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	xx

Description

DM: Select the display operation mode.

DM	Interface Mode
0	Internal system clock
1	RGB Interface

RM: Select the interface to access the GRAM.

RM	Interface for GRAM access
0	via System interface
1	via RGB interface

RCM: RGB interface selection.

RCM	RGB transfer mode
0	DE Mode
1	SYNC Mode

BYPASS: Select the display data path, when RGB interface is used.

BYPASS	Display data path
0	Memory
1	Direct to shift register

PTG[1:0]: Sets the scan mode in non-display area.

PTG[1]	PTG[0]	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with PT[2:0]
0	1	Setting prohibited	--
1	0	Interval	Set with PT[2:0]
1	1	Setting prohibited	--

PT[1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT[1]	PT[0]	Source outputs in non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: select the shift direction of outputs from the source driver.

SS	Source output scan direction
0	S1 à S960
1	S960 à S1

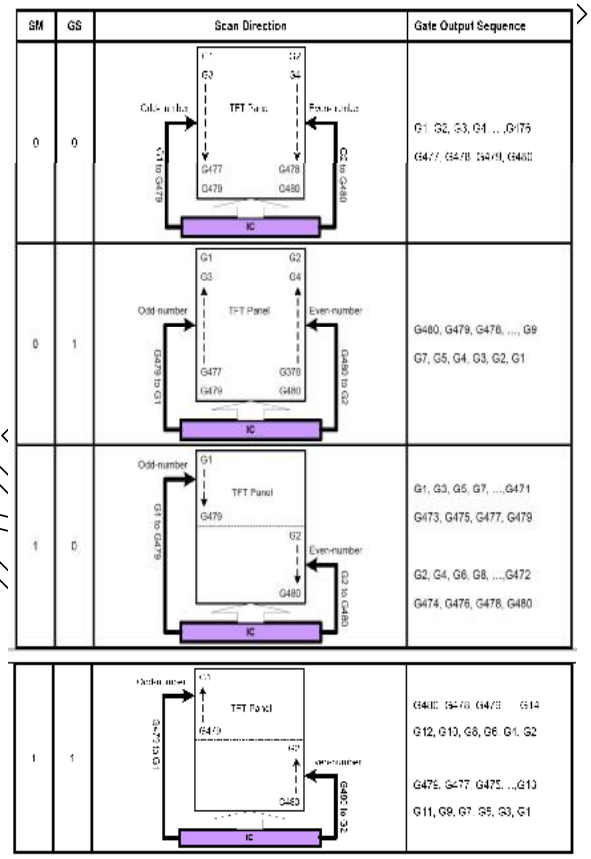
ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(fFRAME)=60Hz
4'h0	Setting inhibited	—
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

GS: select the direction of scan by the gate driver.

GS	Source output scan direction
0	G1 **à** G480
1	G480 **à** G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.



NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL5:0]+1) lines
Others	Setting inhibited

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value						
	PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]
Power On Sequence	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011
HW Reset	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011

Status	Default Value		
	RM	DM	BYPASS
Power On Sequence	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

ETMOD (B7h) : Entry Mode Set

B7H	Interface Mode Control												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	1	1	B7
Parameter	1	1	↑	x	EPF[1]	EPF[0]	0	0	DSTB	GON	DTE	GAS	xx

Description

DSTB: enter the Deep Standby Mode when DSTB = "1". In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Staandby Mode is exited.

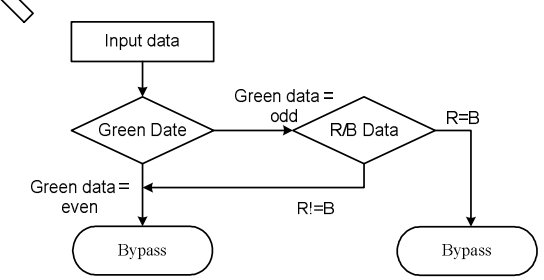
GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1~G320 as follows

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

EPF[1:0]: set the data format when 16bbp(R,G,B) to 18bbp(R,G,B) is stored in the internal GRAM



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	EPF[1:0]	DSTB	GON	DTE	GAS
Power On Sequence	2'b00	1'b0	1'b1	1'b1	1'b0
HW Reset	2'b00	1'b0	1'b1	1'b1	1'b0

PWCTRL1 (C0h): Power Control 1

C0H	PWCTRL1 (Power Control 1)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1st parameter	1	1	↑	x	0	0	0	VRH1[4]	VRH1[3]	VRH1[2]	VRH1[1]	VRH1[0]	xx
2nd parameter	1	1	↑	x	0	0	0	VRH2[4]	VRH2[3]	VRH2[2]	VRH2[1]	VRH2[0]	xx

Description

VRH1[4:0]: Sets the VREG1OUT voltage for positive gamma

VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT
5'h00	Halt	5'h10	1.25 x 3.65 = 4.5625V
5'h01	1.25 x 2.90=3.6250V	5'h11	1.25 x 3.70 = 4.6250V
5'h02	1.25 x 2.95 = 3.6875V	5'h12	1.25 x 3.75 = 4.6875V
5'h03	1.25 x 3.00 = 3.7500V	5'h13	1.25 x 3.80 = 4.7500V
5'h04	1.25 x 3.05 = 3.8125V	5'h14	1.25 x 3.85 = 4.8125V
5'h05	1.25 x 3.10 = 3.8750V	5'h15	1.25 x 3.90 = 4.8750V
5'h06	1.25 x 3.15 = 3.9375V	5'h16	1.25 x 3.90 = 4.8750V
5'h07	1.25 x 3.20 = 4.0000V	5'h17	1.25 x 4.00 = 5.0000V
5'h08	1.25 x 3.25 = 4.0625V	5'h18	1.25 x 4.05 = 5.0625V
5'h09	1.25 x 3.30 = 4.1250V	5'h19	1.25 x 4.10 = 5.1250V
5'h0A	1.25 x 3.35 = 4.1875V	5'h1A	1.25 x 4.15 = 5.1875V
5'h0B	1.25 x 3.40 = 4.2500V	5'h1B	1.25 x 4.20 = 5.2500V
5'h0C	1.25 x 3.45 = 4.3125V	5'h1C	1.25 x 4.25 = 5.3125V
5'h0D	1.25 x 3.50 = 4.3750V	5'h1D	1.25 x 4.30 = 5.3750V
5'h0E	1.25 x 3.55 = 4.4375V	5'h1E	1.25 x 4.35 = 5.4375V
5'h0F	1.25 x 3.60 = 4.5000V	5'h1F	1.25 x 4.40 = 5.5000V

VRH2[4:0]: Sets the VREG2OUT voltage for positive gamma

VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT
5'h00	Halt	5'h10	-1.25 x -3.65 = -4.5625V
5'h01	-1.25 x 2.90=-3.6250V	5'h11	-1.25 x -3.70 = -4.6250V
5'h02	-1.25 x 2.95 = -3.6875V	5'h12	-1.25 x -3.75 = -4.6875V
5'h03	-1.25 x 3.00 = -3.7500V	5'h13	-1.25 x -3.80 = -4.7500V
5'h04	-1.25 x 3.05 = -3.8125V	5'h14	-1.25 x -3.85 = -4.8125V
5'h05	-1.25 x 3.10 = -3.8750V	5'h15	-1.25 x -3.90 = -4.8750V
5'h06	-1.25 x 3.15 = -3.9375V	5'h16	-1.25 x -3.90 = -4.8750V
5'h07	-1.25 x 3.20 = -4.0000V	5'h17	-1.25 x -4.00 = -5.0000V
5'h08	-1.25 x 3.25 = -4.0625V	5'h18	-1.25 x -4.05 = -5.0625V
5'h09	-1.25 x 3.30 = -4.1250V	5'h19	-1.25 x -4.10 = -5.1250V
5'h0A	-1.25 x 3.35 = -4.1875V	5'h1A	-1.25 x -4.15 = -5.1875V
5'h0B	-1.25 x 3.40 = -4.2500V	5'h1B	-1.25 x -4.20 = -5.2500V
5'h0C	-1.25 x 3.45 = -4.3125V	5'h1C	-1.25 x -4.25 = -5.3125V
5'h0D	-1.25 x 3.50 = -4.3750V	5'h1D	-1.25 x -4.30 = -5.3750V
5'h0E	-1.25 x 3.55 = -4.4375V	5'h1E	-1.25 x -4.35 = -5.4375V
5'h0F	-1.25 x 3.60 = -4.5000V	5'h1F	-1.25 x -4.40 = -5.5000V

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	VRH1[4:0]=5'h0E, VRH2[4:0]=5'h0E
SW Reset	No change
HW Reset	VRH1[4:0]=5'h0E, VRH2[4:0]=5'h0E

PWCTRL2 (C1h): Power Control 2

C1H	PWCTRL2 (Power Control 2)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	x	0	0	0	0	0	BT[2]	BT[1]	BT[0]	Xx
2nd parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	Xx

Description

VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1.

VC[2:0]	Vci1 voltage
3'h0	1.0 x Vci
3'h1	3.1 V
3'h2	3.0 V
3'h3	2.9 V
3'h4	2.8 V
3'h5	2.7 V
3'h6	2.6 V
3'h7	2.5 V

BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci.

BT[2:0]	DDVDH	DDVDL	VCL	VGH	VGL
3'h0	Vci1x 2	-5V	- Vci	Vci x 6	- Vci x 5
3'h1					- Vci x 4
3'h2					- Vci x 3
3'h3				Vci x 5	- Vci x 5
3'h4					- Vci x 4
3'h5					- Vci x 3
3'h6				Vci x 4	- Vci x 4
3'h7					- Vci x 3

	Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages. Note 2: Set following voltages within the respective ranges: DDVDH = 6.0V (max) VGH = 18.0V (max) VGL= -12.5V (max) VCL= -3.6 (max).
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VC[2:0]=3'h0, BT[2:0]=3'h0
SW Reset	No change
HW Reset	VC[2:0]=3'h0, BT[2:0]=3'h0

PWCTRL3 (C2h): Power Control 3 for Normal Mode

C2H	PWCTRL3 (Power Control 3 for Normal Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	x	DCA1[3]	DCA1[2]	DCA1[1]	DCA1[0]	DCA0[3]	DCA0[2]	DCA0[1]	DCA0[0]	xx

Description

DCA0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Normal mode.

DCA0[3]	DCA0[2:0]	Step-up cycle for Step-up circuit 1/2
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCA1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Normal mode.

DCA1[3]	DCA1[2:0]	Step-up cycle for Step-up circuit 3
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DCA0[3:0]=4'b0011, DCA1[2:0]=4'b0100
SW Reset	No change
HW Reset	DCA0[3:0]=4'b0011, DCA1[2:0]=4'b0100

PWCTRL4 (C3h): Power Control 4 for Idle Mode

C3H	PWCTRL4 (Power Control 4 for Idle Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	x	DCB1[3]	DCB1[2]	DCB1[1]	DCB1[0]	DCB0[3]	DCB0[2]	DCB0[1]	DCB0[0]	xx

Description

DCB0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Idle mode.

DCB0[3]	DCB0[2:0]	Step-up cycle for Step-up circuit 1/2
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCB1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Idle mode.

DCB1[3]	DCB1[2:0]	Step-up cycle for Step-up circuit 3
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

Register availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: DCB0[3:0]=4'b0011, DCB1[2:0]=4'b0100 SW Reset: No change HW Reset: DCB0[3:0]=4'b0011, DCB1[2:0]=4'b0100

PWCTRL5 (C4h): Power Control 5 for Partial Mode

C4H	PWCTRL5 (Power Control 5 for Partial Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	x	DCC1[3]	DCC1[2]	DCC1[1]	DCC1[0]	DCC0[3]	DCC0[2]	DCC0[1]	DCC0[0]	Xx

Description

DCC0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Partial mode.

DCC0[3]	DCC0[2:0]	Step-up cycle for Step-up circuit 1/2
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCC1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Partial mode.

DCC1[3]	DCC1[2:0]	Step-up cycle for Step-up circuit 3
1'b1	3'b000	1/8 H
1'b1	3'b001	1/4 H
1'b1	3'b010	1/2 H
1'b1	3'b011	1 H
1'b1	3'b100	2 H
1'b1	3'b101	4 H
1'b1	3'b110	8 H
1'b1	3'b111	16 H
1'b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	DCC0[3:0]=4'b0011, DCC1[2:0]=4'b0100
SW Reset	No change
HW Reset	DCC0[3:0]=4'b0011, DCC1[2:0]=4'b0100

VCOM Control (C5h)

C5H	VCOM Control												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	C5
1st parameter	1	↑	1	x	0	0	0	0	0	0	0	NVM	xx
2nd parameter	1	1	↑	x	VCM_REG[7]	VCM_REG[6]	VCM_REG[5]	VCM_REG[4]	VCM_REG[3]	VCM_REG[2]	VCM_REG[1]	VCM_REG[0]	xx
3rd parameter	1	1	↑	x	VCM_REG_EN	0	0	0	0	0	0	0	xx
4rd parameter	1	↑	1	x	VCM_OUT[7]	VCM_OUT[6]	VCM_OUT[5]	VCM_OUT[4]	VCM_OUT[3]	VCM_OUT[2]	VCM_OUT[1]	VCM_OUT[0]	xx

Description

NVM : When the NV memory is programmed, the NVM will be set as '1' automatically.

0 : NV memory is not programmed
1 : NV memory is programmed

VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM
8'h00	-2	8'h20	-1.5
8'h01	-1.98438	8'h21	-1.48438
8'h02	-1.96875	8'h22	-1.46875
8'h03	-1.95313	8'h23	-1.45313
8'h04	-1.9375	8'h24	-1.4375
8'h05	-1.92188	8'h25	-1.42188
8'h06	-1.90625	8'h26	-1.40625
8'h07	-1.89063	8'h27	-1.39063
8'h08	-1.875	8'h28	-1.375
8'h09	-1.85938	8'h29	-1.35938
8'h0A	-1.84375	8'h2A	-1.34375
8'h0B	-1.82813	8'h2B	-1.32813
8'h0C	-1.8125	8'h2C	-1.3125
8'h0D	-1.79688	8'h2D	-1.29688
8'h0E	-1.78125	8'h2E	-1.28125
8'h0F	-1.76563	8'h2F	-1.26563
8'h10	-1.75	8'h30	-1.25
8'h11	-1.73438	8'h31	-1.23438
8'h12	-1.71875	8'h32	-1.21875
8'h13	-1.70313	8'h33	-1.20313
8'h14	-1.6875	8'h34	-1.1875
8'h15	-1.67188	8'h35	-1.17188
8'h16	-1.65625	8'h36	-1.15625
8'h17	-1.64063	8'h37	-1.14063
8'h18	-1.625	8'h38	-1.125
8'h19	-1.60938	8'h39	-1.10938
8'h1A	-1.59375	8'h3A	-1.09375
8'h1B	-1.57813	8'h3B	-1.07813
8'h1C	-1.5625	8'h3C	-1.0625
8'h1D	-1.54688	8'h3D	-1.04688
8'h1E	-1.53125	8'h3E	-1.03125
8'h1F	-1.51563	8'h3F	-1.01563

VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM
8'h40	-1	8'h62	-0.46875
8'h41	-0.98438	8'h63	-0.45313
8'h42	-0.96875	8'h64	-0.4375
8'h43	-0.95313	8'h65	-0.42188
8'h44	-0.9375	8'h66	-0.40625
8'h45	-0.92188	8'h67	-0.39063
8'h46	-0.90625	8'h68	-0.375
8'h47	-0.89063	8'h69	-0.35938
8'h48	-0.875	8'h6A	-0.34375
8'h49	-0.85938	8'h6B	-0.32813
8'h4A	-0.84375	8'h6C	-0.3125
8'h4B	-0.82813	8'h6D	-0.29688
8'h4C	-0.8125	8'h6E	-0.28125
8'h4D	-0.79688	8'h6F	-0.26563
8'h4E	-0.78125	8'h70	-0.25
8'h4F	-0.76563	8'h71	-0.23438
8'h50	-0.75	8'h72	-0.21875
8'h51	-0.73438	8'h73	-0.20313
8'h52	-0.71875	8'h74	-0.1875
8'h53	-0.70313	8'h75	-0.17188
8'h54	-0.6875	8'h76	-0.15625
8'h55	-0.67188	8'h77	-0.14063
8'h56	-0.65625	8'h78	-0.125
8'h57	-0.64063	8'h79	-0.10938
8'h58	-0.625	8'h7A	-0.09375
8'h59	-0.60938	8'h7B	-0.07813
8'h5A	-0.59375	8'h7C	-0.0625
8'h5B	-0.57813	8'h7D	-0.04688
8'h5C	-0.5625	8'h7E	-0.03125
8'h5D	-0.54688	8'h7F	-0.01563
8'h5E	-0.53125	8'h80	0
8'h5F	-0.51563	8'h81~8'hFE	Inbibit
8'h60	-0.5	8'hFF	Halt
8'h61	-0.48438		

VCM_REG_EN: Select the Vcom value from VCM_REG [7:0] or NV memory.

0: VCOM value from NV memory.
1: VCOM value from VCM_REG [7:0].

VCM_OUT [7:0]: NV memory programmed value.

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	VCM_REG[7:0]=8'hC0, VCM_REG_EN=1'b0
SW Reset	No change
HW Reset	VCM_REG[7:0]=8'hC0, VCM_REG_EN=1'b0

NVMWR (D0h): NV Memory Write

D0H	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0
1st parameter	1	1	↑	x	VM_D[7]	VM_D[6]	VM_D[5]	VM_D[4]	VM_D[3]	VM_D[2]	VM_D[1]	VM_D[0]	xx
Description	This command is used to program the NV memory data. VM_D[7:0]: Use to write the data (including VCM and ID code) into the NV memory data.												

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	VM_D[7:0]=8'h00
SW Reset	No change
HW Reset	VM_D[7:0]=8'h00

NVMPKEY (D1h): NV Memory Protection

D1H	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1st parameter	1	1	↑	x	KEY[23]	KEY[22]	KEY[21]	KEY[20]	KEY[19]	KEY[18]	KEY[17]	KEY[16]	55
2nd parameter	1	1	↑	x	KEY[15]	KEY[14]	KEY[13]	KEY[12]	KEY[11]	KEY[10]	KEY[9]	KEY[8]	AA
3rd parameter	1	1	↑	x	KEY[7]	KEY[6]	KEY[5]	KEY[4]	KEY[3]	KEY[2]	KEY[1]	KEY[0]	66
Description	KEY[23:0]: NV memory programming protection key. When writing OTP data, this register must be set as 0x55AA66 to enable OTP programming. If register is not written with 0x55AA66, NV memory programming will fail.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Availability
Power On Sequence	KEY[23:0]=24'h55AA66
SW Reset	No change
HW Reset	KEY[23:0]=24'h55AA66

RDNVM (D2h): NV Memory Status Read

D2H	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	1	0	D2
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	x	0	0	0	0	0	0	PGM_CNT1	PGM_CNT0	xx
3rd parameter	1	↑	1	x	NV_VCM[7]	NV_VCM[6]	NV_VCM[5]	NV_VCM[4]	NV_VCM[3]	NV_VCM[2]	NV_VCM[1]	NV_VCM[0]	xx
Description	PGM_CNT[1:0]: NV memory programmed record. The bit will increase "+1" automatically when writing the NV_VCM [7:0].												
Restriction													

Description

PGM_CNT[1:0]	Description
00	NV Memory clean
01	NV Memory programmed 1
10	NV Memory programmed 2

These bits are read only.

NV_VCM [7:0]: NV memory VCM data read value. These bits are read only.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

RDID2(D3h) : Read ID4

D3H	RDID4 (Read ID4)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	xx	ID41[7]	ID41[6]	ID41[5]	ID41[4]	ID41[3]	ID41[2]	ID41[1]	ID41[0]	00
3rd parameter	1	↑	1	xx	ID42[7]	ID42[6]	ID42[5]	ID42[4]	ID42[3]	ID42[2]	ID42[1]	ID42[0]	94
4th parameter	1	↑	1	xx	ID43[7]	ID43[6]	ID43[5]	ID43[4]	ID43[3]	ID43[2]	ID43[1]	ID43[0]	86
Description	Read ID device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID4=24'h009486h
SW Reset	No change
HW Reset	ID4=24'h009486h

Gamma Setting (E0h)

E0H	Gamma Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	1	0	0	0	E0
1st parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	00
2nd parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	44
3rd parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	06
4th parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	44
5th parameter	1	1	↑	x	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	0A
6th parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	08
7th parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	17
8th parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	33
9th parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	77
10th parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	44
11th parameter	1	1	↑	x	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	08
12th parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0C
Description	KP5-0[2:0] : γ fine adjustment register for positive polarity RP1-0[2:0] : γ gradient adjustment register for positive polarity VRP0[4:0], VRP1[4:0] : γ amplitude adjustment register for positive polarity KN5-0[2:0] : γ fine adjustment register for negative polarity RN1-0[2:0] : γ gradient adjustment register for negative polarity VRN0[4:0], VRN1[4:0] : γ amplitude adjustment register for negative polarity												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default		

Status	Default Value
Power On Sequence	As above
SW Reset	No change
HW Reset	As above