Raydium

8. Command

8.1. Command List

Operational	Command	Command(C)	Number Of
Code (Hex)		/Read(R) /Write(W)	Parameter
00h	nop	C	0
01h	soft_reset	c //	0
04h	get_display_ID	R	/3
05h	get_DSI_err	18	// 1
09h	read_display_status		× 4
0Ah	get_power_mode	> \\	1
0Bh	get_address_mode	\\R\\	1
0Ch	get_pixel_format	/ K),	1
0Dh	get_display_mode	\\ R	1
0Eh	get_signal_mode	∨ R	1
0Fh	get_diagnostic_result	R	1
10h	enter_sleep_mode	C	0
11h	exit_sleep_mode	С	0
12h	enter_partial_mode	С	0
13h	enter_normal_mode	С	0
20h	exit_invert_mode	С	0
21h	enter_invert_mode()	С	0
28h	set_display_off	С	0
29h	set_display_on	С	0
2Ah	set_column_address	W	4
2Bh	set_page_address	W	4
2Ch	write_memory_stark	W	Variable
2Eh	read_memory_start	R	Variable
30h	set partial area	W	4
33h (set scholl sivea	W	6
34h	set tear off	С	0
(35h)	set tear on	W	1
((36h 🔨	set_address_mode	W	1
38h	exit idle mode	C	0
391	enter idle mode	C	0
3Ah	set_pixel_format	W	1
3Ch	write_memory _continue	W	Variable
3Eh	read_memory _continue	R	Variable
44h	set_tear_scanline	W	2
45h	get_scanline	R	2
51h	set_display_brightness	W	1
52h	get_display_brightness	R	1
53h	set_control_display	W	1

Operational Command(C) **Number Of** Command Code (Hex) /Read(R)/Write(W) Parameter 54h get_control_display R 55h W 1 set_cabc_mode 56h get_cabc_mode R 1 W 5Eh set_cabc_min_brightness 1 get cabc min brightness R AAh read_first_checksum 1 AFh read_continue_checksum R / 1 DAh read_ID1 R DBh read ID2 read_ID3 DCh B0h Interface_mode_control ωV B1h 2 frame_rate_control (in normal mode) B2h frame rate control (in idle mode/8 colors) 2 B3h frame_rate_control (in partial mode) 2 B4h display_inversion_control W 1 B5h blanking_porch_control W 4 display_function_control W 3 B6h W B7h entry_mode_set 1 BFh device_code_read R 5 W 2 C0h power_control_1 C1h power_control_2 W 2 C2h power_control_3 W 1 W C4h power control 4 1 W C5h vcom_control_1 4 D0h nv_memory_write W 2 D1h nv_memory_protection_key W 3 D2h nv_memory_status_read R 3 read 4D4 R D3h 3 Gamma setting E0h W 15

8.2. Command Description

NOP (00h)

00H					NO	P (No	Operat	tion)								
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	0	1	1	X	0	0	0	0	0	0	0	0	00			
Parameter	NO P	ARAME	TER							_						
Description	Howe	ver it ca	an be us	empty comn ed to termin RAMRD (Me	ate Fra	ame Me	emory \	Write o		`						
	X = D	on't car	e.					/)`		\ <u>\</u>	~					
Restriction	None								/	7/						
								7		<u> </u>						
				Status Availability												
			Norma	Normal Mode On, Idle Wode Off, Sleep Out Yes												
Register			Normal Mode On, Idle Mode Off Sleep Out Yes Normal Mode On, Idle Mode On, Sheep Out Yes													
Availability																
			Partia	KMode On, 1	dle)Mo	de On,	Sleep	Out	`	⁄es						
					leep Ir	1			,	⁄es						
			\bigcirc	<i>> ></i>												
	~	_//						D /								
	//	/_	<u> </u>	Sta	atus			Derau	lt Value	9						
5			L	Power On	Seque	ence		Ν	I/A							
Default	`)) ~		SW I	Reset			N	I/A							
				HW I	Reset			N	I/A							
)		,													
Flow Chart	None															



SWRESET(01h) : Software Reset

OWNED	-1 (0111)	. 301tw	are Re	3EL									
01H					SWRES	SET(S	oftware	Rese	t)				
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	Х	0	0	0	0	0	0	0	1	01
Parameter	No pa	ramete	r										
Description	comm comm Note:	nands a	nd parar scriptior ame Me	Reset commanders to the command to t	eir S/W	Reset	defaul	t value	s. (See				ch
Restriction	5ms. before	If Softw	are Res ng Sleep	oads all disp et is applied Out comma	during	Sleep	Qutm	ode, it	will be	necess	ary to	wait 12	:0ms
Register Availability			Norma	I Mode On, I Mode On, I Mode On, I	dle Mo	de Off, de On,	Sleep	Out Out)	res res res res res res res res res			
petault			,	Power On	Seque Reset Reset	nce		N	it Value I/A I/A	9			

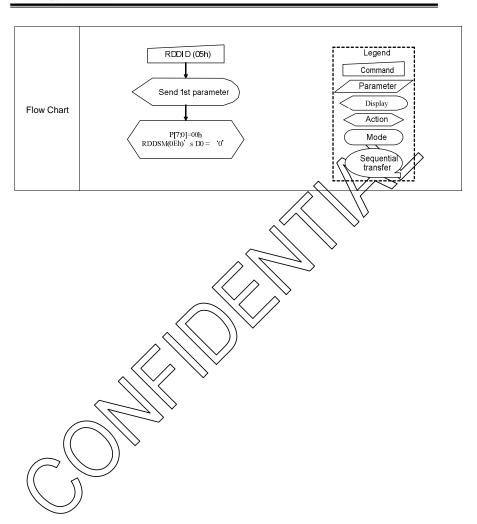
RDDIDIF	(0411) :	Read D	ispiay	טו									
04H						RDE	DIDIF						
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	00h	0	0	0	0	0	1	0	0	04
1 st parameter	1	1	1	Х	х	х	х	х	х	х	х	х	Χ
2 nd parameter	1	1	1	00h	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	54
3 rd parameter	1	1	1	00h	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	80
4 th parameter	1	1	1	00h	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	1D3[2]	NQ3[1]	ID3[0]	66
Parameter	-								7			//_	
	The 1	st paran	neter (ID	1): dummy	data.			^	\ \	$\backslash \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	<i>>></i>		
	The 2	nd parar	neter (II	D2): the LCE) modu	ıle's ma	anufact	MeJD					
Description	The 3	rd paran	neter (II	03): the LCD	modu	le/drive	r versi	gh yb		γ_{\wedge}			
	The 4	th paran	neter (IE	04): the LCD	modu	le/drive	r VQ	/					
						(=	=-/		~				
Restriction	-							\rightarrow					
				Stati	15	\rightarrow			۸	vailabi	lity		
						\//	,				шу		
		Nor	mal Mo	de On, Idle	уюде (Xff, Sele	ep Out			Yes			
Register		Nor	mal Mo	de On, lale	Model (On, Sle	ep Out			Yes			
Availability		Par	rtial Mo	de On, Idle I	Mode C	Off, Slee	ep Out			Yes			
		(Pa	rtial Mo	de On, Idle I	Mode C	n, Sle	ep Out			Yes			
			7/	Sleep	ln .					Yes			
	=	\mathbb{R}	\Rightarrow										
((1//	,										
))		Status				Default	Value				
	\smile		Pov	ver On Sequ	ence	ID	1=54h	/ ID2=8	80h / II	D3=66h	1		
Default)			SW Reset		ID	1=54h	/ ID2=8	80h / II	D3=66h	1		
				HW Reset		ID	1=54h	/ ID2=8	80h / II	D3=66h	1		
						1							

RDNUMED(05h): Read Number of Errors on DSI

KDNOWE	-D(0311)	. Keau	Nullib	ei oi Eilois	on Da)I								
05H				RDNUME) (Rea	d Num	ber of	the Er	ror on	DSI)				
	DCX	RDX	WRX	D15-D8	x 0 0 0 0 0 1 0 1 05 x P[7] P[6] P[5] P[4] P[3] P[2] P[1] P[0] 00 elling a number of the parity errors on DSI. The more detailed low. Index of the parity errors. Diverflow with P[60] bits. as well as RDDSM(0Eh)'s Defare set '0" at the same time) after arameter information (—The read function is completed). MIPI DSI only. It is no function for others interface operation. Status Availability © On, Idle Mode Off, Sleep Out Yes E On, Idle Mode On, Sleep Out Yes									
Command	0	1	1	х	0	0	0	0	0	1	0	1	05	
1 st parameter	1	1	1	х	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]	00	
Parameter	NO P	ARAME	TER											
Description	descr P[60 P[7] is P[70 there	iption of iption of ibits ar s set to ibits ar is sent	the bits re telling "1" if the re set to the seco	s is below. g a number of the area is overflow "0"s (as welcomed parameter)	of the pa ow with I as RE er infor	arity er P[60] DDSM(mation	rors. bits. 0Eh)'s	Dø are	set Q	" at the	same	time) a	fter	
Restriction	-	is command is used for MIPI DSI only. It is no function for others interface operation.												
					Status	/			Ava	ilability	,			
			Norma	al Mode On,	palg/Wg	ode Off	, Sleep	Out	,	Yes				
Register			Norma	Node Qn,	Idle Mc	ode On	, Sleep	Out	,	Yes				
Availability		<	Partia	LMode On,	øle Mo	de Off,	Sleep	Out	,	Yes				
			Rantia	l Mode On, I	dle Mo	de On,	Sleep	Out	,	Yes				
	_ <			> s	Sleep Ir	1			,	Yes				
))	· [atus				It Valu	е				
Default				Power On		ence			0h					
)			SW I	Reset			0	0h					
				HW I	Reset			0	0h					

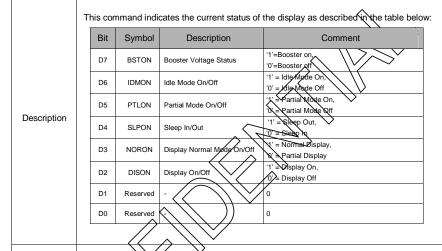
RDDST (09h): Read Display Status

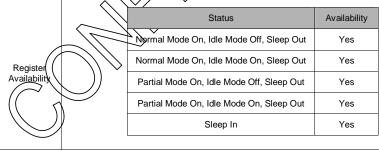
		ead Displa	, c.a.us										
09H				RDD	ST (Re	ad Di	splay	Status)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	0	1	0	0	1	09
1 st parameter	1	1	1	х	х	х	х	х	х	х	х	х	xx
2 nd parameter	1	1	1	х	D31	D30	D29	D28	D27	D26	D25	0	xx
3 rd parameter	1	1	1	х	0	D22	D21	D20	D19	Ф'n	D17	D16	XX
4 th parameter	1	1	1	х	D15	0	D13	0	Q	D10	Æ9	<i>P</i> 78	xx
5 th parameter	1	1	1	х	D7	D6	D5	0	18	12/2	\8\\	0	XX
	This co	mmand ind	licates th	e current	status	of the	displa	y a code	escribe	d in th	etable	e belov	/ :
	Bit	Symbol		Descriptio	n	V	alue		S	tatus			
	D31	BSTON	Boos	ster Voltage	Statue		8		₽ø	oster of	f		
	551	BOTON	5000	ster vortage	Otatus	Booster on Top¹to Bottom (36H- D7='0') Bottom to Top (36H-D7='1') Left to Right (MADCTL D6='0') Right to Left (MADCTL D6='1') Normal (36H-D5='1')							
	D30	MY	Ro	w Address (Order	\neq	Booster off						
					\nearrow	X	0						
	D29	MX	Colu	ımn Address	Order	> <	Ž						
	D28	MV	Pow/	Column Ord	or (M)		0						
	D26	IVIV	KOW/	Column	EI KNIA)		1	Row/co	olumn ex	change	(36H-D5	i='1')	
	D27	ML	√ _e k	ical Refresh	drder	/_						_	
)		0	LC	D Refre		o Botton	n	
	D26	RGE	1/4	GBABORO	der		1			RGB BGR			
	D25	\ <u>\</u>	Horiz	ontal Refres	h Ordor		0	LC	D Refre	esh Left	to Right		
	D25		HOIIZ	onerReires	n Order		1	LC	D Refre	esh Righ	t to Left		
Description	D22	// /	NOBI E	ixel Formati	Control		101		16-1	bits / pix	el		
2000	(D21	TEPP(2:0)		face Color F		-	110		18-1	oits / pix	el		
	D20	\nearrow	1			ot	hers			-	.,		
((<i>p</i> /3	DOMOD	lo	lle Mode On	/Off		0			Mode O Mode O			
\sim //) 					0			l Mode (
		PTLON	Pa	rtial Mode O	n/Off		1		Partia	l Mode (On		
(()	\						0		S	leep In			
	D17	SLPOUT		Sleep In/O	ut		1			eep Out			
	D16	NORON	Diaploy	Normal Ma	do On/O	"	0		Parti	al Displa	ay		
	D10	NOKON	Display	Normal Mo	ue On/O	"	1		Norm	nal Displ	ay		
	D15	VSSON	Vertic	cal scrolling	status		0			crolling			
							1		/ertical:	scrolling	is On		
	D13	INVON	In	version On/0	Off		0			sion is (
		1					1			sion is (
	D10	DISPON		Display On/0	Off		0			splay Of			
							1		Dis	splay On	ı		



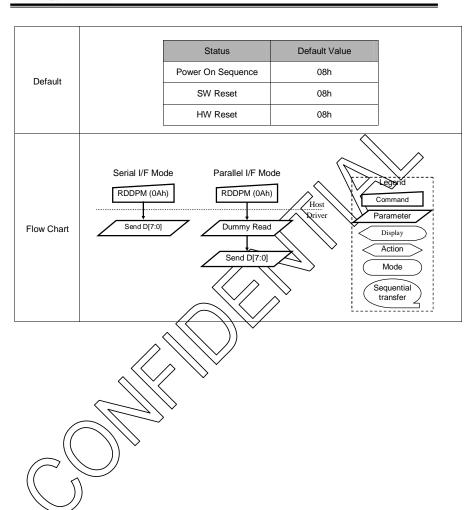
RDDPM (0Ah): Read Display Power Mode

0AH			R	DDPM (R	ead D	isplay	Pow	er Mo	de)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	0	1	0	1	0	0A
1 st parameter	1	1	1	х	D7	D6	D5	D4	D3	D2	0	0	08

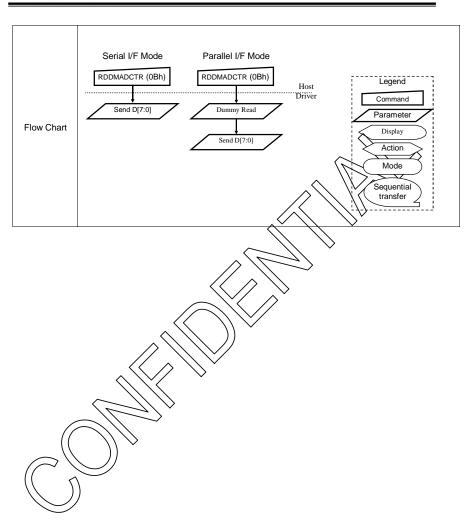




TODAII, C	70 IN (0B	ny. Roda E	ropidy iii										
0BH			RI	DDMADC	TR (R	ead D	isplay	MAD	CTR)				
	DCX	RDX	WRX	D15-8	### ADDITECT Comment C		HE						
Command	0	1	1	х	0	0	0	0	1	0	1	1	OE
1 st parameter	1	1		0	00								
	Bit	Symbol	D	escription	t status	'1' =	Bottom	C to Top	ommer	nt	the ta	ble be	low:
					er	'1' =	Right to	Left (N	IADICTL	D8='4')	ŠŤ		
	D5	MV	Row/Colu	mn Order (M	/IV)	'1' =	Rowco	lumn e	change		5='1')		
Description	D4	ML	Vertical R	efresh Orde	r	'1'€	LED RE	nesh To	op to Bo	tom Top			
	D3	RGB	RGB/BGF	R Order	~		77.		>				
	D2	MH	Horizonta	Refresh Or	øler	·1'=	LCD R	fresh L et esh R	eft to Ri light to I	ght _eft			
				$\prec \! \langle$	/	8/	>						
					<u>) </u>						_		
				Statu	IS				Availa	bility			
		Nore	nal Mode	On, Idle N	Mode C	Off, Sle	еер О	ut	Ye	s			
Register	(1	Moli	nalMode	On, Idle N	Mode C	n, Sle	еер О	ut	Ye	s			
Availability		Part	ial Mode	On, Idle M	lode C	ff, Sle	ep Ou	t	Ye	s			
		Part	ial Mode	On, Idle M	Node C	n, Sle	ep Ou	t	Ye	s			
				Sleep	In				Ye	s			
				Status				Defa	ault Va	lue			
	D5 MV Row/Columbia Power D5 MV Row/Columbia D4 ML Vertical R D3 RGB RGB/BGF D2 MH Horizonta D1 Reserved D0 Reserved Normal Mode Partial Mode Partial Mode Partial Mode Power D5 Market Power D5 MV Row/Columbia D5 MV Row/Colu		On Seque	ence				00h					
Default			SI	N Reset				No	Chan	ge			



0CH			R	DDCOLM	OD (R	ead [Display	Pixel	Forma	it)			
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	Х	0	0	0	0	1	1	0	0	0C
1 st parameter	1	1	1	Х	D7	D6	D5	D4	0	D2	D1	D0	66
	This co	mmand in	dicates th	ne current	status	of th	ne displa	y as d	escrib	ed in th	ne table	e belo	N:
	Bit	Symbol		Descriptio	n			(Comme	ent			
	D7	VIPF[3]							<i>(</i> -			\nearrow	
	D6	VIPF[2]	DPI Pix	el Format(R	GB	٠,	0101' = 16	-bits / piz	cel,	>	\mathcal{N}		
	D5	VIPF[1]	Interfac	e Color For	mat)	٥,	0110' = 18 others are	reserve	cel, \	$\langle \langle \rangle$	~		
Description	D4	VIPF[0]	erved -							>//			
2 ccomparent	D3	Reserved	IFPF[2]						\	•			
	D2	DBI Pixel Format(Control											
	D1	DBI Pixel Formati (Control Interface Color Formati)					N0' = 18-1		el,				
	D0	IFPF[0]		$\langle \langle$	$\sqrt{/}$		onners are	reserve	a				
		DI IFPF[1] DBI Pixel Formati(Control Interface Color Format) No' = 18-bits / pixel, Others are reserved											
			~/	+)								
				Sta	itus				Avail	ability			
		\ \mathready	ngal Mod	le On, Idle	e Mode	Off.	Sleep C	Out	Y	es			
	~		$\overline{}$	le On, Idle						es			
Register Availability	1	77,	$\overline{}$	e On, Idle					-	es			
		//		e On, Idle			•			es			
	(),)			ep In				Y	es			
(-			
	Chatting Default Value												
		Status Default Value											
Default			Powe	r On Seq	uence				66h				
Delault				SW Rese	t			N	o Chai	nge			
				HW Rese	t				66h				



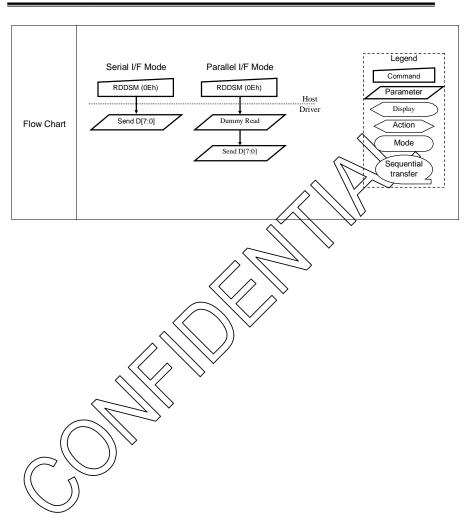
PDDIM (0Db): Pood Display Image Mode

KDDIM (C	DDh): Rea	ad Displa	y Im	age Mode									
0DH				RDDIM	(Read	Displ	ay Ima	age Mo	ode)			,	
	DCX	RDX	WF	RX D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HΕ
Command	0	1	1	x	0	0	0	0	1	1	0		0D
1 st Parameter	1	1	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00
	The disp	play mod	ule re	turns the disp	lay ima	age mo	ode sta	itus.					
	Bit	Syml	ool	Descripti	on				Comme	ent			
	D7	VSSO		Vertical scrolling			" = Vertic			n,		//	
	D6	Reserv		vertical seroining	Jotalus	,0,	° = Vertion	cal scrol	ling is 0		\	/	
Description	D5	INVO		Inversion On/Of	í		" = Inver	sion is (1	\forall			
	D4	Reserv		IIIVersion On/Or		"0"	°=/Inver	sion is (Off //	\rightarrow			
	D3	Reserv				.0,	+	+	>				
	D2~D0				$\overline{}$	70	$\overline{\gamma}$		•				
	D2~D0	Keserv	eu		/_	7/6		~					
			_			^	\vee		_	_			
				Sta	itus				Avail	ability			
		No	ormal	Mode On, Idle	Mode	Off, S	Sleep C	Out	Y	es			
Register		M	rmal	Mode On, Jale	Mode	On, S	Sleep C	Out	Y	es			
Availability		, (F	artial	Mode On, Idle	Mode	Off, S	leep O	ut	Y	es			
		P	antial I	Mode On, Idle	Mode	On, S	leep O	ut	Y	es			
	7	\Rightarrow	<i>(</i>		p In		•		Y	es			
			<u> </u>	0.00	,p								
((\rightarrow	\rightarrow											
		'		Status				De	fault V	alue			
((7			P	ower On Seq	uence				00h				
Default	/			SW Rese	t				00h				
_				HW Rese	t				00h				
				nvv kese	ι				uun				

RDDSM (0Eh): Re	ad Displa	y Signa	l Mode									
0EH				RDDSM	(Read	d Disp	olay Sig	gnal M	ode)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	0	1	1	1	0	0E
1 st parameter	1	1	1	х	D7	D6	D5	D4	D3	D2	D1	D0	00
	The dis	play modu	le return	s the Disp	lay Si	gnal N	lode.						
	Bit	Symbol		Descriptio	n			(Comme	ent			
	D7	TEON	Tearing	Effect Line	On/Off	и,	1" = On, "	0" = Off	1	$\overline{}$	\angle	//	
	D6	TELOM	Tearing	effect line n	node					$\sqrt{}$	2		
	D5	HS	Horizor	ntal Sync On	/Off	·()' = HSYN I' = H8YN	C is Or		$\overline{\ }$			
Description	D4	VS	Vertica	Sync On/O	ff	() /				>			
	D3	PCLK	Pixel C	lock On/Off					>				
	D2	DE	Data E	nable On/Off		1	Y-DEVS P-DEVS	Off Off					
	D1	Reserved	-		//	>							
	D0	DSI ERROR	PCLK Pixel Clock On/Off DE Data Enable On/Off DE Data Enable On/Off DE Soft DE S										
			$-\langle$	$\langle \cdot \rangle$	1	+							
				Sta	itus				Avail	ability			
		Moi	mal Mod	le On, Vale	Mode	Off,	Sleep C	Out	Υ	es			
5		No	rnal Mod	de On, Idle	Mode	On,	Sleep C	Out	Υ	es			
Register Availability	(Pa	rtial Mod	e On, Idle	Mode	Off, S	Sleep C	ut	Υ	es			
		Pa	rtial Mod	e On, Idle	Mode	On, S	Sleep C	ut	Υ	es			
_ (()	1		Slee	p In				Υ	es			
		/											
)											1	
	•			Status				De	fault V	alue			
			Powe	r On Seq	uence				00h				
Default				SW Rese	t	_			00h				
				HW Rese	t				00h				
		1											

RDDSDR (0Fh): Read Display Self-Diagnostic Result

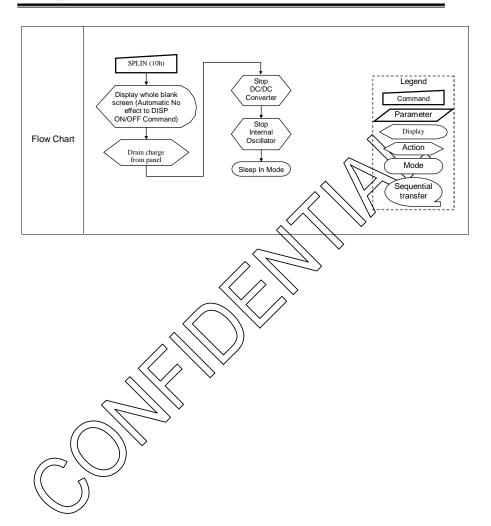
RDDSDR	(0Fh): F	Read Disp	olay Self-	Diagnost	ic Res	sult							
0FH			RDD	SDR (Rea	ad Dis	play S	elf-Dia	agnos	tic Re	sult)			
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	х	0	0	0	0	1	1	1	1	0F
I st Parameter	1	0 1 1 x 0 0 0 0 1 1 1 1		00									
	The dis	play modu	ile returns	the self-o	diagno	stic res	ults fo	llowing	g a Sle	ep Ou	t comn	nand.	
	Bit	Symbo	ol	Descrip	tion				Com	ment			
	D7	SDR	Registe	er Loading D	etection		In	vert the	D7(if_reg	sister va	lues loa	ding	
	D6	FUNCD	Functio	nality Detec	tion		Inve	ert tige Q	- 1 1	\sim	$\overline{}$	nality	
	D5	Reserve	t				100	\rightarrow	D3 D2 D1 D0 1 1 1 1 0 0 0 D0 g a Sleep Out command. Comment D7 of resister values loading with reoperty 6 if the display is reoptionality was are same ums are not the same Availability Yes Yes Yes Yes Yes				
Description	D4	Reserve	d			^	(₀)		/	D2 D1 D0 1 1 1 1 0 0 D0 ep Out command ment sister values loading sopretive same not the same ability es es es es			
	D3	Reserve	t		_	_ \	16.	/	>				
	D2	Reserve	t		\nearrow	1	12	\sum					
	D1	Reserve	t		7	> /	,0,						
	D0	CKSCMF	Checks	sums compa	risop						same		
			$- \langle$	$\langle \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	//	/_							
			$\overline{}$	Sta	tus				Avail	ability			
			rmalMoo	n Idle	Mode	Off S	leen C	Out					
		$\wedge \rightarrow$	//-										
Register Availability		- //	$+\!$	-									
		/ >	<u> </u>	-									
		P	artial Mod	e On, Idle	Mode	On, S	leep O	ut	Υ	es			
	())		Slee	p In				Y	es			
(
)			Status				De	fault V	alue			
			Powe	r On Seq	uence				00h				
Default				SW Rese	t				00h				
				HW Rese	t				00h				



10H					SL	.PIN (S	leep li	1)					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	1	0	0	0	0	10
Parameter	No Para	meter			I	I	I	I	I	I			
	This co	mmand	causes th	ne display	modul	e to en	ter the	Sleep	mode.				
Description	conver operati send P	ter, interronal and	nal oscilla the fram and VS	ne module ator and pa e memory informatio odule is in	anel sc mainta n to dis	anning ains its splay m	stop. I conter nodules	DBI or	DSI Co	ommar	nd Mod seor ooi	e rema	to
Restriction	The ho	est proces followinge. The he	ssor mus g this cor ost proce	fect when t wait 5 mi mmand to ssor must command	llisecoi allow t	ds bet	fore se	nding a	any neo	w comi	mands lock ci	cuits to)
				S	tatus				Avail	ability			
		Z	lormal/M	ode On, 16	le Mod	le Off,	Sleep	Out	Y	es			
Register			lormal M	ode On, Id	le Mod	le On,	Sleep	Out	Y	es			
Availability	Rahtjal Mode On, Idle Mode Off, Sleep Out Yes												
		F	Partial Mo	ode On, Id	e Mod	e On, S	Sleep (Out	Y	es			
)) >		Sle	eep In				Υ	es			
Detault			Pow	Status ver On Sec SW Res HW Res	et .	: :	Defau Sleep I Sleep I Sleep I	n Mod n Mod	e e				

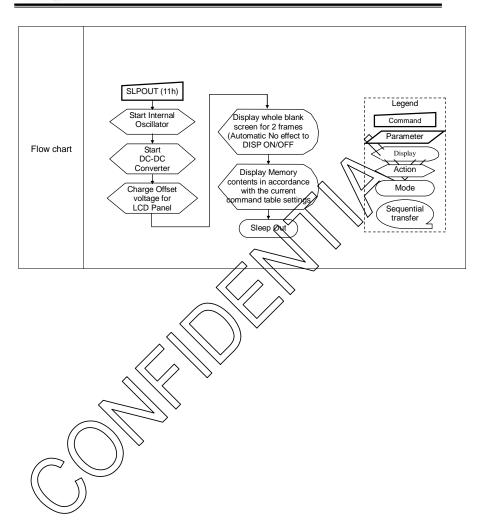
SI BOLLT (11h): Sloop Out

	SLPOUT	(11h): \$	Sleep O	ut										
Parameter No Parameter This command causes the display module to exit Sleep mode. All blocks inside the commodule are enabled. The host processor sends PCLK, HS and VS information to dismodules two frames before this command is sent when the display module is in Normal module is not in Sleep mode. The host processor must wall five military module is not in Sleep mode. The host processor must wall five military module is not in Sleep mode. The host processor must wall five military module is contained at the command. This delay allows the supply voltary clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command sending a Sleep-In command. The display module leasts the display module's default to the registers when exiting the Sleep mode. There-shall not be any abnormal visual the display device when loading the registers if the factory default and register value same or when the display module is not in Sleep mode. The display module runs the diagnostic functions after this command is provided. Status Register Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes	11H					SLI	POUT	(Sleep	Out)					
Parameter This command causes the display module to exit Sleep mode. All blocks inside the commodule are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode On, Sleep Out This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five military module is not in Sleep mode. The host processor must wait five military module is clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command sending a Sleep-In command. The display module leads the display module's default to the registers when exiting the Sleep mode. There shall not be any abnormal visual the display device when loading the registers in the factory default and register value same or when the display module's not in Sleep mode. The display module runs the diagnostic functions after this command is processed. Status Availability Register Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes		DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
This command causes the display module to exit Sleep mode. All blocks inside the commodule are enabled. The host processor sends PCLK, HS and VS information to dismodules two frames before this command is sent when the display module is in Nor This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must want five militarcends after so this command before sending another command. This delay allows the supply voltage clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command sending a Sleep-In command. The display module basis the display module's default to the registers when exiting the Sleep mode. There shall not be any abnormal visual the display device when loading the registers if the factory default and register value same or when the display module is not in Sleep mode. The display module runs the diagnostic functions after this command is processed. Status Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes	Command	0	1	1	×	0	0	0	1	0	0	0	1	11
module are enabled. The host processor sends PCLK, HS and VS information to dismodules two frames before this command is sent when the display module is in Nor This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wall five military conds after so this command before sending another command. This delay allows the supply voltage clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command sending a Sleep-In command. The display module has the display module's default to the registers when exiting the Sleep mode. There shall not be any abnormal visual the display device when loading the registers if the factory default and register value same or when the display module is not in Sleep mode. The display module runs the diagnostic functions after this command is received. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes	Parameter	No Pa	aramete	r										
module is not in Sleep mode. The host processor must wall five militarconds after so this command before sending another command. This delay allows the supply voltage clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command sending a Sleep-In command. The display module loads the display module's default to the registers when exiting the Sleep mode. There shall not be any abnormal visual the display device when loading the registers in the factory default and register value same or when the display module is not in Sleep mode. The display module runs the diagnostic functions after this command is peceived. Status Availability Register Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes	Description	modul	e are er	nabled. T	Γhe host pr	ocesso	r send	s PCLł	K, HS a	and VS	inform	ation to	o displa	ay
Register Availability Register Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes	Restriction	modul this co clock of The ho sendir to the the dis same	le is not ommand circuits t ost proc ng a Sler register splay de or when	in Sleep I before so stabilizeessor meep-In cook so when evice when the disp	o mode. The sending and ze. ust wait 12 mmand. The exiting the en loading, olay modul	e host other of 0 millis ne disp Sleep she reg	proces comma second: lay mo mode. iisters i	sor mu nd. Thi s safter there the fa	st watt g delay sending ads the shall no ctory o	allows allows ga Sle displa ot be an	ep Out ny modiny abnorand regard	commule's de primal v	er send oltages and be afault virisual ei alues a	ding and fore alues ffect on
Register Availability)) Status				Ava	ilability	,		
Register Availability Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes			. <	Normar	Mode On.	Idle M	ode Of	f. Sleer	Out					
Register Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes				$\stackrel{\checkmark}{\leftarrow}$										
Partial Mode On, Idle Mode On, Sleep Out Yes		(+/-/	>									
	Availability			-Kartiyal I	Mode On,	idle Mo	de Off	, Sleep	Out	<u> </u>	Yes			
Sleep In Yes	((/	// 🏂	Partial I	Mode On,	Idle Mo	de On	, Sleep	Out	,	Yes			
\\ 			リ L		5	Sleep II	n			,	Yes			
\ \ J)												
Status Default Value Power On Sequence Sleep In Mode		,					ionco							
Default SW Reset Sleep In Mode	Default													
HW Reset Sleep In Mode														





4011				DTLO	I /Dow	ial Dia	nlov I	Mada	2=1				
12H				PTLO					Jn)	T			
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	1	0	0	1	0	12
Parameter	No Para	meter											
Description	Mode will To leave The host	ndow is one Partial Exprocess	described Display Mo or continu	display moby the Pa ode, the Notes to send is sent wh	rtial Ar ormal d PCL	ea (30 Displa K, HS	h) com y Mod and V	nmand e On (S infor	13h) c matiok	omma to dis	nd sho	uld be	writte
Restriction	This com	nmand ha	s no effe	ct when Pa	artial C	isplay	Mode	is alre	ady ad	hive.			
Register Availability		Nor	rmal Mode	State On, Idle On, Idle On, Idle Sleet	Mode Mode Mode	On, SI	eep O	ut	Availa Ye Ye Ye Ye	s s s			
Default			Powe On SW HW	tatus n Sequend Reset Reset	се	Norm Norm	al disp	lay mo	e ode Or ode Or	1			
Flow Chart	Refer to	Partial A	rea (30h)										



NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	0	1	0	0	1	1	13
Parameter	No Para	meter					I	I	I	I			
Description		nmand ca al Display					r the N	lormal	mode	. Norm	nal Mo	de is d	efined
Restriction	This cor	This command has no effect when Normal Display mode is already active.											
		Status Availability Normal Mode On, Idle Mode Off Sleep Out Yes											
		Normal Mode On, Idle Mode Off Sleep Out Yes Normal Mode On, Idle Mode On Sleep Out Yes											
Register													
Availability		Pa	rtial Mode	On, Idle	yode (OH, SIE	ep Ot	n\	Ye	s			
		Pa	rtial Mode	On, hale	Møde (On, Sle	ep Ou	ıt	Ye	s			
			_//	Sleep) YO	//			Ye	s			
				21-1-1-)	N = 6 = 1.16	\						
Default				Status On Segue		Default Norm		olay M	ode O	n			
Derault		\mathcal{M}		N Reset		Norm	al Disp	olay M	ode O	n			
	HW Reset Normal Display Mode On												
Flow Chart	w Chart Refer to the description of Partial Area (30h)												

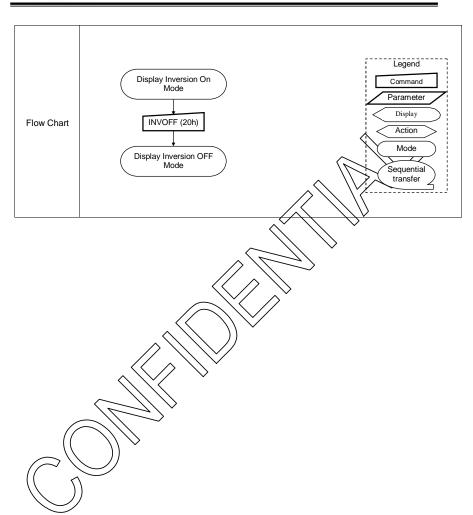


INVOFF (20H): Display Inversion Off

	. , , ,												
20H				INVOFF	(Disp	lay Inv	versio	n Off)					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	0	0	0	0	20
Parameter	No Paramete	r											
	This comman device. The fr		emory co	ntents rer				No sta	tus bit	s are o			у
Description		evice. The frame memory contents remain unchanged. No status bit Memory Display P Display P Display P Display P Display P											
Restriction	This command	d has no	effect w	then the	isplay	príodu	le is n	ot inve	erting t	he dis	play ir	nage.	
			_//	Status	\searrow			-	Availab	oility			
		Mormal	Mode C	n, Valle M	ode O	ff, Sle	ep Ou	t	Yes	6			
Register		Norma	Mode	n, Idle M	ode O	n, Sle	ep Ou	t	Yes	5			
Availability		Partial	Mode O	n, Idle Mo	ode Of	f, Slee	p Out		Yes	3			
		Partial	Mode O	n, Idle Mo	ode Oı	n, Slee	p Out		Yes	6			
((,		Sleep I	n				Yes	3			
Default		ı	Power O SW	tatus n Sequen Reset Reset	ce	Displa Displa	ay Inve	Value ersion ersion ersion	off				

INVON (21H): Display Inversion On

21H				INV	ON (D	isplay	Invers	sion O	n)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	х	0	0	1	0	0	0	0	1	2
Parameter	No Para	meter											
Description	This cc device.	ommand . The fran	Mem	ne display	modul ts rema	e to invain und	vert the	e imaged. No	status	only or bits are	e chan	isplay ged.	
Restriction	This co	mmand			\sim								
	+	- Innana	has no et	fect when	nodul	e is ali	eady i	n invei	rsion o	n mod	e.		
		Jimana I	has no ef		nodul	e is ali	eady i	n inve		n mod			
			(tatus				Avai				
			ormal Me	S	tatus	le Off,	Sleep	Out	Avai	ilability			
Register Availability	\(\frac{\pi}{2}\)		ormal Me	S sode On 10	tatus lle Mod	le Off,	Sleep	Out Out	Avai	ilability ⁄es			
Register			ormal Mo	Some On, of ode On, Id	tatus lle Moo	le Off, le On, e Off, S	Sleep Sleep	Out Out Out	Avai	ilability /es /es			
Register			ormal Mo	Since On Ideode On, Id	tatus lle Moo	le Off, le On, e Off, S	Sleep Sleep	Out Out Out	Avai	rilability r/es r/es r/es			
Register			ormal Mo	Single On Ide ode On, Ide ode On, Ide ode On, Ide	tatus lle Mod le Mod le Mod	le Off, le On, e Off, S	Sleep Sleep	Out Out Out	Avai	/es /es /es /es			
Register			ormal Mo cartial Mo Partial Mo	Sade On, Idade O	tatus Ile Mod Ile Mod Ile Mod Ile Mod Ile Mod Ile Mod	le Off, le On, e Off, S	Sleep Sleep (Out Out Out	Avai	/es /es /es /es			
Register			ormal Mo Partial Mo	Sounder On, Ideal on, Idea	tatus Ile Mod	de Off, de On, de Off, de On,	Sleep (Sleep (Defa	Out Out Out Out Out	Avai	/es /es /es /es			



DISPOFF (28h): Display Off

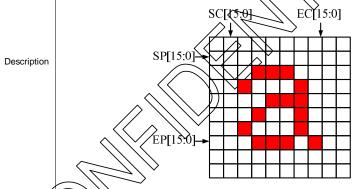
28H					DISPO	OFF (D	isplay	Off)					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	1	0	0	0	28
Parameter	No Par	ameter											
Description				e display rry contents		tatus b		chang		ay			
Restriction	This so	his command has no effect when module is afready in display off mode.											
Restriction	11115 CO	illillallu l	10 EII	lect when	IIIdodia	2 15 gill	eauy II	uispia	iy Oii II	ioue.			
				Sta	atus	·			Availa	ability			
		M	ormal Mo	nde On, la	e Mod	e Off, S	Sleep (Out	Ye	es			
Register		N	ormal Mo	ode On, Idl	e Mod	e On, S	Sleep (Out	Ye	es			
Availability		Partial Mode On, Idle Mode Off, Sleep Ou						Out	Ye	es			
		Partral Mode On, Idle Mode On, Sleep Out							Ye	es			
		Sleep In								es			
Default	Status Default Vall Power On Sequence Display Of SW Reset Display Of HW Reset Display Of					y Off y Off							

29H					DISPO	ON (Di	splay	On)					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	1	0	0	1	29
Parameter	No Par	ameter											
	This co device.	mmand The frai	causes t	he display ory conter	modu nts rem	le to s ain ur	tart dis	splayin jed. No	g the i statu	image s bits	data o are cha	n the danged	display
			Memor	У					Dis	splay F	^o anel	^	
		#			_			+				\vdash	
Description					_			7				H	
								⇉					
					-			\dashv				Н	
					_			7	\blacksquare	\blacksquare			
		1 1			//	^		ı	1 1	1 1	1 1	ı ı	
Restriction	This co	mmand	has no é	ffect whei	rusógi	ye is a	lready	in dis	play o	n mod	е.		
					\ <u>\</u>								
					Status				Av	ailabili'	ity		
			Normal W	ode On, I	dle Mo	de Off	, Slee	o Out		Yes			
		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ormal M	ode On, I	dle Mo	de On	, Slee	p Out		Yes			
Register Availability	(=		Partral Mo	ode On, Id	dle Mo	de Off	, Sleep	Out		Yes			
			Partial Mo	ode On, Id	dle Mo	de On	, Sleep	Out		Yes			
				S	eep In	1				Yes			
((1)													
			Po	Statu wer On Se		ce		ault Va splay C					
Der aul t /				SW Re	set		Dis	splay C	Off				
				HW Re	set		DIS	splay C	וו				

CASET (2Ah): Column Address Set

2AH				C	ASET (Colum	n Addr	ess Se	et)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	1	0	1	0	2A
1 st parameter	1	1	1	х	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00
2 nd parameter	1	1	1	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
3 rd parameter	1	1	1	х	EC15	EC14	EC13	EC12	EC11	E €100	EC9	EC8	01
4 th parameter	1	1	1	х	EC7	EC6	EC5	EC4	E¢3	EC2	EG1	ξŵ	DF
									- 11	$\overline{}$	$\overline{}$		

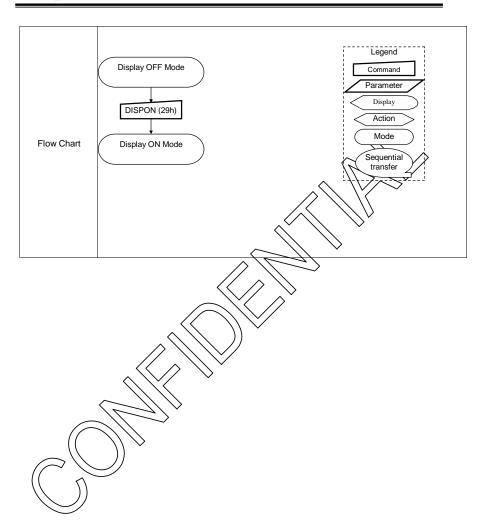
This command defines the column extent of the frame memory accessed by the bost processor with the read_memory_continue and write_memory_continue makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

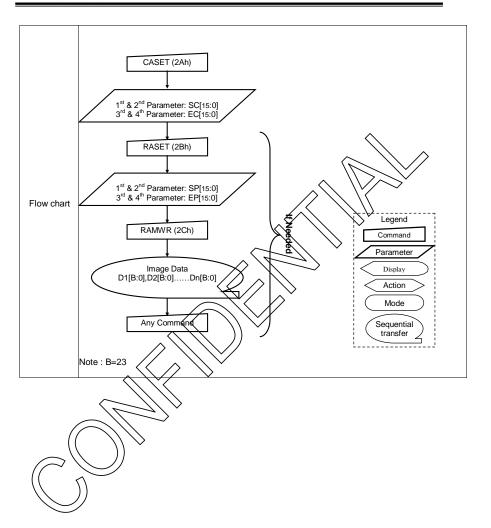


lways must be equal to or less than EC[15:0].

Note 1: M hen SC[15:0] or EC[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh

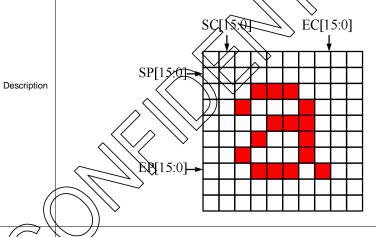
When MADCTL's B5 = 1), data of out of range will be ignored





2BH					RAS	SET (Ro	w Addı	ress Se	t)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	1	0	1	1	2B
1 st parameter	1	1	1	х	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00
2 nd parameter	1	1	1	х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
3 rd parameter	1	1	1	х	EP15	EP14	EP13	EP12	EP11	EP(0	EP9	EP8	01
4 th parameter	1	1	1	х	EP7	EP6	EP5	EP4	EP3	EP2	EPI	EP0	3F

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SPN5:0] and SPN5:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



SP[15:0] always must be equal to or less than EP[15:0]

When SP[15:0] or EP[15:0] is greater than 01DFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data ofout of range will be ignored.

Restriction

		Status	Availability	
	Normal Mode C	On, Idle Mode Off, Sleep Out	Yes	
Register	Normal Mode C	On, Idle Mode On, Sleep Out	Yes	
Availability	Partial Mode O	n, Idle Mode Off, Sleep Out	Yes	
	Partial Mode O	n, Idle Mode On, Sleep Out	Yes	
		Sleep In	Yes	. ^
			M	
	Status	Default	Value	
	Status	SP[15:0]	EP[15:0]	
Default	Power On Sequence	0000h	013Fh	
	SW Reset	0000h	MDFh (If MADCTI 013Fh (If MADCTI	L's B5=0) 's B5=1)
	HW Reset	0000b	01EFh	



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commands is written to undefined locations.

Restriction

	Status Availability
	Normal Mode On, Idle Mode Off, Sleep Out Yes
Register	Normal Mode On, Idle Mode On, Sleep Out Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out Yes
	Partial Mode On, Idle Mode On, Sleep Out Yes
	Sleep In Yes
	Status Default Value
Default	Power On Sequence Contents of memory is set applicable SW Reset Contents of memory is not cleared
	HW Reset Contents of memory is not cleared
Flow chart	RAMWR (2Ch) Command Parameter Display Action Mode Sequential transfer

Raydium

RAMRD (2Eh): Memory Read

2EH					RA	AMRD (Memor	y Read)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	0	1	1	1	0	2E
1 st parameter	1	1	1	х	х	х	х	х	х	х	х	х	х
2 nd parameter	1	1	1	D1[158]	D17	D16	D15	D14	D13	D12	D11	D10	
:	1	1	1	Dx[158]	Dx7	Dx6	Dx5	Dx4	Dx3	DXX	Dx1	Dx0	
(N+1)th parameter	1	1	1	Dn[158]	Dn7	Dn6	Dn5	Dn4	Dn3	1802	DN	Dn0	

This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.

RM68140 Data Sheet

Rev: 0.3

If MV(36h-B5) = 0:

The column and page registers are reset to the Start-Column (SC) and Start Page (SP), respectively. Pixels are read from trame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value on the lost processor sends another command.

If MV(36p-B5)

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (SP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value of the host processor sends another command.

Restriction

Description

There is no restriction on length of parameters.

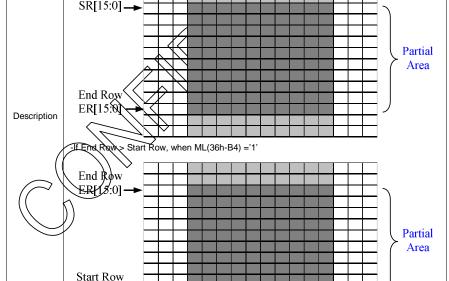
PTLAR (30h): Partial Area

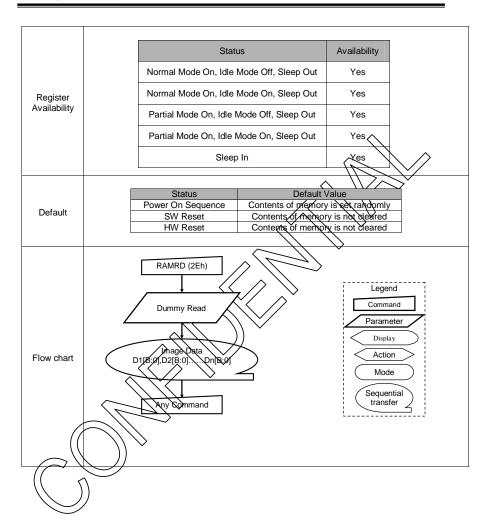
Start Row

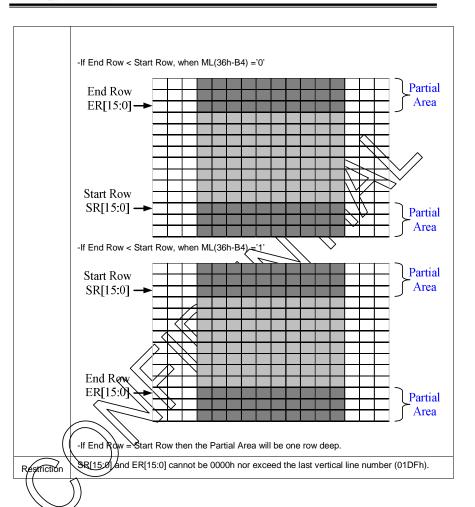
SR[15:0] →

30H					PT	LAR (F	Partial A	Area)					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	0	0	0	0	30
1 st parameter	1	1	1	х	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2 nd parameter	1	1	1	х	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3 rd parameter	1	1	1	х	ER15	ER14	ER13	ER12	ER11	ER18	ĘR9	ER8	01
4 th parameter	1	1	1	х	ER7	ER6	ER5	ER4	ER3(ER2	ERT	₽RØ	DF
	This co	nmand	define	the Da	rtial Di	enlay n	nodo's	dienlay	area	thoras	aro w	Vnaran	notore

This command defines the Partial Display mode's display (SR) and the second the End associated with this command, the first defines the Start Row Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory. -If End Row > Start Row, when ML(36h-B4) ='0'







		Status	Availability
	Normal Mode On	, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On	, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On,	Idle Mode Off, Sleep Out	Yes
	Partial Mode On,	Idle Mode On, Sleep Out	Yes
		Sleep In	Xes
	24.4	Default	Value
	Status	SR[15:0]	ER[15:0]
Default	Power On Sequence	0000h	01DFh
	SW Reset	9000h	01DFh
	HW Reset	000000	01DFh
Flow chart	1. To Enter Partial Mode PTLAR (30h) 1 st & 2 st Parameter: SR(15:0) PTLONL(72h) Partial Mode	Partial Mode DISPOFF (28h) NORON (13h) Partial Mode OFF RAMRW (2Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] DISON (29h)	Optional to prevent tearing effect image display Legend Command Parameter Display Action

Description

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VSCRDEF (33h): Vertical Scrolling Definition

33H					VSCRD	EF (Ve	tical Sc	rolling	Definiti	ion)			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	0	0	1	1	33
1 st parameter	1	1	1	х	TFA[15]	TFA[14]	TFA[13]	TFA[12]	TFA[11]	TFA[10]	TFA[9]	TFA[8]	xx
2 nd parameter	1	1	1	х	TFA[7]	TFA[6]	TFA[5]	TFA[4]	TFA[3]	TFA[2]	TFA[1]	TFA[0]	xx
3 rd parameter	1	1	1	х	VSA[15]	VSA[14]	VSA[13]	VSA[12]	VSA[11]	VSA[10]	VSAYQI	VSA[8]	xx
4 th parameter	1	1	1	х	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	V\$A[2]	VSA[1]	V\$A[0]	xx
5 th parameter	1	1	1	х	BFA[15]	BFA[14]	BFA[13]	BFA[12]	BEA[11]	BFA[10]	BFA[9]	BFA[8]	xx
6 th parameter	1	1	1	х	BFA[7]	BFA[6]	BFA[5]	BPA(4)	BEA[3]	BFAIRI	BFA[1]	BFA[0]	xx

This command defines the display vertical crolling area

Memory Data Access Control (36h) 84 = 0;

The 1st & 2nd parameter, TFA[15:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[15:0], describes the height of the Vertical Scrolling Area in number of lines of trame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th with parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

TFA[15:0] Top Fixed Area First line Read from memory BFA[15:0] Bottom Fixed Area Set_scroll_area_set_address_mode_B4 = 0 Example Memory Data Access Control (36h) B4

The 1st & 2nd parameter, TFA[16:0], describes the Jop Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

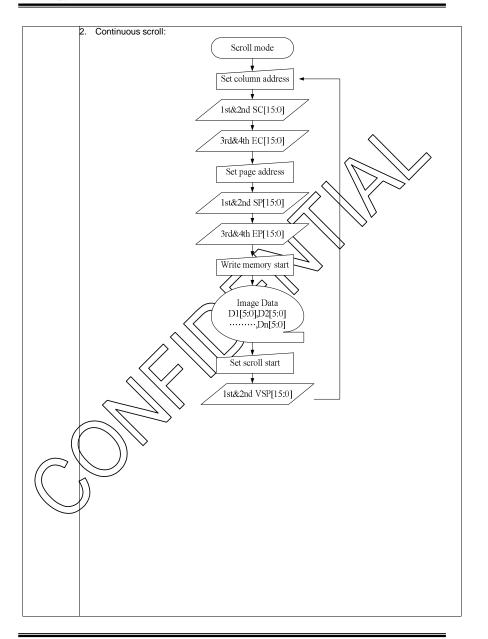
The 3rd & 4th parameter. VSA[15:8] describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory.

The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

			•			ce's horizontal lines
Restriction		pe set to '0' – this				set_address_mode
			Status		Availability	1
		Normal Mode	On, Idle Mode O	f, Sleep Out	Yes	
Register		Normal Mode	On, Idle Mode O	n, Sleep Out	Yes <	
Availability		Partial Mode	On, Idle Mode Of	f, Sleep Out	(PS)	
		Partial Mode	On, Idle Mode Or	n, Sleep Out	Yes	\searrow
			Sleep In		Yes	
		Status	TEAL		ault Value	EALLS OF COORDIES
		On Sequence	~		\vee	FA[15:0]=0000HEX
Default	S	SW Reset	TFA[15:0]=0600	HEX YSAING	:0]=01E0HEX B	FA[15:0]=0000HEX
Dorault	Н	IW Reset	TFA[15:0]=0000	HEX VSA[15	:0]=01E0HEX B	FA[15:0]=0000HEX
				//		



TEOFF (34h): Tearing Effect Line OFF

•	,	J	Line Or										
34H				TEOFF	(Teari	ng Eff	ect Li	ne OF	F)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	0	1	0	0	34
Parameter	NO PARA	METER											
Description	This comn line.												
Restriction	This comm	his command has no effect when the Tearing Effect output is already off											
		Norm	nal Mada	State		Off CI		2	Availa	bility			
Register				On, Idle			\wedge	$\overline{}$) Ye	§			
Availability		Part	ial Mode	On, Idle I	Mode (Off, SIG	sep 61	ıt \	> Ye	s			
		Part	ial Mode	On, Idle	(Jøde)	on, sie	ep O	т	Ye	s			
				Sleep	lp/	, \ -/>	>		Ye	s			
Default			PR	Statu SW Re HW Re	equer eset	nce	De	fault V OFF OFF OFF					
Plow Chart		TEO	FF (34h)]							Comm Param Displ Actic Moo	and eter ay on de	

tvdh

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35H				TE	ON (Te	earing	Effect	Line (ON)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	0	1	0	1	35
1 st parameter	1	1	1	х	0	0	0	0	0	0	0	TELOM	00
	This co	mmand	turns on	the tearin	g Effe	ct outp	ut sign	al on t	he TE	signal	line. 1	he TE si	gnal is
		oatod by		MADOTE	(266)	D4/I:	na	draga (\\	^			

not affected by changing MADCTR (36h) B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

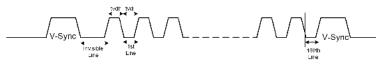
If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.

Vertical Time Scale Description

If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



The Tearing Effect Qutput line shall be active low when the display module is in Sleep mode.

This command has no effect when Tearing Effect output is already ON. Restriction

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

	Status	Default Value	
	Power On Sequence		
Default		OFF OFF	
	SW Reset	OFF	
	HW Reset	OFF	
Flow Chart	TE Line Output OFF TEON (35h) 1st Parameter: TELOM TE Line Output ON		Command Parameter Display Action Mode Sequential transfer

MADCIR (R (36h): Memory Data Access Control												
36H				MADCTR	(Mem	ory Da	ata Ac	cess (Contro	ol)			
	DCX	RDX	WRX	D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	х	0	0	1	1	0	1	1	0	36
1 st parameter	1	1	1	x	В7	В6	B5	B4	В3	B2	B1	В0	00
	This c	ommand	defines	read/writ	e scar	nning	direction	on of	frame	memo	ory. Th	nis cor	nmand
	makes	no chan	ge on the	e other driv	er sta	tus.							
									R				
	Bit	Symb	ool	Descript	ion				Comr	nent			
	В7	U = 100 to Bottom											
	В6	MX	MX Column Address Order Right to Left 0 = Left to Right ANY Revi/Column Order (AN) Revi/Column exchange										
	B5	MV	Row	/Column Ord	er (MV)	_ `	'1' = Roi '0 = Noi		excha	nge			
	B4	ML	Verti	cal Refresh (Orgher	1				Bottom n to Top			
	В3	RGB	RGB	/BGR Order		> \	//	R, "0"=R					
	B2	MH	Horiz	zontal Refres	h Order		1' =LCD	Refres Refres	h Left to h Right t	Right to Left			
Description	B1	H_FLI	P Horiz	ontal Flip			'0' = Nor '1' = Flip						
	В0	V_FLI	P Verti	bal Flip))		'0' = Nor '1' = Flip						

	B5	В6	В7	Image in Frame Memory	B5	В6	В7	Image in Frame Memory					
	0	0	0	B	1	0	0	B					
	0	О	1	E	1	0	1						
	0	1	0	B	1	1	0						
	0	1	1	B	1	1	1						
				ВЗ :	= 0								
				Memory Sent	RGB →	D	isplay R G						
				Memory	Sent BGR								
Restriction													



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VSCRSADD (37h): Vertical Scrolling Start Address

VOCKO	אטט (3	rii). ver	ucai 30	rolling S	tart A0	uress								
37H				VSCRS	ADD (\	/ertical	Scrolli	ing Sta	rt Addre	ess)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	х	0	0	1	1	0	1	1	1	37	
1 st parameter	1	1	↑	х	0	0	0	0	0	0	0	VSP8	xx	
2 nd parameter	1	1	1	х	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	xx	
	This command sets the start of the vertical scrolling area in the frame memory. The vertical												ertical	
	scrollin	ng area i	s fully de	efined wh	en this	comma	nd is us	ed with	the set	_scroll_	eirea co	mmand		
									11	\sim	\swarrow			
	The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defi												efines	
the line in the frame memory that is written to the display device as the first												of the v	ertical	
	scroll area.													
								/		•				
	The displayed image also depends on the setting of the Line Address Order bit, B4, in the													
i		set_address_mode register. See the examples below.												
	If set_address_mode (R36h) B4 = 0													
	Example:													
			Fixed A	rea = Bott	om Fik	d Area	= 0 Ve	ertical S	crolling	Area =	480 and	d VSP =	3	
	•••	.о гор		ba 126.	J	7		inter	o. og		.00 0		0.	
Description			Г	rame Mem	ory			1=0			Display	/		
	(O,	0) -	Ш		\Box			0	-					
			ш			4		1	- -		-		4	
	VSP	[8:0]				4		2	-				4	
	_		\vdash			_		3 - 4					-	
				-		-		4	⊢	++	++	HH	-	
((┪				+	++	HH	┥	
			Н			1		 77	ŀ	+	+	Н	_	
			\Box	+	\top	1	4	78	F			Ш	┪	
[[) (a, 4	1/9) 🛶					4	/9						
	//			DOCK) DA	4.									
			_rnoae (R36h) B4	= 1:									
	Examp		l A	D-44-	Figure 2. 2		00 M- "		- 10: A			(OD : 101		
	when	op Fixe	ed Area	= Bottom	rixed A	area = C	υ, verti	cai Scr	oiling Ar	ea = 48	su and \	/SP='3'.		

	Status	Availability				
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes				
	Normal Mode On, Idle Mode On, Sleep Out	Yes				
	Partial Mode On, Idle Mode Off, Sleep Out	No				
	Partial Mode On, Idle Mode On, Sleep Out	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\				
	Sleep In	Yes				
Default	Status Power on Sequence SW Reset RW Reset	Default Value 0000HEX 0000HEX 0000HEX				
Flow chart	Refer to the description Vertical Scrolling Definition (33h)					

IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	1	0	0	0	38
Parameter	NO PAI	NO PARAMETER											
Description	This co	This command causes the display module to exit Idle mode.											
Restriction	This co	This command has no effect when the display module is not in Idle mode.											
	Status Availal Normal Mode On, Idle Mode Off, Sleep Out												
Register Availability		-		de On, Idle	\leftarrow	∑ Y∈ Y∈							
			artial Mo	\rightarrow	Yes								
				Sle	epin	//	>		Ye	s			
Default		Status Default Value Polvex On Sequence Idle Mode Off SW Reset Idle Mode Off HW Reset Idle Mode Off											
Flow Chart		IDMOI	ode ON FF (38h) ode OFF)])						Para Di Ad M Seq	gend nmand ameter splay ction lode uential nsfer		

IDMON (39h): Idle Mode ON

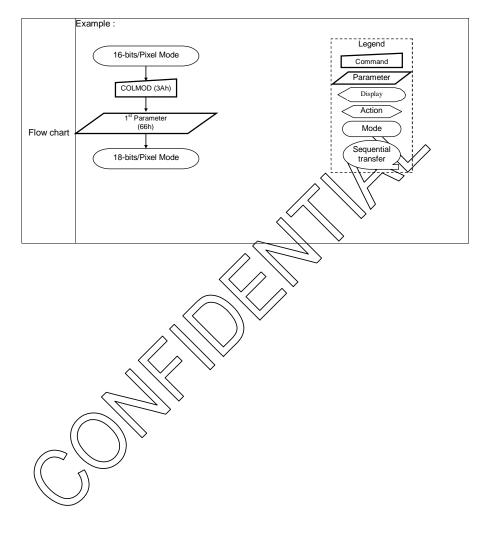
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39H		IDMON (Idle Mode ON)													
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	0	0	1	1	1	0	0	1	39		
Parameter	NO PAR	AMETER	₹				I			1			I		
	This com	nmand ca	auses the	display m	odule t	o ente	Idle M	lode.							
		In Idle Mode, color expression is reduced. Colors are shown on the display device using the													
											(2)	/100 do	ing the		
	MSB of each of the R, G and B color components in the frame memory. Memory Panel Display														
	1	Me	emory	1 1 1				10	I P	anel D	Display	10.00			
											-				
					-		1								
					-		V								
Description															
								_			-		_		
	Į.							l,		1 1		. V/ (8			
	Colo	r R7	R6 R5(R)	R3 R2 R1 R0)) (37 G6 G	5 G4 G3	G2 G1 (G0	B7 B6	B5 B4 E	33 B2 B1	В0		
	Blac	_	OXXXXXXX OXXXXXXXX							0XXXXXX					
	Blue		1XXXXX	\rightarrow	_	0XXXXXXX 0XXXXXXX				1XXXXXXX 0XXXXXXX					
	Magen	- · ·	12/2/XXXX				(XXXXX		1XXXXXXX						
	Gree		QXXXXX				(XXXXX		0XXXXXXX						
	Cyan	- /,	Coxxxxx				(XXXXX			1XXXXXXX					
	Yello	<u> </u>	Z JXXXXX	XXX		1XXXXXXX				0XXXXXXX					
	White		1XXXXXXX 1XXXXXXX								1XXXXXXX				
(()	1/1/2													
Restriction	This com	mand ha	as no effe	ct when m	odule	is alrea	ıdy in i	dle on	mode.						
(($ \sqrt{1} $														
))			Stat	us				Availab	ility					
\sim		No	Normal Mode On, Idle Mode Off, Sleep Out							;					
Register		No	rmal Mod	le On, Idle	ıt	Yes									
Availability		Pa	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
		Pa	rtial Mod	e On, Idle	Mode (On, Sle	ep Ou	t	Yes						
				Slee	o In				Yes	;					

COLMOD (3Ah): Interface Pixel Format

3AH				COLN	IOD (Ir	nterfac	e Pixe	l Form	nat)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	1	0	1	0	ЗА
1 st parameter	1	1	1	х	0	D6	D5	D4	0	D2	D1	D0	66
Description	This command sets the pixel format for the RGB image data used by the interface. Bits D[6:4] – DPI Pixel Format Definition Bits D[2:0] – DBI Pixel Format Definition Bits D7 and D3 are not used. If a particular interface, either DBI or DPI, is not used then the corresponding bits in are ignored. Control Interface Color Format D6/D2 D5/D1 D4/D0 Reserved 0 0 0 Reserved 0 1 Reserved 0 0 1 Reserved 0 0 1 Reserved 0 0 0 Reserved 0 0 1 1 Reserved 0 0 0 Reserved 0 0 1 1 Reserved 1 0 0 0 16bit/pixel (65,536 colors) 1 0 1 Reserved 1 0 0 1											the par	ramete
Restriction	There is r	no visible	e effect or	til the Frau	ne Me	mory is	writte	n to.					
			Status A							oility			
	(-	Nø	rmal Moo	e On, Idle	Mode	Off, Sle	еер Ос	ıt	Yes	;			
Register Availability		No	rmal Mod	e On, Idle	Mode	On, Sl	еер Ос	ıt	Yes	;			
Availability	())) \ \p\z	rtial Mod	e On, Idle	Mode	Off, Sle	ep Ou	t	Yes	i			
		Pa	rtial Mod	e On, Idle	Mode	On, Sle	ep Ou	t	Yes	;			
)			Slee	p In				Yes	;			
			Status						Default Value				
Default			Power On Sequence						66h				
20.00.0				SW Rese	et			66h					
				HW Rese	et			66h					

Default		Status Power On Sequence SW Reset HW Reset	Default Value Idle Mode Off Idle Mode Off Idle Mode Off	
Flow Chart	IDN	mode OFF MON (39h) mode ON		Legend Command Parameter Psupay Action Mode Sequential transfer





RAMWRC (3Ch): Write_Memory_Continue

3CH	Write_Memory_Continue												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	0	1	1	1	1	0	0	3C
1 st parameter	1	1	1	D1[158]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	xx
X st parameter	1	1	1	Dx[158]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	DXQ	Dx[1]	Dx[0]	xx
N st parameter	1	1	1	Dn[158]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	100 A	(FG	Øn[0]	xx

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If MV(36h-B5) = 0:

Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then resecto SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor the number of pixels exceeds (EC - SC + 1) * (EP - SP + 1) the sends another command. extra pixels are ignored

Description

If MV(36h-B5)

Data is written continuing from the pixel location after the write range of the previous RAMWR(20h) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame normory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra xels are ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

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	DCX 0 1 1	RDX 1	WRX ↑	D15-8	ad_Me	emory_ D6		nue											
1 st parameter 2 nd parameter X st parameter N st parameter	0	1	1		D7	DCX RDX WRX D15-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX													
1 st parameter 2 nd parameter X st parameter N st parameter	1	↑	'	х			טט	D4	D3	D2	D1	D0	HEX						
2 nd parameter X st parameter N st parameter			1		0	0	1	1	1	1	1	0	3E						
X st parameter N st parameter	1			х	х	х	х	х	х	х	х	х	х						
N st parameter		1	1	D1[158]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	XX						
•	1	1	1	Dx[158]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	bX13+	Dx[2]	DXII	∫ x[0]	xx						
	1		1	Dn[158]	Dn[7]	Dn[6]	Dn[5]	4	Dn[3]	On[2]) Dn[1]	Dn[0]	xx						
Description	This commprocessor read_mem If MV(36h-Pixels are RAMWR(2 from the	continuitory_start 35) = 0: read c Ch) or F ame mer then resulting the p mmand 35) B5 = 0:	continuing AMWRC	the local d. If from the property of the column the property of the column and the property of the column the col	e pixe e solution registre registre e pixe e page	ster ed gister i: End P	tion a dister is incre large (E	fter the then the then increase.	ne rea increm Colund. Pixe lue or	d rangented nn (EC) els are the ho	ge of and pice read frost progeries.	the p ixels are the posterior the p are rea	revious re read column e frame sends						

Ontil the column register equals the End Column (EC) value or the host processor sends another

A Memory Read should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMRD(2Eh) and any following RAMRDC(3Eh) commands

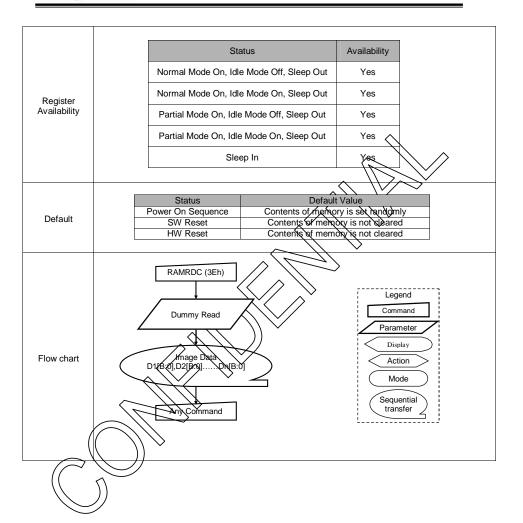
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is written to undefined locations.

Restriction

44H				TE	ESLWR (Write	Tear S	can lir	ne)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	1	0	0	0	1	0	0	44
1 st parameter	1	1	1	xx	0	0	0	0	0	0	0	STS[8]	00
2 nd parameter	1	1	1	xx	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00
Description	display The Teamode. Vertical	reaches aring Eff	urns on t	The TE	signal is	not af	fected that d	by challescribe	anging es the	set ac	dorese of Ette	priode et Outp	bit B4.
Restriction	-			//	111								
		(10	ormal (No		Status	0# 0	Noon C	Dust .	Availa				
Register	~	$\langle \leftarrow \rangle$	ormal Mo						Ye Ye				
Availability	_		artial Mo	de On, I	dle Mode	Off, S	leep O	ut	Υe	es			
		\\\P	artial Mo	de On, I	dle Mode	On, S	leep O	ut	Υe	es			
		$))$ $\dot{\mathbb{L}}$		S	leep In				Υe	es			
Default)		Po	wer On	itus Sequend Reset	ce	STS	efault \ [8:0]=9 lo chan)'h000				



HW Reset

STS[8:0]=9'h000

	. ,												
45H				TE	SLRD (Read 1	ear So	can Lir	ie)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1								1	45	
1 st parameter	1	1	1	х	х	х	х	х	х	х	х	х	х
2 nd parameter	1	1	1	xx	0	0	0	0	0	0	0	GTS[8]	0x
3 rd parameter	1	1	1	xx	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GТ\$(2)	GTS[1]	GTS[0]	XX
Description	number scan lin	of scan	lines on a	a display e first lin	device e of V-Sy	is defir /nc and	ned as d is der	VSYNOTED S	C + VE s Line	P + V	` / '	vige The	e total ne first
Restriction							$ \wedge $	//		\rightarrow			
Register Availability		N P	1										
Flow Chart				Walt	Read ter GTS[8:0]			[Common Paramonia Dia Action M	neter splay			

51H	WRDISBV (Write Display Brightness)														
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	0	1	0	1	0	0	0	1	51		
1 st parameter	1	1	1	х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00		
Description															
Restriction	The di	The display supplier cannot use this command for tuning													
			Norma	al Mode	Sta	tus Mode (Off Slee	n Out	Availa						
5			+	//-	$\rightarrow \!$	Mode C			Ye						
Register Availability	<		//	$+\!$	-	Mode C			Ye						
			Partia	al Mode	On, Idle	Mode C	n, Slee	o Out	Ye	es					
))[$\overline{}$		Slee	p In			Ye	es					
	$\widetilde{\mathfrak{H}}$				Status				Default \	/alue					
Default				Powe	r On Se	quence			00h	ı					
20.00.1				•	SW Res	et			00h	1					
				I	HW Res	et			00h	1					

RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)														
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	0	1	0	1	0	0	1	0	52		
1 st parameter	1	1	1	х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00		
	This cor	mmand re	eturns brig	htness valu	ıe.										
Description		iple relat brightnes		that 00h	value r	neans	the low	est bri	ghtness	s and I	FFh va	lue me	ans the		
Restriction	-								1						
								\wedge	_ //	$\sqrt{\ }$	<u>~</u>				
				S	tatus				Ava	ailabilit	у				
		١	Normal M	ode On, Id	dle Mo	de Off,	Sleep	Spil		es					
Register		Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Steep Out Yes													
Availability															
		Partial Mode On, title Mode On, Steep Out Yes													
		Partial Mode Ork, Kille Mode On, Sheep Out Yes Sleep In Yes													
			7	7)										
				Status				De	efault \	/alue					
	<	\sim	Pow	er On Sed	quence)			00h	I					
Default	(SW Res	et				00h	ı					
	7/-		> <u> </u>	HW Res	et				00h	ı					
Flow Chart	RDDDISBV (52hH) Host Command Parameter Display Action Mode Sequential														
						ransfer	<u> </u>								

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WRCTRI D (53h): Write CTRI Display

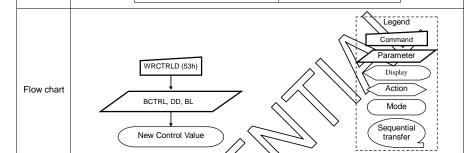
	WRCTRLD (White CTRL Display)													
53H	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
			WIX	D13-0										
Command	0	1	1	Х	0	1	0	1	0	0	1	1	53	
1 st parameter	1	1	1	Х	0	0	BCTRL	Х	DD	BL	Х	Х	00	
Description	BCTRI The BC BCTRL 0 1 DD: Di DD 0 1 BL: Ba When	L: Brightr CTRL bit DES Off, DB\ On, DB\ isplay Dir Display Display acklight C	is alwa SCRIPT V[7:0] a V[7:0] a mming 0 SCRIPT blay dim control 0 hange f	ontrol Bloomys used to a second KBV[7] and K	ck On/Off o switch o switch o PWM Pi 7:0] are 0 on/Off on thout Dis "" to "Off"	brightne	rightness ss for disp DESCRIF LEDPWP	play with PTION LI OL="0": OL="1"; OL="1"; OL="1";	dimmine EDPWM keep low keep high PWM out	effect (a	n level is d	duty) luty)		
Postrietion	The dia	Off On Omming for	Inchion I	s adapte	→0.	brightnes	LEDON F LEDONP LEDPWP LEDPWP LEDPWP ss register	OL="0": "OL="1": "OL="0": "OL="1":	keep high keep high PWM out	n (non-lit) n (lit) put (lit)		anged at		
Restriction	1 The di	Off On Omming for	Inchion I	s adapte	→0.	brightnes	LEDONP LEDPWP LEDPWP LEDPWP	OL="0": "OL="1": "OL="0": "OL="1":	keep high keep high PWM out	n (non-lit) n (lit) put (lit)		anged at		
Restriction	The dia	Off On Omming for	Inchion I	s adapte	→0. use this	brightnes	LEDONP LEDPWP LEDPWP LEDPWP	OL="0": "OL="1": "OL="0": "OL="1":	keep high keep high PWM out	n (non-lit) n (lit) put (lit) bit BCT		anged at		
Restriction	The dia	Off On Omming for	naction in the control of the contro	annot cannot	→0. use this	brightnes	LEDONP LEDPWP LEDPWP LEDPWP	OL="0": 'OL="1": 'OL="0": 'OL="1": S for disp	keep high keep high PWM out olay wher	n (non-lit) n (lit) put (lit) n bit BCT		anged at		
Register	The dia	Off On Omming for	Inction I	cannot Mode	→0. use this Sta	comma	LEDONP LEDPWP LEDPWP LEDPWP ss register	OL="0": 'OL="1": 'OL="0": 'OL="1": s for disp	keep high keep high PWM out blay wher	n (non-lit) n (lit) put (lit) bit BCT		anged at		
	The dia	Off On Omming for	Norma Partia	cannot al Mode	→0. use this Sta On, Idle On, Idle	comma tus Mode (LEDONP LEDPWP LE	OL="0": OL="1": OL="1": OL="1": OL="1": OL="1": OL="1": OUTHING	keep high keep high keep high keep high keep high pwww. Availa Availa Yee Yee	ability ability assesses		anged at		
Register	The dia	Off On Omming for	Norma Partia	cannot al Mode	→0. use this Sta On, Idle On, Idle	comma tus Mode (LEDONP LEDPWP LEDPWP LEDPWP LEDPWP as register and for tu	OL="0": OL="1": OL="1": OL="1": OL="1": OL="1": OL="1": OUTHING	keep high keep high PWM out Availa Yee	ability es es		anged at		

Default

00h

<u></u>	
Status	Default Value
Power On Sequence	00h
SW Reset	00h

HW Reset



54H						F	RDCTRL	D					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	1	0	1	0	1	0	0	54
1 st parameter	1	↑	1	х	0	0	BCTRL	х	DD	BL	х	х	00
Description	BCTRL The Be BCTRL 0 1 DD: DD 0 1 BL: Ba When	L: Bright CTRL bit DE: Off, DB: On, DB: Dis Dis acklight C BL bit c ng on (D	mess Co is alwa SCRIPT V[7:0] a mming SCRIPT play din play din D="1") i	ontrol Bloomys used to FION LED and KBV[7] Control Con	ck On/Off o switch oPWM Pi 7:0] are 0 7:0] are a on/Off off on thout Dist	f brightne n Oh. active	ss for disp DESCRIF LEDPWF	play with PTION LE POL="0":	dimming EDPWM keep low keep low keep low keep low keep high keep high	effect (a (No) n (No) put (high put (high put (high n (non-lit) n (non-lit) n (iti)	n level is d level is d	duty) uty)	

adapted to the brightness registers for display when bit BCTRL is changed at

The display supplier cannot use this command for tuning Restriction

_ \			
		Status	Availability
	())	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register		Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

WRCABC (55h): Write Content Adaptive Brightness Control

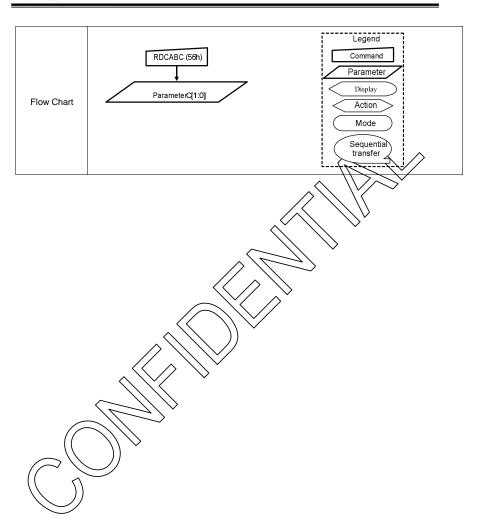
55H			١	NRCAB	C (Write	Conte	nt Adap	tive Bri	ghtness	Contro	l)				
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	0	1	0	1	0	1	0	1	55		
I st parameter	1	1	1	х	0	0	0	0	0	0	C1	C0	00		
	This	ommand	l is use	d to set p	aramete	ers for im	age cont	ent based	d adaptive	e brightn	ess contr	ol			
	function	onality. ⁻	There is	s possible	to use 4	different	modes f	or conter	nt adaptiv	e image	functiona	ılity, whic	:h		
	are de	fined on	a table	below.					(·					
		(C1				C0			$\langle \rangle$	Etroctió	n			
Description			0				0		, //		Off				
			0				1 ,			20	UI Mod	е			
		1 0 Still Mode													
		1 Moving Mode													
Destriction	This ro	register is synchronized with V-sync by interpalacircuit													
Restriction	1111010	giotor io t	Syrioriic	JIIIZOG WII	۷ ၁, 1, 2			\rightarrow							
					Sta	itus			Availa	ability					
			Norm	al Mode	Øn, Idle	Mode (Off, Slee	p Out	Υe	es					
Register			Norm	al Mode	Sp. 1846	Mode (On. Slee	p Out	Ye	es					
Availability			\leftarrow	al Mode	\rightarrow				Ye	25					
		~ }	\leftarrow	al Mode					Ye						
	<	1	- SING	al Mode			n, siee	p Out							
/		///	_		Slee	p In			Ye	es					
					Status				Default \	/alue					
Default	\bigcap			Powe	r On Se	quence	quence 00h								
				;	SW Reset				00h	1					
		HW Reset 00h													

PDCARC (56h): Pood Content Adnative Prightness Control

56H			RDCA	BC (Read	Conte	nt Ad	oative	Brigh	tness	Contr	ol)		
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	x	0	1	0	1	0	1	1	0	56
1 st parameter	1	1	1	х	0	0	0	0	0	0	C1	C0	00
Description		functionality. There is possible to use 4 different modes for content adaptive image which are defined on a table below. C1 C0 Function 0 0 Off 1 UNING 1 1 Moving Mode											
Restriction	-					7	\Rightarrow	<u> </u>					
Register Availability	\(\frac{1}{4}\)		formal M	ode On, la ode On, la ode On, la	le Mod	de On, de Off, de On,	Sleep Sleep	Out		Yes Yes Yes Yes	у		
		Sleep In Yes Status Default Value											
Default		Power On Sequence 00h SW Reset 00h											
			HW Reset						00h			1	



5EH						WI	RCABC	МВ							
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	0	1	0	1	1	1	1	0	5E		
I st parameter	1	1	1	х	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00		
Description	In prin		ationshi	ip is that	00h valu			ue of the		^		ue means	S		
Restriction	-							^	$\overline{\langle \langle \rangle \rangle}$	$\langle \rangle$	\searrow	,			
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default															
Flow chart		HW Reset 00h Legend Command Parameter Display Action New Display Luminance Value Loaded Sequential transfer													



RDCABCMB (5Fh): Read CABC Minimum Brightness

5FH						RI	CABC	ИΒ					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	0	1	0	1	1	1	1	1	5F
1 st parameter	1	1	1	х	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00
	This co	ommand	return t	the minim	num brigh	ntness va	lue of CA	BC funct	ion				
	In prin	ciple rela	ationship	is that 0	00h value	means t	he lowes	t brightne	ess for CA	ABC sol	FFh valu	e means	
Description	the hig	hest brig	ghtness	for CAB	C .				(_ `		\nearrow	
	CMB[7	7:0] is mi	nimum l	brightnes	s forCAE	3C specifi	ed with "	WRCABO	CMB Writ	e CABC	minimum	brightne	ss
	(5Eh)"	commar	nd.					$\rightarrow \rightarrow$	-//	$\prec \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	~		
Restriction	-							$\langle \wedge \rangle$	——————————————————————————————————————	$\forall n$			
					Sta	itus	^		Availa	ability			
			Norm	al Mode		e Mogle (Att Zeleo	1400	Υe				
						Mode ($\rightarrow \rightarrow$	\sim	<u> </u>				
Register Availability						$\overline{}$	<u>/`</u>	\Diamond	Ye				
					-	Mode C	$\checkmark\!\!/\!\!-$		Ye	es			
			Partia	al Mode	On, Idle	Моде С	Xx, Slee	Out	Ye	es			
				>//	Stee	ep/lp/			Υe	es			
			$\langle \langle$	\nearrow	1	/							
					Status				Default \	/alue			
Default	<	7	\overline{Z}	Powe	r On Se	quence			00h	1			
/				~	SW Res	et			00h	1			
))		ı	HW Res	et			00h	l			
Flow chart		_		RDCABCI Send Par CMB[rameter		7			Comm Param Displ: Actic	neter ay		
										Seque trans		j	

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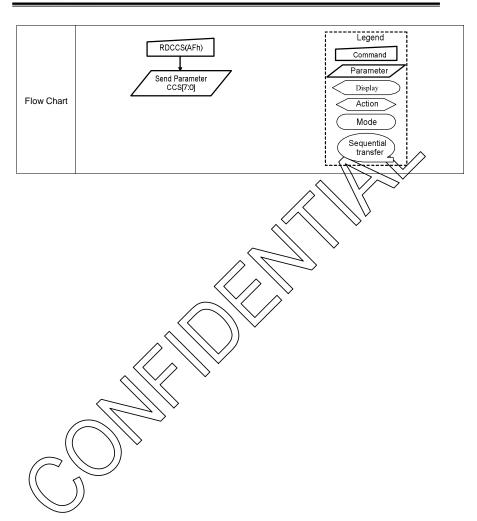
RDFCS (AAh): Read First Checksum

AAH					RI	OFCS (R	ead Fire	st Chec	ksum)						
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	1	0	1	0	1	0	1	0	AA		
1 st parameter	1	1	1	х	FCS7	FCS6	FCS5	FCS4	FCS3	ed from "User Command Set" emory after the write access to the sess on Vizer Command Set" Availability					
Description	regi	isters (not inclu	de "Manı	ufacture (d Set) an								
Restriction				•		after the necksum		last writ	te access	s dn vos	er Comm	nand Set	" area		
					Status					A	vailabilit	у			
		No	ormal M	ode On,	Idle Mo	de Off,	Sieep O	#	>		Yes				
Register		No	ormal M	lode On,	Idle Mo	geon, S	Sleed of	At)			Yes				
Availability		Pa	artial M	ode On,	Idle Mo	de Ott, &	leep Ou	À .			Yes				
		Pa	artial M	ode Ork	Isle Mo	de On, S	leep Ou	ıt			Yes				
				<i></i>	Sleep h	//					Yes				
		·	$\langle \langle$		1	✓ <u> </u>									
				Status						Default \	Value				
Default /		11	Pow	er on Se	quence					00h					
((7	1	S/W Res	set					00h					
				H/W Re	set					D2 D1 D0 0 1 0 3 FCS2 FCS1 FCS0 d from "User Command Set" mory after the write access to the sess on Valer Command Set" Availability Yes Yes Yes Yes					
-((

RDCFCS (AFh): Read Continue Checksum

	(/	,		ntinue									
AFH					RDCF	CS (Re	ad Cont	inue Ch	ecksun	n)			T
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE.
Command	0	1	1	х	1	0	1	0	1	1	1	1	AF
1 st parameter	1	↑	1	х	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	che	cksum	has cal	eturns the culated fr gisters ar	om "Usei	Comma	nd Set" a	area regis	ters and	^		•	
Restriction				y to wait					///	s dovue	er Comn	nand Set	" are
					Status					A	/ailabilit	y	
		No	ormal M	lode On,	Idle Mo	de Off, S	Sleep Or	1/	>		Yes		
Register		No	ormal M	lode On,	Idle Mo	øe On, S	Sleab O	AL.			Yes		
Availability		Pa	artial M	ode On,	Idle Mo	te Ott, &	leep Ou	À			Yes		
		Pa	artial M	ode Ork	Idle Mod	de on, s	leep Ou	ıt			Yes		
				2	Sleep h	//_					Yes		
		<	\bigwedge		7	V							
				Status						Default V	Value		
Default /			Pow	er on Se	quence					00h			
((//	S/W Res	set					00h			
]]		H/W Re	set					00h			
	\cap												

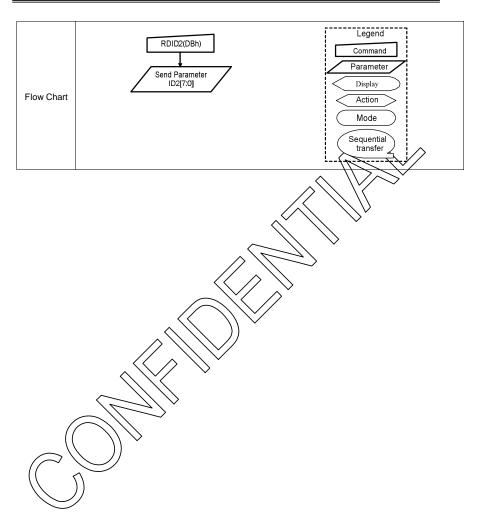
DAH	-		IG ID I				RDID	1					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	1	1	0	1	0	DA
1 st parameter	1	1	1	х	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
Description	This	read b	yte iden	tifies the	TFT LCD	module'	s manufa	cture ID.		^			
Restriction	-											_^	
Register Availability		No Pa	ormal Martial M		Idle Mo	de On, S	Sleep Ou			A	Yes Yes Yes	//	
		Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
					Status					De	fault Va	lue	
Default				Powe	on Sed	uence					00h		
Doraun		•		$\langle \langle \rangle$	SW Res	et					00h		
	·	7		70	HW Res	et					00h		
Flow Chart		RDID1(DAh) Command Parameter Display Action Mode Sequential transfer											



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RDID2(DBh) : Read ID2

DBH							RDID	2					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	1	1	0	1	1	DB
1 st parameter	1	\rightarrow	1	х	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00
Description	mad	e to the	e display	sed to tra , materia ID2 = 80h	al or cons				sion. It is	change	d each tir	ne a ver	sion is
Restriction	-								\triangle		^>`		
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes											
						$\overline{}$	/	\leftarrow			Yes		
					Sleep In	\mathcal{T}	∀				Yes		
					01-1					De	efault Va	lue	
	-	-			Status				4	After MT	P	Before M	ITP
Default				Power	r On Sec	quence			N	ITP Valu	ie	80h	
))	\rightarrow	9	SW Res	et			N	ITP Valu	ie	80h	
		9		ŀ	HW Res	et			N	ITP Valu	ie	80h	
)) 												



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RDID3(DCh): Read ID3

DCH							RDID	3					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	1	1	1	0	0	DC
1 st parameter	1	1	1	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	This	param	eter rea	d byte ide	entifies th	e TFT LC	D modul	e/driver.		^			
Restriction	-											\triangle	
		No	ormal M	lode On,	Status Idle Mo	de Off, S	Sleep Ou	ıt /		A	vailability Yes	//	
Register		No	ormal M	lode On,	Idle Mo	de On, S	Sleep &	/t/ \		\Diamond	Yes		
Availability		P	artial M	ode On,	Idle Mo	de Off, S	Sleep Ou	rt //	\rightarrow		Yes		
		Pa	Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes										
					Status	<i></i>	<u> </u>			De	efault Va	lue	
					Status				Д	fter MTI	P	Before N	MTP
Default		·		Rowe	r On Sed	quence			M	ITP Valu	ie	00h	
		7	=	70	SW Res	et			М	ITP Valu	ie	00h	
				ŀ	HW Res	et			M	ITP Valu	ie	00h	
Flow Chart	RDID3(DCh) Send Parameter ID3[7:0] Legend Command Parameter Display Action Mode Sequential transfer												

IFMODE (B0h): Interface Mode Control

вон							IFMOD	DE					
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	0	1	1	0	0	0	0	В0
1 st parameter	1	1	1	х	SDA_E N	х	х	х	VSPL	HSPL	DPL	EPL	xx
Description	DPL HSF VSF SDA SDA SDA	DINS	(polarity (NC pola (NC	o"= High of set ("0"= arity ("0"=	enable for data fetch data fetch Low level Low level Low level size used for the face so the fetch data fetch data fetch low level Low l	RGB interpretation and at the sync close election. The used from 3/4 with the sync close election. The used from 3/4 with the sync close election.	erface, "1" er rising tir ck, "1" er sock, "1" er sock, "1" er e social in mand	"=Low er me, "1"=c ligh level High level High level High level High level III III III III III III III III III I	nable for lata fetch sync clores of the content of	RGB integer and the ed at	not used. Day D2	\wedge	

	SDA_EN=0			
			Command	Read Data
	CSX	_	*	
	SCL			www
	DIN/SDA		0 \ \D5 \ \D5 \ \D5 \ \D3 \ \D2 \ \D1 \ \D0	
	DOUT			DI DO DI DO
	SDA_EN=1			
	CSX		Command	Read Data
	SCL DIN/SDA			`nnnnnn_
	DIN/SDA			D7 \ D6 \ D5 \ D4 \ D8 \ D2 \ D1 \ D0 \
	DOUT		1)-2	
	<	\langle / \rangle		'
Restriction			\rightarrow	
(Status	Availability
	Norma	Mode	On, Idle Mode Off, Sleep Out	Yes
Register	Norma	l Mode	On, Idle Mode On, Sleep Out	Yes
Availability	Partial	Mode	On, Idle Mode Off, Sleep Out	Yes
	Partial	Mode	On, Idle Mode On, Sleep Out	Yes
			Sleep In	Yes

	Status	Default	Value
		After MTP	Before MTP
Default	Power On Sequence	MTP Value	00h
	SW Reset	MTP Value	0 00h
	HW Reset	MTP Value	00h
		-//	
	RDID3(DCh)	Legend]
Flow Chart	Send Parameter ID3[7:0]	Parameter Display Action	
Tiow chair		Mode)
		Sequential transfer)
	· · · · · · · · · · · · · · · · · · ·		
((
	•		

FRMCTR1 (B1h): Frame Rate Control (In Normal Mode/Full Colors)

B1H		FRMCTR2 (Frame Rate Control (in Idle Mode/8 Colors)) D/CX RDX WRX D15-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX											
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	х	1	0	1	1	0	0	0	1	B1
1 st Parameter	1	1	1	х	FRS3	FRS2	FRS1	FRS0	0	0	DIVA1	DIVA0	XX
2 nd parameter	1	1	1	х	0	0	0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0	Xx
	FRS	8[3:0]:	Sets tl	ne fram	ne frequ	iency o	f full c	olor nori	nal mod	de.		^	
		RT	NB[3:0)]	Frame	rate(Hz	<u>z</u>)		RTNB[4:0]	Fram	e rate(F	Hz)
		-	0000		:	28			1000)		50	
			0001			30			1001			56	
			0010			32			1010			62	
			0110			34 36			1011			70 81	
			0100			39			1100			96	
			0110		42				1110				
			0111			46			1111			117	
			/>`	V	DIV	'A[1:0]		Divi	sion Rat	io			
	DIV	A [1:0]	: divis	SION PAL			Mocks	when N					
Description		(//	<u> </u>	$\sqrt{\circ}$	0			fosc				
Description		\langle / \rangle	${}$	_	Y 0	1			osc/2				
	<u>(</u> -	_//	//	> -	1	1			osc/4				
			2)		'				USC/O				
))												
	\mathcal{D}												

		/ (-1.0) 13 d3Cd t0 C	set in (line) pendu	of Idle mod	e at CPU interface
	RTNB[4:0]	Clock per L	ine RT	NB[4:0]	Clock per Line
	00000	Setting prohib	ited	10000	16 clocks
	00001	Setting prohib	ited	10001	17 clocks
	00010	Setting prohib	ited	10010	18 clocks
	00011	Setting prohib	ited	10011	19 clocks
	00100	Setting prohib	pited	10100	20 clocks
	00101	Setting prohib	pited	10101	21 clocks
	00110	Setting prohib	pited	10110	22 clocks
	00111	Setting prohib	pited	10111	23 clocks
	01000	Setting prohib	pited	11000	24 clocks
	01001	Setting prohib	pited	11001	25 clocks
	01010	Setting prohib	ited	11010	26 clocks
	01011	Setting prohib	ited	11011	27 clocks
	01100	Setting prohib	ited	11100	28 clocks
	01101	Setting prohib	ited	11101	29 clocks
	01110	Setting prohib	ited	11110	30 clocks
	01111	Setting prohib	ited	11111	31 clocks
		mal Mode On, Idl	e Mode Off, Sleep (Out	ailability Yes Yes
gister Availability			e Mode Off, Sleep C		Yes
	Pai	rtial Mode On, Idle	e Mode On, Sleep (Out	Yes
		Sle	ep In		Yes
		Status	Defau	It Value	
		ORIUS	DIVA[1:0]	RTNA	A[4:0]
		Ciaido	DIVA[1.0]		
Default	Pow	er On Sequence	2'b00	5'b1	-

В2Н			FRM	CTR2 (F	rame	Rate	Contr	ol (in lo	lle Mod	le/8 Col	ors))		
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	0	1	1	0	0	1	0	B2
1 st Parameter	1	1	↑	х	0	0	0	0	0	0	DIVB1	DIVB0	Xx
2 nd parameter	1	1	1	х	0	0	0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0	Xx
	Sets t	he divis	sion ratio	o for inte	rnal cl	ocks o	of Idle	mode a	at CPU	interfac	3		
	DIVB	[1:0] : c	livision i	ratio for i	nterna	al cloc	ks wh	en Idle	mode(\	·			
				יום	VB[1:0	0]		Division	n Ratio		>>\		
				0		0		180	sc	\overline{N}	•		
				0		1		Tos	c/2	\mathbb{Z}_h			
				1		0		fos	C/A				
				1		₹		fos	c/8>				
						, //	7	2)					
	RTNE	3 [4:0] :	RTNB[4	l:0] is use	ed to s	set/IH	(linge)	period	of Idle i	mode at	CPU ir	iterface.	
		RTNB	[4:0]	Clock	per L	ine		R ⁻	TNB[4:0)]	Clock p	er Line	
		000	00	Setting	prohil	oited			10000		16 cl	ocks	
		000	01	Setting	prohil	oited			10001		17 cl	ocks	
		000	10	Setting prohibited				10010			18 clocks		
Description		000	11	Setting	prohil	prohibited			10011		19 cloc		
	1	001		Setting	-				10100		20 cl		
	<	001		Setting			1		10101		21 cl		
		001		Setting					10110		22 d		
		001		Setting					10111		23 cl		
1.1	01000	Setting prohibited					11000		24 cl				
))	010	01001	Setting prohibited				11001			25 clocks		
									11010		26 d	ocks	
		010 010 010	10	Setting	prohil	oited			11010		26 cl 27 cl		
		010	10 11		prohit prohit	oited	_					ocks	
		010 010	10 11 00	Setting Setting	prohib prohib prohib	oited oited			11011		27 cl	ocks ocks	
		010 010 011	10 11 00 01	Setting Setting Setting	prohib prohib prohib prohib	oited oited oited	-		11011 11100		27 cl 28 cl	ocks ocks	

Restriction		
	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Pes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	799
	Status Default Val	ue RTNB[4:0]
Default	Power On Sequence 22000	5'b10001
	HW Reset 2'b00	5'b10001
<		

взн	FRMCTR3 (Frame Rate Control (in Partial Mode/Full Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	0	1	1	0	0	1	1	ВЗ
1 st Parameter	1	1	1	х	0	0	0	0	0	0	DIVC1	DIVC0	xx
2 nd parameter	1	1	1	х	0	0	0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0	xx
	Sets the division ratio for internal clocks of							mode a	t CPU i	interfac	8	l	I
	DIVC [1:0]: division ratio for internal clocks when Partial mode.									È._`		/	
	DIVC[1:0]							Division	n Ratio				
				0		0	Posc						
				0		1	/	\fos	-	$\angle A$			
	1 0						$\langle \rangle$	fos	Ç/M	~			
	1 1							fos	c/8				
						//	<u></u>	<i>-</i> 2					
RTNC [4:0] : RTNC[4:0] is used to set H (line) period of Partial mode at CPU interface											ice.		
		RTNB[4:0] Clock per Line						R	TNB[4:0)]	Clock p	er Line	
		000	00	Setting	prohil	oited			10000		16 cl	ocks	
		000	01	Setting prohibited					10001		17 clocks		
		000	10	Setting prohibited					10010		18 cl	ocks	
Description		000	11	Setting prohibited			_		10011		19 cl	ocks	
	1	001	00	Setting	prohil	oited			10100		20 clocks		
		001	01	Setting	prohil	oited			10101		21 clocks		
	1/	001	10	Setting	prohib	oited			10110			22 clocks	
		001	11	Setting	prohil	oited			10111		23 clocks		
((010	00	Setting	prohil	oited			11000		24 cl	ocks	
	//	010	01	Setting	prohil	oited			11001		25 clocks		
	レノト			Setting prohibited					11010		26 cl	ocks	
		010	10	Setting									
		010 010		Setting	prohil	oited			11011		27 cl	ocks	
			11						11011 11100		27 cl 28 cl		
		010	11 00	Setting	prohib	oited						ocks	
		010	11 00 01	Setting	prohit prohit	oited			11100		28 cl	ocks ocks	

Restriction		
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Register Availability	Partial Mode On, Idle Mode Off, Sleep Out	res
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	795
	Status DIVC[1:0]	lue RTNC[4:0]
Default	Power On Sequence 2'b00	5'b10001
	HW Reset 2'080	5'b10001

Rev : 0.3

	INVTR (Display Inversion Control)													
B4H				IN	VIK (DISPI	ay inv	ersion	Contro	1)				
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	х	1	0	1	1	0	1	0	0	B4	
Parameter	1	1	1	х	0	0	0	ZINV	0	0	DINV1	DINV0	xx	
	ZINV	: Set Z-	inversio	n mode			^							
					ZINV Status									
					0		+	isable Z-		\sim		//		
					0		Е	nable Z-	inversio	$\langle \downarrow \rangle$	>> <u>`</u>			
										\mathcal{M}				
	-	DINV[1:0] : Set the inversion mode.												
		DINV[1:	:0]				Dot i	nversior	n mode					
		2'b00		lumn ersion	Lines	1 + 2 + 3 + 4 +		+ - + - + - + -		2 ^{nc} 1 - 2 - 3 - 4 -	+ - + - + - + -	+ + + + +		
Description		2'b01		-dot ersion	Lines	1 + 2 - 3 + 4 -	+	+ - + + - + - + + - + + - + + + - + + + - +		2 ^{nc} 1 - 2 + 3 - 4 +	+ - + + - + + - + + + + + + + + + + + +	+ + + -		
		2'b10		-dot ersion	Lines	1 + 2 + 3 -	1 st Fr	ame + - + - + - + + + + +		2 ^{nc} 1 - 2 - 3 + 4 +	Frame + - + - + - + + - + +	+ +		
		2'b11					Set	ting proh	ibited	•				

Restriction		
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Register Availability	Partial Mode On, Idle Mode Off, Sleep Out	(Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	No.
	Status Default Value	
	Status ZINV	DINV[1:0]
Default	Power On Sequence	2'b00
	HW Reset	2'b00
•	$\langle \langle \rangle \rangle$	
F		
	→	
(

В5Н		PRCTR (Blocking Porch Control)											
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	0	1	1	0	1	0	1	B5
1 st Parameter	1	1	1	x	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	xx
2 nd parameter	1	1	1	х	VBP7	VFB6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	Xx
3 rd parameter	1	1	1	х	0	0	0	HFP4	HFP3	HPR2	HFP1	HFP0	Xx
4 nd parameter	1	1	1	х	HBP7	HFB6	HBP5	HBP4	HBP3	HBP2	HBR1	ивро	Xx
		•	•				•	•	- + +	$\overline{}$	$\overline{}$		

VFP [7:0] / VBP [7:0]: The VFP [7:0] and VBP [7:0] bits specify the lime number of vertical front and back porch period respectively.

VFP[7:0]	Number of lines of front porch
00000000	Setting prohibited
0000001	Setting prohibited
0000010	2
00000011	3
:	:
=	:
11111100	252
11111101	253
11111110	254
11111111	255

VBP[7:0]	Number of lines of front porch
00000000	Setting prohibited
0000001	Setting prohibited
00000010	2
00000011	3
:	:
:	:
11111100	252
11111101	253
11111110	254
11111111	255

Description

HBP [7:0]: The HFP [4:0] and HBP [7:0] bits specify the dotclk number of horizontal back porch period.

//		front porch
]]	00000	Setting prohibited
	00001	Setting prohibited
	00010	2
	00011	3
	:	:

11100

11101

11110

11111

HBP[7:0]	Number of dotclk of front porch
00000000	Setting prohibited
0000001	Setting prohibited
00000010	2
00000011	3
:	:
11111100	252
11111101	253
11111110	254
11111111	255

00000000	Setting prohibited
0000001	Setting prohibited
00000010	2
00000011	3
:	:
:	:
11111100	252
11111101	253
11111110	254
11111111	255

28

29

30 31

Number of dotclk of

DISCTRL (Display Function Control) DISPLAY FUNCTION CONTROL (DISPLAY FUNCTION CONTROL (DIS	DISCTRL	_ (B6h): Display Function Control												
Command 0 1 ↑ x 1 0 1 1 0 1 1 0 B6 1st parameter 1 1 ↑ x BYPASS RCM RM DM PTG[1] PTG[0] PT[1] PT[0] x PT[0] x 2nd parameter 1 1 ↑ x 0 GS SS SM ISC[3] ISC[2] ISC[1] ISC[0] xx 3rd parameter 1 1 ↑ x 0 NL[5] NL[4] NL[3] NL[2] NL[1] ML[0] xx DM Interface Mode 0 Interface Mode 0 Interface Mode RM Interface for GRAM access 0 Via System interface	В6Н					DISC	TRL (D	isplay F	unction	Contro	ol)			
1st parameter 1 1 ↑ x BYPASS RCM RM DM PTG[1] PT[0] x 2nd parameter 1 1 ↑ x 0 GS SS SM ISC[3] ISC[2] ISC[1] ISC[0] xx 3rd parameter 1 1 ↑ x 0 0 NL[5] NL[4] NL[2] NL[1] NL[0] xx DM Interface Mode 0 Interface Mode 0 Interface Mode 0 RGB Interface RM Interface for GRAM access 0 Na System interface 0 Na System interface		D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
2 nd parameter 1 1 1	Command	0	1	1	х	1	0	1	1	0	1	1	0	В6
DM: Select the display operation mode. DM Interface Mode 0 Internal system block 1 RM: Select the interface to access the GRAM. RM Interface for GRAM access 0 Via System interface	1 st parameter	1	1	1	x	BYPASS	RCM	RM	DM	PTG[1]	PTG[0]	PT[1]	PT[0]	x
DM: Select the display operation mode. DM	2 nd parameter	1	1	1	х	0 GS		SS	SM	ISC[3]	ISC[2]	ISC[1]	ISC[0]	xx
DM Interface Mode 0 Internal system block 1 RGB Interface RM: Select the interface to access the GRAM. RM Interface for GRAM access 0 Yea System interface	3 rd parameter	1	1	1	х	0	0	NL[5]	NL[4]	NL[3]	NL[2]	WL[1]	NT[0]	xx
0 Internal system dook 1 RGB Interface RM: Select the interface to access the GRAM. RM Interface for GRAM access 0 Via System interface		DM: Select the display operation mode.												
RM: Select the interface to access the GRAM. RM Interface for GRAM access 0 Via System interface		DM Interface Mode												
RM: Select the interface to access the GRAM. RM Interface for GRAM access 0 Wa System interface														
RM Interface for GRAM access 0 Wa System interface														
0 Na System interface														
		RM Interface for GRAM access												
1 Via RGB interface														
RCM: RGB interface selection.		RCM: RGB interface selection:												
RCM RGB transfer mode		RCM RGB transfer mode												
DE Mode				,	$\sqrt{\sum}$	18	<i>))</i>		DE M	ode				
1 SYNC Mode						/1/								
BYPASS: Select the display data path, when RGB interface is used.		BYP	ASS:	Select	the disp	lay data	path, w	hen RGI	B interfa	ice is us	ed.			
Description BYPASS Display data path	Description	~	_ /			BYPASS		Di	isplay da	ata path				
0 Memory			=	$\overline{\gamma}_{\prime}$	\ <u>\</u>				Mem	ory				
1 Direct to shift register		(` _		1		Dire	ct to shi	ift registe	er			
((PTG(10)]: Sets the scan mode in non-display area.	((PTĠ	1/1/0]:	Sets th	e scan	mode in	non-dis	play area	a.					
PTG[1] PTG[0] Gate outputs in non-display area Source outputs in non-display area)	РТ	G[1] P	TG[0]	ate outp	uts in n	on-displa	ay area	Source of	outputs in	n non-di	splay are	ea
0 0 Normal scan Set with PT[2:0]	((7		()	0		Normal	scan			Set witl	h PT[2:0]	
0 1 Setting prohibited			(0	1	Se	etting pr	ohibited						
1 0 Interval Set with PT[2:0]				1	0		Inter	/al			Set witl	n PT[2:0]	
1 1 Setting prohibited				1	1	Se	etting pr	ohibited						
]													

PT[1]	PT[0]	Source outputs in non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: select the shift direction of outputs from the source driver.

SS	Source output scan direction
0	S1à S260
1	S960 2 S1

ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where h is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

	_		//	
		ISC[3:0]	Scan cycle	(fFRAME)=60Hz
		4'h0	Setting inhibited	_
		47K1	3 frames	50ms
		1 4 HZ) 5 frames	84ms
		4×3	7 frames	117ms
	$\cdot \cdot \cdot \cdot \cdot$		9 frames	150ms
		4'h5	11 frames	184ms
		→ 4'h6	13 frames	217ms
		4'h7	15 frames	251ms
((4'h8	17 frames	284ms
\sim //))	4'h9	19 frames	317ms
\sim $\stackrel{\backslash}{\scriptstyle}$		4'hA	21 frames	351ms
()		4'hB	23 frames	384ms
		4'hC	25 frames	418ms
		4'hD	27 frames	451ms
		4'hE	29 frames	484ms
		4'hF	31 frames	518ms

GS: select the direction of scan by the gate driver.

GS	Source output scan direction
0	G1à G480
1	G480 à G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0	Colds in that THT form THT form GATTS GA	G1 G2, G3, G4,G475 G477, G478 G480
0	1	Odd number G1 G2 G3 G4 Even-number G477 G378 G479 G479 G470 G470	G480, G479, G478,, G9 G7, G5, G4, G3, G2, G1
1	O.	Odd-number G1 TFT Punel G479 G2 G2 G3 G480 G480	G1, G3, G5, G7,, G471 G473, G475, G477, G479 G2, G4, G6, G8,, G472 G474, G476, G478, G480
1	1	1 TET FO X:1	G4III: 6476, G478 - G14 G12, G13, G8, G8, G1, G2 G478, G477, G475,G13 G11, G8, G7, G5, G3, G1

	NL[5	:0]: Sets the num	nber (of lines to o	drive the L	.CD at	an inten	al of 8	lines. The	GRAM addres	ss	
	map	oing is not affect	ed by	the number	er of lines	set by	NL[5:0]	. The nu	ımber of li	nes must be the	ie	
	same	e or more than th	e nur	nber of line	s necess	ary for	he size	of the li	quid crysta	al panel.		
			N	L[5:0]		LCD I	Orive Lir	ne				
			6'h00	0 ~ 6'h3B	8	3 * (NL5	i:0]+1) li	nes				
			C	thers Setting inhibited								
										\wedge		
								R				
Restriction							\wedge		>/>>	/		
				Status			Avei	lability	ĺ			
				Status		$\overline{}$	Avai		-}			
		Normal Mode On, Idle Mode Off, Sle€ Out Yes Yes										
		Normal Mod	le On	, Idle Mode	On, Slee	p Oby		es				
Register Availability		Partial Mode	e On,	Idle Mode	Off, Shee	QOut	> ,	'es				
		Partial Mode	e On,	Idle Mode	Øŋ, Sleej	λ Out	Υ	'es				
				Sleep In		/	Y	'es				
			/	$\langle \cdot \rangle$					_			
Default		\nearrow			,							
		Status		222			efault V					
		11 11		PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]		
	~	Power On Seque	ence	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011		
		HW-Reset		2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011		
		Otataa				С	Default Value					
	\supset	Status		R		DM		BY	BYPASS			
(())		Power On Seque	ence	1'	b0		1'b0			1'b0		
		HW Reset		1'	b0		1'b0			1'b0		

ETMOD (B7h) : Entry Mode Set

В7Н	Interface Mode Control													
D/III	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	Х	1	0	1	1	0	1	1	1	B7	
Parameter	1	1	1	Х	EPF[1]	EPF[0]	0	0	DSTB	GON	DTE	GAS	XX	
				ep Stan	•					Α.				
		internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory powent and												
		-							te Fra	me M	emory	conen	and	
	instru	ctions a	ifter the	Deep St	aandby	/ Mode	is exite	ed.		$\langle \rangle \rangle$				
							,	/	/ /	$\langle \langle \rangle$	~			
	GAS:	GAS: Low voltage detection control.												
	GAS Low voltage detection 0 Enable 1 Disable													
	GON/	GON/DTE: Set the output level of gate driver G1~G320 as follows												
	GON DTE G1~G320 Gate Output													
				8	b)	× \	/GH							
Description			> //	$\ell / /$	/1/_	1	/GH							
Description			\triangle	1//	0	1	/GL							
	\ \		//	1	1	ı	Normal	display	/					
		// .												
	EPFT	H:0]: set	the dat	a format	when '	16bbp(l	R,G,B)	to 18b	bp(R,G	i,B) is s	tored i	n the in	ternal	
	GRAN	X												
((1)	\lor	Inr	out data										
				Jui Gala										
((^					G	reen d	ata =	<u> </u>						
			Gre	een Date	>—	odd	(RÆ	B Data	>R	=B ¬				
				\ <u></u>				~						
			en data =	= ├ ──										
			even	_			R!=B			<u> </u>				
			(1	Bypass)			(Ву	pass)			
					_						_			
Restriction														

			5	Status		Availability	
		Norma	al Mode On, I	Sleep Out	Yes		
		Norma	al Mode On, I	Sleep Out	Yes		
Register Availability		Partia	l Mode On, Id	Sleep Out	Yes		
		Partia	l Mode On, Id	Sleep Out	Жęs		
					Yes		
				eep In	(1001	\checkmark
					$\rightarrow \wedge$	\ <u>/</u> /^>	> <u>*</u>
	01-1				Default Value		
Default	Status	5	EPF[1:0]	DSTB	GON	DTE	GAS
	Power On Se	quence	2'b00	1'b0	1'b\	1'b1	1'b0
	HW Re	set	2'b00	120	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	1'b1	1'b0
					>		

PWCTF	RL1 (C	0h): I	Power (Control	1									
СОН		PWCTRL1 (Power Control 1)												
	D/CX	RDX	WRX	D15-8	5-8 D7 D6 E		D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	х	1	1	0	0	0	0	0	0	C0	
1 st parameter	1	1	1	х	0	0	0	VRH1[4]	VRH1[3]	VRH1[2]	VRH1[1]	VRH1[0]	xx	
2 nd parameter	1	1	1	х	0	0	0	VRH2[4]	VRH2[3]	VRH2[2]	VRH2[1]	VRH2[0]	xx	
	VRH1	[4:0]:	Sets the	e VREG	1OUT v	oltage f	or pos	itive gan	nma	^		\triangle		
				1			T			A.		//		
		VI	RH1[4:0]	V	REG10	UT	VRI	11[4:0]	XRE	G100T		•		
			5'h00		Halt			'h10	125 x 34	5 = 4.562	5V			
			5'h01	1.25	1.25 x 2.90=3.6250V			'h11	125 x 3.	70 = 46250	οV			
			5'h02	1.25	× 2.95 = 3	.6875V	5	'h12	1.25 x 3.	7 5 = 4.6875	5V			
			5'h03	1.25	3.00 = 3	.7500V	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	713	1.85 x 3.8	30 = 4.7500	υV			
			5'h04	1.25	1.25 x 3.05 = 3.8128V			'n\	1.25 x 3.85 = 4.8125V		5V			
			5'h05	1.25	(3.10 -3	8758V	5	'M\$	1.25 x 3.9	90 = 4.8750	υV			
			5'h06	1.25	(8.15 = 3	.9375	V ₅	'h16	1.25 x 3.90 = 4.87		υV			
			5'h07	1230	(3.20=4	.000gV)	5	'h17	1.25 x 4.0	00 = 5.0000	υV			
Description			5'h08	1,25	325 = 4	.0625V	5	'h18	1.25 x 4.0	05 = 5.0625	5V			

5'h19

5'h1A

5'h1B

5'h1C

5'h1D

5'h1E

5'h1F

1.25 x 4.10 = 5.1250V

1.25 x 4.15 = 5.1875V

1.25 x 4.20 = 5.2500V

1.25 x 4.25 = 5.3125V

1.25 x 4.30 = 5.3750V

1.25 x 4.35 = 5.4375V

1.25 x 4.40 = 5.5000V

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	VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT
	5'h00	Halt	5'h10	-1.25 x -3.65 = -4.5625V
	5'h01	-1.25 x 2.90=-3.6250V	5'h11	-1.25 x -3.70 = -4.6250V
	5'h02	-1.25 x 2.95 = -3.6875V	5'h12	-1.25 x -3.75 = -4.6275V
	5'h03	-1.25 x 3.00 = -3.7500V	5'h13	-1.25 x -3.80 = -4.7500V
	5'h04	-1.25 x 3.05 = -3.8125V	5'h14	-1.25 x -3.85 = -4.8125V
	5'h05	-1.25 x 3.10 = -3.8750V	5'h15	1.25 x 3.90 = -48150V
	5'h06	-1.25 x 3.15 = -3.9375V	5'h16	1.25 x -3.90 = 4.8750V
	5'h07	-1.25 x 3.20 = -4.0000V	5'h1X	-1.25 x-4.00 = -5.0000V
	5'h08	-1.25 x 3.25 = -4.0625V	€h18	1.25 x -4.05 = -5.0625V
	5'h09	-1.25 x 3.30 = -4.1250V	5'M9	-1.25 x -4.10 = -5.1250V
	5'h0A	-1.25 x 3.35 = -4.18\(\)5\(\)	5'h14	-1.25 x -4.15 = -5.1875V
	5'h0B	-1.25 x 3.40 = -4.2500V	5/h1B	-1.25 x -4.20 = -5.2500V
	5'h0C	4.26 x 3.45 = -4.3125V	5'h1C	-1.25 x -4.25 = -5.3125V
	5'h0D	-1.25 x 3.50 = -4.3750V	5'h1D	-1.25 x -4.30 = -5.3750V
	S/OE	1.25 x 3.55 = -4.4375V	5'h1E	-1.25 x -4.35 = -5.4375V
	5'h0F	1.25 x 3.60 = -4.5000V	5'h1F	-1.25 x -4.40 = -5.5000V
		>		
	11/7			
⋾∖	<i>))</i>			
7				

1.25 x 3.30 = 4.1250V

25 x 3.35 = 4.1875V

1.25 x 3.40 = 4.2500V

1.25 x 3.45 = 4.3125V

1.25 x 3.50 = 4.3750V

1.25 x 3.55 = 4.4375V

1.25 x 3.60 = 4.5000V

5'h0D

5'h0E

5'h0F

PWCTRL2 (C1h): Power Control 2

C1H						PWCT	RI 2 (D	ower Co	ntrol 2\				
СІП						1	,	1				I	
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	0	0	0	0	1	C1
1 st parameter	1	1	1	х	0	0	0	0	0	BT[2]	BT[1]	BT[0]	Xx
2 nd parameter	1	1	1	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	Xx
	VC[2	2:0] Se	ts the r	atio facto	r of Vo	i to ger	nerate t	he refere	ence volta	ages Vci	1.	\wedge	
						VC[2:0]	Vci1 v	oltage	1		//	
İ						3'h0		1.0 x	VA ($\sqrt{}$	/~		
						3'h1 8.7V					\rangle		
						3'h2 30 V							
						3'h3	3 5	2.0	ZV.				
						3'K4/	$\langle \rangle$	2.8	V				
						3'h\$		<u>∕</u> 2.7	V				
							3'h6 2.6 V						
			,	$^{\wedge}$		3'h7)	2.5	V				
Description				/ />.		V .				_			
	ВП2	0] Sę BT[2	<i>\ \</i>	Step up fa DDVDH		nd outp DDVDL		ige level VCL	from the VGH		e voltage VGL	es Vci.	
	•	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	_ \	1							- Vci x 5	i	
		3'h		\rightarrow					Vci x (6	- Vci x 4		
_ ((3'1	2								- Vci x 3	i	
		₹h	3	\/-:4·-0		5 \/) / - :			- Vci x 5	i	
	$)) \mid$	3'h	14	Vci1x 2		-5V		- Vci	Vci x	5	- Vci x 4		
		3'h	5								- Vci x 3	i	
		3'h	16						Vci x 4	4	- Vci x 4		
		3'h	7						V CI X	7	- Vci x 3		

C2H				Р	WCTRL	3 (Powe	r Contr	ol 3 for	Normal	Mode)			
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	х	1	1	0	0	0	0	1	0	C
I st parameter	1	1	1	x	DCA1[3]	DCA1[2]	DCA1[1]	DCA1[0]	DCA0[3]	DCA0[2]	DCA0[1]	DCA0[0]	XX
Description	pum [[Not DC# Norm]]	pp) foor DCA0 1 b 1 b 1 b 1 b 1 b 1 b 1 b 1 b 1 b 1	r Normal	at the ope at mode. CAO[2:0] 3'b000 3'b001 3'b010 3'b101 3'b110 3'b110 3'b111 x 30=34.70 3'b010 3'b111 x 30=34.70 3'b110 3'b110 3'b110 3'b110 3'b110 3'b110	Degrating	Step-u	cy of th	for Step- 1/8 H 1/4 H 1/2 H 2 H 2 H 2 H 18 H 18 H	pupreircu	tit va			

	Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.									
	Note 2: Set following voltages within the respective ranges:									
	DDVDH = 6.0V (max)									
	VGH = 18.0V (max)									
	VGL= -12.5V (max)									
	VCL= -3.6 (max).									
	Status Availability									
	Normal Mode On, Idle Mode Off, Steep Out Yes									
Register	Normal Mode On, Idle Mode On, Sleep Out Yes									
Availability	Partial Mode On, Idle Mode Off, Steep Out Yes									
	Partial Mode On, Idne Mode On, Sleep Out Yes									
	Steep In Yes									
	Status Default Value									
Default	Power on Sequence VC[2:0]=3'h0, BT[2:0]=3'h0									
Delauit	SVX Reset No change									
	VC[2:0]=3'h0, BT[2:0]=3'h0									

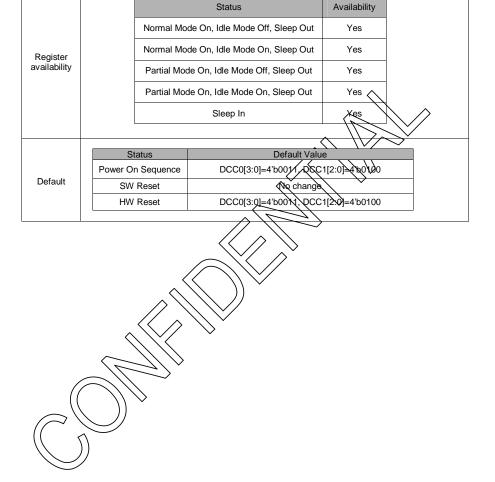
СЗН	PWCTRL4 (Power Control 4 for Idle Mode)														
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	х	1	1	0	0	0	0	1	1	C3		
1 st parameter	1	1	1	x	DCB1[3]	DCB1[2]	DCB1[1]	DCB1[0]	DCB0[3]	DCB0[2]	DCB0[1]	DCB0[0]	xx		
	pum E	p) for DCB0 1'b' 1'b' 1'b' 1'b' 1'b' 1'b' 1'b' 1'b	r Idle m r Idle m r Idle m 1 1 1 1 1 1 1 1 1 1 1 1 1	ode. OCB0[2:0 3'b000 3'b001 3'b010 3'b100 3'b101 3'b110 3'b110 3'b111 x 30=34.7()] 	Step-L	ip cycle	step-up for Step- 1/8 H 1/4 H 1/2 H 2 H 18 H 18 H 18 H	upreircu	it &					
Description	mod				S. Francis J.		, 00	otop up		(. 0, 0		pap/c	u.		
	Е	CB1	/ /	CB1[2:0)]	Step-	up cycle	for Step	-up circ	uit 3					
		1'b'	_ \	3,9000				1/8 H							
		140	$\overline{}$	375010				1/4 H							
		1'b.		3'b010				1/2 H 1 H							
((1'b	$\overline{}$	3'b100				2 H							
\bigcirc	M	1/2	1	3'b101				4 H							
		1'b'	1	3'b110				8 H							
((,	\ \	411	1	3'b111				16 H							
((.)) ∟	1'b'		00111											
		1'b()	x 30=34.7u				2H							

C4H				Р	WCTRL	.5 (Pow	er Contr	ol 5 for	Partial I	Mode)			
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
Command	0	1	1	x	1	1	0	0	0	1	0	0	C4
1 st parameter	1	1	1	x	DCC1[3]	DCC1[2]	DCC1[1]	DCC1[0]	DCC0[3]	DCC0[2]	DCC0[1]	DCC0[0]	Χ
Description	pum C Note DCC Parti	p) for cCC0 1'b1 1'b1 1'b1 1'b1 1'b1 1'b1 1'b1 1'b	Partial [3] [1]	ct the opoli mode. OCC0[2:0 3'b000 3'b001 3'b010 3'b101 3'b110 3'b111 x 80=34.7u 3'b080 3'b011 3'b100 3'b011 3'b110 3'b111 x 80=34.7u	B = 1/28	Step-L	up cycle	for Step- 1/8 H/ 1/4/14 1/2 H 2 H 2 H 2 H 18 H 18 H	up circui	it vo		/GL pun	

		Status	Availability				
	Normal Mo	Normal Mode On, Idle Mode Off, Sleep Out					
Register	Normal Mo	de On, Idle Mode On, Sleep Out	Yes				
availability	Partial Mod	de On, Idle Mode Off, Sleep Out	Yes				
	Partial Mod	de On, Idle Mode On, Sleep Out	Yes				
		Sleep In	Xes				
				\swarrow			
	Status	Default Valu	e				
	Power On Sequence	DCB0[3:0]=4'b001/ DCB	1[2:0]=4 b0 100				
Default	SW Reset	(No change					
	HW Reset	DCB0[3:0]=4'b00'M, DCB	1[2:0]=4'b0100				
	(17)						

Rev: 0.3

С5Н						VC	OM Con	itrol					
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	1	0	0	0	1	C5
1 st parameter	1	1	1	х	0	0	0	0	0	0	0	NVM	xx
2 nd parameter	1	1	1	х	VCM_R EG[7]	VCM_R EG[6]	VCM_R EG[5]	VCM_R EG[4]	VCM_R EG[3]	VCM_R EG(2)	VCM_R EG[1]	VCM_R EG[0]	xx
3 rd parameter	1	1	1	х	VCM_R EG_EN		0	0	0 (.	9/	B	\rangle	XX
4 rd parameter	1	1	1	х	VCM_O UT[7]	VCM_O UT[6]	VCM_O UT[5]		0.1[3] XCW ⁻ 0	VCM VTJZ]	VCM O UT[1]	VCM_O UT[0]	хх





- 0 : NV memory is not programmed
- 1 : NV memory is programmed

VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

	VILUZUUT.			
	VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM
	8'h00	-2	8'h20	-1.5
	8'h01	-1.98438	8'h21	-1.48438
	8'h02	-1.96875	8'h22	-1,46875
	8'h03	-1.95313	8'h23	-1/45313
	8'h04	-1.9375	8'h24	-1.4378
	8'h05	-1.92188	8'h25	-1,42188
	8'h06	-1.90625	8'h2ø	-1.40628
	8'h07	-1.89063	8627	-1.39063
	8'h08	-1.875	8'h28	-1.375
	8'h09	-1.85938	78429	-1.35938
	8'h0A	-1.84375	84h8A	-1.34375
	8'h0B	-1.82813	8'h2B	-1.32813
	8'h0C	-1.8125	8 1/2 C	-1.3125
escription	8'h0D	-1.79688	8'h2D	-1.29688
	8'h0E	-1,78125	8'h2E	-1.28125
	8'h0F	-4,76568/	8'h2F	-1.26563
	8'h10	1.75	8'h30	-1.25
	8(h)1	-1.73438	8'h31	-1.23438
	8'h12	-1.71875	8'h32	-1.21875
	78p13-7	-1.70313	8'h33	-1.20313
	8 k 14	-1.6875	8'h34	-1.1875
	8'h 15	-1.67188	8'h35	-1.17188
\sim //) \$ 'h16	-1.65625	8'h36	-1.15625
~ /:	8'h17	-1.64063	8'h37	-1.14063
\mathcal{L}	8'h18	-1.625	8'h38	-1.125
	8'h19	-1.60938	8'h39	-1.10938
	8'h1A	-1.59375	8'h3A	-1.09375
	8'h1B	-1.57813	8'h3B	-1.07813
	8'h1C	-1.5625	8'h3C	-1.0625
	8'h1D	-1.54688	8'h3D	-1.04688
	8'h1E	-1.53125	8'h3E	-1.03125
	8'h1F	-1.51563	8'h3F	-1.01563

	VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM	
	8'h40	-1	8'h62	-0.46875	
	8'h41	-0.98438	8'h63	-0.45313	
	8'h42	-0.96875	8'h64	-0.4375	
	8'h43	-0.95313	8'h65	-0.42188	
	8'h44	-0.9375	8'h66	-0.40625	
	8'h45	-0.92188	8'h67	-0.39063	
	8'h46	-0.90625	8'h68	-0.375	
	8'h47	-0.89063	8'h69	-0.35938	$\langle \rangle$
	8'h48	-0.875	8'h6A	-0.37925	\bigvee
	8'h49	-0.85938	8'h6B	-0.32818	>*
	8'h4A	-0.84375	8'h6C	0.3125	
	8'h4B	-0.82813	8'h6Ø	-959688	
	8'h4C	-0.8125	8 % 8Ě	-0.28125	
	8'h4D	-0.79688	8'h6F	-0.26563	
	8'h4E	-0.78125	8470	-0.25	
	8'h4F	-0.76563	8th\1	-0.23438	
	8'h50	-0.75	8'h72	-0.21875	
	8'h51	-0,73438	/8'yr73	-0.20313	
	8'h52	0.71875	8'h74	-0.1875	
	8'h53	20.70313	8'h75	-0.17188	
	8'h54	0.68 Z 5	8'h76	-0.15625	
	8'h56	-0.6×188	8'h77	-0.14063	
	8(h56	-0.65625	8'h78	-0.125	
	8'h5₹	-0.64063	8'h79	-0.10938	
	78458	-0.625	8'h7A	-0.09375	
	8 N 59	-0.60938	8'h7B	-0.07813	
((β'h5₩	-0.59375	8'h7C	-0.0625	
	\$'h5B	-0.57813	8'h7D	-0.04688	
	8'h5C	-0.5625	8'h7E	-0.03125	
11 1	8'h5D	-0.54688	8'h7F	-0.01563	
	8'h5E	-0.53125	8'h80	0	
	8'h5F	-0.51563	8'h81~8'hFE	Inbibit	
	8'h60	-0.5	8'hFF	Halt	
	8'h61	-0.48438			
	VCM_REG_EN: Se	elect the Vcom valu	e from VCM_REG [7:0] or NV memory	
	0: VCOM va	alue from NV memo	iry.	•	
		alue from VCM_RE			
	VOLUE DE LE CELLE		and a street con-		

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VCM_OUT [7:0]: NV memory programmed value.

NVMWR (D0h): NV Memory Write

D0H						NVMV	VR (NV N	Memory	Write)					
2011	D/CV	BDV	WRX	D1E 0	D7	D6	D5	D4	D3	D2	D1	D0	HE	
			WKX	טוס-8										
Command	0	1	1	Х	1	1	0	1	0	0	0	0	D	
1 st parameter	1	1	1	х	VM_D[7]	VM_D[6]	VM_D[5]	VM_D[4]	VM_D[3]	VM_D[2]	VM_D[1]	VM_D[0]	ХХ	
	This	This command is used to program the NV memory data.												
Description	VM_	D[7:0)]: Use	to write	the dat	a (inclu	ding VCM	1 and ID	code) ii	nto the I	VX memo	ry daţa.		
										R	_ //			
									\wedge	\mathcal{H}		/		
		Status Availability												
			No	ormal M	lode On	, Idle M	ode Off, \$	Sleep Ô	bil	Yes	∇			
		Normal Mode On, Idle Mode On, Slee Out Yes												
Register Availability	Partial Mode On, Idle Mode Off, Steep Out Yes													
		Partial Mode On, Ide Mode On, Shep Out Yes												
		Sleep Vn Yes												
				^	$\langle \langle$	1	\bigvee							
				\nearrow)							
					Sta				efault V					
Default		Power on Sequence VM_D[7:0]=8'h00												
		SW Reset No change HW Reset VM_D[7:0]=8'h00												
	<	7		7/-	> ''''' '	10301		VIVI	0[7.0]-	-01100				
				→										
((1)	1 />											
		رار	/											
((,	\sim	_												

Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Status Default Value Power On Sequence VCM_REG[7:0]=8'hCs_VCM_REG_EN=1'b0			Status	Availability
Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Status Default Value Power On Sequence VCM_REG[7:0]=8*hCs_CM_REG_EN=1*b0 SW Reset		Normal Mode	On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Status Default Value Power On Sequence VCM_REG[7:0]=8*hCq_CM_REG_EN=1*b0 SW Reset		Normal Mode	On, Idle Mode On, Sleep Out	Yes
Status Default Value Power On Sequence VCM_REG[7:0] & hCs CM_REG_EN=1'b0 Default SW Reset No change	Register vailability	Partial Mode (On, Idle Mode Off, Sleep Out	Yes
Status Default Value Power On Sequence VCM_REG[7:0]=8"hCt_NCM_REG_EN=1"b0 Default SW Reset No change		Partial Mode (On, Idle Mode On, Sleep Out	Yes
Power On Sequence VCM_REG[7:0]=8'hC0 VCM_REG_EN=1'b0 Default SW Reset No change			Sleep In	Yes
Power On Sequence VCM_REG[7:0]=8'hC0 VCM_REG_EN=1'b0 Default SW Reset No change			<u> </u>	
Power On Sequence VCM_REG[7:0]=8'hC0 VCM_REG_EN=1'b0 Default SW Reset No change		Status	Default Va	ilue
SVV Reset No change			/ / /	
HW Reset VCM_REG_F-0_E***CO, VCM_REG_EN=1'b0	Default	SW Reset	No chan	de
		HW Reset	VCM RECTTO STACO, V	CM_REG_EN=1'b0
~				

NVMPKEY (D1h): NV Memory Protection

D1H		NVMPKEY (NV Memory Protection Key)											
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	x	1	1	0	1	0	0	0	1	D1
1 st parameter	1	1	1	х	KEY[23]	KEY[22]	KEY[21]	KEY[20]	KEY[19]	KEY[18]	KEY[17]	KEY[16]	55
2 nd parameter	1	1	1	х	KEY[15]	KEY[14]	KEY[13]	KEY[12]	KEY[11]	KEY[10]	KEYISI	KEY[8]	AA
3 rd parameter	1	1	1	х	KEY[7]	KEY[6]	KEY[5]	KEY[4]	KEY[3]	KEK[X]	KENAT	KEY[0]	66
Description	Description KEY[23:0]: NV memory programming protection key. When writing OV P data, this register must be set as 0x55AA66 to enable OTP programming. If register is not written with 0x55AA66, NV memory programming will fail.												
Restriction													
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On Idle Mode On, Sleep Out Yes Sleep In Yes											
Offault (Status											



RDNVM (D2h): NV Memory Status Read

RDNVM (DZII). NV Melliory Status Read													
D2H	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	1	0	0	0	1	0	D2
1 st parameter	1	↑	1	х	х	х	х	х	х	х	х	х	х
2 nd parameter	1	1	1	х	0	0	0	0	0	(\	PGM_C NT1	PGM_C NT0	xx
3 rd parameter	1	1	1	х	NV_VCM [7]	NV_VCM [6]	NV_VCN [5]	NV_VCN [4]	[3]/ / NA^ACM	NV_VCN	MAY VCW	NX_XCM [0]	xx
	PGM.	_CNT[1:0]: N\	/ memo	ory prog	ramme	d recor	d. The	bit will	increas	e "+j"/	automa	tically
	when	writing	the N\	/_VCM	[7:0].			/)		\ <u>\</u>	~		
				PGN	1 CNTI	1:01	Descrip	otion		$\stackrel{\searrow}{\longrightarrow}$			
				00	OITI			nory cle	an				
				01		\downarrow	MA-We	ydy bi	ogramn	ned 1			
Description	10 NV Memory programmed 2												
		These bits are read only.											
					\sim	Ϋ́,							
	NV_V	NV_VCM [7:0]: NV memory VCM plata read value. These bits are read only.											
				///	\/)							
Destriction			//	<i>>//</i>	$\stackrel{\checkmark}{\checkmark}$								
Restriction		$\langle \cdot \rangle$	$\swarrow /$		<u> </u>								
i	~				0.	,				2 1 22			
	//					atus				/ailabilit	У		
			Norm	al Mode	e On, Id	le Mode	Off, SI	eep Ou	t	Yes			
)	Norm	al Mode	e On, Id	le Mode	On, SI	eep Ou	t	Yes			
Register Availability		'	Parti	al Mode	On, Idl	e Mode	Off, Sle	eep Out		Yes			
			Parti	al Mode	On, Idl	e Mode	On, Sle	eep Out		Yes			
					Sle	ep In				Yes			

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RDID2(D3h): Read ID4

D3H		RDID4 (Read ID4)											
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	1	0	0	1	1	D3
1 st parameter	1	\uparrow	1	x	x	х	x	х	х	x	х	x	х
2 nd parameter	1	↑	1	xx	ID41[7]	ID41[6]	ID41[5]	ID41[4]	ID41[3]	ID41[2]	ID41[1]	ID41[0]	00
3 rd parameter	1	↑	1	xx	ID42[7]	ID42[6]	ID42[5]	ID42[4]	ID42[3]	ID42[2]	1042[1]	ID42[0]	94
4 th parameter	1	1	1	xx	ID43[7]	ID43[6]	ID43[5]	ID43[4]	ID43[3]	VD4312)	HD43[V]	xD43[0]	86
Description	Read ID device code. The 1 st parameter is dummy read period. The 2 nd parameter means the IC version. The 3 rd and 4 th parameter mean the IC model name.												
Restriction	-												
Register Availability		Status Availability Normal Mode On, Kile Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default				Status er On Se SW Res HW Res	equence				D4=24'h No cl	It Value n009486 nange n009486			

Gamma Setting (E0h)

Gamma Setting (E0h)													
E0H						Ga	mma S	etting					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	х	1	1	0	0	1	0	0	0	E0
1 st parameter	1	1	1	х	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	00
2 nd parameter	1	1	1	х	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	44
3 rd parameter	1	1	1	х	0	KP5[2]	KP5[1]	KP5[0]	0	KP\$[2]	KP4[1]	KP4[0]	06
4 th parameter	1	1	1	х	0	RP1[2]	RP1[1]	RP1[0]	0~	RP0[2]	RP0[1]	RP 0[0]	44
5 th parameter	1	1	1	х	0	0	0	VRP0[4]	VRP0(3)	VRP0[2]	VRPOYI	VRP0[0]	0A
6 th parameter	1	1	1	х	0	0	0	VRP1[4	VRP1[3)	VPP 1(2)	VRP1[1]	VRP1[0]	08
7 th parameter	1	1	1	х	0	KN1[2]	KN1[1]	KN/(0)	Ø	KN0[2]	KN0[1]	KN0[0]	17
8 th parameter	1	1	1	х	0	KN3[2]	KN3[1]	KN3101	0	KN2[2]	KN2[1]	KN2[0]	33
9 th parameter	1	1	1	х	0	KN5[2]	KNS[N	KN5[0]	9	KN4[2]	KN4[1]	KN4[0]	77
10 th parameter	1	1	1	х	0	RN1(2)	RN1[1]	RN1[0]	V	RN0[2]	RN0[1]	RN0[0]	44
11 th parameter	1	1	1	х	0/	\nearrow_{0}	6	VRNO(4)	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	08
12 th parameter	1	1	1	х	$\langle \! \langle$	9>	B	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0C
Description	RP1-0 VRP0 KN5-0 RN1-0	0[2:0] : [4:0], V 0[2:0] :	in the adjustment register for positive polarity in the interior of the polarity in the interior of the polarity in the interior of the polarity in the po										
Register Availability			~			Status				Availab	ility		
			Norma	al Mode	On.	Idle Mo	de Off.	Sleep C	Out	Yes			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes



Default	Status	Default Value
	Power On Sequence	As above
	SW Reset	No change
	HW Reset	As above

