EE 2000 Logic Circuit
Design Semester A 2021/22A

Tutorial 4

1. (i) Draw the truth table for a half adder.
(ii) Design a half adder using NOR gates only.

2. With the following functions, design a circuit with a 3-to-8-line decoder and external gates.

$F_1(x, y, z) = x'y'z' + xz$
$F_2(x, y, z) = xy'z' + x'z$

3. With the following functions, design a circuit with a 2-to-4-line decoder with enable input and external NAND gates.

$F_1(x, y) = \Sigma m(0, 3)$
$F_2(x, y) = \Sigma m(1, 2, 3)$

4. (i) Complete the truth table of the following circuit given in Fig. 4(a).
(ii) Write down the logic expression of the following circuit and simplify as much as possible.
(iii) Draw the simplified logic expression obtained in (ii) using 2-input NAND gate(s) only.

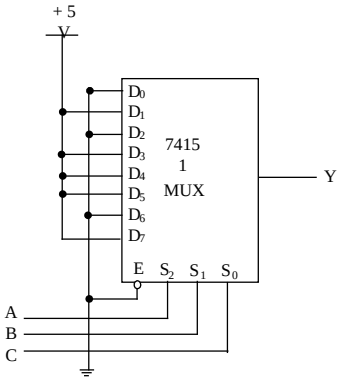

Fig. 4(a)

5. (i) Show Boolean expression for the function $f(a,b,c)$ of the circuit shown in Fig. 5(a).
(ii) Simpify your answer in (i) by K-Map.

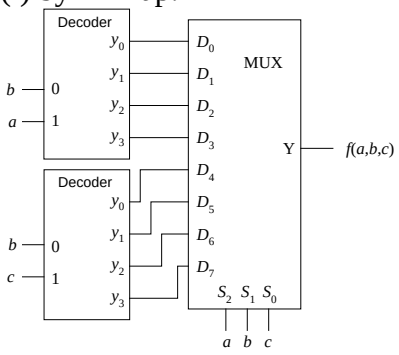

Fig. 5 (a)