EE 2000 Logic Circuit Design
Semester A 2021A

Tutorial 8

1. An active-LOW *SR* latch is shown in Fig. 1, sketch the output waveform of *Q* based on the inputs as shown in Fig. 1. Assume that *Q* starts LOW.

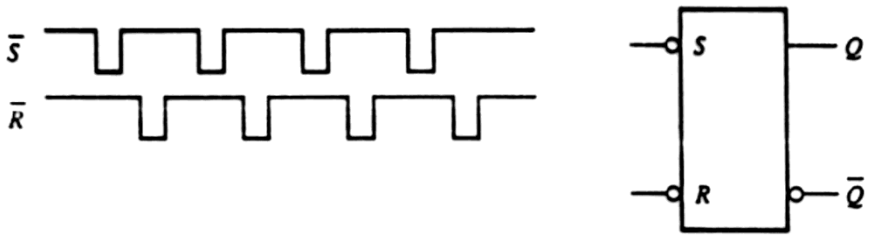


Fig. 1

2. Two edge-triggered *SR* flip-flops are shown in Fig. 2. If the inputs are as shown, sketch the *Q* output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.

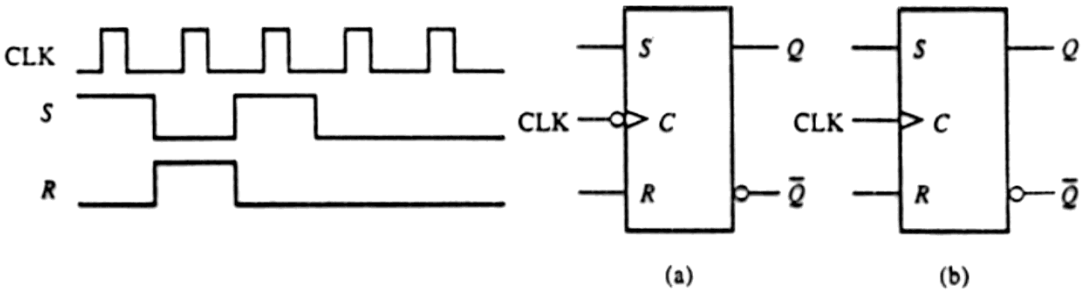


Fig. 2

3. The waveforms of Fig. 3 are applied to the inputs of an SN7476 *JK* flip-flop (negative-edge triggered). Complete the timing diagram by drawing the waveforms of flip-flop output *Q*.

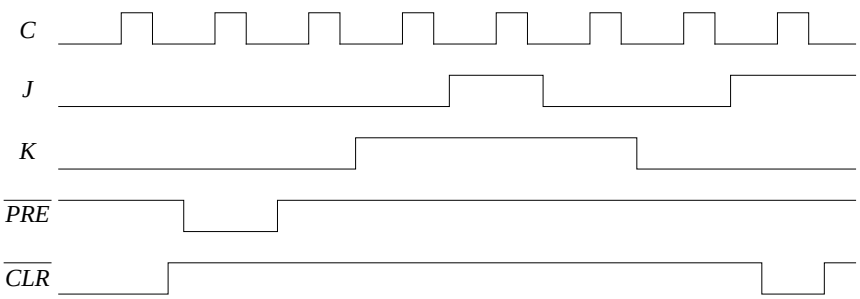


Fig. 3

4. The circuit of Fig. 4 contains a *D* latch, a positive-edge-triggered *D* flip-flop, and a negative edge-triggered *D* flip-flop. Complete the timing diagram for the waveform of signals y_1, y_2 and y_3.

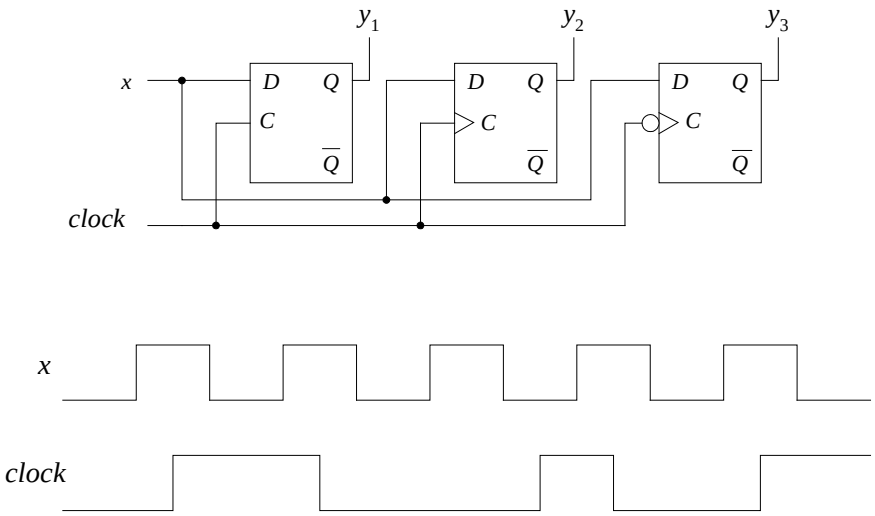
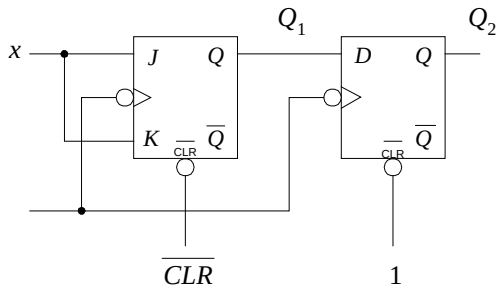


Fig. 4

5. The circuit of Fig. 5 contains a negative edge–triggered *JK* flip-flop and a *D* flip-flop. Complete the timing diagram of Figure 6-7b by drawing the waveforms of signals Q_1 and Q_2.



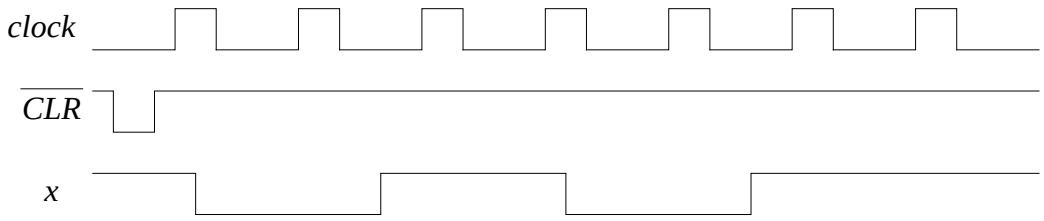


Fig. 5