EE 2000 Logic Circuit Design
Semester A 2021/22A

Tutorial 5

1. What are the mistakes for this VHDL?

```
library ieee;
use ieee.std_logic_1164.all;

ENTITY and_gate IS
PORT (     a & b :IN  STD_LOGIC;
           s     :OUT STD_LOGIC)
    ;)
END;

ARCHITECTURE ckt OF and_gate IS
BEGIN
     s <= a AND b;
END ckt;
```

2. Using VHDL to write the entity declaration for a logic design entity named NaDe that has two inputs named A1 and A2, and one output named O1.

3. Write a complete VHDL design module (with entity and architecture) to implement a circuit with the following Boolean expressions. Use concurrent statements and without NAND and NOR operators in your design.

   - x1 = AB'C + A(BC)'
   - x2 = (A'B + C)(BC' + A)'
   - x3 = (A(BC)' + AC')'

4. Write a complete VHDL design module to implement a circuit with the following Boolean expressions. Assign a signal name sigW1 to represent the common logic term in your design.

   - A = (XYZ')' + XZ
   - B = (XYZ')'(X + Z)
   - C = ((XYZ')'+X')'