EE 2000 Logic Circuit Design
Semester A 2021A

Tutorial 10

1. Using JK FFs and with the minimum number of states to design a counter with counting sequence: 0,4,2,1,6 and repeat. State whether the circuit is a self started circuit.

2. Design a sequential circuit with two JK FFs, *A* & *B*, and two inputs, *x* & *E*. if *E*=0, the circuit remains in the same state regardless of the value of *x*. When *E* = 1 and *x* = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When *E* =1 and *x* = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

3. Using a synchronous binary counters as shown in Figure 1, design and draw a counter to generate the following repeating sequences 2 to 9 repeatedly for a free running clock.

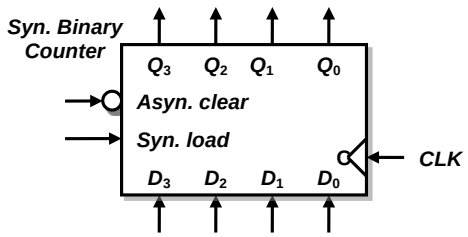

Figure 1.

4. Write the VHDL code for a D-FF with (i) asynchronous Preset and Clear, and (ii) synchronous Preset and Clear.