EE 2000 Logic Circuit Design
Semester A 2021A

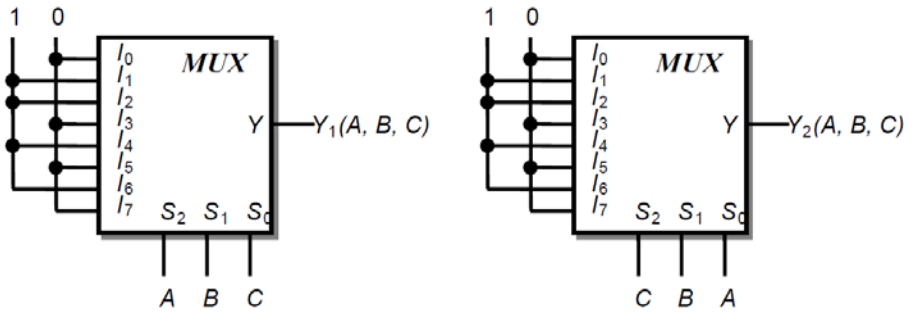
Tutorial 9

1. Construct a 4 x 16 decoder (with enable input) using five 2 x 4 decoder (with enable input) modules. Show the schematic diagram neatly.

2. How many selection lines are contained in a multiplexer with 1024 inputs and one output?

   What is the largest number of data inputs which a multiplexer with *k* input selection inputs can handle?

   For the multiplexer circuits shown in the following figure below, what are $Y_1(A, B, C)$ and $Y_2(A, B, C)$ respectively? Please list in standard sum of products form.



3. Implement the function $f(a, b, c, d) = \Sigma m\ (1, 2, 5, 7, 9, 11, 13)$ using:
   (a) A 8-to-1-line multiplexer and a NOT gate only
   (b) A 2-to-1-line multiplexer and minimum number of AND, OR, NOT gates
   (Hints: Assign variable a as selection input of the MUX, and then express *f* as a function of *b*, *c*, *d* with the help of K-map)

4. Draw the PAL diagram for the following truth table.

Inputs			Outputs			
x	***y***	***z***	***a***	***b***	***c***	***d***
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1