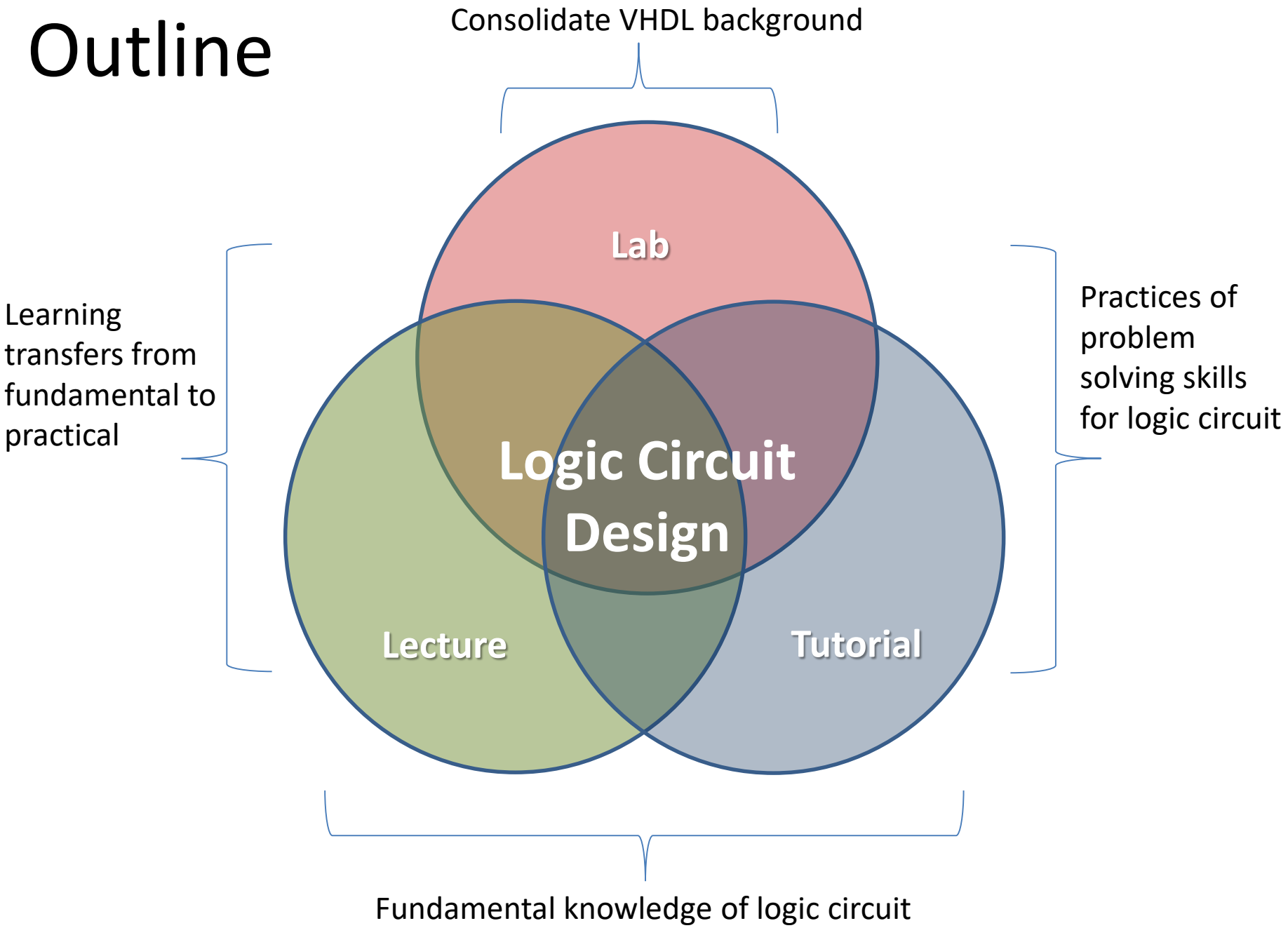
EE 2000 Logic Circuit Design

Year 2021/22, Semester A

Course Instructor: Dr. Steve Wong
Office: G6423
Email: hang.wong@cityu.edu.hk

Outline


Consolidate VHDL background
Lab
Learning transfers from fundamental to practical
Practices of problem solving skills for logic circuit
Logic Circuit Design
Lecture
Tutorial
Fundamental knowledge of logic circuit

Class Logistics

- Lecture: 13 weeks (39 hours)
  by Steve Wong
- Tutorial: 12 weeks (12 hours)
  by W S Chan, Hei Wong and Steve Wong
- Laboratory: 5 weeks (15 hours)
  by W S Chan, Hei Wong and Steve Wong

- Lab report, assignments, tests (50%)
- Written exam (2hours, 50%)

W S Chan

Hei Wong

Steve Wong

Text book

- "Introduction to Logic Design", Alan B. Marcovitz, *Mc Graw Hill, 3rd (or 2nd) Edition.*
- "Digital Systems Design Using VHDL" Charles H Roth, Lizy K. John: Fifth Edition, *Cengage Learning*, 2016.

Lecture Notes

- Download from CANVAS (Ch1 to 10)
- Tutorial questions (Tutorial 1 to 10)
- Lab manual and assignments

https://canvas.cityu.edu.hk

Go to CANVAS to download class materials under the "Files" folder of EE2000.

Lab Schedule

- Our lab of EE2000 are scheduled in weeks 7, 8, 9, 10, and 13 (make-up only)
- Duration: 3 hrs for each
- Grading: (a) Attendance [10 % by *Technicians*]
  (b) Check Points [50% by *Lab helpers*]
  (c) Lab Report [40% *Lab Instructor*]
- All students are **required to submit** the individual lab report before Friday of Week 13 to the lab technicians.

2020A Schedule for EE2000			
	Class	Tutorial	Lab
Week1			
Week2			
Week3	Assignment 1		
Week4			
Week5			
Week6	Test 1		
Week7	Assignment 2		Lab 1
Week8			Lab 2
Week9			Lab 3
Week10	Test 2		Lab 4
Week11	Assignment 3		
Week12			
Week13			Make-up
Week14			

- Attendance: Lab session is required. The attendance is ONLY taken in the first *15 mins* of lab session. *Late* will have *mark deduction* in the lab exercise.

- To pass the course, students are required to achieve at least 30% in course work and 30% in the examination. Also, 75% laboratory attendance rate must be obtained.

EE2000 Logic Circuit Design

Boolean Algebra

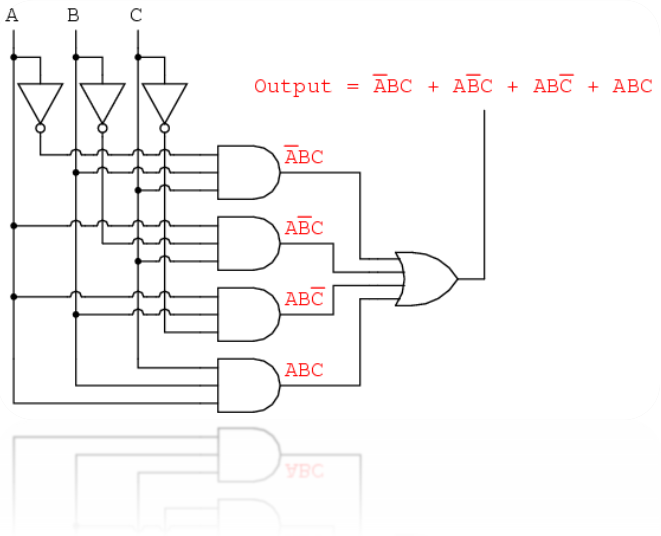
$A(B+C) = AB + AC$

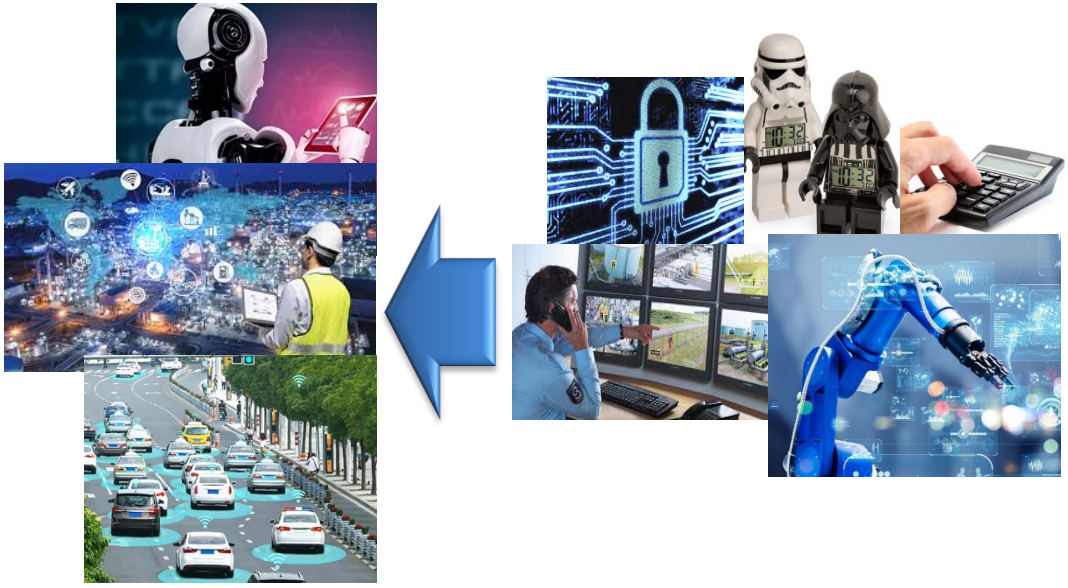
$1 + A = 1$

$A + A' = 1$

VHDL

```
entity mux4 is port(
    in0, in1, in2, in3: in bit;
    S0, S1: in bit;
    Z: out bit_vector( 7 downto 0);
end mux4;
architecture behavioral of mux4 is
    begin
    Z <= in0 after 5 ns when S0 = '0' and S1 = '0' else
         in1 after 5 ns when S0 = '0' and S1 = '1' else
         in2 after 5 ns when S0 = '1' and S1 = '0' else
         in3 after 5 ns when S0 = '1' and S1 = '1' else
         "00000000" after 5 ns;
    end behavioral;
```





Keyword Syllabus:

Boolean Functions and Logic Gates
Boolean algebra and switching functions; logic operations; De Morgan's Laws; minterm and maxterm canonical forms; sum of products and products of sums; basic logic gates.

Combinational Logic Design
Gate minimization by Boolean algebra, Karnaugh map and Quine-McCluskey method; don't-care cases; two-level logic circuits and single-gate type circuits; timing parameters and circuit hazards.

Circuit Design with Functional Blocks
Carry Look Ahead adder; comparators; decoders and encoders; multiplexers and demultiplexers.

Introduction to Hardware Description Language (HDL)
Hardware Description Language (HDL); logic gates and combinational circuit modelling.

Flip-flops
Latches, RS, JK, D-type, edge-triggered and master-slave flip-flops; triggering and setting; timing parameters; HDL circuit modelling.

Synchronous Sequential Logic Circuit
Concept of states; Mealy and Moore Machines; redundant state elimination; sequential digital system analysis and design; programmable logic device; HDL sequential circuit modelling.

Registers and Counter
Various types of registers and counters; ripple counters and synchronous counters, and their applications; construction of registers and counters. HDL circuit modelling.

Field-Programmable Gate Array
Introduction to Look-up Table (LUT), Generic Array Logic (GAL), Programmable Array logic (PAL), simple programmable logic device, complex programmable logic device (CPLD), Field Programmable Gate Array (FPGA), Programmable System-on-Chip (SoC).

FPGA Implementation
Combination and synchronous sequential circuit synthesis; data path component description, debugging and validation.

Logic Families
Introduction to electrical characteristics of TTL and CMOS logic families; transfer characteristics, noise margins; fan-in and fan-out; comparison of families; interfacing between different families.