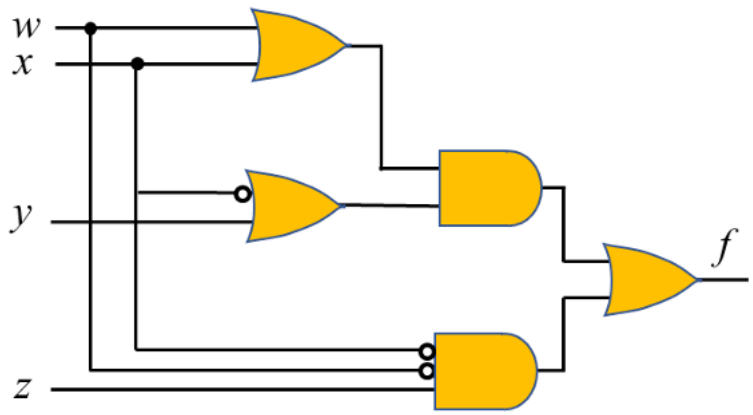
EE 2000 Logic Circuit Design
Semester B 2023/24

Tutorial 3

1. Design a combinational circuit for a 4-bit BCD-2421-to-Gray code converter.

2. Jack, Jen, Joe, and Jim get together once a week to either go to a movie or bowling. To decide what to do, they vote and a simple majority wins. They will go to a movie if a TIE (2 votes each) occurs. Assuming a vote for the movie is represented as a 0, design a NAND gate circuit that automatically computes the decision.

3. (a) Given the following combinational circuit, work out the timing diagram to identify the presence of any timing hazard when the input condition changes from $(w, x, y, z) = (0,0,1,1)$ to $(0,1,1,1)$. Assume that the propagation delay for NOT gate is $\Delta\tau$, and other gates is $2\Delta\tau$.



(b) Redesign the circuit to eliminate the hazard.

4. (a) Determine the Hamming code using both odd and even parity bit for a data code of 11001.

(b) Check for error should we receive the following codes, consider odd parity, and determine the original data code.

(i) 100000110
(ii) 101100110