# **CS3103 Operating Systems**

# **Assignment 2**

## **Instructions**

- 1. **Due Date: Monday, November 20th, 2023**. Submit your answers to Canvas.
- 2. Before you begin, please take the time to review the course policy on academic integrity at: <a href="https://www.cityu.edu.hk/provost/academic\_honesty/rules\_on\_academic\_honesty.htm">https://www.cityu.edu.hk/provost/academic\_honesty/rules\_on\_academic\_honesty.htm</a>. Please write your own solution. All submissions will be scanned by anti-plagiarism software.

### **Questions**

#### Please use the answer sheet provided to write all your answers.

- 1. Consider the traffic deadlock depicted in Figure 1.
  - a. Show that the four necessary conditions for deadlock indeed hold in this example.
  - b. State a simple rule for avoiding deadlocks in this system.

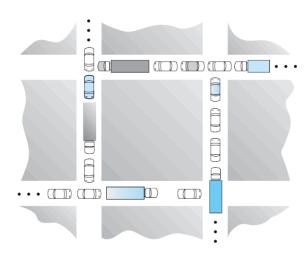


Figure 1 Traffic deadlock.

#### 2. Consider the following snapshot of a system

	Allocation				Max				Available			
	A	В	С	D	A	В	C	D	A	В	С	D
P0	4	0	0	3	4	0	1	3	3	5	3	1
P1	2	0	0	0	2	8	5	0				
P2	1	2	2	5	2	2	3	6				
Р3	0	5	2	2	0	6	5	2				
P4	0	0	1	3	0	3	6	6				

Answer the following questions using the Banker's algorithm.

- a) How many resources of type A, B, C, and D are there?
- b) Is the system in a safe state? If so, list a safe sequence. If not, explain why?
- c) If a request from process P1 arrives for additional resources of (0,6,4,0), can the system grant the request immediately? Explain and show the detailed steps.
- 3. Consider a paging system with the page table stored in memory.
  - a) If a memory reference takes 260 nanoseconds, how long does a paged memory reference take?
- b) If we add TLB, 80 percent of all page-table references are found in the TLB, while accessing TLB takes 15 nanoseconds. What is the effective memory reference time?
- 4. Considering a 16 bits system, use a linear translate page table with the following assumptions:
  - The page size is 32 bytes;
  - The virtual address space for the process is 512 pages or 16KB;
  - Physical Memory consists of 128 pages.
  - Every entry in the page table has one extra VALID bit
  - Page entry per page is 32 PTEs.
  - a) Please design this linear translate page table in detail, including the format of the PTE and virtual/physical address and the meaning of each part.
  - b) Is this page table effective? If not, how to improve it? Describe the improved page table in detail.

- **5**. Given the following reference string:
- 1, 3, 2, 4, 4, 2, 5, 1, 6, 7, 8, 7, 8, 9, 7, 8, 9, 4, 5, 4, 5, 3

Run (a) the Optimal page replacement algorithm, (b) the LRU page replacement algorithm on the above reference string with a 4 free frame physical memory and computing the number of page faults on that string, respectively.