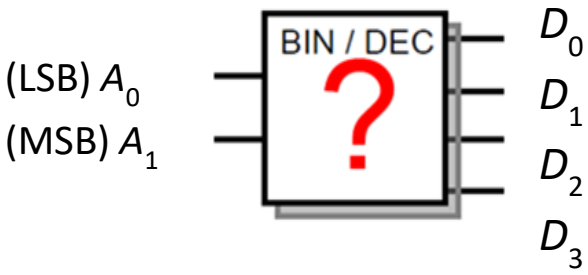
EE 2000 Logic Circuit Design
Semester B 2023/24

Tutorial 8

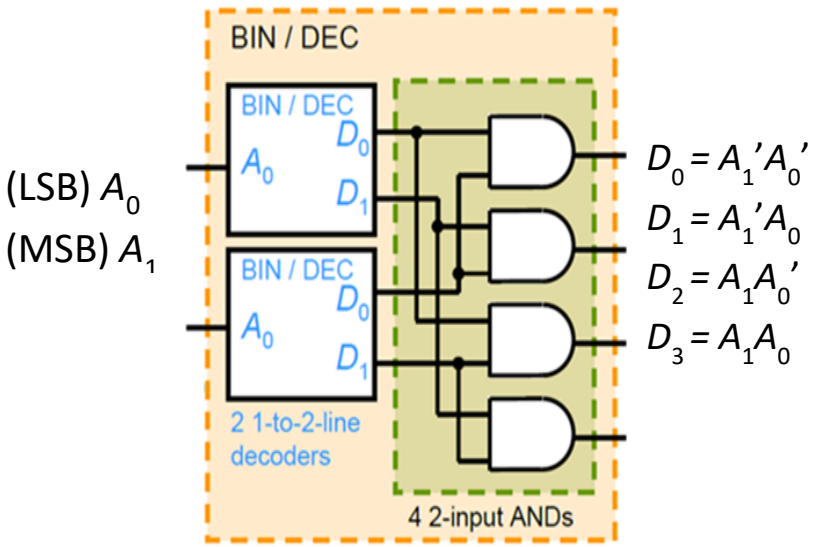
1. *2-to-4 Line Decoder (using 1-to-2 Line Decoder)*

a) Write the entity declaration for a 2-to-4 Line decoder module named LDecoder2_4 that has two input named A0 and A1, and four outputs named D0, D1, D2, D3.



b) Write the architecture declaration for the above 2-to-4 Line decoder named LDecoder2_4 with a component name "LDecoder1_2" using 2 1-to-2 Line decoders.

Inputs		***Outputs***			
A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



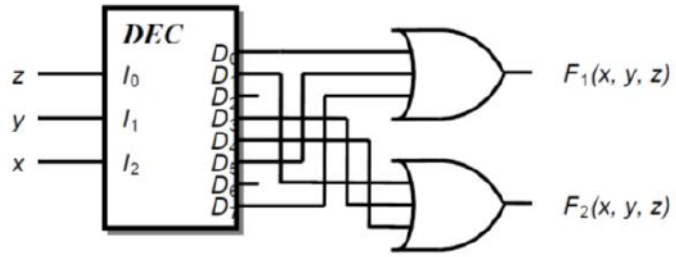
2. *3-to-8 Decoder*

a) Write the entity and architecture declaration for a 3-to-8 decoder module named Decoder3_8 that has one 3-bit input named S and one 8-bit output named Q.

b) Write the circuit named Q1 using VHDL with one 3-to-8 decoder and external gates.

$$F_1(x, y, z) = x'y'z' + xz$$

$$F_2(x, y, z) = xy'z' + x'z$$



3. *Encoder*

Write the entity and architecture declaration for a decimal-to-gray code encoder module named DTG_encoder that has one 10-bit input named D_in and one 4-bit output named G_out.

4. *JK Flip-Flop*

Write the complete VHDL code for a negative-edge triggered JK Flip-Flop with asynchronous CLR.