EE 2000 Logic Circuit Design
Semester B 2022/23

Assignment 3

The solutions must be handwritten (20% deduction if not), scanned and uploaded to CANVAS by 23:59 hours, Apr 02, 2023. Please do not use iPad to write the solution – treat this as practice for your examination and write on paper. **Please write your name and student No on the top of each answer sheet.**

Design a Moore system with 1 input *x* and 1 output *z* such that *z* = 1 if *x* has been '1' consecutively for three or more clock times or '0' consecutively for two or more clock times. An example of a time trace of the system is shown below.

x	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	
z	?	?	1	1	1	0	0	0	0	1	0	0	0	1	0	1	1	0

(a) Determine the states and work out the state diagram. (Hint: 5 states)
(b) Work out the state table.
(c) Use negative edge-triggered D flip flops, 2-input logic gates and NOT gate to design the Moore system. Use K-map to design the state transition logic and output logic. Draw the circuit clearly (Use the least amount of NOT gates).
(d) If negative edge-triggered T flip flops are used to design the Moore system, use K-map to design the state transition logic of each flip-flop input. You do not need to draw the circuit. (Hint: T flip flop changes state when input is '1')

(100 marks)