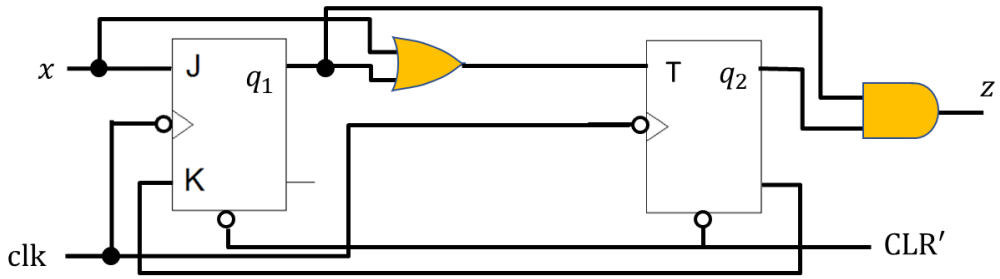
QUESTION 1

For the following circuit, draw the timing diagram for q1, q2 and z without time delay.

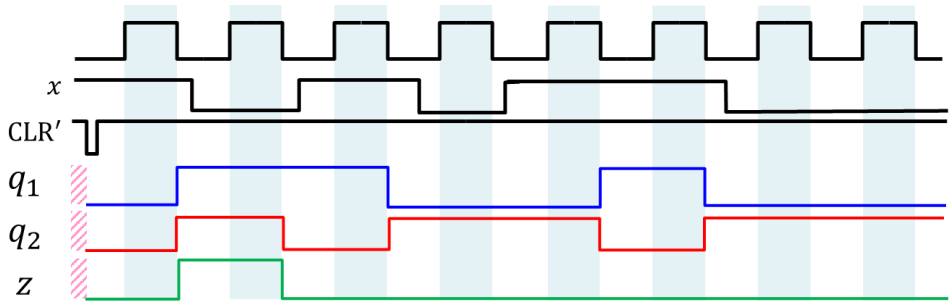


$$J = x$$

$$K = \overline{q_2}$$

$$T = x + q_1$$

$$z = q_1 q_2$$



QUESTION 2

Write a complete VHDL design module (with entity name q4b and architecture name behavior) to implement the combinational circuit shown. Assign signals for intermediate outputs (s1, s2, ….). Use concurrent statements and without NAND and NOR operators in your design.

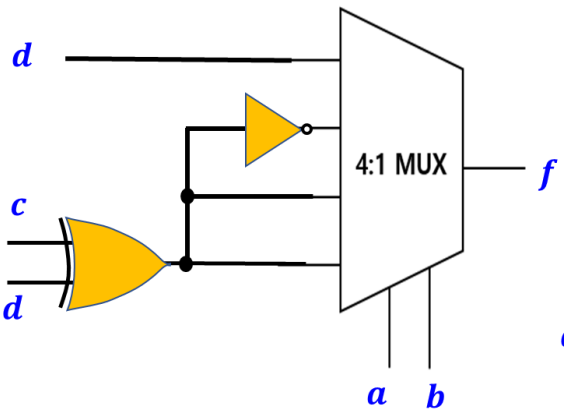
```
ENTITY q4b is
    port (w, x, y, z : in bit;
          F, G: out bit);
End q4b;

architecture behavior of q4b is
signal s1, s2, s3 : bit;
begin
          s1 <= w AND x;
          F <= NOT w OR s1;
          s2 <= w AND y;
          s3 <= NOT (s1 OR s2);
          G <= NOT (s3 AND z);
end behavior;
```

QUESTION 3

(a) Given the following function, implement the function with a 4 × 1 MUX and minimal amount of 2-input external logic gates and NOT gate. Connect inputs a and b to the selection lines.

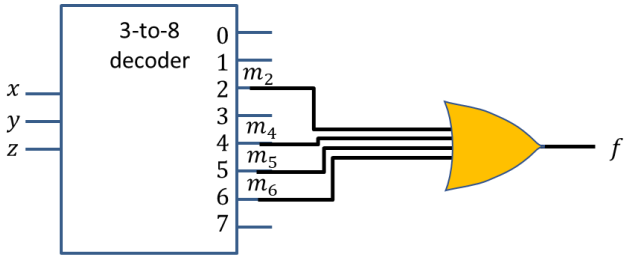
$f(a, b, c, d) = \Sigma m(1, 3, 4, 7, 9, 10, 13, 14)$

cd \ ab	00	01	11	10		
00		1			ab=00	$f = d$
01	1		1	1	ab=01	$f = c'd' + cd$
11	1	1			ab=10	$f = c'd + cd'$
10			1	1	ab=11	$f = c'd + cd'$

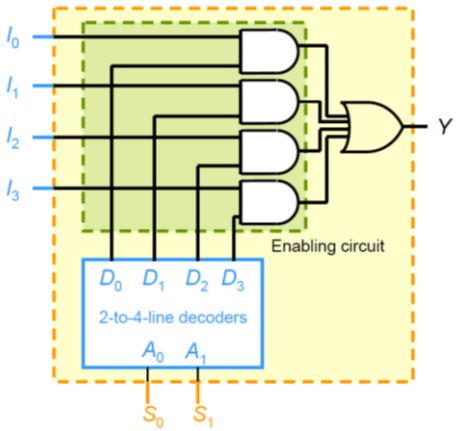


(b) Implement the following function using a circuit with (1) a 3-to-8 active high decoder and (2) minimal amount of external logic gates with multiple inputs.

$$f(x, y, z) = xy' + yz' = xy'z' + xy'z + x'yz' + xyz'$$
$$= \Sigma m(2, 4, 5, 6)$$



(c) Build a 4-to-1 MUX using a 2-to-4 binary decoder and external logic gates.

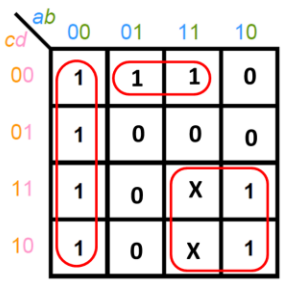


QUESTION 4

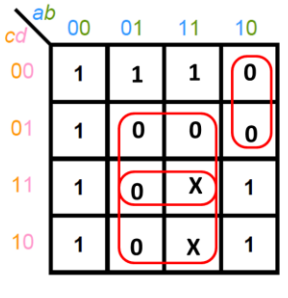
Implement the following functions using the PLA shown in the next page (You can directly draw on it) with a minimum number of switch connections by term sharing.

$$F(a,b,c,d) = \Sigma m(0,1,2,3,4,10,11,12) + \Sigma d(14,15)$$

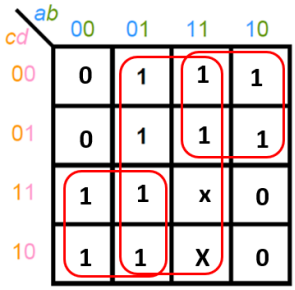
$$G(a,b,c,d) = \Sigma m(2,3,4,5,6,7,8,9,12,13) + \Sigma d(14,15)$$



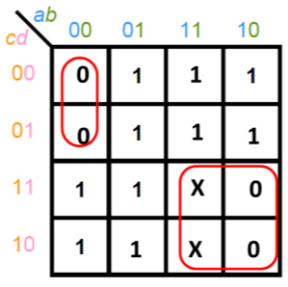
$F = a'b' + bc'd' + ac$



$F' = bd + bc + ab'c'$



$G = a'c + b + ac'$



$G' = a'b'c' + ac$

$$F(a,b,c,d) = a'b' + bc'd' + ac$$

$$G' = a'b'c' + ac$$