EE 2000 Logic Circuit Design

Year 2023/24, Semester B

Course Instructor: Dr. Lip Ket CHIN
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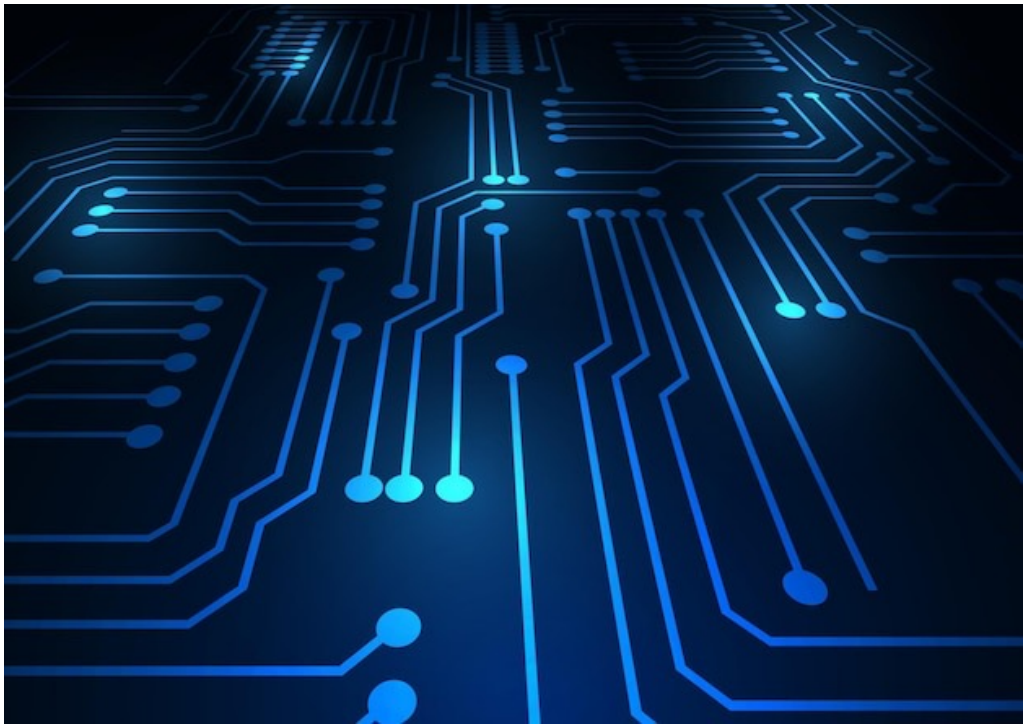


freepik.com

Acknowledgement: Prof Basu Arindam & Steve Wong

EE2000 Logic Circuit Design

Boolean Algebra

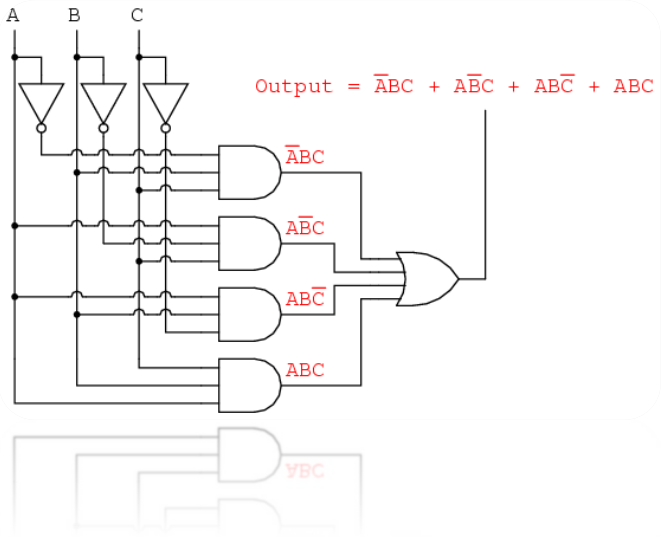
$A(B+C) = AB + AC$

$1 + A = 1$

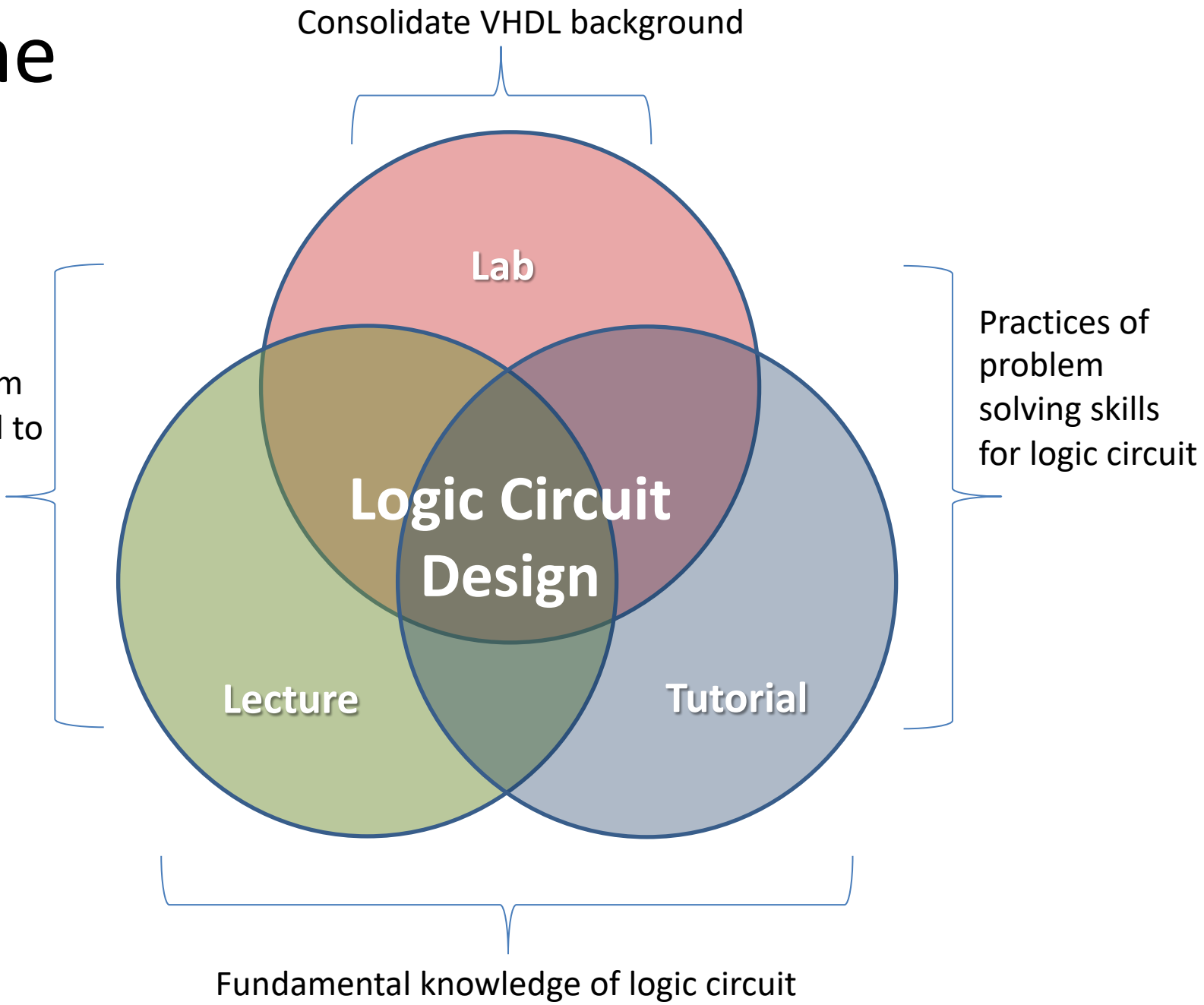
$A + A' = 1$

VHDL

```
entity mux4 is port(
    in0, in1, in2, in3: in bit;
    S0, S1: in bit;
    Z: out bit_vector( 7 downto 0);
end mux4;
architecture behavioral of mux4 is
    begin
    Z <= in0 after 5 ns when S0 = '0' and S1 = '0' else
         in1 after 5 ns when S0 = '0' and S1 = '1' else
         in2 after 5 ns when S0 = '1' and S1 = '0' else
         in3 after 5 ns when S0 = '1' and S1 = '1' else
         "00000000" after 5 ns;
    end behavioral;
```



Outline


Consolidate VHDL background
Lab
Learning transfers from fundamental to practical
Practices of problem solving skills for logic circuit
Logic Circuit Design
Lecture
Tutorial
Fundamental knowledge of logic circuit

Text book

- "Introduction to Logic Design", Alan B. Marcovitz, *Mc Graw Hill, 3rd (or 2nd) Edition.*
- "Digital Systems Design Using VHDL" Charles H Roth, Lizy K. John: Fifth Edition, *Cengage Learning*, 2016.

CANVAS

- Lecture Notes
- Tutorial Questions
- Lab manual and assignments

https://canvas.cityu.edu.hk
Go to CANVAS to download class materials under the "Files" folder of EE2000.

Class Logistics

- Lecture: 13 weeks (39 hours)
  by Lip Ket CHIN
- Tutorial: 10 weeks (10 hours)
  by Ehsan Nekouei and Lip Ket CHIN
- Laboratory: 4 weeks (12 hours)
  by Ehsan Nekouei and Lip Ket CHIN

Ehsan Nekouei

Lip Ket CHIN

2023/24B Schedule for EE2000

	Class	Tutorial	Lab
Week 1 (15 to 19 Jan)	Lecture 1		
Week 2 (22 to 26 Jan)	Lecture 2	Tutorials	
Week 3 (29 to 2 Feb)	Lecture 3 (Assignment 1)		
Week 4 (5 to 9 Feb)	Lecture 4		
Week 5 (19 to 23 Feb)	Lecture 5		Lab 1
Week 6 (26 to 1 Mar)	Test 1 (L1 to L4)		
Week 7 (4 to 8 Mar)	Lecture 6 (Assignment 2)	Tutorials	Lab 2
Week 8 (11 to 15 Mar)	Lecture 7		
Week 9 (18 to 22 Mar)	Lecture 8		Lab 3
Week 10 (25 to 29 Mar)	Lecture 9		
Week 11 (1 to 5 Apr)	Test 2 (L5 to L8) (Assignment 3)		
Week 12 (8 to 12 Apr)	Lecture 10	Tutorials	
Week 13 (15 to 19 Apr)	Revision and Discussion		Lab 4
Week 14 (Mon & Tue)			Make-Up

Assignments

- 15% of the final continuous assessment (CA)
- 1st assignment: Week 3 (Wed)
- Submission: CANVAS by Week 4 (Wed) @ 23:59
- 2nd assignment: Week 7 (Wed)
- Submission: CANVAS by Week 8 (Wed) @ 23:59
- 3rd assignment: Week 11 (Wed)
- Submission: CANVAS by Week 12 (Wed) @ 23:59
- Late submission: **20% deduction per day**

Tests

- 20% of the final continuous assessment (CA)
- 1st Test: Week 6 (Wed)
- 2nd Test: Week 11 (Wed)
- **No make-up test** will be provided; if you missed it, you will score “0”

Lab Sessions

- 15% of the final continuous assessment (CA)
- In Weeks 5, 7, 9, 13
- Make-up: 22 Apr (Mon) & 23 Apr (Tue)
- Duration: 3 hrs for each session

Lab Sessions

- Grading: (a) Attendance [5% by *Technicians*]
  (b) Check Points [35% by *Lab helpers*]
  (c) Lab Report [60% by *Lab Instructor*]
- Attendance: Attendance is ONLY taken in the first *30 mins* of lab session; *Late* will have *mark deduction* in the lab exercise
- All students are **required to submit** the individual lab report before Friday of Week 14 to CANVAS

Course Assessment

Continuous Assessment: 50%

2 Tests (20%), 3 Assignments (15%) and 4 Lab sessions (15%)

Final Exam: 50% (Closed-book, 2 hours)

To pass the course, students are required to achieve **at least 30/100 in continuous assessment** and **30/100 in the final examination**

Also, a **75% laboratory attendance rate** must be obtained

Syllabus

Boolean Functions and Logic Gates
Boolean algebra and functions; logic operations; De Morgan's Laws; canonical forms; sum of products and products of sums; basic logic gates

Combinational Logic Design
Gate minimization by Boolean algebra, Karnaugh map and Quine-McCluskey method; timing hazards

Circuit Design with Functional Blocks
Carry Look Ahead adder; comparators; decoders and encoders; multiplexers and demultiplexers

Field-Programmable Gate Array
Programmable Logic Devices, Field Programmable Gate Array (FPGA)

Introduction to Hardware Description Language (HDL)
Very High Speed Integrated Circuit (VHDL)

Syllabus

FPGA Implementation

Combination and synchronous sequential circuit synthesis; data path component description, debugging and validation

Flip-flops

Latches, RS, JK, D-type, edge-triggered and master-slave flip-flops; triggering and setting

Synchronous Sequential Logic Circuit

Concept of states; Mealy and Moore Machines; redundant state elimination; sequential digital system analysis and design

Registers and Counter

Various types of registers and counters; ripple counters and synchronous counters, and their applications; construction of registers and counters