

EE 2000 Logic Circuit Design
Semester B 2022/23

Tutorial 5

1. What are the mistakes for this VHDL?

```
Library ieEe;
use IEEE.std-logic_1164.all;

ENTITY and_gate IS
    port (a&b : in STD_LOGIC;
          S: out STD_LOGIC);
end;

architecture CKT of and_Gate IS
begin
    s <= a AND b;
end ckt;
```

2. Using VHDL to write the library and entity declarations for a logic design entity named MoZone that has the following inputs and outputs.
- (a) A1 is an array of 8-bit std_logic data with the highest index number holding the most significant bit.
 - (b) A2 is a 5-bit bit vector with the lowest index number holding the most significant bit
 - (c) O1 is a 1-bit std_logic output
3. Write a complete VHDL design module (with entity and architecture) to implement a circuit with the following Boolean expressions. Use concurrent statements and without NAND and NOR operators in your design.
- $x1 = A'B'C + A(BC)'$
 - $x2 = (A'B + C')(BC' + A)'$
 - $x3 = (A(BC)' + A'C')'$
4. Write a complete VHDL design module to implement a circuit with the following Boolean expressions. Assign a signal name sigW1 to represent the common logic term in your design. Use concurrent statements without NAND and NOR operators in your design.
- $A = (XY'Z')' + XZ$
 - $B = (XY'Z')'(X + Z)$
 - $C = ((XY'Z')' + X')'$

5. Write a complete VHDL design module to implement the combinational circuit shown. Assign signals for intermediate outputs. Use concurrent statements (i) without NAND and NOR operators in your design; and (ii) with NAND and NOR operators.

