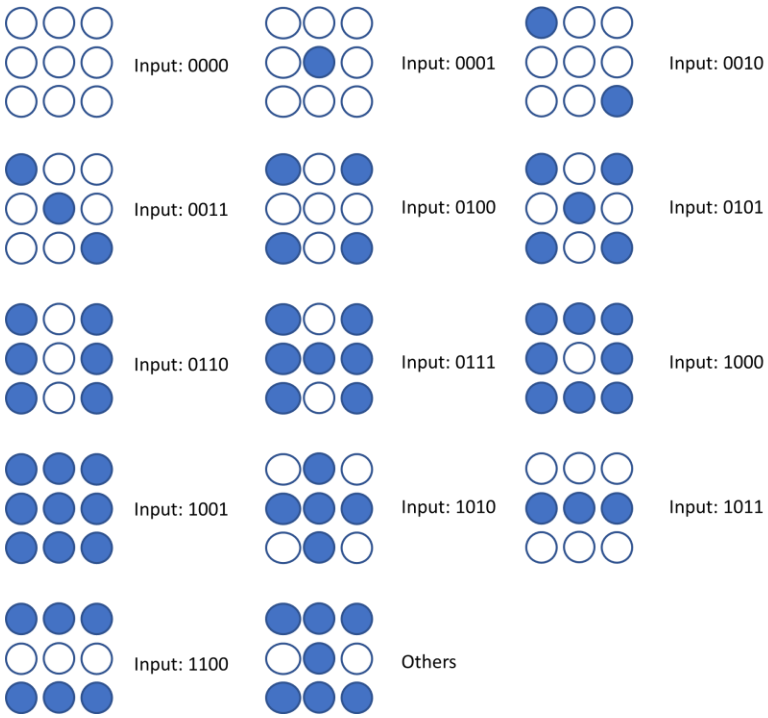
EE 2000 Logic Circuit Design
Semester B 2022/23

Assignment 2

The solutions must be handwritten (20% deduction if not), scanned and uploaded to CANVAS by 23:59 hours, Mar 9, 2023. Please do not use iPad to write the solution – treat this as practice for your examination and write on paper. **Please write your name and student No on the top of each answer sheet.**

Your task is to design a driver for an electronic 9-dotted die display as shown in the following Figure. In operation, it has to display (blue dot represents 'on') the decimal numbers 0 to 9, symbols '+', '-', and '=' with the corresponding binary inputs. Other invalid inputs will display 'I'.

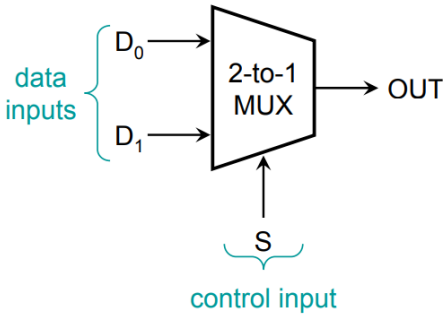


Noted that assign the outputs of the 9-dotted die as follows

Q1. Write down the truth table for all outputs. Denote the inputs as A3, A2, A1 and A0 where A3 represents MSB and A0 represents LSB. (16 marks)

	A3	A2	A1	A0		A	B	C	D	E	F	G	H	I
'0'	0	0	0	0		0	0	0	0	0	0	0	0	0
'1'	0	0	0	1		0	0	0	0	1	0	0	0	0
'2'	0	0	1	0		1	0	0	0	0	0	0	0	1
'3'	0	0	1	1		1	0	0	0	1	0	0	0	1
'4'	0	1	0	0		1	0	1	0	0	0	1	0	1
'5'	0	1	0	1		1	0	1	0	1	0	1	0	1
'6'	0	1	1	0		1	0	1	1	0	1	1	0	1
'7'	0	1	1	1		1	0	1	1	1	1	1	0	1
'8'	1	0	0	0		1	1	1	1	0	1	1	1	1
'9'	1	0	0	1		1	1	1	1	1	1	1	1	1
'+'	1	0	1	0		0	1	0	1	1	1	0	1	0
'-'	1	0	1	1		0	0	0	1	1	1	0	0	0
'='	1	1	0	0		1	1	1	0	0	0	1	1	1
'I"	1	1	0	1		1	1	1	0	1	0	1	1	1
'I"	1	1	1	0		1	1	1	0	1	0	1	1	1
'I"	1	1	1	1		1	1	1	0	1	0	1	1	1

Q2. Design the decoder circuit for die outputs A, B and C using a 2-input multiplexer where A3 is used as the selection input (Use only 2-input gates and NOT gate). (36 marks)



Output A

A3 = 0

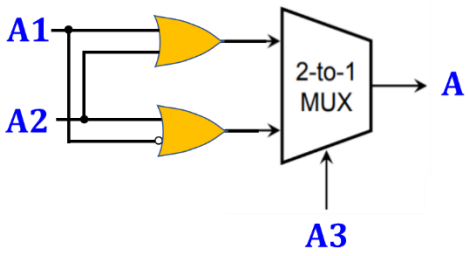
A1A0 \ A2	0	1
00	0	1
01	0	1
11	1	1
10	1	1

$f_0 = \mathrm{A1} + \mathrm{A2}$

A3 = 1

A1A0 \ A2	0	1
00	1	1
01	1	1
11	0	1
10	0	1

$f_1 = \mathrm{A1}' + \mathrm{A2}$



Output B

A3 = 0

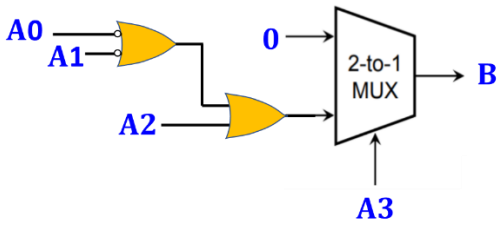
A1A0 \ A2	0	1
00	0	0
01	0	0
11	0	0
10	0	0

$f_0 = 0$

A3 = 1

A1A0 \ A2	0	1
00	1	1
01	1	1
11	0	1
10	1	1

$f_1 = \mathrm{A1}' + \mathrm{A2} + \mathrm{A0}'$



Output C

A3 = 0

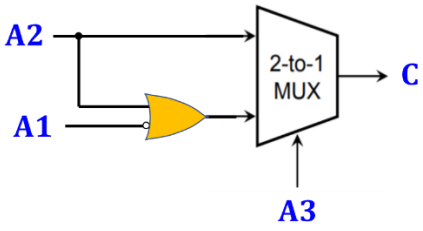
A1A0 \ A2	0	1
00	0	1
01	0	1
11	0	1
10	0	1

$f_0 = \mathrm{A2}$

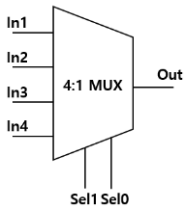
A3 = 1

A1A0 \ A2	0	1
00	1	1
01	1	1
11	0	1
10	0	1

$f_1 = \mathrm{A1}' + \mathrm{A2}$

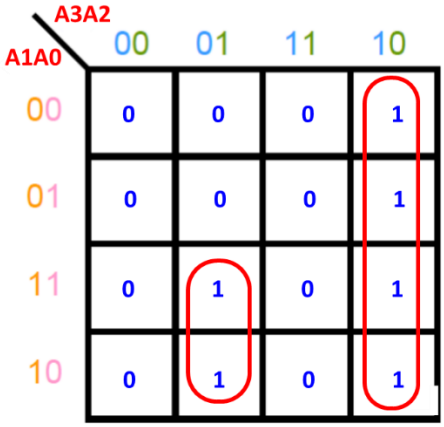


Q3. Design the decoder circuit for die outputs D, E and F using a 4-input multiplexer where A3 and A2 are used as the selection inputs. (36 marks)



S1	S0	Output
0	0	In1
0	1	In2
1	0	In3
1	1	In4

Output D

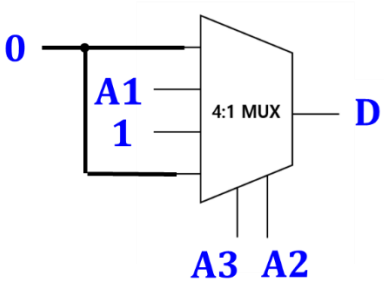


A3A2 = 00 $f_0 = 0$

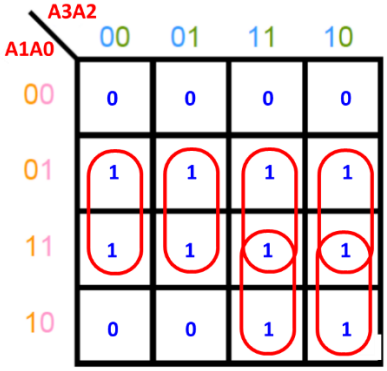
A3A2 = 01 $f_1 = \mathrm{A1}$

A3A2 = 10 $f_2 = 1$

A3A2 = 11 $f_3 = 0$



Output E

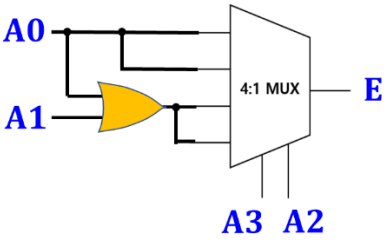


A3A2 = 00 $f_0 = \mathrm{A0}$

A3A2 = 01 $f_1 = \mathrm{A0}$

A3A2 = 10 $f_2 = \mathrm{A0} + \mathrm{A1}$

A3A2 = 11 $f_3 = \mathrm{A0} + \mathrm{A1}$



Output F

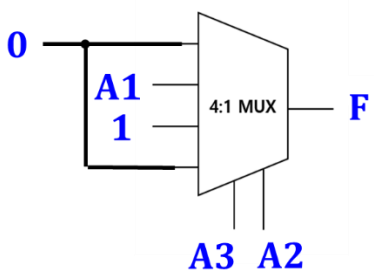
A1A0 \ A3A2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	1	0	1
10	0	1	0	1

A3A2 = 00 $f_0 = 0$

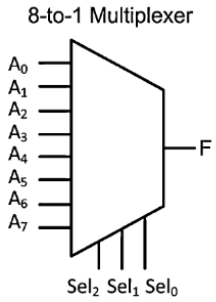
A3A2 = 01 $f_1 = \mathrm{A1}$

A3A2 = 10 $f_2 = 1$

A3A2 = 11 $f_3 = 0$



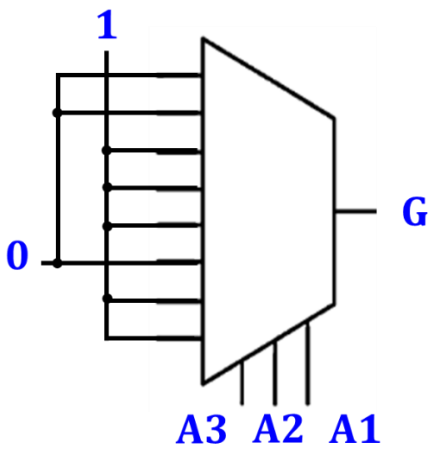
Q4. Design the decoder circuit for die outputs G, H, I and d using a 8-input multiplexer where A3, A2 and A1 are used as the selection inputs. (12 marks)



Sel_2	Sel_1	Sel_0	F
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

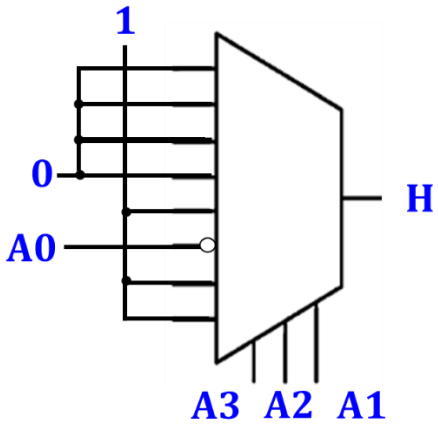
Output G

A3	A2	A1	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



Output H

A3	A2	A1	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	A0'
1	1	0	1
1	1	1	1



Output I

A3	A2	A1	A0	F
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	0
1	1	0	0	1
1	1	1	0	1