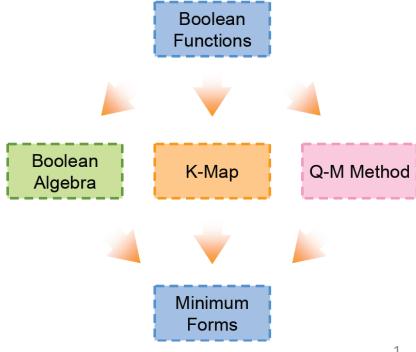
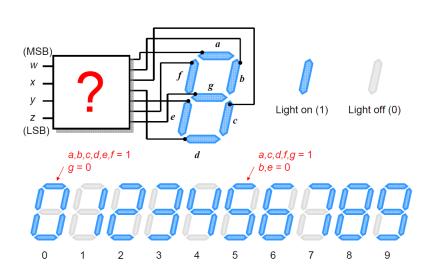
EE2000 Logic Circuit Design

Lecture 4 – Combinational Functional Blocks



Formulation



State the case

Design a circuit to convert the BCD 8421 to the 7-segment display

- w, x, y, z are the input.
- a, b, c, d, e, f, g are the output.

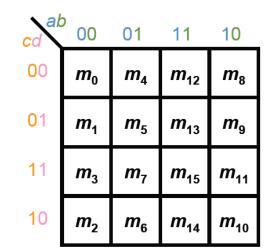
$$a(w,x,y,z) =$$

numbers		Inp	uts)	7-segment display						
Hambers	W	X	y	Z	а	b	С	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	Х	Х	Х	Х	Х	Х	Х
11	1	0	1	1	Х	Х	Х	Х	Х	Х	Х
12	1	1	0	0	Х	Х	Х	Х	Х	Х	Х
13	1	1	0	1	Х	Х	Х	Х	Х	Х	Х
14	1	1	1	0	Х	Х	Х	Х	Х	Х	Х
15	1	1	1	1	Х	Х	Х	Х	Х	Х	Х

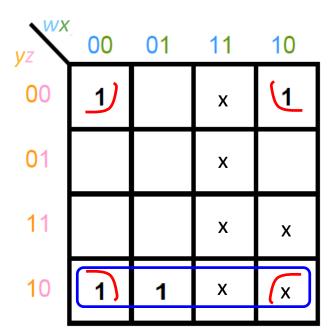
 $\Sigma m (0,2,3,5,6,7,8,9) + \Sigma d(10,11,12,13,14,15)$

K-map for segment 'e'

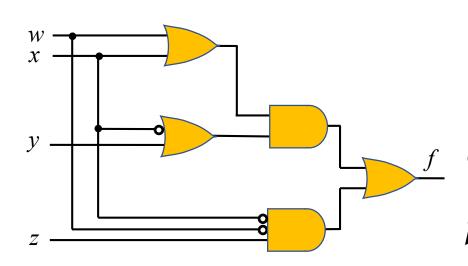
$$e(w, x, y, z) = \Sigma m(0,2,6,8) + \Sigma d(10, 11, 12, 13, 14, 15)$$



yz wx	00	01	11	10
00	1		х	1
01			Х	
11			Х	х
10	1	1	х	х

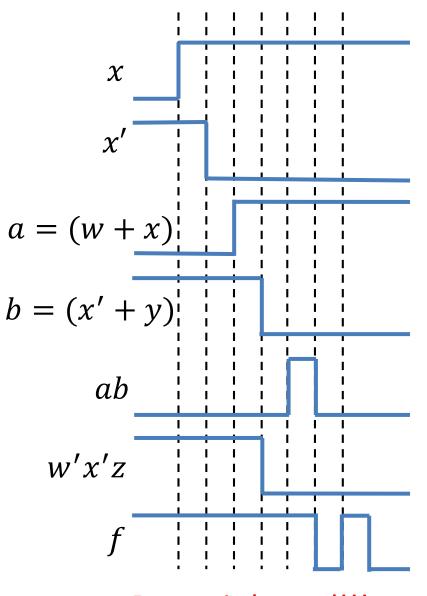


$$e(w, x, y, z) = x'z' + yz'$$



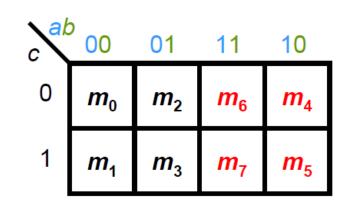
Assume that the propagation delay of NOT gate is $\Delta \tau$ and $2\Delta \tau$ for others .

Work out the timing diagram to identify the presence of any timing hazard when the input condition changes from (w, x, y, z) = (0,0,0,1) to (0,1,0,1).



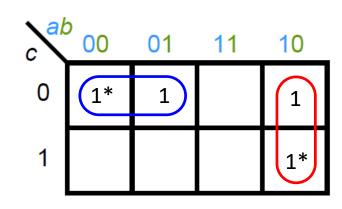
Dynamic hazard!!!

Given $f(a, b, c) = \sum m(0,2,4,5)$



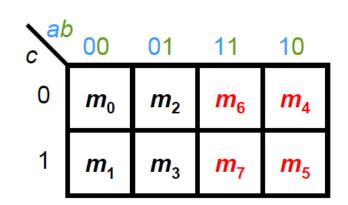
a) Minimize the function f

cak	00	01	11	10
0	1	1		1
1				1

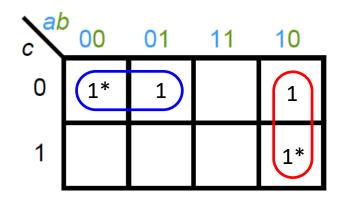


$$f(a,b,c) = a'c' + ab'$$

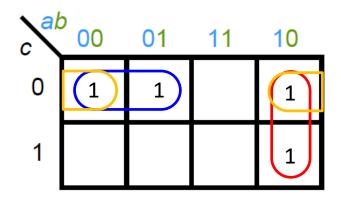
Given $f(a, b, c) = \sum m(0,2,4,5)$



b) Realize f to a hazard-free circuit



$$f(a,b,c) = a'c' + ab'$$



$$f(a,b,c) = a'c' + ab' + b'c'$$

The following block of code is received based on an even parity, identify the errors and generate the corrected data.

	1	0	1	0	0
	0	0	1	1	1
	1	0	0	0	1
	0	0	0	1	1
	1	1	0	0	0
,	1	0	0	0	_

				_
1	0	1	0	0
0	1	1	1	0
1	0	1	0	1
0	0	0	1	1
1	1	0	0	0
1	0	0	0	_

1	0	1	0	0
0	0	1	1	1
1	0	0	0	1
0	0	0	1	1
1	1	0	0	0
1	0	0	0	•

1	0	1	0	0
0	1	1	1	1
1	0	0	0	1
0	0	0	1	1
1	1	0	0	0
1	0	0	0	_

Determine the Hamming code using both odd and even parity bit for a data code of 11100

Step 1: Calculate extra bit (*k*) needed for a *n* bit of code.

Step 2: Place Parity Bits in the positions of powers of 2.

Hamming	H_9	H_8	H_7	H_6	H_5	H_4	H_3	H_2	H_1
Code									
Bit									

Determine the Hamming code using both odd and even parity bit for a data core of 11100

For a 5-bit data
$$d_5d_4d_3d_2d_1$$
, $n = 5$
$$2^k \ge 6 + k$$

Therefore, minimum value of *k* is 4. We need **4 parity** bits!

Step 2: Place Parity Bits in the positions of powers of 2.

Hamming	H_9	H_8	H_7	H_6	H_5	H_4	H_3	H_2	H_1
Code	d_5	p_4	d_4	d_3	d_2	p_3	d_1	p_2	p_1
Bit	9	8	7	6	5	4	3	2	1

Step 2: Place Parity Bits in the positions of powers of 2.

Hamming	H ₉	H ₈	H ₇	H_6	H_5	H ₄	H_3	H ₂	H_1
Code	d_5	p_4	d_4	d_3	d_2	p_3	d_1	p_2	p_1
Bit	9	8	7	6	5	4	3	2	1
Binary Code	1001	1000	0111	0110	0101	0100	0011	0010	0001
p_1									
p_2									
p_3									
p_4									
Even Parity									
Odd Parity									

Step 3: Calculate the number of '1' in each parity bits

Step 4: Place '1' if odd number of '1' for even parity; else '0'; Place '0' if odd number of '1' for odd parity; else '1'

Step 2: Place Parity Bits in the positions of powers of 2.

Hamming	H_9	H_8	H_7	H_6	H_5	H_4	H_3	H_2	H_1
Code	d_5	p_4	d_4	d_3	d_2	p_3	d_1	p_2	p_1
Bit	9	8	7	6	5	4	3	2	1
Binary Code	1001	1000	0111	0110	0101	0100	0011	0010	0001
p_1	1		1		0		0		
p_2			1	1			0		
p_3			1	1	0				
p_4	1								
Even Parity	1	1	1	1	0	0	0	0	0
Odd Parity	1	0	1	1	0	1	0	1	1

Step 3: Calculate the number of '1' in each parity bits

Step 4: Place '1' if odd number of '1' for even parity; else '0'; Place '0' if odd number of '1' for odd parity; else '1'

Example: data $d_4 d_3 d_2 d_1 = 1000$

Hamming Code	H_7	H_6	H_5	H_4	H_3	H_2	H_1
	d_4	d_3	d_2	p_3	d_1	p_2	p_1
Bit	7	6	5	4	3	2	1
Binary Code	0111	0110	0101	0100	0011	0010	0001
p_1	1		0		0		
p ₂	1	0			0		
<i>p</i> ₃	1	0	0				
Even Parity	1	0	0	1	0	1	1
Odd Parity	1	0	0	0	0	0	0

Consider odd parity and if we receive a code of 1001000, check the parity bits

$$c_1 = (H_7 \oplus H_5 \oplus H_3 \oplus H_1)' = (1 \oplus 0 \oplus 0 \oplus 0)' = 0$$

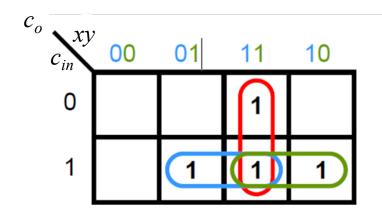
 $c_2 = (H_7 \oplus H_6 \oplus H_3 \oplus H_2)' = (1 \oplus 0 \oplus 0 \oplus 0)' = 0$
 $c_3 = (H_7 \oplus H_6 \oplus H_5 \oplus H_4)' = (1 \oplus 0 \oplus 0 \oplus 1)' = 1$
 $c_3 c_2 c_1 = (100)_2 = 4$

0 x	0 x	1 X	1 x
0 <i>y</i>	1 y	0 <i>y</i>	1 <i>y</i>
$(+)$ 0 c_{in}	$(+)$ 0 c_{in}	$(+)$ 0 c_{in}	$(+)$ 0 c_{in}
0 0	0 1	0 1	1 0
C_o S	C_o S	C_o S	C_o S
0 x	0 x	1 X	1 X
0 x	0 x	1 x	$\begin{bmatrix} 1 & x \end{bmatrix}$
$\begin{array}{ccc} 0 & x \\ 0 & y \end{array}$	$\begin{bmatrix} 0 & x \\ 1 & y \end{bmatrix}$	$\begin{array}{c c} 1 & x \\ 0 & y \end{array}$	$\begin{bmatrix} 1 & x \\ 1 & y \end{bmatrix}$
	1 <i>y</i>	0 <i>y</i>	1 <i>y</i>
0 y	1 <i>y</i>	0 <i>y</i>	1 <i>y</i>

I	nput	Outputs		
x	y	c_{in}	c_o	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- a) Work out the algebraic functions of s and c_o using K-map
- b) Draw the logic circuit diagram of full adder

c ak	00	01	11	10	
0	m_0	m ₂	<i>m</i> ₆	m ₄	
1	<i>m</i> ₁	<i>m</i> ₃	m ₇	m ₅	

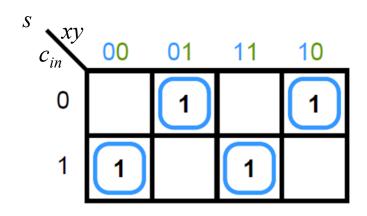


$$c_{o} = xy + xc_{in} + yc_{in} = xy + c_{in}(x + y)$$

$$= xy + c_{in}(xy' + x'y + xy)$$

$$= xy(1 + c_{in}) + c_{in}(xy' + x'y)$$

$$= xy + c_{in}(x \oplus y)$$

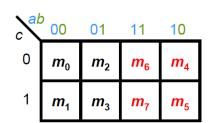


$$s = x'y'c_{in} + xyc_{in} + x'yc'_{in} + xy'c'_{in}$$

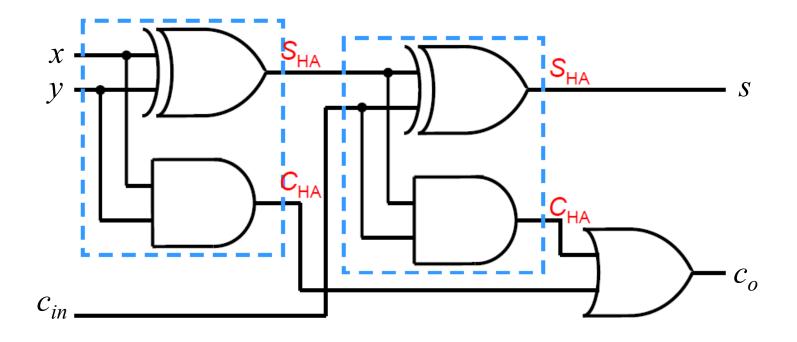
$$= c_{in}(x'y' + xy) + c'_{in}(x'y + xy')$$

$$= c_{in}(x \oplus y)' + c'_{in}(x \oplus y)$$

$$= c_{in} \oplus (x \oplus y)$$



$$c_o = xy + c_{in}(x \oplus y)$$
 $s = c_{in} \oplus (x \oplus y)$

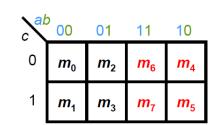


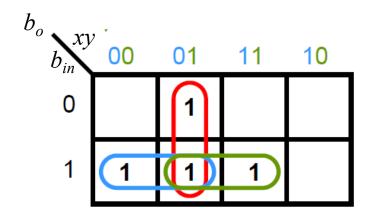
(-) 0 y	$ \begin{array}{c cccc} b_o & 1 & 0 & x \\ (-) & & 1 & y \\ \hline (-) & & 0 & b_{in} \\ \hline & & 1 \\ & & d \end{array} $	$ \begin{array}{cccc} (-) & 0 & y \\ (-) & 0 & b_{in} \\ \hline & 1 & & \\ \end{array} $	(-) 1 <i>y</i>
$(-)$ 0 y $(-)$ 1 b_{in}	$ \begin{array}{c ccccc} b_o & 1 & 0 & x \\ (-) & & 1 & y \\ \hline (-) & & 1 & b_{in} \\ \hline & & 0 \\ & & d \end{array} $	$(-)$ 0 <i>y</i> $(-)$ 1 b_{in}	(-) 1 y

I	nput	Outputs		
x	у	b_{in}	b_o	d
0	0 0		0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

- a) Work out the algebraic functions of d and b_o using K-map
- b) Draw the logic circuit diagram of full subtractor δ

ak	00	01	11	10	
0	m_0	m ₂	m ₆	m ₄	
1	<i>m</i> ₁	m ₃	m ₇	m ₅	



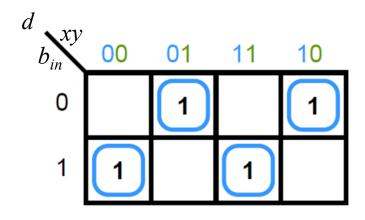


$$b_{o} = x'y + x'b_{in} + yb_{in} = x'y + b_{in}(x' + y)$$

$$= x'y + b_{in}(x'y' + x'y + xy)$$

$$= x'y(1 + b_{in}) + b_{in}(x'y' + xy)$$

$$= x'y + b_{in}(x \oplus y)'$$

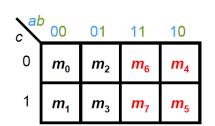


$$d = x'y'b_{in} + xyb_{in} + x'yb'_{in} + xy'b'_{in}$$

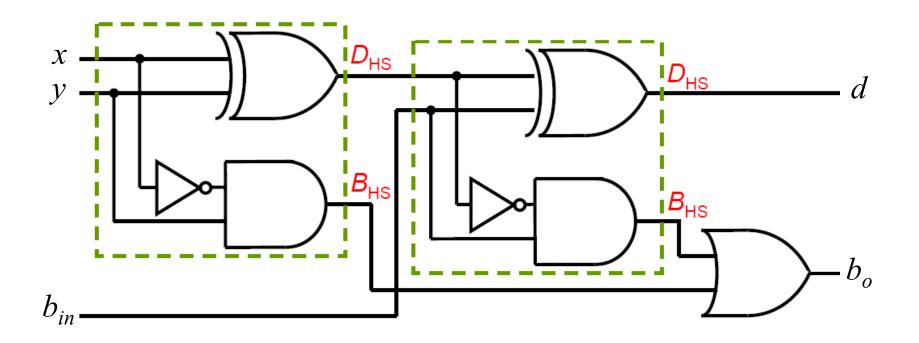
$$= b_{in}(x'y' + xy) + b'_{in}(x'y + xy')$$

$$= b_{in}(x \oplus y)' + b'_{in}(x \oplus y)$$

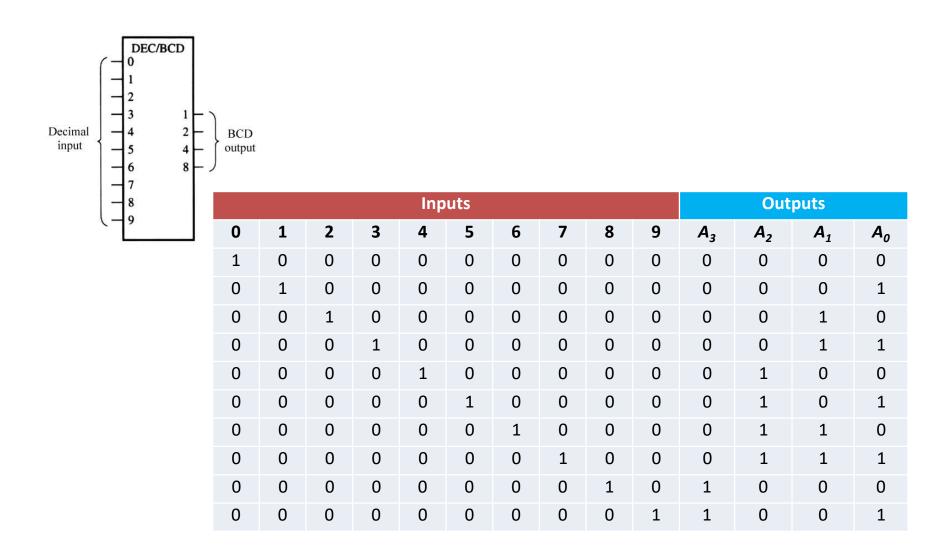
$$= b_{in} \oplus (x \oplus y)$$



$$b_o = x'y + b_{in}(x \oplus y)'$$
 $d = b_{in} \oplus (x \oplus y)$



Exercise (Decimal-to-Binary Encoder)



Exercise (Decimal-to-Binary Encoder)

	Inputs						Outputs						
0	1	2	3	4	5	6	7	8	9	A_3	A_2	A_1	A_{o}
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

