Digital-electronics-1

Labs/01-gates

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1. Link na GitHub repozitár

Digital-electronics-1

2. Verifikácia De Morganových pravidiel funkcie f(c,b,a)

$$f(c,b,a) = \overline{b}\,a + \overline{c}\,\overline{b}$$

$$f(c,b,a)_{\mathrm{NAND}} = \overline{\overline{\overline{b}\,a} \cdot \overline{\overline{c}\,\overline{b}}}$$

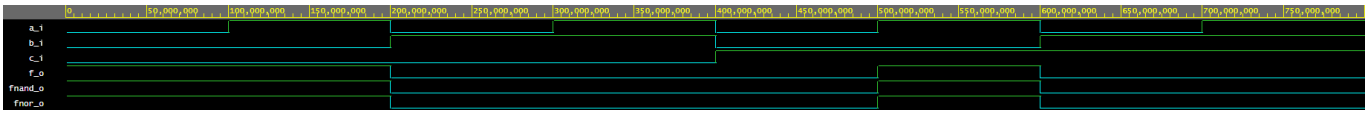
$$f(c,b,a)_{\mathrm{NOR}} = \overline{\overline{b} + \overline{a}} + \overline{c + b}$$

c	b	a	f(c,b,a)	fnand(c,b,a)	fnor(c,b,a)
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	0	0

VHDL kód

```
architecture dataflow of gates is
begin
   f_o  <= ((not b_i) and a_i) or ((not c_i) and (not b_i));
   fnand_o <= not(not(not b_i and a_i) and not(not c_i and not b_i));
   fnor_o <= not(b_i or not a_i) or not(c_i or b_i);
end architecture dataflow;
```

Simulated time waveforms



EDA Playground

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3. Verifikácia distributívnych pravidiel

$$f11(c,b,a) = a \cdot b + a \cdot c$$
$$f12(c,b,a) = a \cdot (b + c)$$
$$f11(c,b,a) = f12(c,b,a)$$

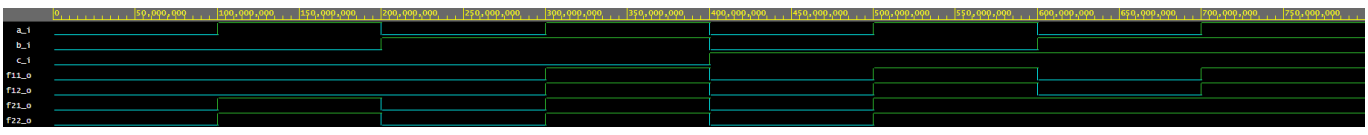
$$f21(c,b,a) = (a + b) \cdot (a + c)$$
$$f22(c,b,a) = a + (b \cdot c)$$
$$f21(c,b,a) = f22(c,b,a)$$

c	b	a	f11(c,b,a)	f12(c,b,a)	f21(c,b,a)	f22(c,b,a)
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	1	1	1	1	1

VHDL kód

```
architecture dataflow of gates is
begin
   f11_o <= (a_i and b_i) or (a_i and c_i);
   f12_o <= a_i and (b_i or c_i);
   f21_o <= (a_i or b_i) and (a_i or c_i);
   f22_o <= a_i or (b_i and c_i);
end architecture dataflow;
```

Simulated time waveforms



EDA Playground