

Digital-electronics-1

Labs/01-gates

Dominik Grenčík, 220815

1. Link na GitHub repozitár

[Digital-electronics-1](#)

2. Verifikácia De Morganových pravidiel funkcie $f(c,b,a)$

$$f(c,b,a) = \bar{b}a + \bar{c}\bar{b}$$

$$f(c,b,a)_{\text{NAND}} = \overline{\bar{b}a \cdot \bar{c}\bar{b}}$$

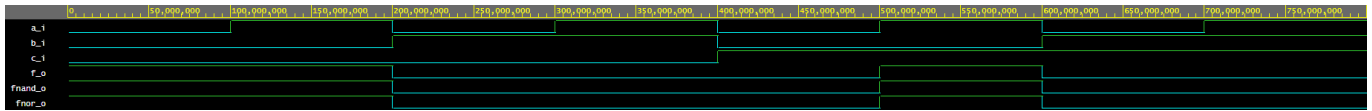
$$f(c,b,a)_{\text{NOR}} = \overline{\bar{b} + \bar{a}} + \overline{c + b}$$

c	b	a	f(c,b,a)	fnand(c,b,a)	fnor(c,b,a)
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	0	0

VHDL kód

```
architecture dataflow of gates is
begin
    f_o <= ((not b_i) and a_i) or ((not c_i) and (not b_i));
    fnand_o <= not(not(not b_i and a_i) and not(not c_i and not b_i));
    fnor_o <= not(b_i or not a_i) or not(c_i or b_i);
end architecture dataflow;
```

Simulated time waveforms



EDA Playground

3. Verifikácia distributívnych pravidiel

$$f_{11}(c, b, a) = a \cdot b + a \cdot c$$

$$f_{12}(c, b, a) = a \cdot (b + c)$$

$$f_{11}(c, b, a) = f_{12}(c, b, a)$$

$$f_{21}(c, b, a) = (a + b) \cdot (a + c)$$

$$f_{22}(c, b, a) = a + (b \cdot c)$$

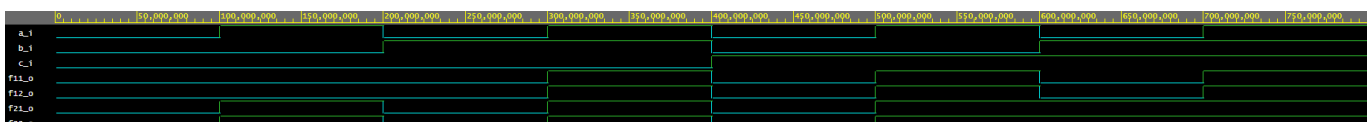
$$f_{21}(c, b, a) = f_{22}(c, b, a)$$

c	b	a	f11(c,b,a)	f12(c,b,a)	f21(c,b,a)	f22(c,b,a)
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	1	1	1	1	1

VHDL kód

```
architecture dataflow of gates is
begin
    f11_o <= (a_i and b_i) or (a_i and c_i);
    f12_o <= a_i and (b_i or c_i);
    f21_o <= (a_i or b_i) and (a_i or c_i);
    f22_o <= a_i or (b_i and c_i);
end architecture dataflow;
```

Simulated time waveforms



[EDA Playground](#)