Revision history

Rev	Date	Description
1.0	May 2004	First official release

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Errata 1: The peripheral controller cannot handle odd bytes.

1.1 Problem Description

During a DMA transfer, data is transferred two bytes at a time. If the data to be transferred is an odd number and the host does not know the exact number of data bytes to be transferred, then the last transfer will be interpreted as of even bytes, even if it is just one byte of valid data.

1.2 Implication

Affects data integrity in systems in which the data to be transferred is not known to the host.

1.3 Workaround

No software workaround is available.

1.4 Status

No fix is planned.

Errata 2: Incorrect updating of the ATL Done Map.

2.1 Problem Description

The HcATLPTDDoneMap register is designed to work with the ATL interrupt. The HcATLPTDDoneMap register will be read if and only if an ATL interrupt has occurred.

If the software does not use the ATL interrupt, the HcATLPTDDoneMap register might be accessed when there is no pending ATL interrupt. This can sometimes lead to an incorrect ATL Done Map content, that is, an ATL that has been completed does not cause the corresponding bit in the HcATLPTDDoneMap register to be set.

2.2 Implication

Software might miss a completed ATL transfer.

2.3 Workaround

Software can be modified to check for the ATL interrupt bit before reading HcATLPTDDoneMap.

2.4 Status

No fix is planned.

Errata 3: Data corruption during a write operation to the ISP1362 peripheral controller.

3.1 Problem Description

After a data write operation, the ISP1362 peripheral controller requires a 132-ns delay before a write assertion can be issued for other devices. This must be fulfilled even after CS_N is deasserted (See Figure 1 and Figure 2).

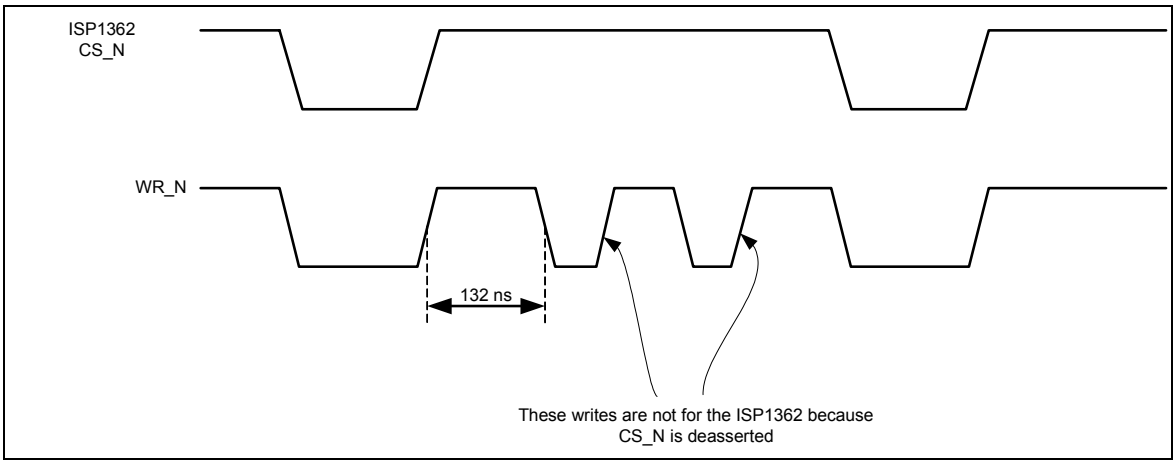

Figure 1

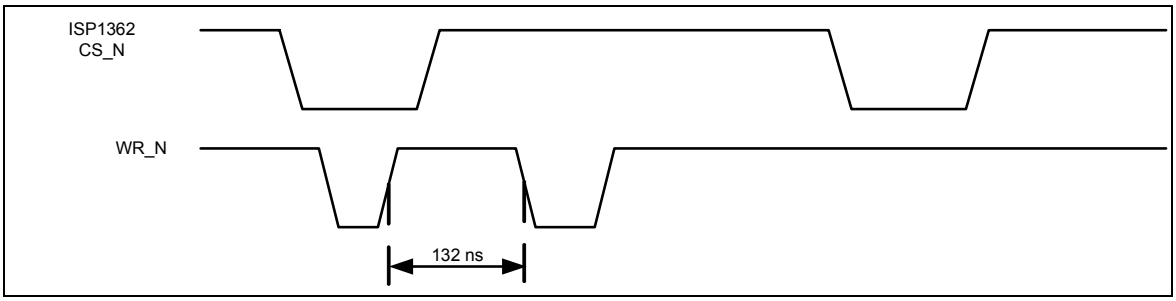

Figure 2

3.2 Implications

Will lead to data corruption if the timing requirements in Figure 1 and Figure 2 are not handled.

3.3 Workaround

Make sure that the system can handle the write timing requirements as given in Figure 1 and Figure 2. If the system is really fast and needs immediate write accesses to other devices, then it is better to qualify WR_N with respect to CS_N and provide the resulting write signal to the ISP1362 (see Figure 3).

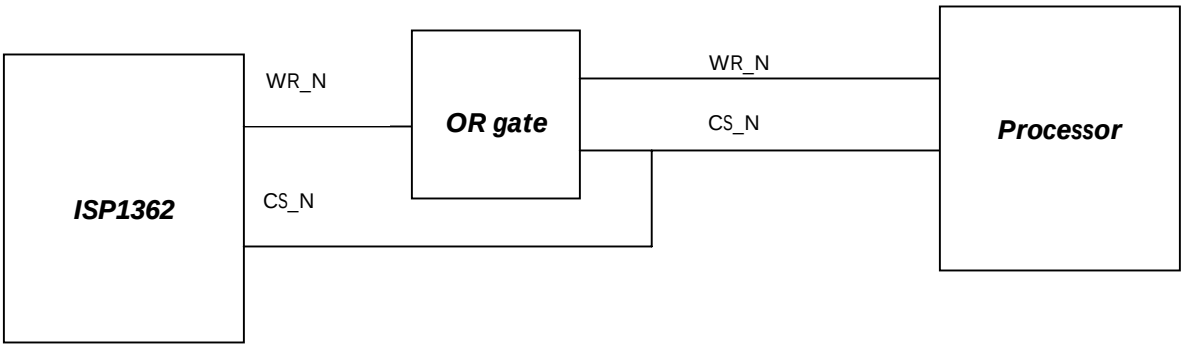

Figure 3

Note: Please take into consideration the propagation delay of the logics.

3.4 Status

No fix is planned.