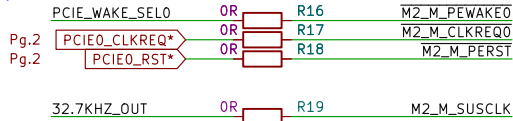
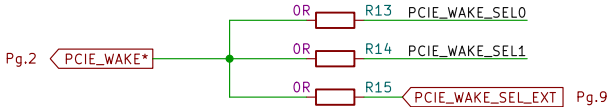


PCIe0 Root Port / Endpoint mode selector

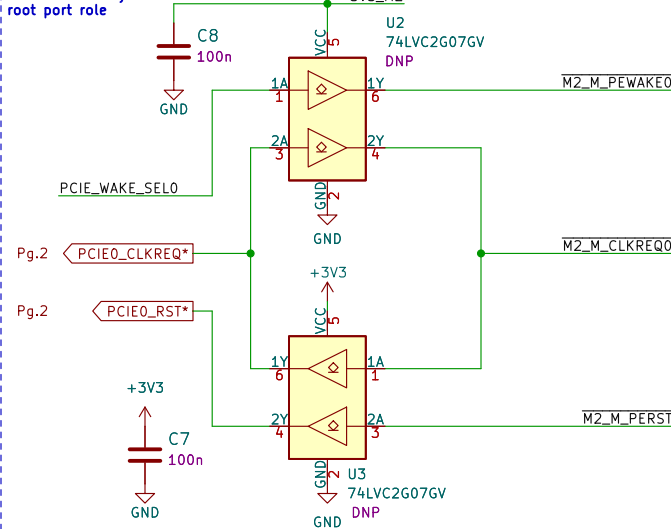
NOTE:
DNP for M.2 key M
endpoint role



M.2 PCIE_WAKE selector

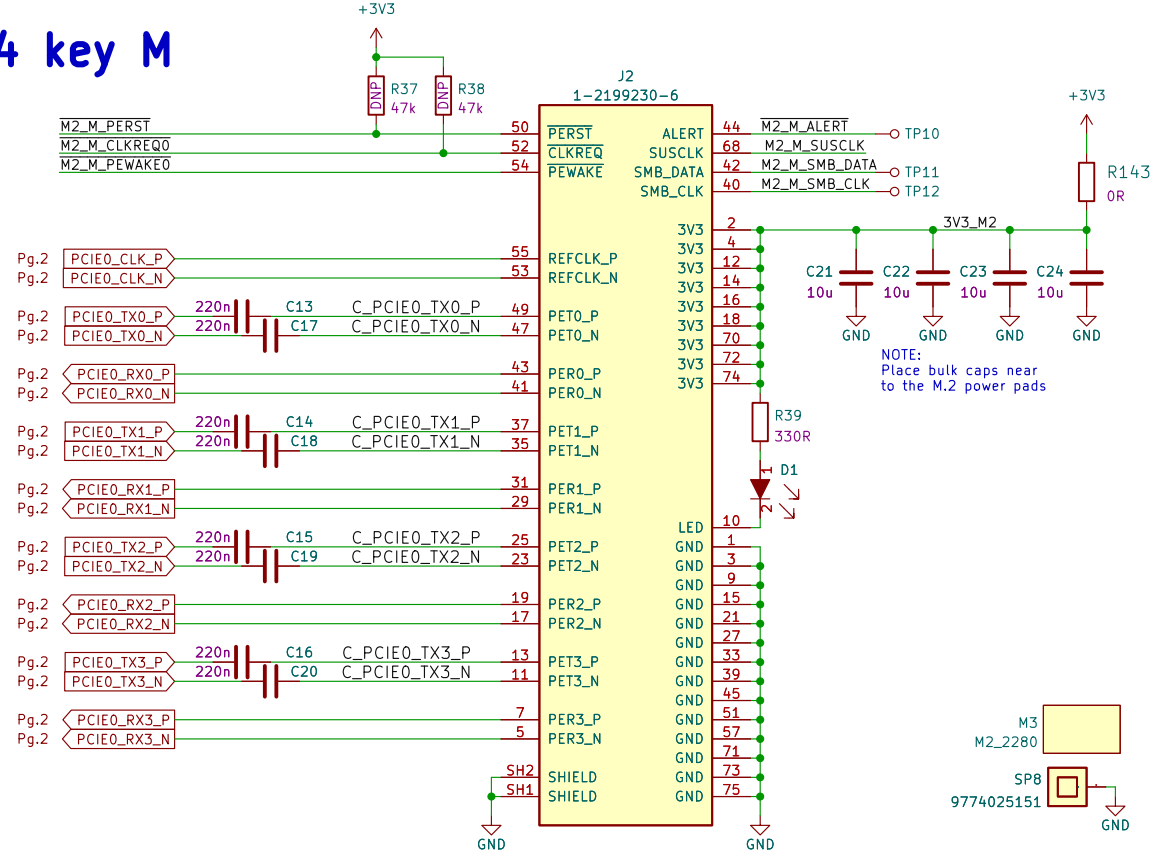


NOTE:
DNP for M.2 key M
root port role

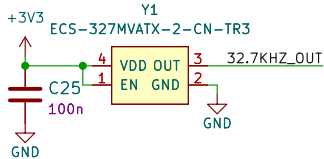


NOTE about PCIe 0 role switching:
For details, refer to the PCIe section of
"Jetson Orin NX Series Product Design Guide"
<https://developer.nvidia.com/jetson-orin-nx-series-design-guide>

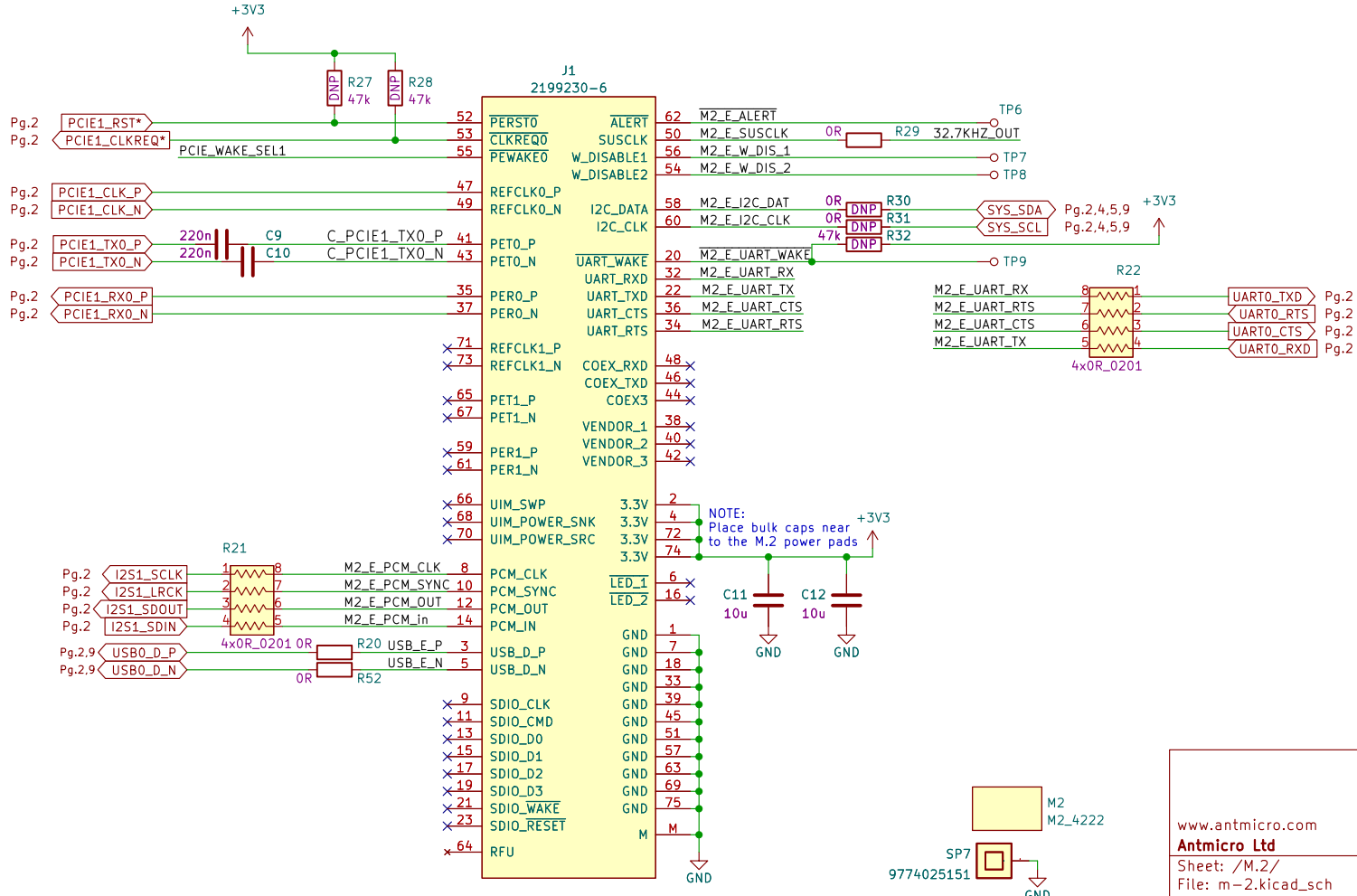
PCIe0 1x4 key M



SUSCLK SOURCE



PCIe1 1x1 key E



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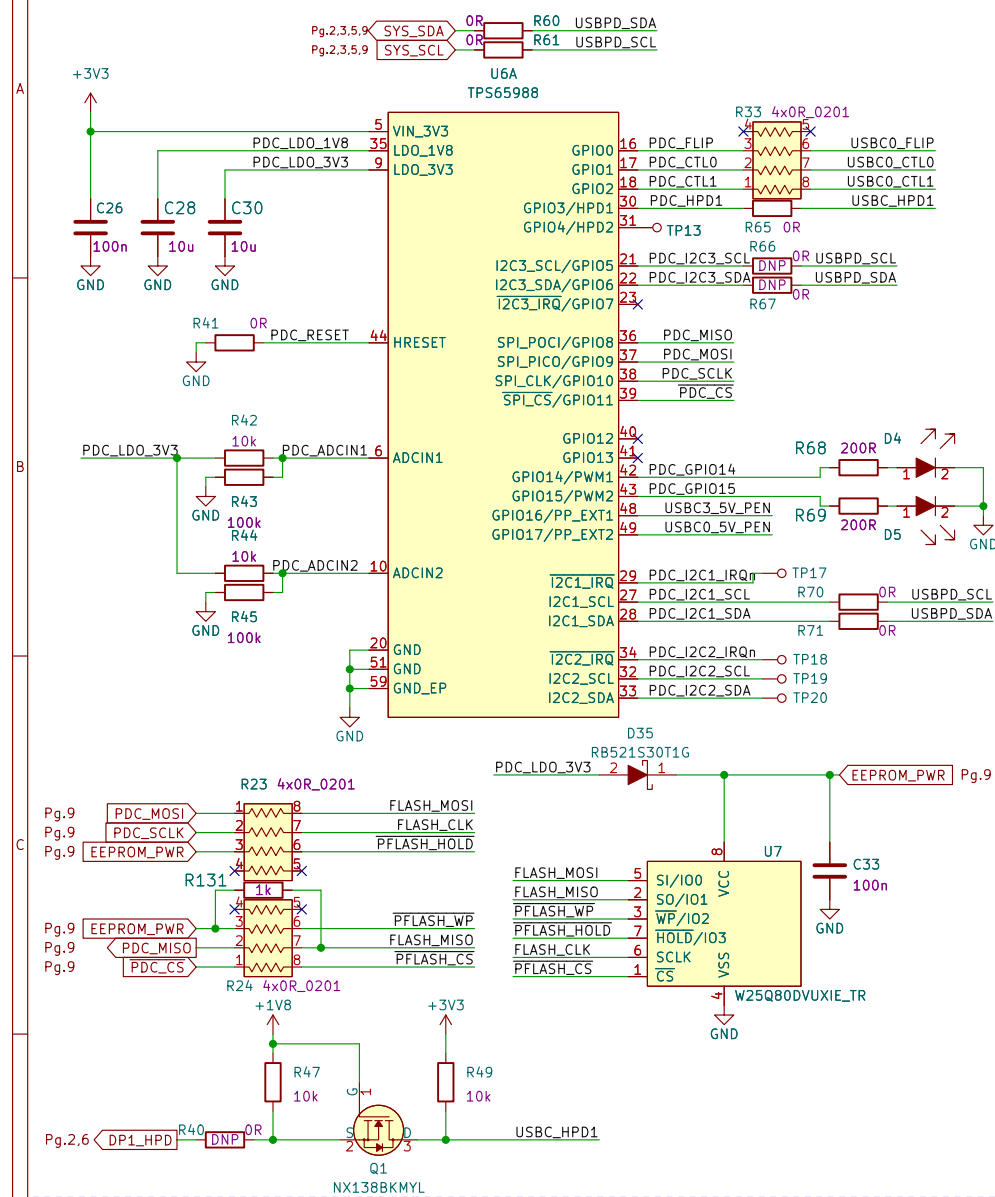
Sheet: /M.2/
File: m-2.kicad_sch

Title: Jetson Orin Baseboard

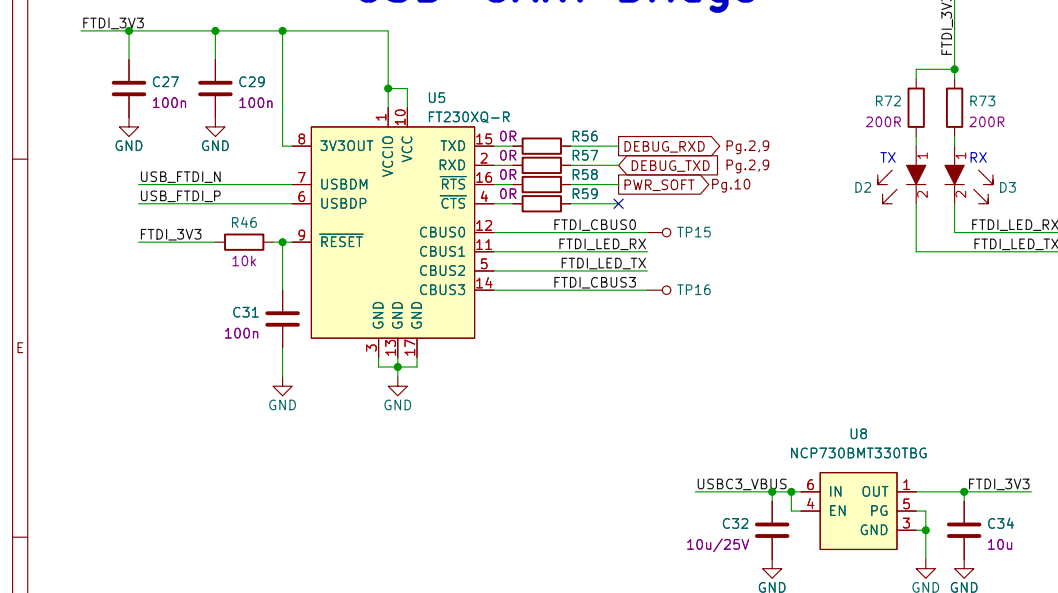
Size: A3	Date: 2022-10-07
KiCad E.D.A. eeschema 6.0.9-8da3e8f707~117-ubuntu22.04.1	

Rev: 1.0.0
Id: 3/10

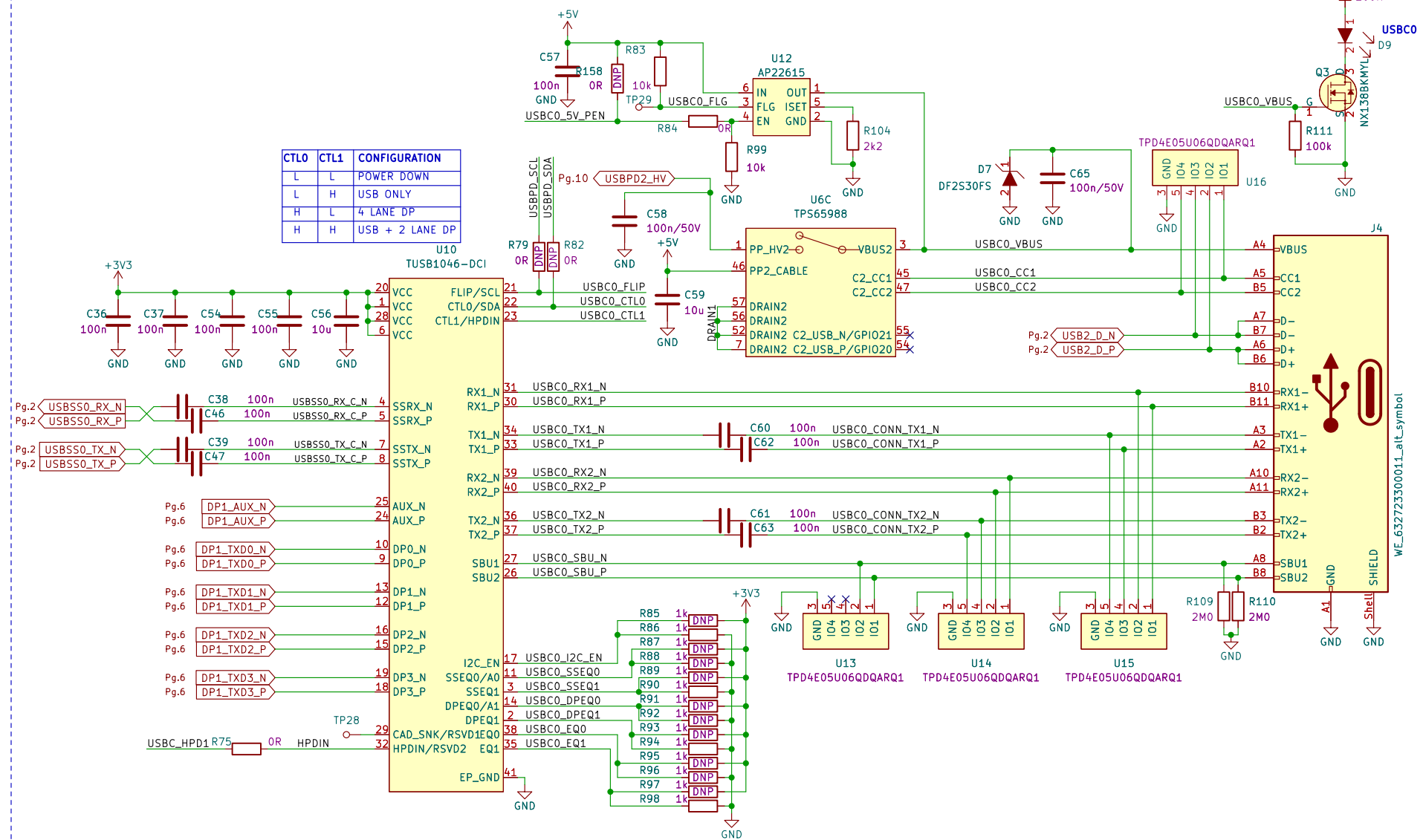
USB PD Controller



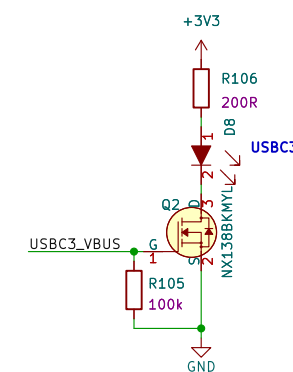
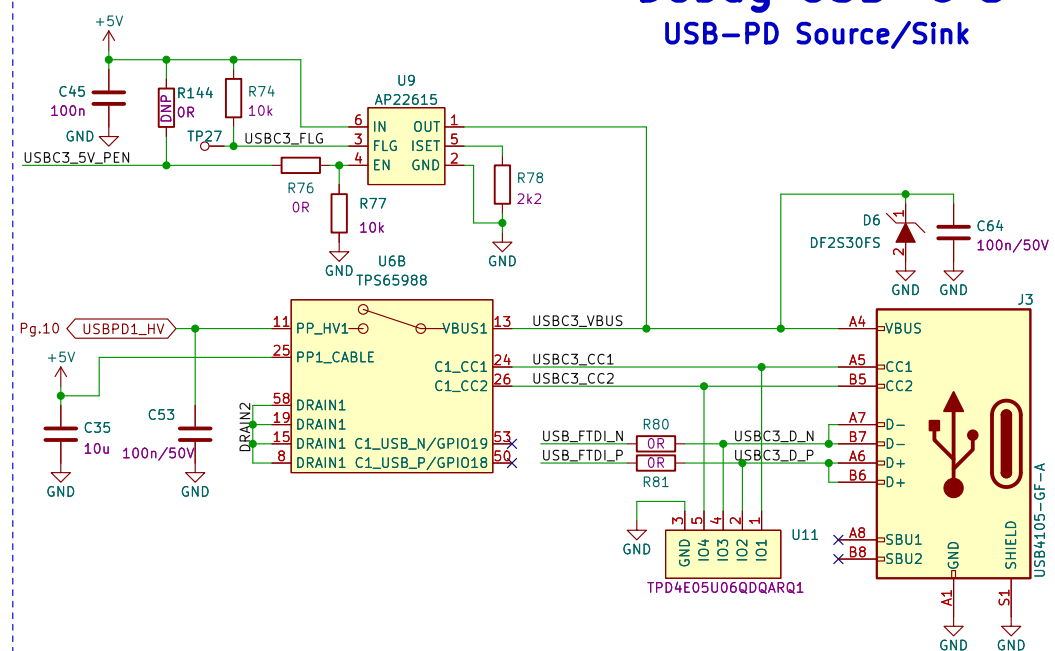
USB-UART Bridge



USB-C 0 Display Port alt mode



Debug USB-C 3



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Sheet: /USB Debug, DP/
File: usb.kicad_sch

Title: Jetson Orin Baseboard

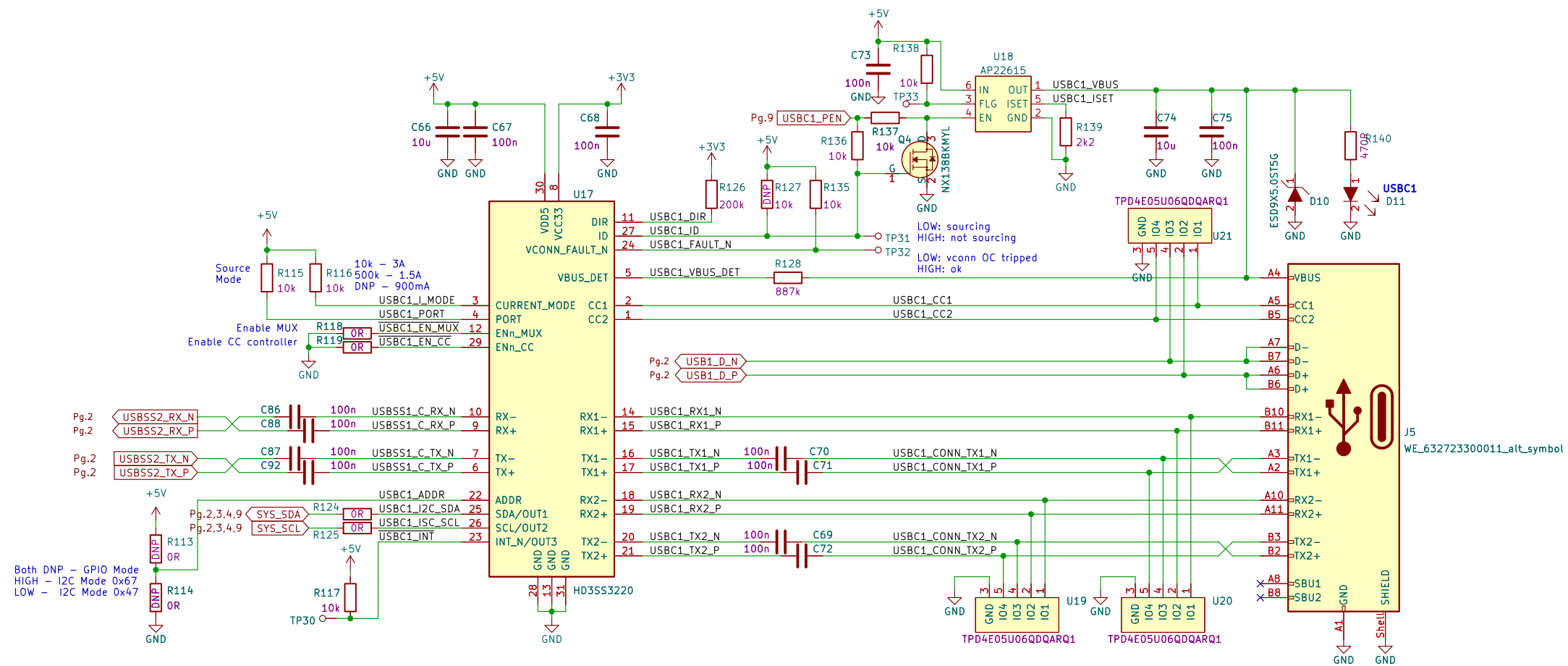
Size: A3

Date: 2022-10-07

Size: AS	Date: 2022-10-07
KiCad E.D.A. eeschema 6.0.9-8da3e8f707~117-ubuntu22.04.1	

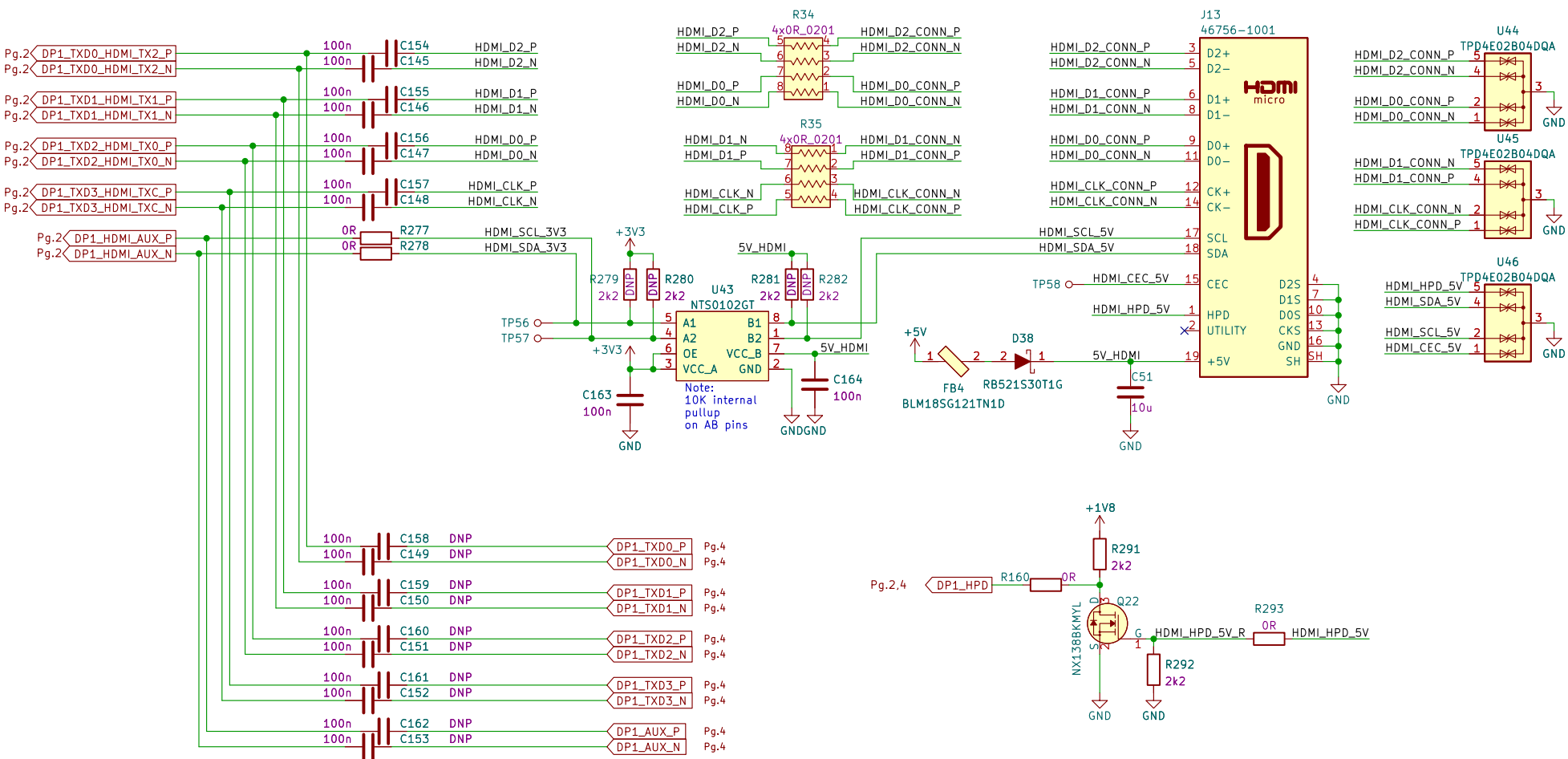
Rev: 1.0.0

USB-C 1

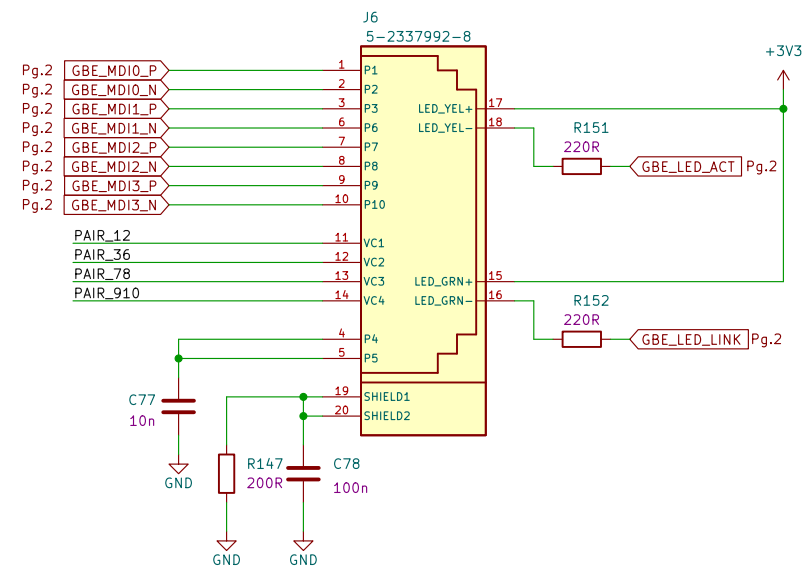


HDMI Connector

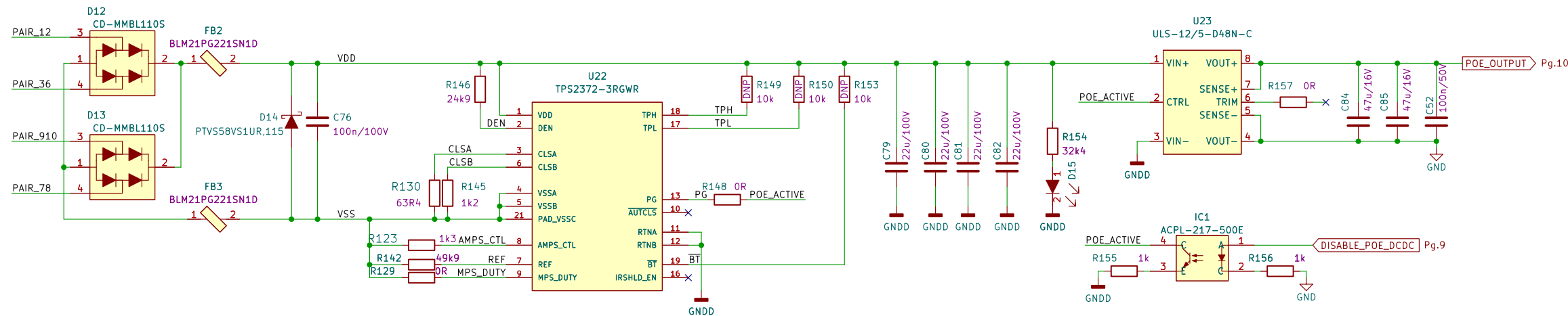
Output selection



Ethernet Connector



Power over Ethernet



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Sheet: /Ethernet/

File: ethernet.kicad_sch

Title: Jetson Orin Baseboard

Size: A3

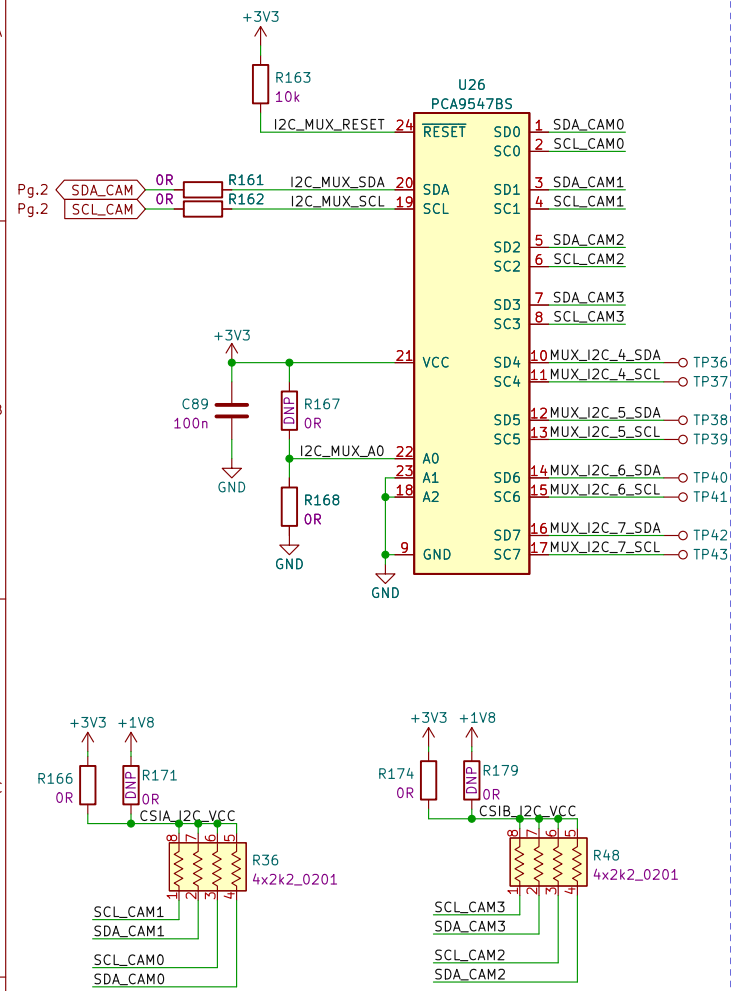
Date: 2022-10-07

Rev: 1.0.0

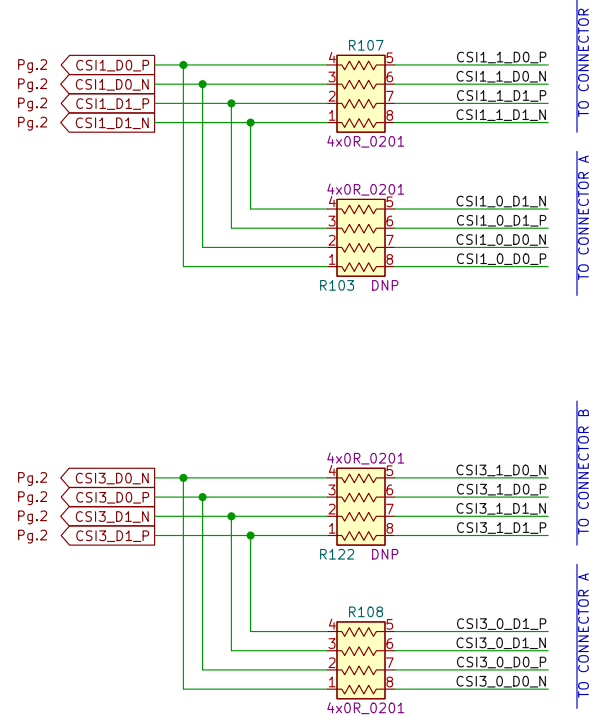
KiCad E.D.A. eeschema 6.0.9-8da3e8f707-117-ubuntu22.04.1

Id: 7/10

I2C Mux



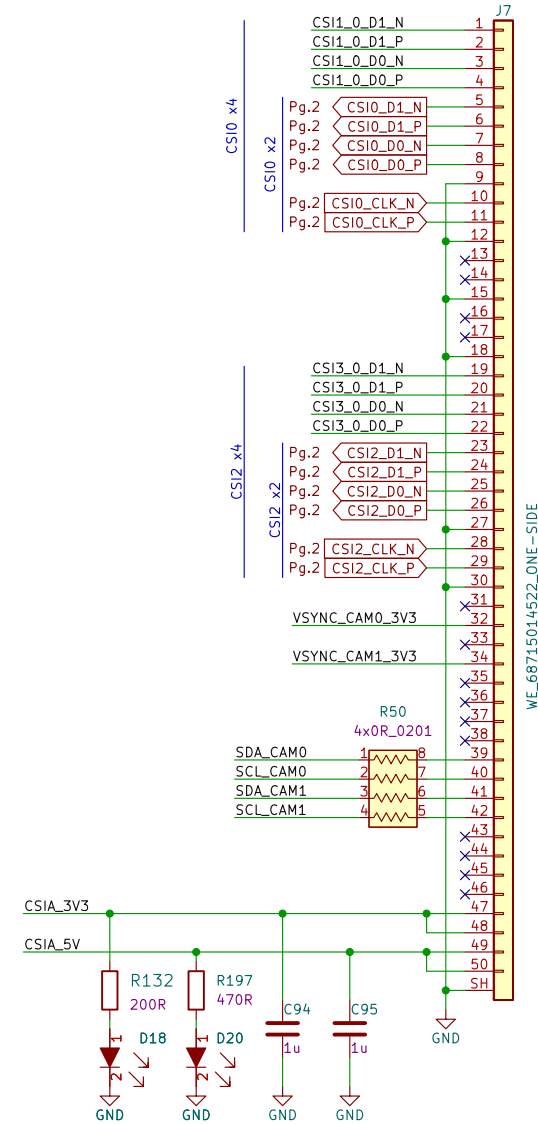
CSI Mux



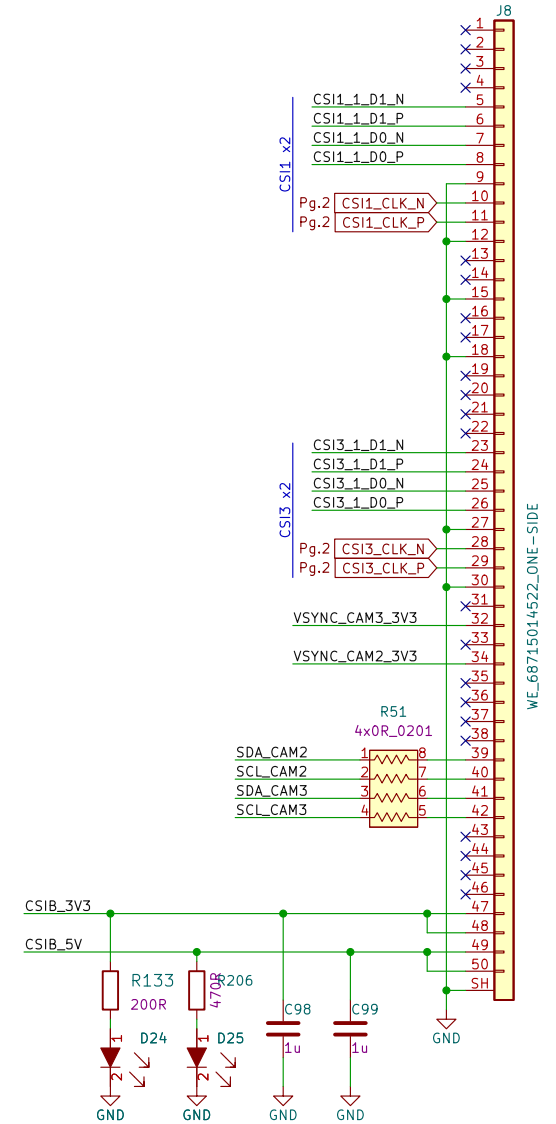
AVAILABLE CSI CONFIGURATIONS:

CONNECTOR A	CONNECTOR B
CSI0x4 CSI2x4	NONE
CSI0x4 CSI2x2	CSI3x2
CSI0x2 CSI2x4	CSI1x2
CSI0x2 CSI2x2	CSI3x2 CSI1x2

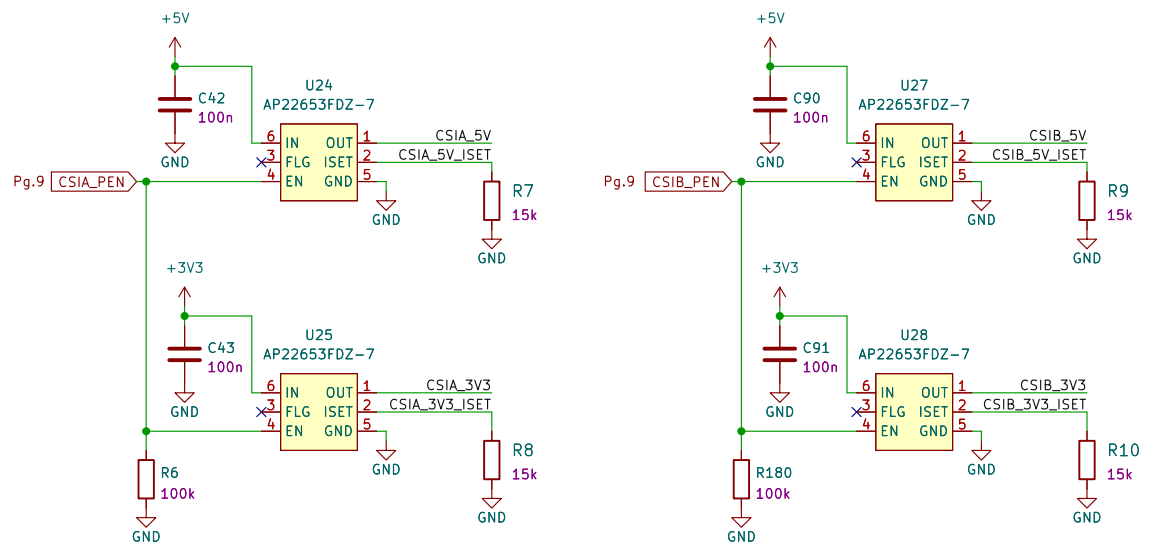
CSI connector A



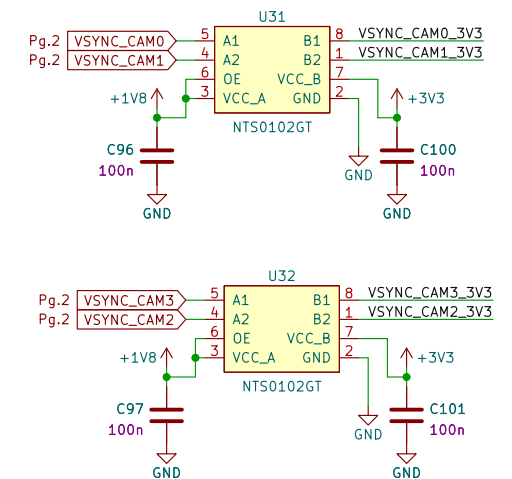
CSI connector B



Power switches



Level shifters



GPIO expander

The schematic diagram illustrates the connection of a PCAL6408ABSHP GPIO expander IC. The IC is powered by a +3V3 supply at pins 15 (Vdd(I2C)) and 14 (Vdd(p)), with a 100nF capacitor (C104) connected to the +3V3 supply. The INT pin (11) is pulled up to +1V8 by resistor R219 (10k2) and connected to the GPIO_INT signal (Pg.2). The SDA (13) and SCL (12) pins are connected to the I2C bus (SYS_SDA and SYS_SCL, Pg.2,3,4,5) through pull-up resistors R215 and R216. The RESET pin (1) is pulled up to +3V3 by resistor R217 and connected to the GPIOEX_RESET signal. The ADDR pin (16) is pulled up to GND by resistor R218. The P0-P7 pins (2-10) are connected to the GPIOEX_P0_0-GPIOEX_P0_3 signals (Pg.8) through a 4x0R_0201 resistor network. The P4-P7 pins are also connected to test points TP1, TP34, TP46, and TP47. The IC is labeled PCAL6408ABSHP.

Expansion connector

Fan connector

The diagram illustrates the electrical connection for a fan connector. It features a central integrated circuit, the NT50102GT (labeled U33), which is configured as a fan speed sensor. The chip's pins are connected as follows:

- Pin 5 (A1):** Connected to the **FAN_PWM** signal from the fan connector (Pg.2).
- Pin 4 (A2):** Connected to the **FAN_TACH** signal from the fan connector (Pg.2).
- Pin 6 (OE):** Connected to a **+1V8** supply through a **100nF** capacitor (C44).
- Pin 3 (VCC_A):** Connected to **GND**.
- Pin 8 (B1):** Connected to the **FAN_PWM_5V** signal from the fan connector.
- Pin 1 (B2):** Connected to the **FAN_TACH_5V** signal from the fan connector.
- Pin 7 (VCC_B):** Connected to a **+5V** supply through a **100nF** capacitor (C48).
- Pin 2 (GND):** Connected to **GND**.

The output signals, **FAN_PWM_5V** and **FAN_TACH_5V**, are routed to a fan connector labeled **J10** (533980471). The connector pins are numbered 1 through 4, corresponding to the signals: 1 (FAN_TACH_5V), 2 (FAN_PWM_5V), 3 (FAN_TACH), and 4 (FAN_PWM).

Expansion connector resistors


Debug connector

TAG-CONNECT


J9
TC2050-IDC-NL

Signal	Pin	Signal	Pin
DEBUG_TXD (Pg. 2, 4)	1	EEPROM_PWR (Pg. 4)	10
DEBUG_RXD (Pg. 2, 4)	2	PDC_MOSI (Pg. 4)	9
SYS_SDA (Pg. 2, 3, 4, 5)	3	PDC_MISO (Pg. 4)	8
SYS_SCL (Pg. 2, 3, 4, 5)	4	PDC_SCLK (Pg. 4)	7
	5	PDC_CS (Pg. 4)	6

GND



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hardware

LED indicators

The image displays two circuit diagrams for LED indicators, labeled Pg.2 USER_LED0 and Pg.2 USER_LED1.

Left Circuit (USER_LED0):

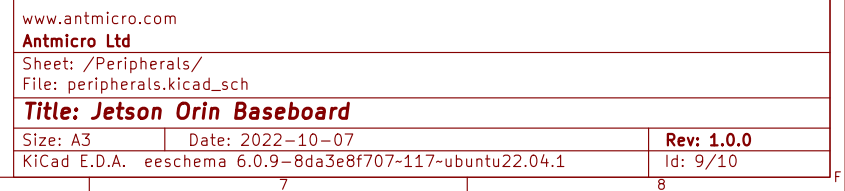
- Power supply: +3V3
- Resistor: R223 (200R)
- Diode: D26
- MOSFET: Q9 (NX1368KMYL)
- Resistor: R222 (100k)
- Ground: GND

Right Circuit (USER_LED1):

- Power supply: +3V3
- Resistor: R231 (200R)
- Diode: D27
- MOSFET: Q10 (NX1368KMYL)
- Resistor: R230 (100k)
- Ground: GND

Buttons

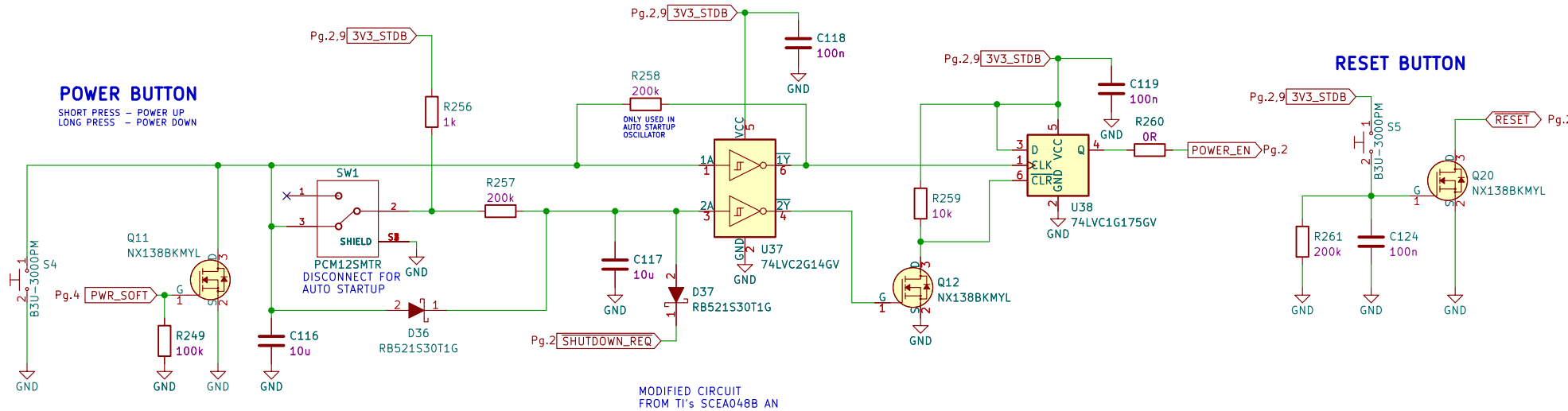
The image displays two circuit diagrams for button connections. Both diagrams show a button connected to a +1V8 supply through a 10k resistor (R232 for the left, R242 for the right). The buttons are labeled S2 and S3, and are 3000PM. The pins are labeled Pg.2. The left diagram shows the connection to USER_BTN0, and the right diagram shows the connection to USER_BTN1. The buttons are connected to GND through a switch.



POWER-UP AND RESET CIRCUITRY

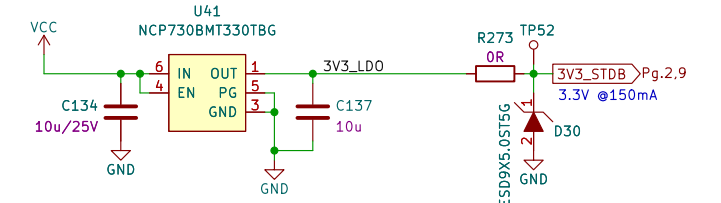
POWER BUTTON

SHORT PRESS - POWER UP
LONG PRESS - POWER DOWN

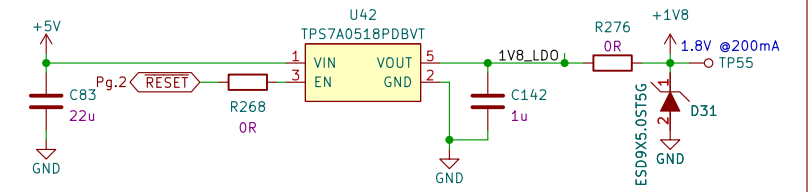


MODIFIED CIRCUIT
FROM TI's SCEA048B AN

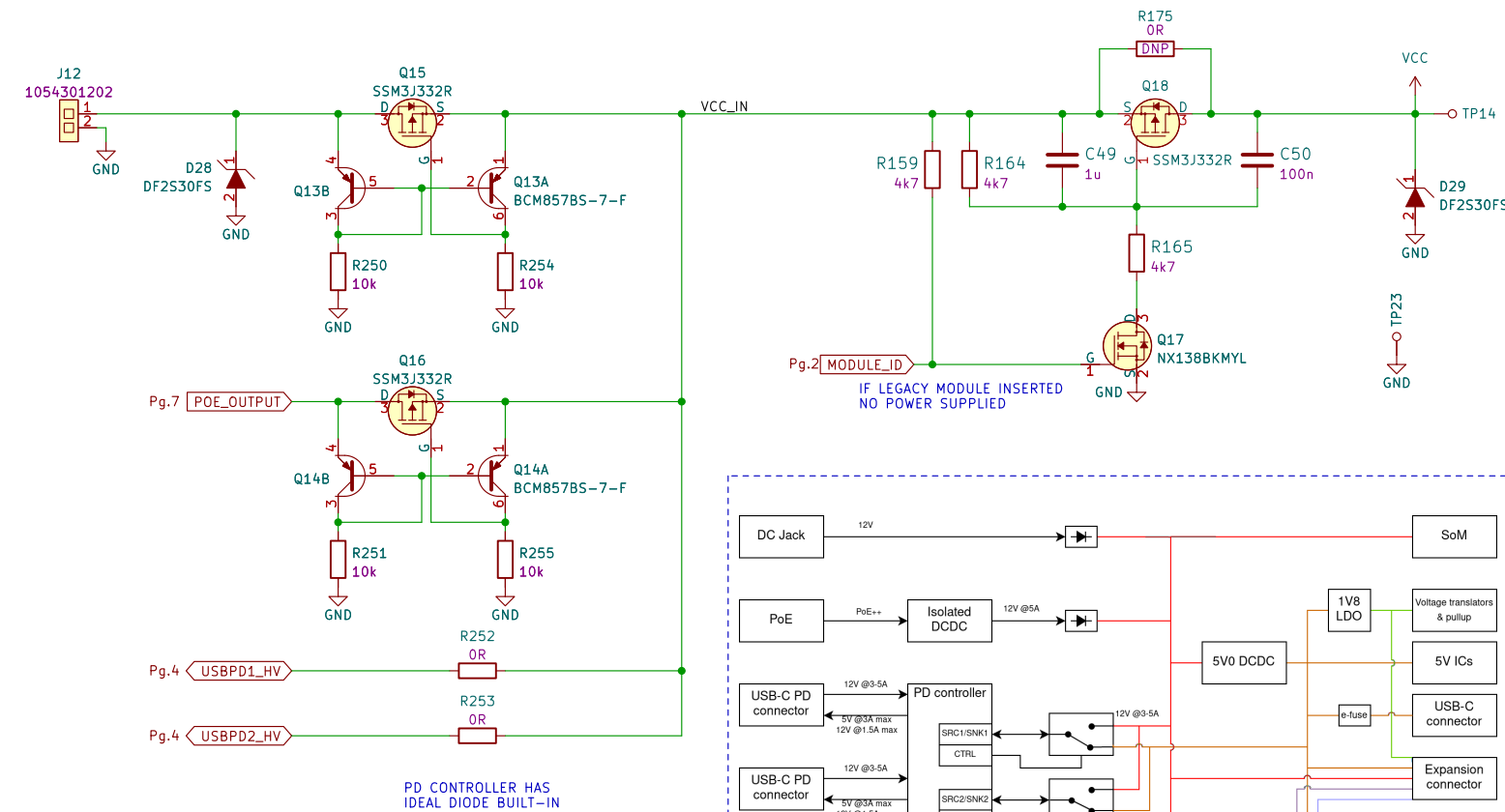
3V3 STANDBY LDO



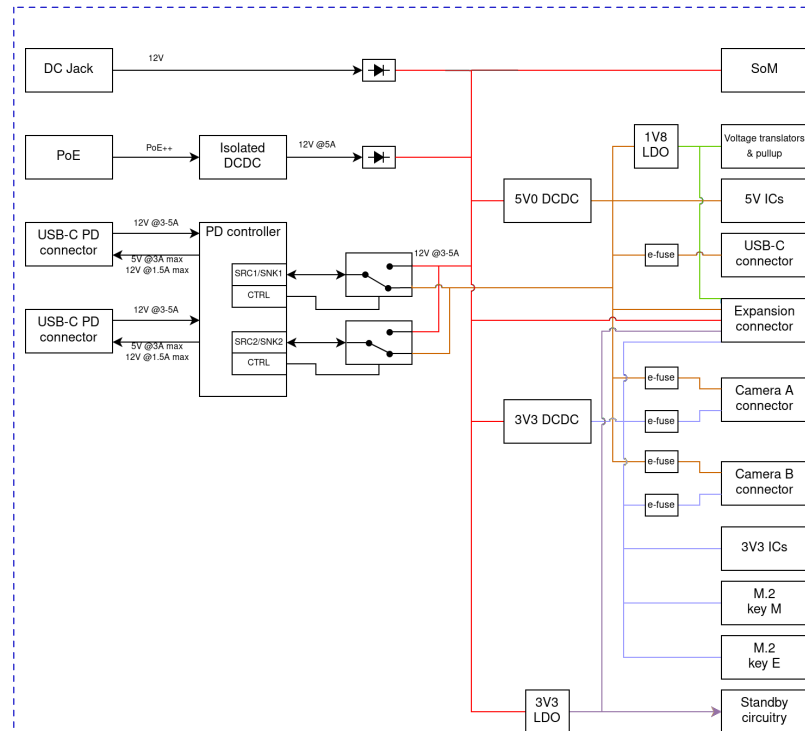
1V8 LDO



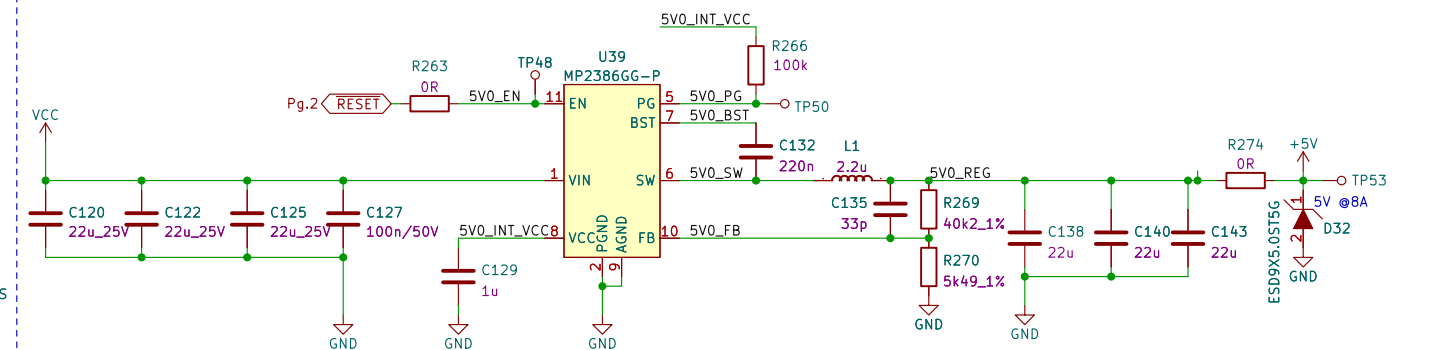
INPUT SELECTOR AND SOFT START



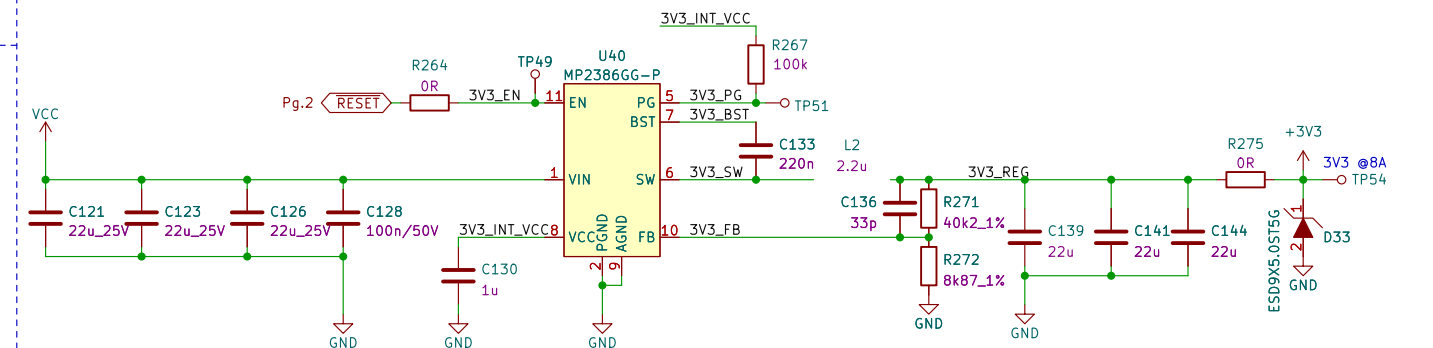
PD CONTROLLER HAS
IDEAL DIODE BUILT-IN



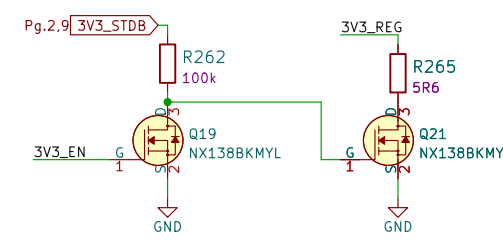
5V DCDC



3V3 DCDC



3V3 rail discharge



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Sheet: /Supply/

File: supply.kicad_sch

Title: Jetson Orin Baseboard

Size: A3

Date: 2022-10-07

Rev: 1.0.0

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Id: 10/10