HARMAN

A SAMSUNG COMPANY

DEVICE TREE (IN LINUX)

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AGENDA

1. Device tree background
2. Device tree semantics
3. Device tree details in Linux
4. Device tree examples in Linux
5. Device tree questions ?

DEVICE TREE

BACKGROUND

- Open Firmware IEEE 1275, ePAPR, DTspec
- FDT, EDT
- HW description
- HW configuration
- Firmware options

DEVICE TREE

OVERVIEW

- Device nodes and properties
- Routing and mapping
- Dependency
- Device Tree Source Format (DTSI, DTS)
- Device Tree Compiler
- Device Tree Blob

DEVICE TREE SOURCE FORMAT

```
[label:] node-name[@unit-address] {
        [properties definitions]
        [child nodes]
}

[label:] property-name = value;
[label:] property-name;

/node-name-1/node-name-2/node-name-N

/memreserve/ <address> <length>
/delete-property/ property-name;
/delete-node/ node-name;
#include „some-dtsi-file.dtsi” or „some-c-header-file.h”
```

DEVICE TREE SOURCE FORMAT

```
/dts-v1/;
#include „some.dtsi-file.dtsi” or <some-c-include-file.h>
/ {
    node1 {
        a-string-property = "A string";
        a-string-list-property = "first string", "second string";
        // hex is implied in byte arrays. no '0x' prefix is required
        a-byte-data-property = [01 23 34 56];
        child-node1 {
            first-child-property;
            second-child-property = <1>;
            a-string-property = "Hello, world";
        };
        child-node2 {
        };
    };
    node2 {
        an-empty-property;
          a-cell-property = <1 2 3 4>; /* each number (cell) is a uint32 */
          a-cell-property-with-phandle = <&some_node 1 2>; /* each number (cell) is a uint32 */
        child-node1 {
        };
    };
};
```

DEVICE TREE NODES

- CPUs
- Memory
- MMIO buses (platform, amba, pci)
- Non MMIO buses (spi, i2c etc.)
- IRQ controller
- PIN controller (muxing, routing, configuration)
- CLOCK controller
- GPIO controller
- DMA controller
- IOMMU controller

- Firmware options
- Aliases

DEVICE TREE PROPERTIES

- compatible
- status
- reg
- phandle
- #address-cells
- #size-cells
- ranges, dma-ranges
- interrupts (interrupt-controller, #interrupt-cells, interrupt-parent)
- clocks (#clock-cells, assigned-clocks, assigned-clock-parents)
- gpios (gpio-controller, #gpio-cells)
- pinctrl-*
- dmas (#dma-cells)
- iommus (#iommu-cells)

DEVICE TREE EXAMPLES - ARMV7-M.DTSI INTERRUPT CONTROLLER, CLOCKSOURCE

```
/ {
        nvic: interrupt-controller@e000e100  {
                compatible = "arm,armv7m-nvic";
                interrupt-controller;
                #interrupt-cells = <1>;
                reg = <0xe000e100 0xc00>;
        };

        systick: timer@e000e010 {
                compatible = "arm,armv7m-systick";
                reg = <0xe000e010 0x10>;
                status = "disabled";
 };

        soc {
                #address-cells = <1>;
                #size-cells = <1>;
                compatible = "simple-bus";
                interrupt-parent = <&nvic>;
                ranges;
        };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES - STM32F429.DTSI PLATFORM DEVICES, CLOCKS

```
clocks {
        clk_hse: clk-hse {
                #clock-cells = <0>;
                compatible = "fixed-clock";
                clock-frequency = <0>;
        };
};
soc {
        rcc: rcc@40023800 {
                #clock-cells = <2>;
                compatible = "st,stm32f42xx-rcc", "st,stm32-rcc";
                reg = <0x40023800 0x400>;
                clocks = <&clk_hse>, <&clk_i2s_ckin>;
                st,syscfg = <&{/soc/pwrcfg@40007000}>;
        };
        usart1: serial@40011000 {
                compatible = "st,stm32-usart", "st,stm32-uart";
                reg = <0x40011000 0x400>;
                interrupts = <37>;
                clocks = <&rcc 0
                        STM32F4_APB2_CLOCK(USART1)>;
                status = "disabled";
        };
        pwrcfg: power-config@40007000 {
                compatible = "syscon";
                reg = <0x40007000 0x400>;
        };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES - STM32F429.DTSI PLATFORM DEVICES, CLOCK ROUTING

```
/ {
    soc {
        i2c3: i2c@40005c00 {
            compatible = "st,stm32f4-i2c";
            reg = <0x40005c00 0x400>;
            interrupts = <72>,<73>;
            clocks = <&rcc 0 STM32F4_APB1_CLOCK(I2C3)>;
            #address-cells = <1>;
            #size-cells = <0>;
            status = "disabled";
        };
        spi5: spi@40015000 {
            #address-cells = <1>;
            #size-cells = <0>;
            compatible = "st,stm32-spi";
            reg = <0x40015000 0x400>;
            interrupts = <85>;
            clocks = <&rcc 0 STM32F4_APB2_CLOCK(SPI5)>;
            status = "disabled";
            dmas = <&dma2 3 2 0x30400 0>,<&dma2 4 2 0x30400 0>;
            dma-names = "rx","tx";
        };
    };
};
&systick {
    clocks = <&rcc 1 SYSTICK>;
    status = "okay";
};
```

DEVICE TREE

DEVICE TREE EXAMPLES - STM32F429.DTSI PIN CONTROLLER

```
/ {
    soc {
        pin-controller {
            #address-cells = <1>;
            #size-cells = <1>;
            compatible = "st,stm32f429-pinctrl";
            ranges = <0 0x40020000 0x3000>;
            interrupt-parent = <&exti>;
            pins-are-numbered;
            gpioa: gpio@40020000 {
                gpio-controller;
                #gpio-cells = <2>;
                reg = <0x0 0x400>;epolpier
                clocks = <&rcc 0
                    STM32F4_AHB1_CLOCK(GPIOA)>;
                st,bank-name = "GPIOA";
            };
            i2c3_pins: i2c3@0 {
                pins {
                    pinmux =
                    <STM32F429_PC9_FUNC_I2C3_SDA>,
                    <STM32F429_PA8_FUNC_I2C3_SCL>;
                    bias-disable;
                    drive-open-drain;
                    slew-rate = <3>;
                };
            };
        };
    };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES
STM32F429-DISCO.DTS – BOARD NODES

```
/ {
    model = "STMicroelectronics STM32F429i-DISCO board";
    compatible = "st,stm32f429i-disco", "st,stm32f429";
    chosen {
        bootargs = "root=/dev/mmcblk0p1 rootwait init=/linuxrc";
        stdout-path = "serial0:115200n8";
    };
    memory {
        reg = <0x90000000 0x800000>;
    };
    aliases {
        serial0 = &usart1;
        spi5 = &spi5;
    };
    leds {
        compatible = "gpio-leds";
        red {
            gpios = <&gpiog 14 0>;
         };
        green {
            gpios = <&gpiog 13 0>;
            linux,default-trigger = "heartbeat";
        };
    };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES
STM32F429-DISCO.DTS - I2C BUS, CLK RATE

```
&clk_hse {
        clock-frequency = <8000000>;
};
&i2c3 {
        status = "okay";
        pinctrl-0 = <&i2c3_pins>;
        pinctrl-names = "default";
        stmpe: i2c@41 {
                compatible = "st,stmpe811";
                reg = <0x41>;
                irq-gpio = <&gpioa 15 IRQ_TYPE_EDGE_FALLING>;
                stmpe_touchscreen {
                        compatible = "st,stmpe-ts";
                        st,sample-time = <4>;
                        st,mod-12b = <1>;
                        st,ref-sel = <0>;
                        st,adc-freq = <1>;
                        st,ave-ctrl = <1>;
                        st,touch-det-delay = <2>;
                        st,settling = <2>;
                        st,fraction-z = <7>;
                        st,i-drive = <1>;
                };
        };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES STM32F429-DISCO.DTS – SPI BUS

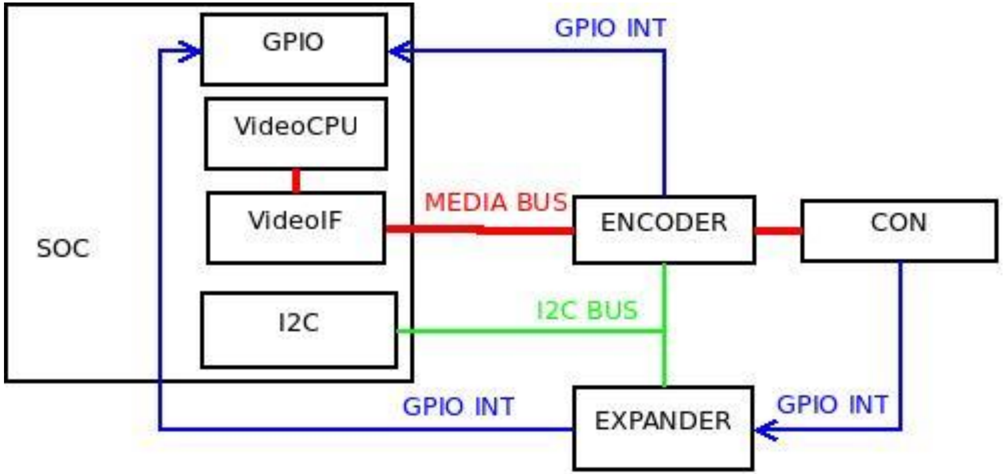
```
&spi5 {
        status = "okay";
        pinctrl-0 = <&spi5_pins_a>;
        pinctrl-names = "default";
        cs-gpios =  <&gpioc 1 1>,
                <&gpioc 2 1>,
                <&gpioa 5 1>;
        spi-max-frequency = <48000000>;
        gyro: spi@0 {
                reg = <0>;
                compatible = "l3gd20";
                spi-max-frequency = <3000000>;
                spi-cpol;
                spi-cpha;
        };
        spidev: spi@1 {
                reg = <1>;
                compatible = "spidev";
                spi-max-frequency = <3000000>;
        };
        sd: spi@2 {
                reg = <2>;
                compatible = "mmc-spi-slot";
                gpios = <&gpiob 4 0>;
                voltage-ranges = <3000 3300>;
                spi-max-frequency = <1000000>;
        };
};
```

DEVICE TREE

DEVICE TREE EXAMPLES
STM32F429-DISCO.DTS – AUDIO, GRAPH

```
sound_card {
        compatible = "audio-graph-card";
        dais = <&sai1a_port>;
};
sai1: sai1@40015800 {
        compatible = "st,stm32h7-sai";
        #address-cells = <1>;
        #size-cells = <1>;
        ranges = <0 0x40015800 0x400>;
        reg = <0x40015800 0x4>;
         sai1a: audio-controller@40015804 {
                compatible = "st,stm32-sai-sub-a";
                reg = <0x4 0x1C>;
                sai1a_port: port {
                        cpu_endpoint: endpoint {
                                remote-endpoint = <&codec_endpoint>;
                                format = "i2s";
                        };
                };
        };
};
audio-codec {
        codec_port: port {
                codec_endpoint: endpoint {
                        remote-endpoint = <&cpu_endpoint>;
                };
        };
};
```

DEVICE TREE EXAMPLES
ADVANCED ROUTING - GRAPH



```
device {
  ...
  ports {
    #address-cells = <1>;
    #size-cells = <0>;

    port@0 {
      ...
      endpoint@0 { ... };
      endpoint@1 { ... };
    };
    port@1 { ... };
  };
};
```

DEVICE TREE EXAMPLES ADVANCED ROUTING – GRAPH

```
/ {
    video@0x40000000 {
        ...
        port {
            video_in: endpoint {
                remote-endpoint = <&dcim_out>;
            };
        };
    };
    dcim@0x50000000 {
        ...
        port@0 {
            dcim_out: endpoint {
                remote-endpoint = <&video_in>;
            };
        };
        port@1 {
            dcim_in: endpoint {
                remote-endpoint = <&codec_out>;
            }
        };
    };
    conn {
        ...
        port {
            conn: endpoint {
                remote-endpoint = <&codec_in>;
            };
        };
    };
    i2c@0x60000000 {
        ...
        expander: expander@0x20 {
            ...
        };
        codec@0x40 {
            ...
            port@0 {
                codec_in: endpoint {
                    remote-endpoint = <&conn>;
                }
            };
            port@1 {
                codec_out: endpoint {
                    remote-endpoint = <dcim_in>;
                };
            };
        };
    };
    gpio: gpio@0x70000000 {
        ...
    };
};
```

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THANK YOU