Politehnica University of Bucharest

Operational Transconductance Amplifier

EDC2 project

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Content

1. Problem

A two-stage Operational Transconductance Amplifer (OTA) with a differential input and a single-ended output, implemented using bipolar transistors, is shown below.

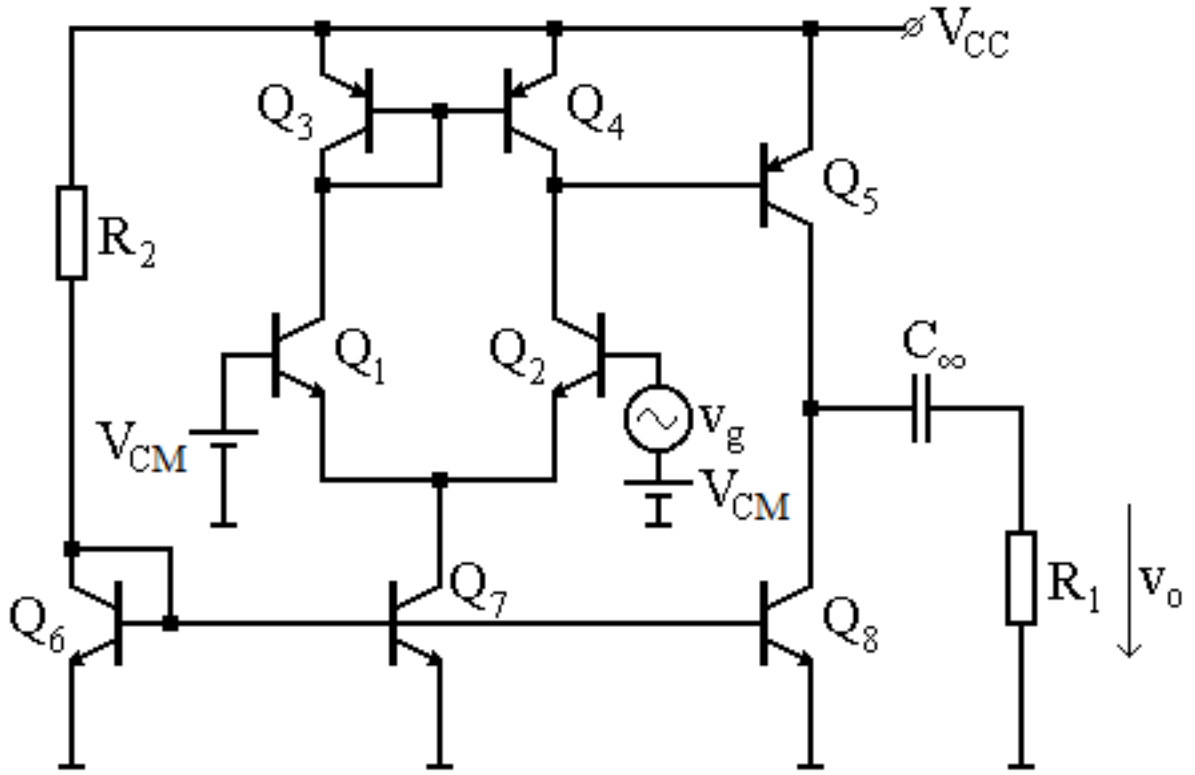
1. Calculate the theoretical expressions of the DC collector currents of bipolar transistors Q1 - Q8, considering V_{BE} ~= 0.6V. Calculate the theoretical expression of the small-signal voltage gain $A_V = V_O/V_g$.

2. Implement the schematic in a circuit simulation software (LTSpice). Design the circuit (i.e. select transistor types for Q1 - Q8, choose a value for R_2 and C_{inf} in order to have a (theoretical) gain value $A_V = 1250$.

3. Simulate the circuit (transient, AC sweep), choosing an appropriate amplitude for V_g in order to minimize output signal distortion.

4. Compare the theoretical AV_v value from point b) with the value obtained from the simulation. Name a possible cause for differences between the two values.

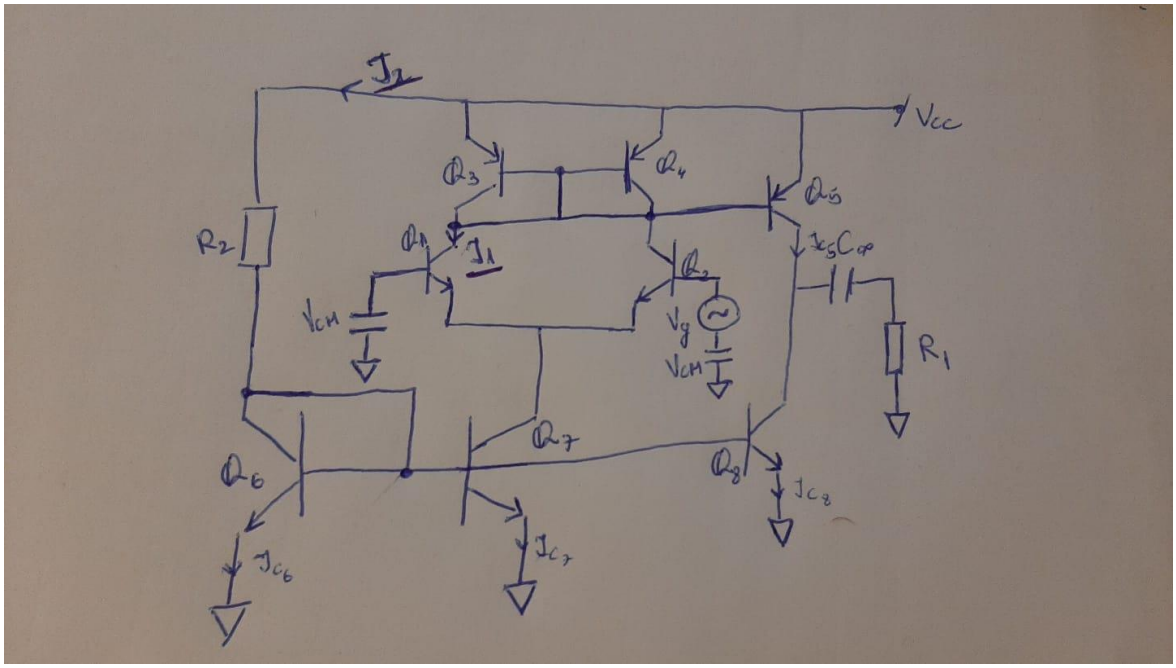
5. Specify a method for decreasing the voltage gain (without changing R_1, R_2, V_{CC} or V_{CM}). Implement the change and re-simulate the circuit in order to demonstrate the effect.



2. DC Circuit

We have the represented scheme in the problem with the intensities I_1 and I_2 taking in consideration that I_2 passes through R_2 and I_1 through Q_1. Q_6, Q_7 and Q_8 being current mirrors with Q_3 and Q_4, the current is passing and is exiting with the same intensity(I_2).

Q_6 – input terminal for the transistors on the buttom. (Q6, Q7 and Q8)



This means that the currents I_1 and I_2 are equal with the same values with the intensities that correspond with the transistors:

$I_1 = I_{C1} + I_{C2} + I_{C3} + I_{C4}$

$I_2 = I_{C5} + I_{C6} + I_{C7} + I_{C8}$

$V_{BE} = V_{CE} = 0.6V$

Writing for the branch from V_{CC} from Q_6 we have then:

$V_{CC} = R_2I_2 + V_{CE} \Rightarrow I_2 = (V_{CC} - V_{CE})/R_2$

Writing for the branch from V_{CC} from Q_7 we have then:

$I_1 = (V_{CC} - V_{CE})/2*R_2$

3. LTSpice simulation

We used at the implementation of the circuit:

NPN transistors: BC847B at Q_1, Q_2, Q_6, Q_7, Q_8

PNP transistors: BC857B at Q_3, Q_4, Q_5

C_{inf} = 1F

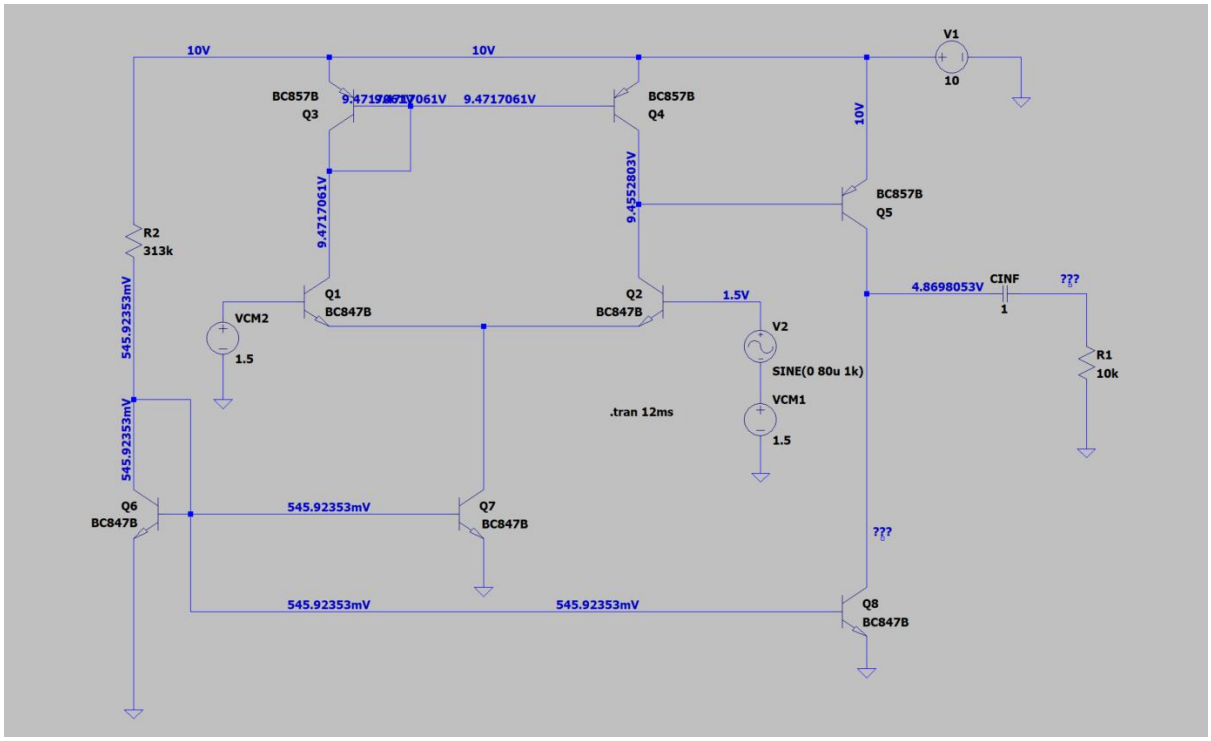
V_{CM} = 1.5V

V_{CC} = 10V

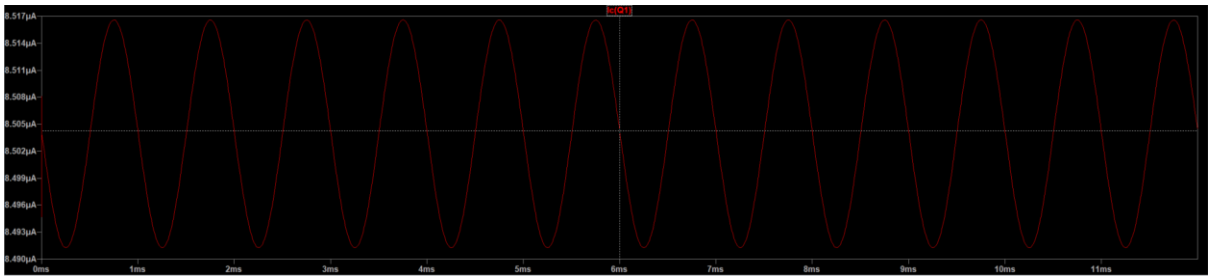
R_1 = 313k

R_2 = 10k

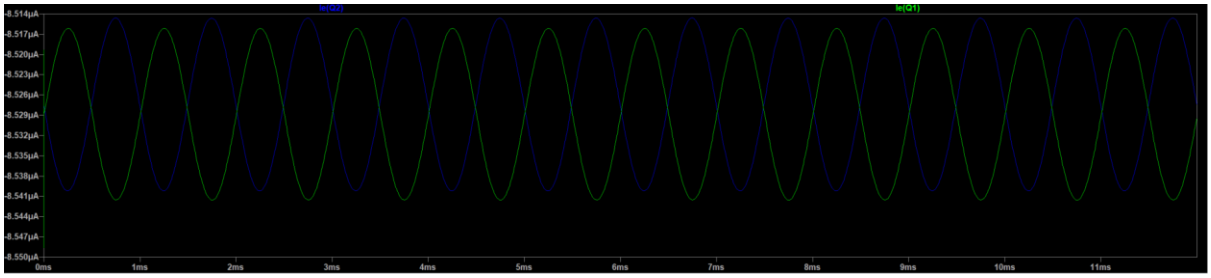
The scheme of the circuit in LTSpice:



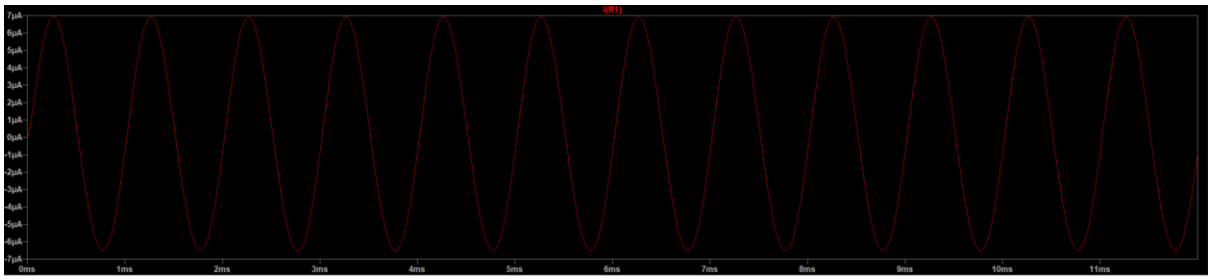
Intensities at Q_1:



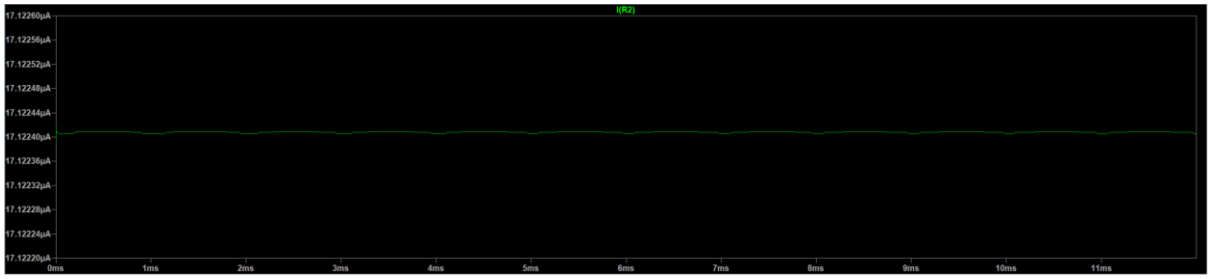
At Q_1 and Q_6:



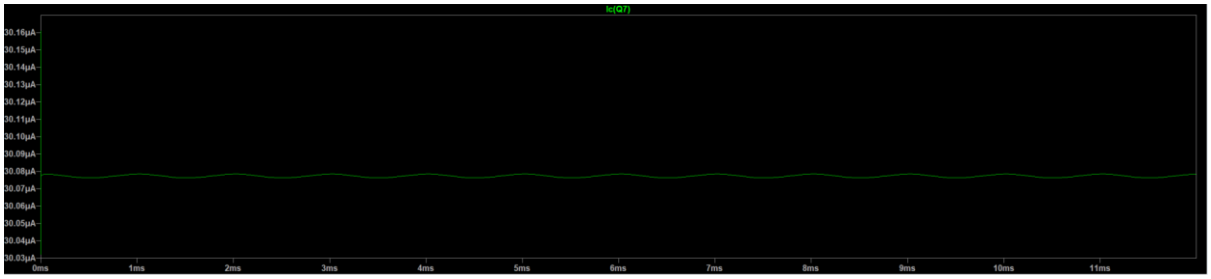
At R_1:



At R_2:



At Q_7:



4. Finding the best Vg

On transient simulation: