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3-Bit Pipeline ADC

Design Project

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336.001 Advanced Integrated Circuit Design SS25

2025-06-02

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Overview

- Introduction
- Specifications
- Principle of Operation
- System-Level Simulation
- Digital Core
- ADC Macro Model
- MDAC Design
- Circuit-Level Simulation

Introduction

- Tools
  - IIC_OSIC_TOOLS Docker container
  - IHP SG13G2 open-source PDK
  - Xschem/ngspice/verilator (analog/mixed-signal simulation)
  - Modelsim (digital simulation)
- Objective
  - Design and simulate a 3-bit pipeline ADC w/ 1.5 bit architecture
  - Mixed-signal/level simulation w/ Xschem/ngspice/verilator
  - Digital core using RTL and gate-level simulation
  - Design CMOS OTA
  - ADC: macro models
  - Switches: ideal

Specifications

- $n = 3\,\text{bit}$
- $n_{1,2} = 1.5\,\text{bit}$
- $n_3 = 1\,\text{bit}$
- $f_\mathrm{s} = 2\,\text{MHz}$
- $V_\mathrm{DD} = 1.5\,\text{V}$
- $V_\mathrm{ref} = V_\mathrm{DD}$

Principle of Operation

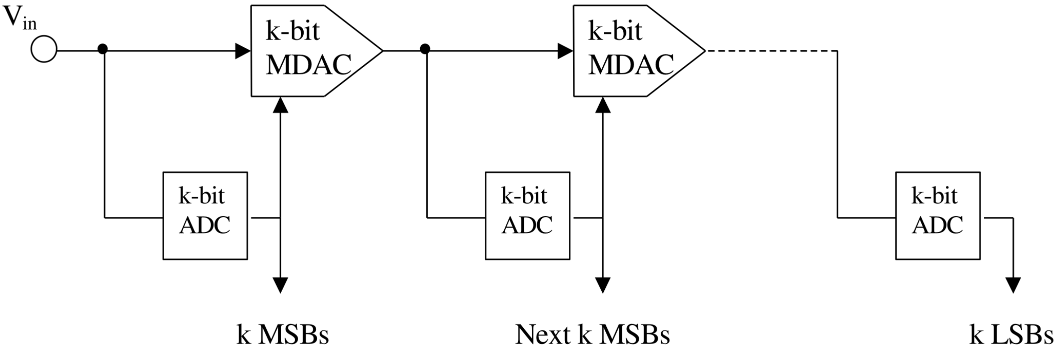


Figure 1: Block diagram.

System-Level Simulation

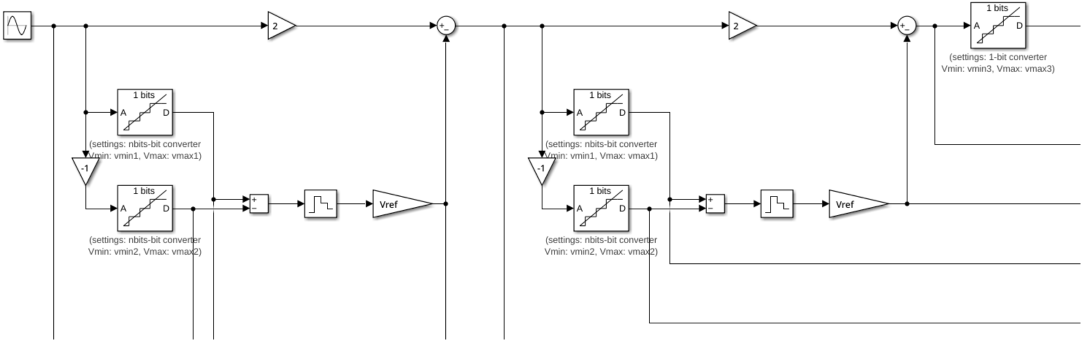

2
2
1 bits
A
D
(settings: 1-bit converter
Vmin: vmin3, Vmax: vmax3)
1 bits
A
D
(settings: nbits-bit converter
Vmin: vmin1, Vmax: vmax1)
-1
1 bits
A
D
(settings: nbits-bit converter
Vmin: vmin2, Vmax: vmax2)
Vref
1 bits
A
D
(settings: nbits-bit converter
Vmin: vmin1, Vmax: vmax1)
-1
1 bits
A
D
(settings: nbits-bit converter
Vmin: vmin2, Vmax: vmax2)
Vref

Figure 2: Simulink model.

System-Level Simulation cont’

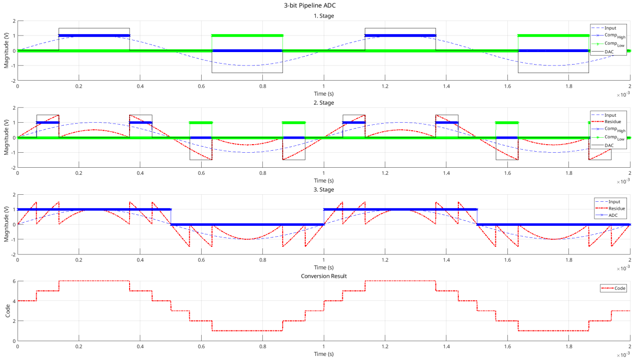


Figure 3: $A_{\text{sig}} = 1\,\text{V}_{\text{peak}}\ f_{\text{sig}} = 1\,\text{kHz}$

3-bit Implementation w/ 1.5-bit Architecture

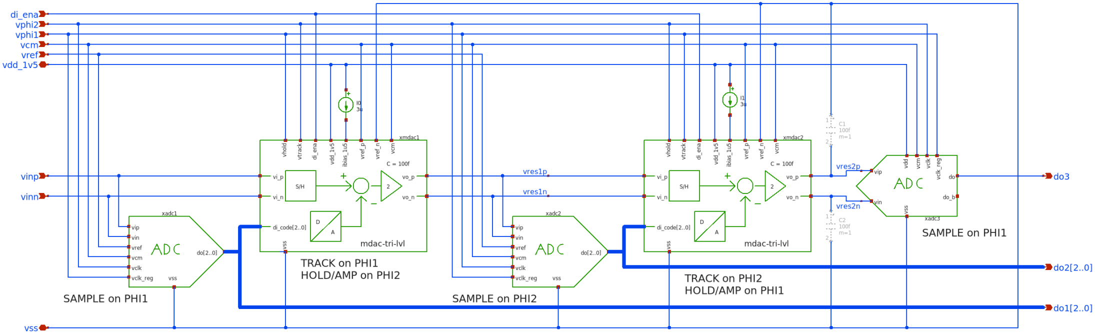


Figure 4: Schematic of ADC core.

Digital Core

- Add ADC outputs from each stage
- RTL simulation using Modelsim and Xschem
- Digital models generated from Ngspice circuits
- HDL (Verilog) used for digital model implementation
- Verilator creates a .so (shared object) file (referenced by Xschem symbol)

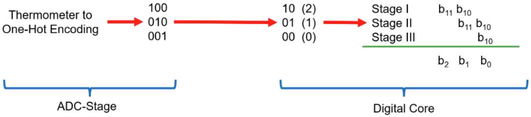
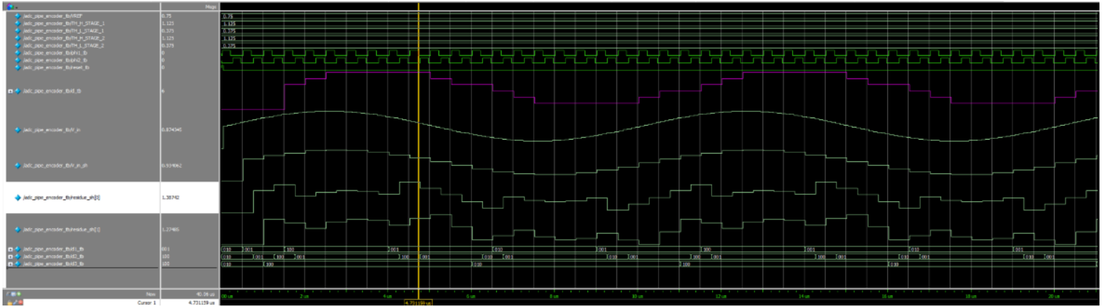


Figure 5: Summation.

Digital Core cont’

- Modelsim simulation



	Msgs
/adc_pipe_encoder_tb/VREF	0.75
/adc_pipe_encoder_tb/TH_H_STAGE_1	1.125
/adc_pipe_encoder_tb/TH_L_STAGE_1	0.375
/adc_pipe_encoder_tb/TH_H_STAGE_2	1.125
/adc_pipe_encoder_tb/TH_L_STAGE_2	0.375
/adc_pipe_encoder_tb/phi1_tb	0
/adc_pipe_encoder_tb/phi2_tb	0
/adc_pipe_encoder_tb/reset_tb	0
/adc_pipe_encoder_tb/d_tb	6
/adc_pipe_encoder_tb/V_in	0.874345
/adc_pipe_encoder_tb/V_in_sh	0.934062
/adc_pipe_encoder_tb/residue_sh[0]	1.38742
/adc_pipe_encoder_tb/residue_sh[1]	1.27465
/adc_pipe_encoder_tb/d1_tb	001
/adc_pipe_encoder_tb/d2_tb	100
/adc_pipe_encoder_tb/d3_tb	100
Now	40.06 us
Cursor 1	4.731159 us

Figure 6: Summation.

Digital Core cont’

- Synthesis using Yosys (generating a xspice-file)
- Target size 100 x 100 µm

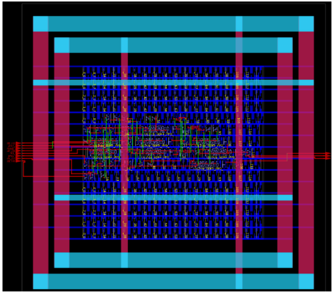
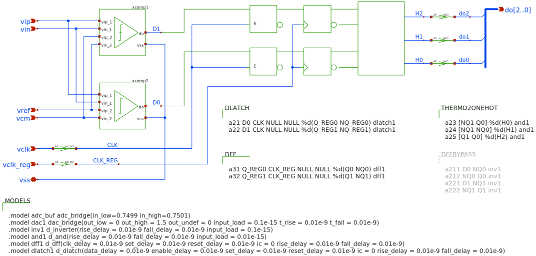


Figure 7: Layout after P&R.

Tri-Level ADC Macro Model

- Ideal comparator implemented using ADC bridges
- Data is latched during vclk and synchronized on the rising edge of vclk_reg
- Use DAC bridges to convert analog signals to digital format



DLATCH

```
a21 D0 CLK NULL NULL %d(Q_REG0 NQ_REG0) dlatch1
a22 D1 CLK NULL NULL %d(Q_REG1 NQ_REG1) dlatch1
```

DFF

```
a31 Q_REG0 CLK_REG NULL NULL %d(Q0 NQ0) dff1
a32 Q_REG1 CLK_REG NULL NULL %d(Q1 NQ1) dff1
```

THERMO2ONEHOT

```
a23 [NQ1 Q0] %d(H0) and1
a24 [NQ1 NQ0] %d(H1) and1
a25 [Q1 Q0] %d(H2) and1
```

DFFBYPASS

```
a211 D0 NQ0 inv1
a212 NQ0 Q0 inv1
a221 D1 NQ1 inv1
a222 NQ1 Q1 inv1
```

MODELS

```
.model adc_buf adc_bridge(in_low=0.7499 in_high=0.7501)
.model dac1 dac_bridge(out_low = 0 out_high = 1.5 out_undef = 0 input_load = 0.1e-15 t_rise = 0.01e-9 t_fall = 0.01e-9)
.model inv1 d_inverter(rise_delay = 0.01e-9 fall_delay = 0.01e-9 input_load = 0.1e-15)
.model and1 d_and(rise_delay = 0.01e-9 fall_delay = 0.01e-9 input_load = 0.01e-15)
.model dff1 d_dff(clk_delay = 0.01e-9 set_delay = 0.01e-9 reset_delay = 0.01e-9 ic = 0 rise_delay = 0.01e-9 fall_delay = 0.01e-9)
.model dlatch1 d_dlatch(data_delay = 0.01e-9 enable_delay = 0.01e-9 set_delay = 0.01e-9 reset_delay = 0.01e-9 ic = 0 rise_delay = 0.01e-9 fall_delay = 0.01e-9)
```

Figure 8: ADC macro model.

MDAC Design

- Sample/Track and hold, k-bit DAC, subtract and amplify

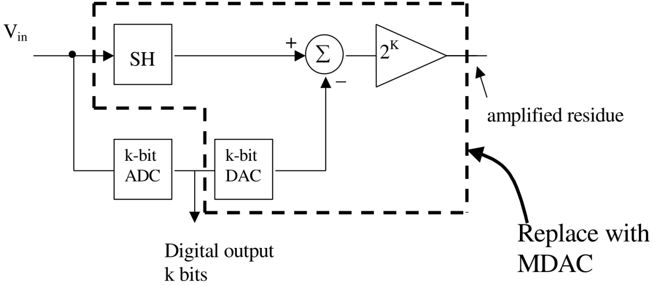


Figure 9: MDAC block diagram.

MDAC Design cont'

- $V_{\text{out}}[n+1] = -2V_{\text{in}}[n] - V_{\text{ref}}[n+1]$

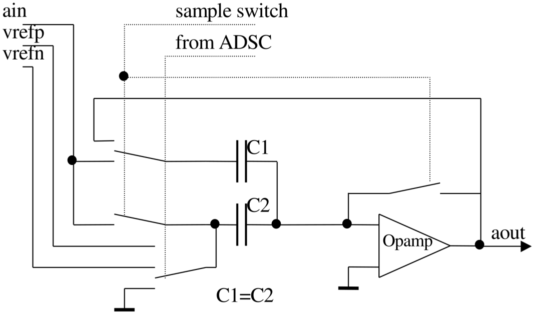


Figure 10: MDAC schematic (single-ended).

MDAC Design cont’

- Fully-differential: invert input to get desired operation

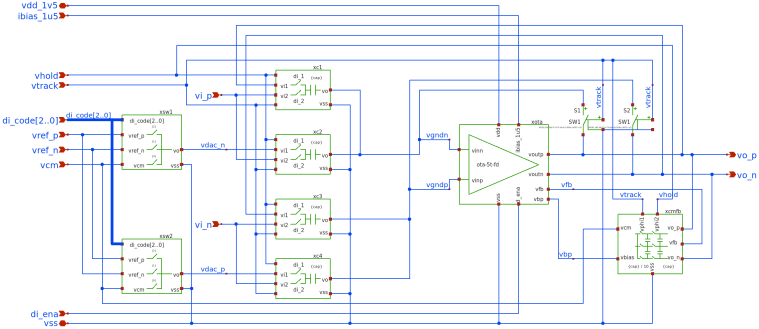


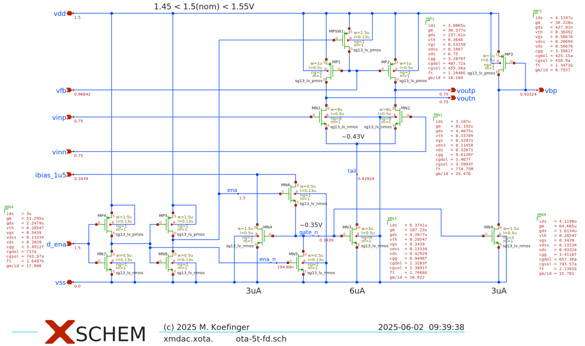
Figure 11: MDAC schematic (fully-differential).

MDAC Design cont’

- $V_o(t) = -V_{step}\frac{1}{\beta}\frac{L_0}{1+L_0}(1 - e^{-t/\tau_o}) \quad \rightarrow \quad \epsilon_d = e^{-t/\tau_o}$
- $\tau_o \approx \omega_{ug}$
- Settling accuracy: $\epsilon_{d,target} = 1/2^{n-n_1} = 2^{-2} = 0.25$
- $T_{settle} = 1/f_s/2$
- $N_{settling} = \frac{T_{settle}}{\tau_o} = -\ln(\epsilon_{d,target}) = 1.4 \quad \rightarrow \quad 2$
- $C_1 = C_2 = 100\,$fF (sufficient in terms of kT/C noise for 3-bit)
- DC gain from static error
- Slew-rate: $\mathrm{SR} = V_{o,step}/T_{settle} = I_d/C_{load}$
- $\rightarrow$ use gm/Id design script for OTA design

MDAC Design cont’

- Keep it simple: basic 5T OTA w/ SC-CMFB (account for additional loading)



```
MP1
ids   = 3.0065u
gm    = 30.377u
gds   = 237.61n
vth   = 0.3646
vgs   = 0.53158
vdss  = 0.1867
vds   = 0.75
cgg   = 3.2878f
cgdol = 407.72a
cgsol = 455.56a
ft    = 1.1646G
gm/id = 10.104
```

```
MP3
ids   = 4.1197u
gm    = 36.228u
gds   = 427.91n
vth   = 0.36492
vgs   = 0.56676
vdss  = 0.20694
vds   = 0.56676
cgg   = 3.3981f
cgdol = 425.15a
cgsol = 456.9a
ft    = 1.3471G
gm/id = 8.7937
```

```
MN1
ids   = 3.187u
gm    = 81.192u
gds   = 4.4675u
vth   = 0.33789
vgs   = 0.32071
vdss  = 0.11458
vds   = 0.32071
cgg   = 9.6128f
cgdol = 3.467f
cgsol = 3.5993f
ft    = 774.75M
gm/id = 25.476
```

```
MN4
ids   = 3u
gm    = 51.295u
gds   = 2.2479u
vth   = 0.28547
vgs   = 0.3439
vdss  = 0.13334
vds   = 0.3439
cgg   = 3.4912f
cgdol = 717a
cgsol = 743.57a
ft    = 1.6487G
gm/id = 17.098
```

```
MN3
ids   = 6.3741u
gm    = 107.23u
gds   = 4.2677u
vth   = 0.28547
vgs   = 0.3439
vdss  = 0.13334
vds   = 0.42929
cgg   = 6.9498f
cgdol = 1.3203f
cgsol = 1.3891f
ft    = 1.7668G
gm/id = 16.822
```

```
MN9
ids   = 4.1198u
gm    = 64.685u
gds   = 1.6134u
vth   = 0.28547
vgs   = 0.3439
vdss  = 0.13334
vds   = 0.93324
cgg   = 3.4118f
cgdol = 657.36a
cgsol = 743.57a
ft    = 2.1391G
gm/id = 15.701
```

Figure 12: 5T-OTA schematic (ac-params annotated)

Circuit Level Simulation

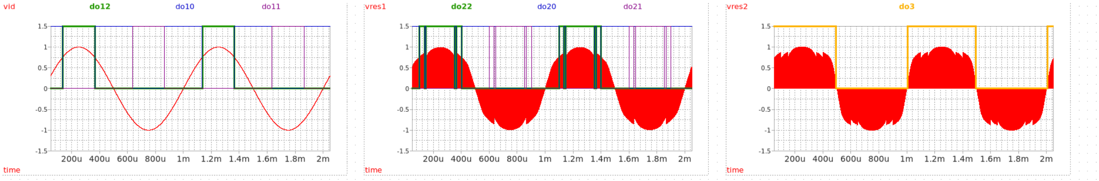


Figure 13: $A_{\text{sig}} = 1\,\text{V}_{\text{peak}}$ $f_{\text{sig}} = 1\,\text{kHz}$

Circuit Level Simulation

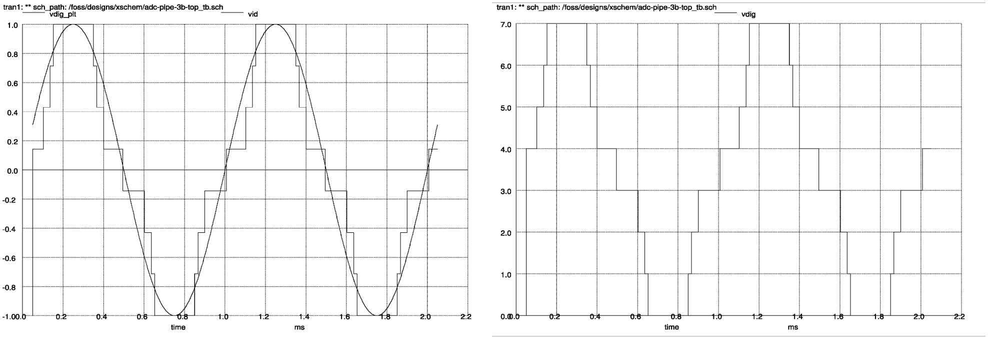


Figure 14: $A_{\mathrm{sig}} = 1\,\mathrm{V_{peak}}$ $f_{\mathrm{sig}} = 1\,\mathrm{kHz}$

Circuit Level Simulation

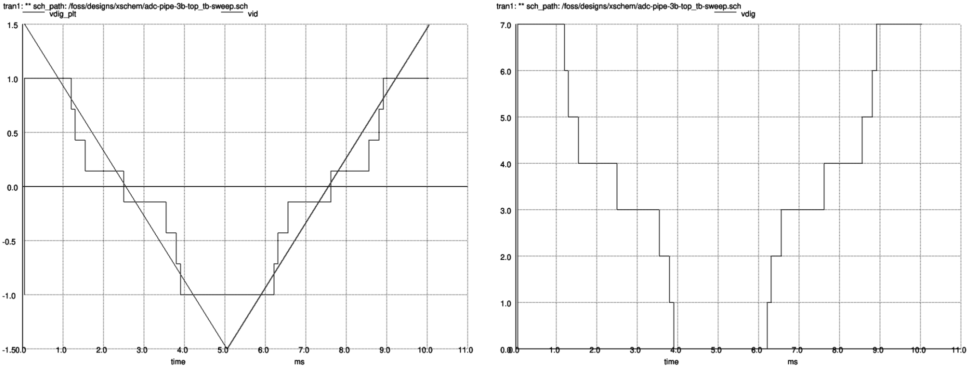


Figure 15: 100 Hz triangle input and scaled code; code only

Summary and Known Issues

- Mixed-signal/level simulation of pipeline ADC was implemented
- Redesign OTA for more gain (different architecture e.g. two-stage, folded-cascode)
- Limitations
  - INL/DNL looks bad, must be calculated
  - ADC macro only handles $\mathrm{f_{sig}} < \mathrm{f_s}/10$ → implement **CMOS comparators**!
- Gain error