

## 21.1.2 Master Mode

When the SPI is configured as a Master (MSTR in SPCR is set), the user can determine the direction of the  $\overline{SS}$  pin.

If  $\overline{SS}$  is configured as an output, the pin is a general output pin which does not affect the SPI system. Typically, the pin will be driving the  $\overline{SS}$  pin of the SPI Slave.

If  $\overline{SS}$  is configured as an input, it must be held high to ensure Master SPI operation. If the  $\overline{SS}$  pin is driven low by peripheral circuitry when the SPI is configured as a Master with the  $\overline{SS}$  pin defined as an input, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a Slave. As a result of the SPI becoming a Slave, the MOSI and SCK pins become inputs.
2. The SPIF Flag in SPSR is set, and if the SPI interrupt is enabled, and the I-bit in SREG is set, the interrupt routine will be executed.

Thus, when interrupt-driven SPI transmission is used in Master mode, and there exists a possibility that  $\overline{SS}$  is driven low, the interrupt should always check that the MSTR bit is still set. If the MSTR bit has been cleared by a slave select, it must be set by the user to re-enable SPI Master mode.