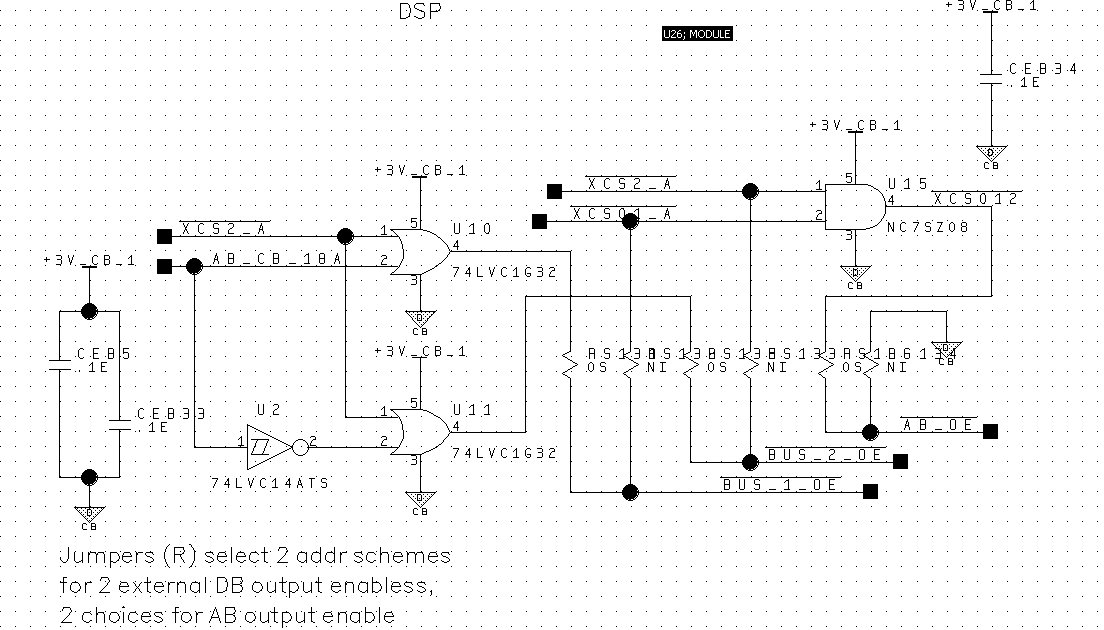
Bus\_Enable\_and\_Address\_Scheme.docx – als0 pins & Addresses for TB3IOMB, below

T:\TS3\_CPLD\_Design\



In TS3CMA, for purposes of experimentation, I provided hardware for 2 separate data busses. And I routed both of them through the inter-module connector to TB3IOMA. In fact I routed both busses into different sets of input pins on TB3IOMA’s FPGA, and I configured it to act as if it were two separate FPGAs.

The 2 different data busses are differentiated by having 2 different output enable signals, ~BUS\_1\_OE and ~BUS\_2\_OE, to enable the output of their respective bus driver chips (SN74LVTH16245). The circuit above shows how the output enable signals are derived from the DSP address bus and external interface signals. This maps our address space like so:

|  |  |  |  |
| --- | --- | --- | --- |
| **Scheme / Option** | **DSP Address Space** | **External Address Space** |  |
| Bus\_1 | 0x08,0000 – 0x0B,FFFF | 0x00,0000 – 0x03,FFFF | XCS2 or AB18 |
| Bus\_2 | 0x0C,0000 – 0x0F,FFFF | 0x04,0000 – 0x07,FFFF | XCS2 or ~AB18 |
|  |  |  |  |
| Bus\_1 optional | 0x00,2000 – 0x00,5FFF | 0x00,2000 – 0x00,5FFF | XCS01 |
| Bus\_2 optional | 0x08,0000 – 0x0F,FFFF | 0x00,0000 – 0x07,FFFF | XCS2 |

In preparing for TB3IOMB, here are some decisions:

(1) I never tried the 2 optional / jumper activated schemes, and it appears we don’t need them. So they can go away.

(2) Bus\_1 scheme works just fine for TBIOMA, so let’s use it for TBIOMB. We won’t run Bus\_2 to TBIOMB. We will reserve Bus\_2 for TBPMB when we get to that.

(3) The CPLD doesn’t see the bus\_output\_enable signal, it acts based on bits 8:18 of the address bus. So, by fiat, lets declare that we use Address\_Bit:18 to select between the CPLD on TBIOM (AB:18=0) and the CPLD on TBPM (AB:18 = 1).

|  |  |  |  |
| --- | --- | --- | --- |
|  | **DSP Addr Space** | **External Addr Space** | **AB18** |
| TBIOMB whole addr. space | 0x08,0000 – 0x0B,FFFF | 0x00,0000 – 0x03,FFFF | 0 |
| Misc J/K Latched outputs | 0x08,0000 – 0x08,FFFF | 0x00,0000 – 0x00,FFFF | 0 |
| TBIOM FPGA1 | 0x09,0000 – 0x09,FFFF | 0x01,0000 – 0x01,FFFF | 0 |
| TBIOMFPGA2 | 0x0A,0000 – 0x0A,FFFF | 0x02,0000 – 0x02,FFFF | 0 |
| Unused address space | 0x0B,0000 – 0x0B,FFFF | 0x03,0000 – 0x03,FFFF | 0 |
|  |  |  |  |
| TBPMB whole addr. space | 0x0C,0000 – 0x0F,FFFF | 0x04,0000 – 0x07,FFFF | 1 |
| Misc J/K Latched outputs | 0x0C,0000 – 0x0C,FFFF | 0x04,0000 – 0x04,FFFF | 1 |
| TBIPM FPGA1 | 0x0D,0000 – 0x0D,FFFF | 0x05,0000 – 0x05,FFFF | 1 |
| TBIPM FPGA2 | 0x0E,0000 – 0x0E,FFFF | 0x06,0000 – 0x06,FFFF | 1 |
| Unused address space | 0x0F,0000 – 0x0F,FFFF | 0x07,0000 – 0x07,FFFF | 1 |
|  |  |  |  |

**J/K Flipflops Latched Output TB3IOMB**

**Set (1) by write, reset (0) by read at specific address**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Schematic  Circuit | CPLD Circuit | Initial Value | CPLD Pin | DSP addr | Ext Addr |  |
| ~RS\_232 | RS\_232 | 0 | 21 | 0x08,0100 | 0x0100 | 1=RS485,0=RS232 |
| ~TX2\_BUF\_ENA | TX2\_BUF\_ENA | 1 | 23 | 0x08,0200 | 0x0200 | Option for RS232 to be driven by DSP SCI or by FPGA.  0=DSP-SCI  1=FPGA  Make F\_TX2 Hi-Z on FPGA2 before enabling DSP-SCI. |
| ~WP\_I2C\_EEPROM | WP\_I2C\_EEPROM | 0 | 29 | 0x08,0300 | 0x0300 | 1=Write Enabled  0 = Write Protected |
| ~EE\_I2C\_CLK\_ENA | EE\_I2C\_CLK\_ENA | 1 | 30 | 0x08,0400 | 0x0400 | 0 = connects EE\_I2C\_CLK\_IO circuit from DSP to EEprom clk input.  1 = use clk from EEprom JTAG connector. |
| ~FPGA1\_RESET | FPGA1\_RESET | 0 | 31 | 0x08,0500 | 0x0500 | ~Reset signal to TBIOM\_FPGA1 |
| ~FPGA2\_RESET | FPGA2\_RESET | 0 | 32 | 0x08,0600 | 0x0600 | ~Reset signal to TBIOM\_FPGA2 |
| ~MISO\_ENA | MISO\_ENA | 1 | 33 | 0x08,0700 | 0x0700 | 0 = DSP reads from SPI device on TB3IOM |
| ~WP\_FLASH\_2 | WP\_FLASH\_2 | 0 | 42 | 0x08,0800 | 0x0800 | 0 = FLASH for FPGA2 is Write Protected |
| ~CS\_FLASH\_1 | CS\_FLASH\_1 | 1 | 44 | 0x08,0900 | 0x0900 | 0 = Chip Select FLASH for FPGA1 |
| ~CS\_FLASH\_2 | CS\_FLASH\_2 | 1 | 45 | 0x08,0A00 | 0x0A00 | 0 = Chip Select FLASH for FPGA2 |
| ~WP\_FLASH\_1 | WP\_FLASH\_1 | 0 | 46 | 0x08,0B00 | 0x0B00 | 0 = FLASH for FPGA1 is Write Protected |
| CPLD\_TP\_0 | CPLD\_TP\_0 | 0 | 52 | 0x08,0C00 | 0x0C00 | Unallocated  (default qualifier) |
| CPLD\_TP\_1 | CPLD\_TP\_1 | 0 | 54 | 0x08,0D00 | 0x0D00 | unallocated  (default qualifier) |
| CPLD\_TP\_2 | CPLD\_TP\_2 | 0 | 55 | 0x08,0E00 | 0x0E00 | Unallocated  (alt. debounced qual) |
| CPLD\_TP\_3 | CPLD\_TP\_3 | 0 | 57 | 0x08,0F00 | 0x0F00 | unallocated  (alt. debounced qual) |
| CPLD\_LED\_0 | CPLD\_LED\_0 | 0 | 76 | 0x08,1000 | 0x1000 | CPLD\_LED\_0  (alt. debounced qual) |
| CPLD\_LED\_1 | CPLD\_LED\_1 | 1 | 64 | 0x08,1100 | 0x1100 | CPLD\_LED\_1  (alt. debounced qual) |
|  |  |  |  |  |  |  |

**Asynch Mux Output**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| ~CS\_FPGA\_1 | CS\_FPGA\_1\_AL | 1 | 47 | 0x09,xxxx | 0x1,xxxx | 0 = Chip Select FLASH for FPGA2 |
| ~CS\_FPGA\_2 | CS\_FPGA\_2\_AL | 1 | 48 | 0x0A,xxxx | 0x2,xxxx | 0 = Chip Select FLASH for FPGA2 |
| CPLD\_SPARE\_0 | (not implemented) | 1 | 76 | 0x0B,xxxx | 0x3,xxxx | QUALIFIER\_02 |
| CPLD\_SPARE\_1 | (not implemented) | 1 | 68 | 0x0B,xxxx | 0x3,xxxx | QUALIFIER\_03 |
| CPLD\_SPARE\_2 | (not implemented) | 0 | 69 | 0x0B,xxxx | 0x3,xxxx | QUALIFIER\_02 |
| CPLD\_SPARE\_3 | (not implemented) | 0 | 71 | 0x0B,xxxx | 0x3,xxxx | QUALIFIER\_03 |

Note, this address scheme was implemented in

T:\Atmel\_WinCUPL\_Proj\ATF1504\_JK\_n\_Mux\_100\ATF1504\_JK\_N\_MUX\_100.PLD

Comments about qualifiers are better explained in comments in the PLD file. Essentially we look at several control signals generated by the DSP’s external bus interface. And you use these to make a time-window during which you look at the address on the address bus. Depending on which control signals you use, you can make that time window a little wider or narrower, or you can move it a little bit forward or back in time. Although I could see the effect on an oscilloscope, it didn’t seem to have any macro effect on the functioning of the DSP / CPLD / FPGA bus system. If at some later date we see or suspect bus problems – maybe if we try to speed up our external bus – if we need to adjust the qualifiers then there are examples and explanations in the CPLD’s source file (ATF1504\_JK\_N\_MUX\_nnn.PLD).