CPLD\_Addr\_and\_Pins.docx

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On TB3CMA, we provided 2 separate Addressing Schemes, and also jumpers for 2 more addressing schemes. In practice the primary Bus\_1 scheme (no jumpers) works just fine. So we will go with that as we move to Rev B.

|  |  |  |  |
| --- | --- | --- | --- |
| **Scheme / Option** | **DSP Address Space** | **External Address Space** |  |
| **Bus\_1** | **0x08,0000 – 0x0B,FFFF** | **0x00,0000 – 0x03,FFFF** | **XCS2 or AB18** |
| Bus\_2 | 0x0C,0000 – 0x0F,FFFF | 0x04,0000 – 0x07,FFFF | XCS2 or ~AB18 |
|  |  |  |  |
| Bus\_1 optional | 0x00,2000 – 0x00,5FFF | 0x00,2000 – 0x00,5FFF | XCS01 |
| Bus\_2 optional | 0x08,0000 – 0x0F,FFFF | 0x00,0000 – 0x07,FFFF | XCS2 |

CPLD Address Usage in DSP Firmware for **TB3IOMA**

|  |  |  |  |
| --- | --- | --- | --- |
|  | DSP addr | Ext Addr |  |
| CPLD\_LED\_1 (latched J/K flip flop output) | 0x080900 | 0x0,0900 | ??  Actually ~MISO\_ENA |
| all 4 test points (non-latched async multiplexor outputs) | 0x08,0000 ,  0x0C,0100,  0x08,0200,  0x0C,0300 | 0x0,0000  0x4,0100  0x0,0200  0x4,0300 | 🗹🗹🗹🗹 |
| CPLD\_LED\_0 | 0x080A00 | 0x0,0A00 | 🗹 |
| CPLD\_LED\_1 | 0x0C0900 | 0x4,0900 | 🗹 |
| CPLD\_LED\_2 | 0x080C00 | 0x0,0C00 | 🗹 |
| CPLD\_LED\_3 | 0x0C0B00 | 0x4,0B00 | 🗹 |
| CS\_IO\_FLSH | 0x080400  CS\_IO\_FLSH\_ALT 0x002400 | 0x0,0400 | 🗹 |
| CS\_IO\_EEPRM | 0x0C0500  CS\_IO\_EEPRM\_ALT 0x080500 | 0x4,0500 | 🗹 |
| MISO\_ENA | 0x0C0800  MISO\_ENA\_ALT 0x080900 | 0x4,0800 | 🗹 |
| EE\_I2C\_WP | 0x080600  EE\_I2C\_WP\_ALT 0x0x002600 | 0x0,0600 | 🗹 |
| F\_DONE\_ENA | 0x0C0700  F\_DONE\_ENA\_ALT 0x080700 | 0x4,0700 | 🗹 |
|  |  |  |  |
| FPGA\_1\_BASE\_ADDR | 0x09,xxxx | 0x1,xxxx | 🗹 |
| FPGA\_2\_BASE\_ADDR | 0x0E,xxxx | 0x6,xxxx | 🗹 |