EGB240 Electronic Design

Assessment 1: PCB Alarm Circuit Design Portfolio

Submitted 5/04/2020

Don Misura Minduwara Kaluarachchi

Executive Summary

This portfolio documents the design for a two-tone buzzer which can be used as a siren or alarm, implemented on a printed circuit board. The design is constructed to the following specifications.

- Power Supply from two AA batteries (3V supply)
- Can be activated using the single pole double throw switch
- Has two frequencies that oscillate between 2.9kHz and 2kHz
- The dimensions of the PCB are 65.45 mm x 32.51 mm

This design is constructed on single sided PCB to reduce costs associated with the design. Examples of applications of this design includes a siren and alarm due to the LEDs and oscillating frequency

Contents

1. Circuit schematic

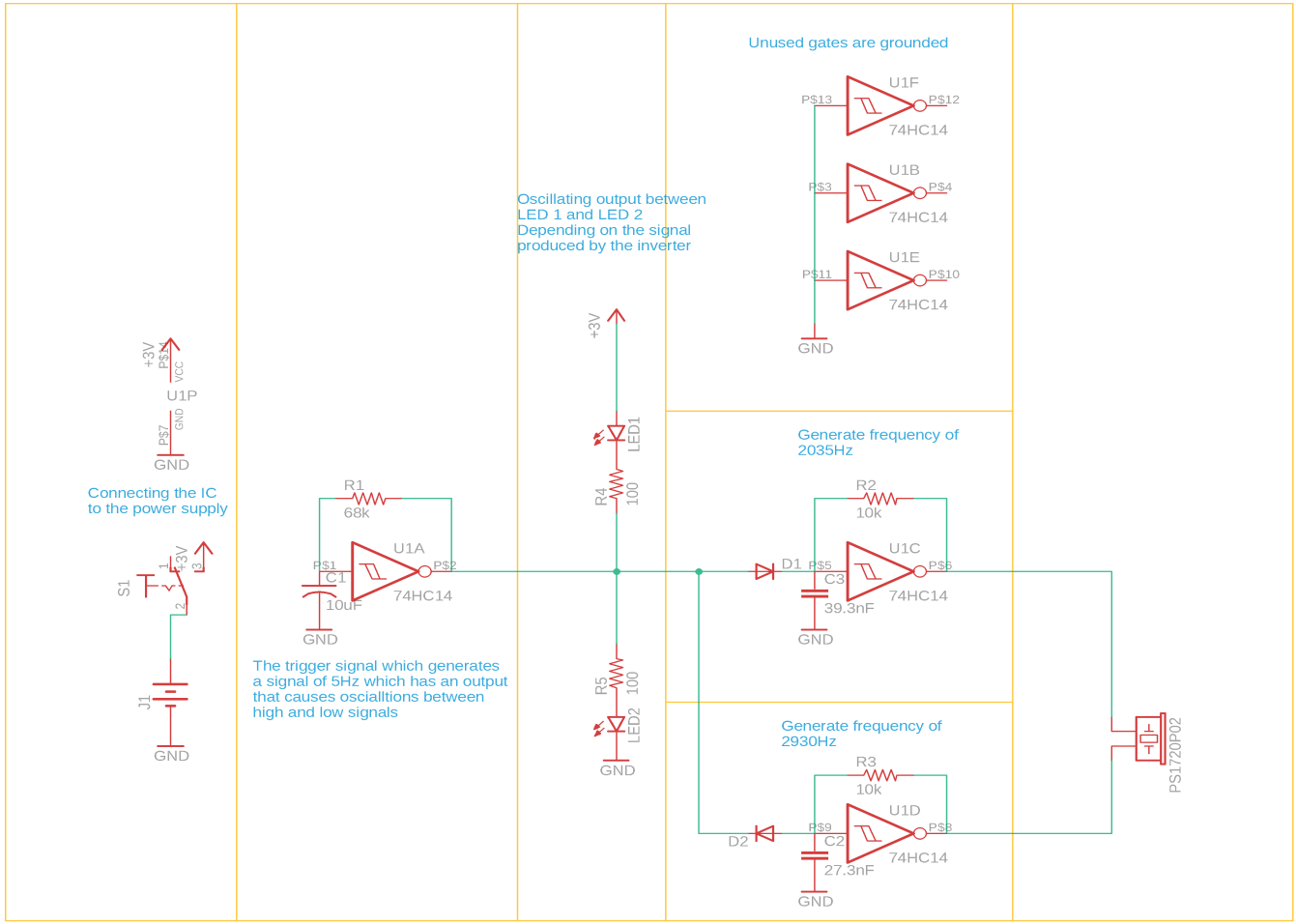


Figure 1 - PCB alarm circuit schematic

2. Summary of design and operation

This design has a few key components which are

- Hex Inverting Schmitt Trigger
- Tone Generator/ Buzzer
- LEDs

Hex Inverting Schmitt Trigger

This design aims to utilize the three gates of the Hex Inverting Schmitt Trigger alongside a resistor and a capacitor to produce relaxation oscillators. The first one acts as a trigger signal which switches between the two frequencies and the other two which produce distinct frequencies that are within the audible range (20 Hz – 20kHz).

Tone Generator/ Buzzer

As shown in the diagram below the optimum frequencies for the buzzer to work are between the ranges of 2000Hz and 2800Hz.

The values of were calculated as follows;

$f = \frac{1}{T} \approx \frac{1}{K*R*C}$ in Hz

$f = \frac{1}{1.25*10k*39.3nF}$ f = 2035Hz

$f = \frac{1}{1.25*10k*27.3nF}$ f = 2930Hz

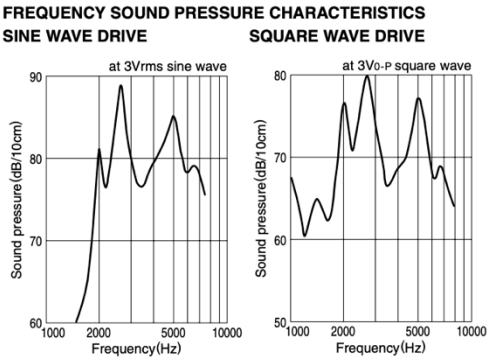
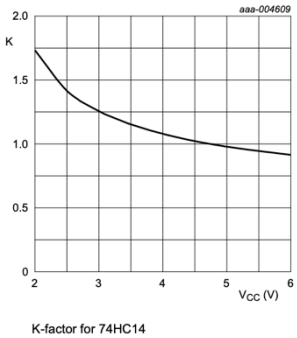


Figure 2A – Plot of sound vs Frequency from PS1720P02 buzzer datasheet



K factor graph for 3V from 74HC14 schmitt trigger IC datasheet

The reason the same value for resistance was chosen as less packs of resistors need to be bought which makes the design more cost effective. During the experimentation phase when a low resistor was used the circuit acted as a voltage divider along with the resistance of the gate, which is why a higher resistor value was chosen

Given the inverse proportionality of resistance and capacitance a smaller capacitance value was used to get the same time constant and frequency.

LEDs

The pair of LEDs light up corresponding to the signal generated which allows to visual evaluate the effectiveness of the circuit. When the output is high (3V) LED 1 will light up and when the output is low (0V)

3. PCB layout

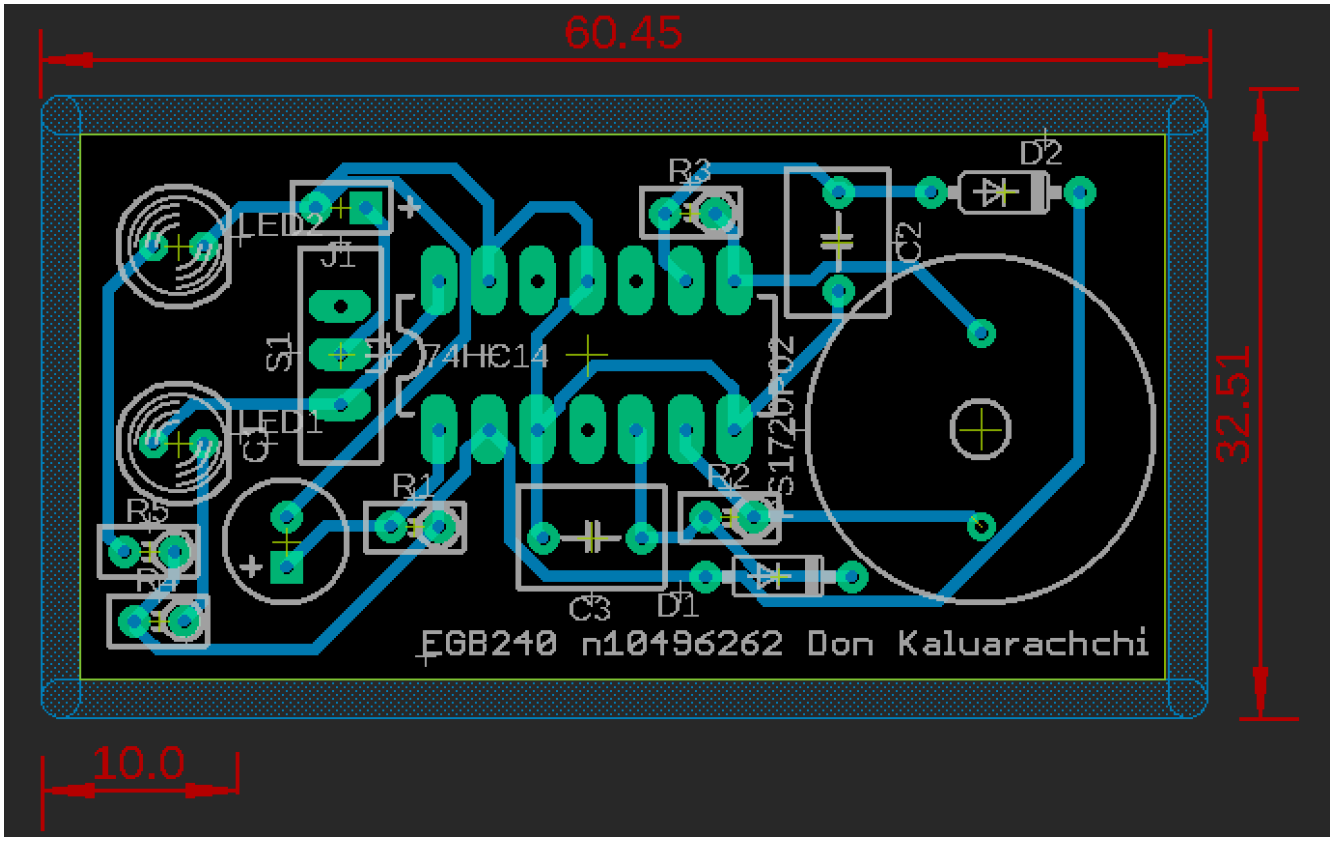


Figure 3 - PCB Layout of alarm circuit (component side view) showing overall board dimensions.

4. Bill of materials

Designator	Value	Description	QTY	Footprint
C1	10u	Capacitor, Polarised, Electrolytic, 10uF 63V, Radial, 2mm Pitch	1	CAP-RB-P2.54-D6.3
C2	27.3n	Capacitor, Polyester, 27.3nF 100V 10%, Greencap, 5mm Pitch	1	CAP-MKT-7.5X5.0-P5.08
C3	39.3n	Capacitor, Polyester, 29.3nF 100V 10%, Greencap, 5mm Pitch	1	CAP-MKT-7.5X5.0-P5.08
J1		Battery holder, 3V, 2xAA, flying leads	1	BATT-3V
S1		Switch, SPDT, Slide, On-On, 0.1” pitch	1	SS-12
R1	68k	Resistor, Axial, Metal film, 68k 1% 0.5W	1	AXIAL-P2.54
R2, R3	10k	Resistor, Axial, Carbon film, 10k 5% 1W	2	AXIAL-P2.54
R4, R5	100	Resistor, Axial, Carbon film, 100ohm 5% 1W	2	AXIAL-P2.54
D1, D2		Zener Diode 1N4739, 9.1V 1W	2	DO35-P7.62
U1	74HC14	IC, Hex inverting Schmitt trigger, DIP-14 ??	1	DIP-14
U1		IC socket, DIP-14	1	DIP-14
LED 1, LED 2		LED – 3mm, Green and Yellow	2	LED5MM (Version 1)
X1		Piezoelectric buzzer	1	PS1720P02

Designator	Manufacturer	MPN	Supplier	SKU	MOQ	Price
C1	Generic	Capacitor, Polarised, Electrolytic, 10uF 63V, Radial, 2mm Pitch	Jaycar	RE-6075	1	$ 0.35
C2	Generic	Capacitor, Polyester, 27.3nF 100V 10%, Greencap, 5mm Pitch	Jaycar	RG-5090	1	$ 0.30
C3	Generic	Capacitor, Polyester, 29.3nF 100V 10%, Greencap, 5mm Pitch	Jaycar	RG-5100	1	$ 0.30
J1	Generic	Battery holder, 3V, 2xAA, flying leads	Jaycar	PH-9202	1	$ 0.95
S1	N KK Switches	SS12SDP4	Digikey	360-2992-ND	1	$ 3.42
R1	Generic	Resistor, Axial, Metal film, 68k 1% 0.5W	Jaycar	RR-0616	8	$ 0.55
R2, R3	Generic	Resistor, Axial, Carbon film, 10k 5% 1W	Jaycar	RR-2798	2	$ 0.48
R4, R5	Generic	Resistor, Axial, Carbon film, 100ohm 5% 1W	Jaycar	RR-2550	2	$ 0.48
D1, D2	Generic	Zener Diode 1N4739, 9.1V 1W	Jaycar	ZR-1409	1	$ 0.65
U1	Texas Instruments	SS12SDP4	Jaycar	ZC-4821	1	$ 1.15
U1	Generic	SN74HC14N	Jaycar	PI-6501	1	$ 0.35
LED 1, LED 2	Generic	LED – 3mm, Green and Yellow	Jaycar	ZD-0122	1	$ 0.75
X1	TDK	PS1720P02	Element14	1669968	1	$ 0.95
				Price		$ 12.08

5. Assembly overlay

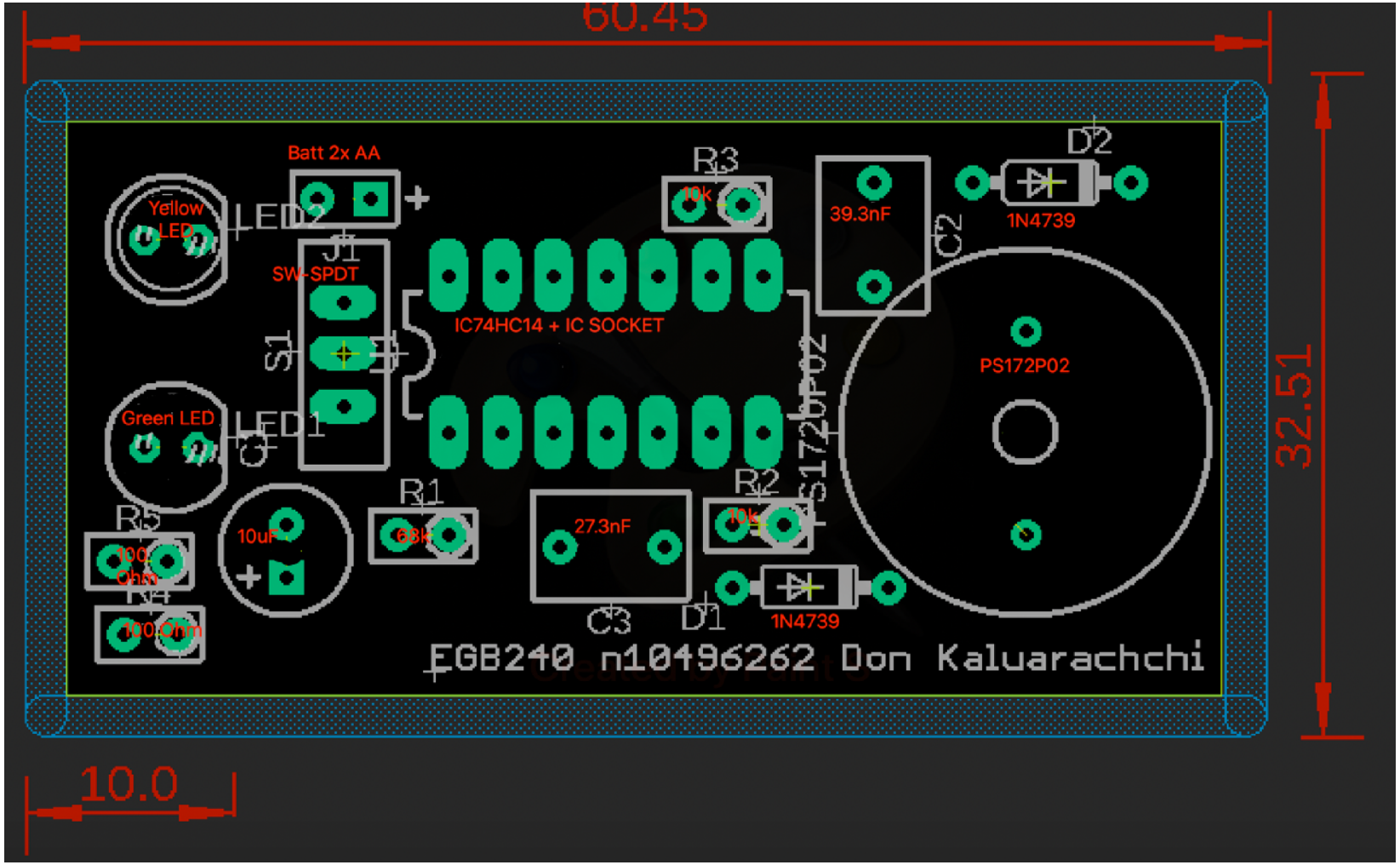


Figure 3 – Assmebly overlay

6. Photos of assembled prototype

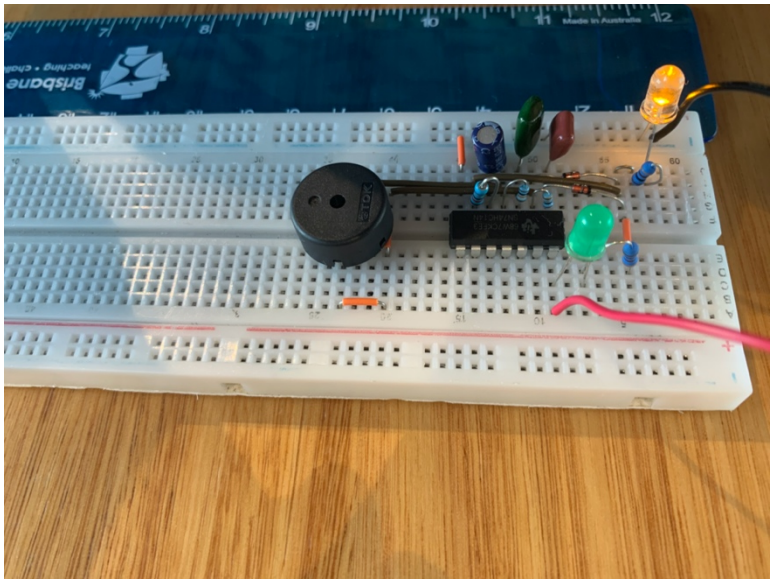


Figure 6A – Circuit prototype on breadboard

3V (red) and 0V (black). Scale in cm.

Yellow(LED 2) flashing.

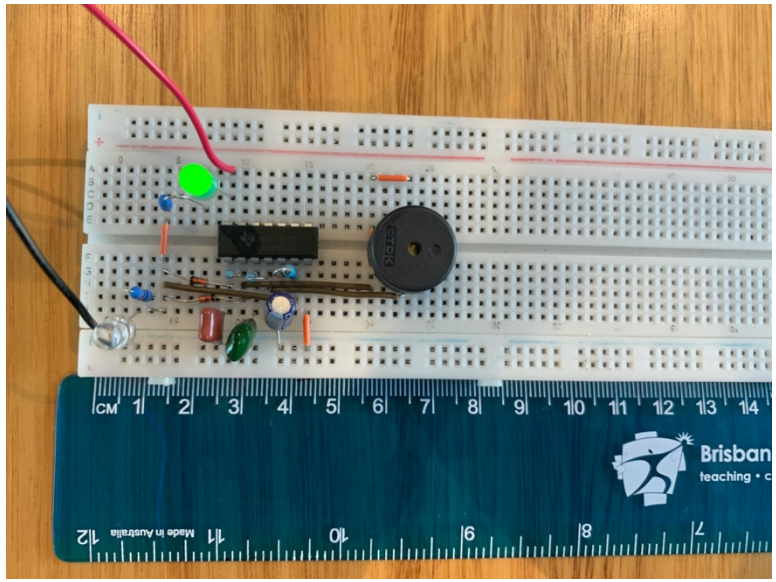


Figure 6B – Top view of prototype on breadboard.

Scale in cm. Green(LED 1) flashing.

7. Simulation circuit and results

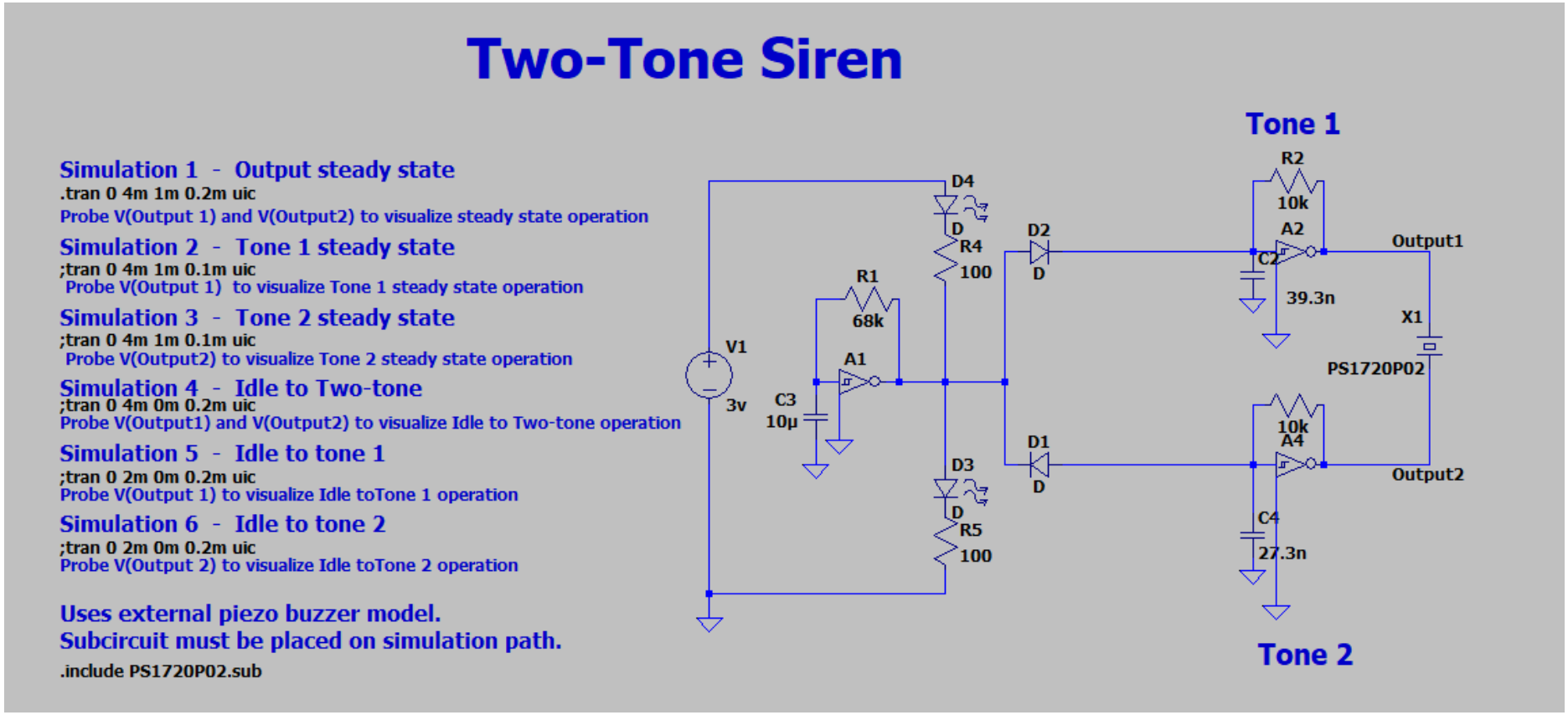


Figure 7 – Circuit Schematic in LTspice

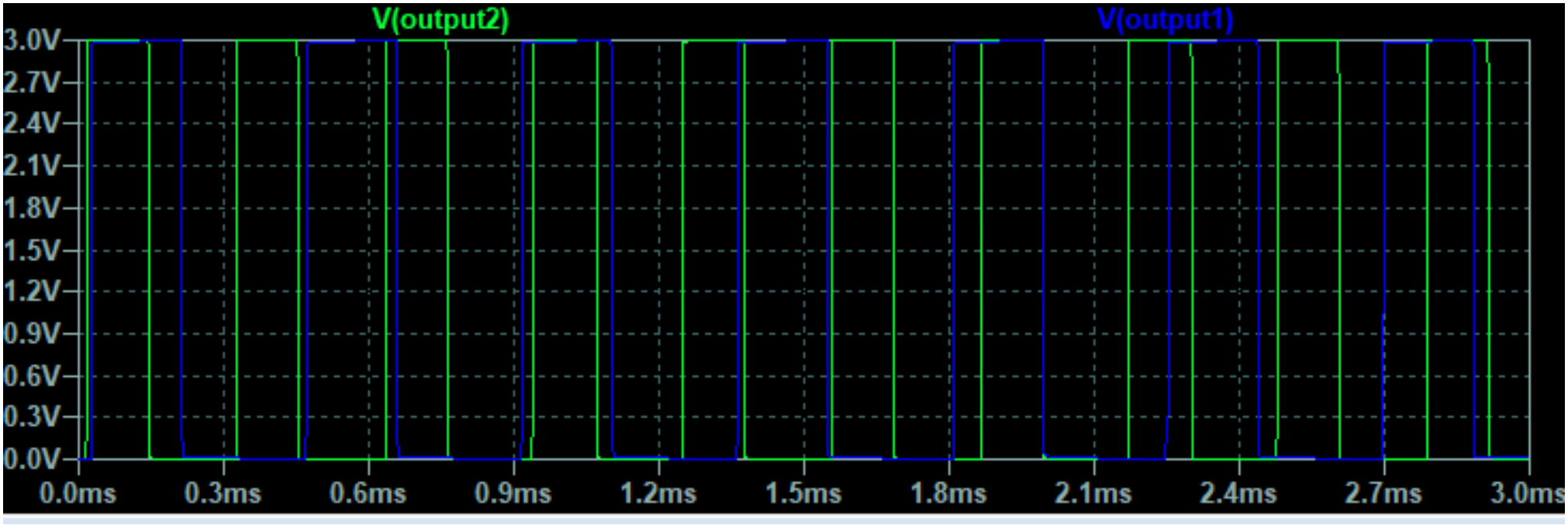
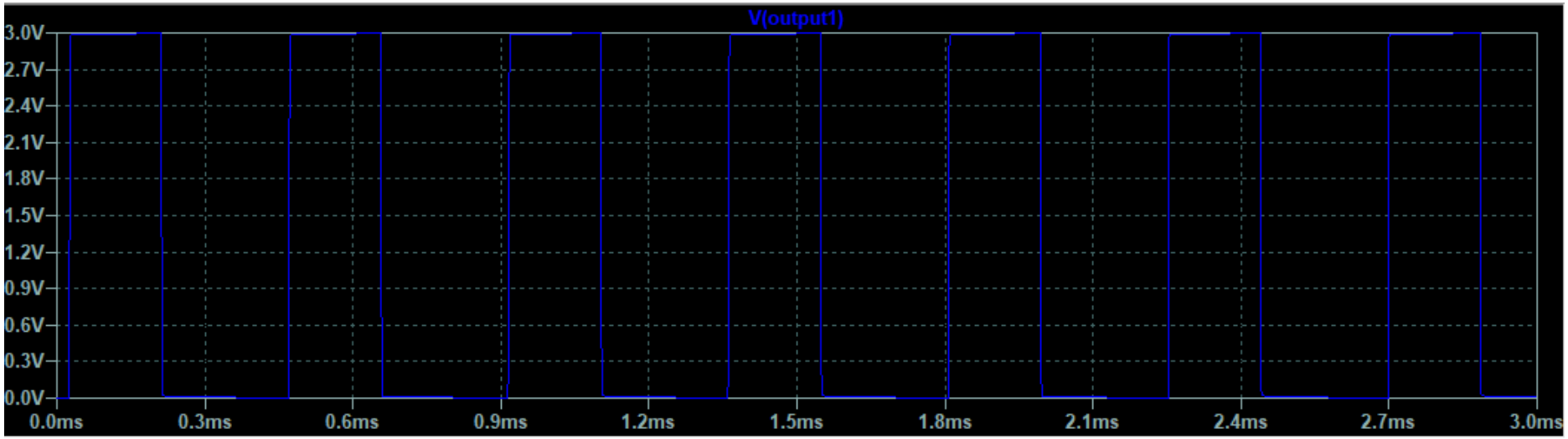


Figure 7A – Simulation 1. Output steady state

Figure 7B – Simulation 2. Tone 1 steady state



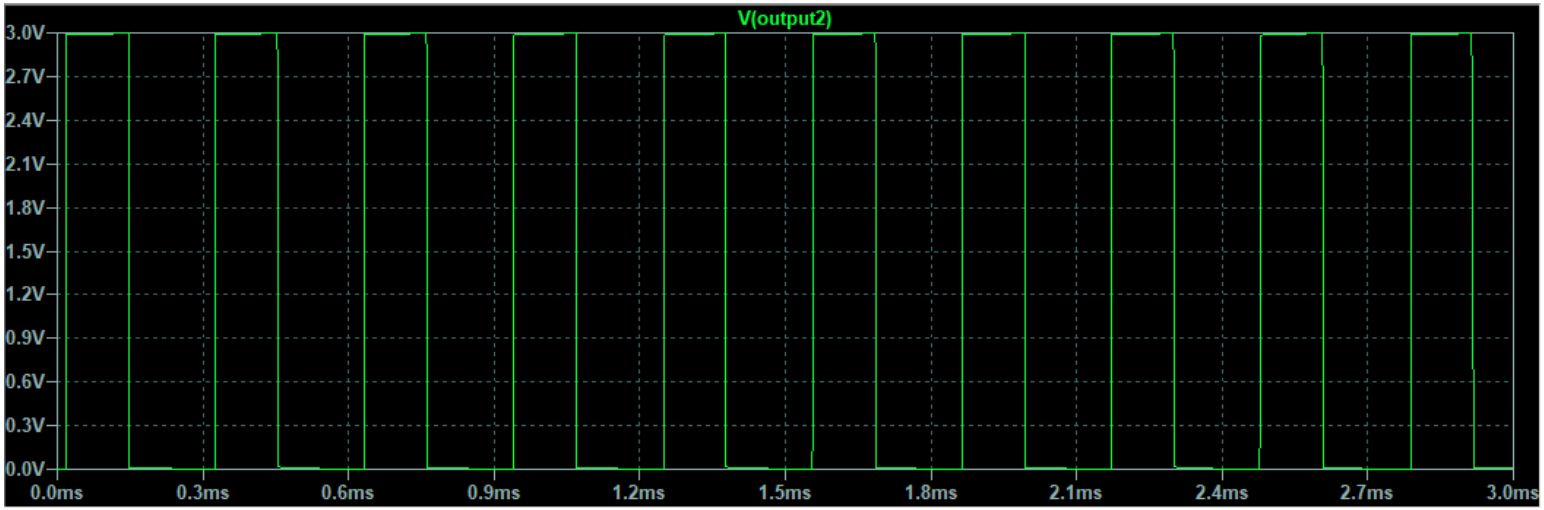


Figure 7C – Simulation 3. Tone 2 steady state

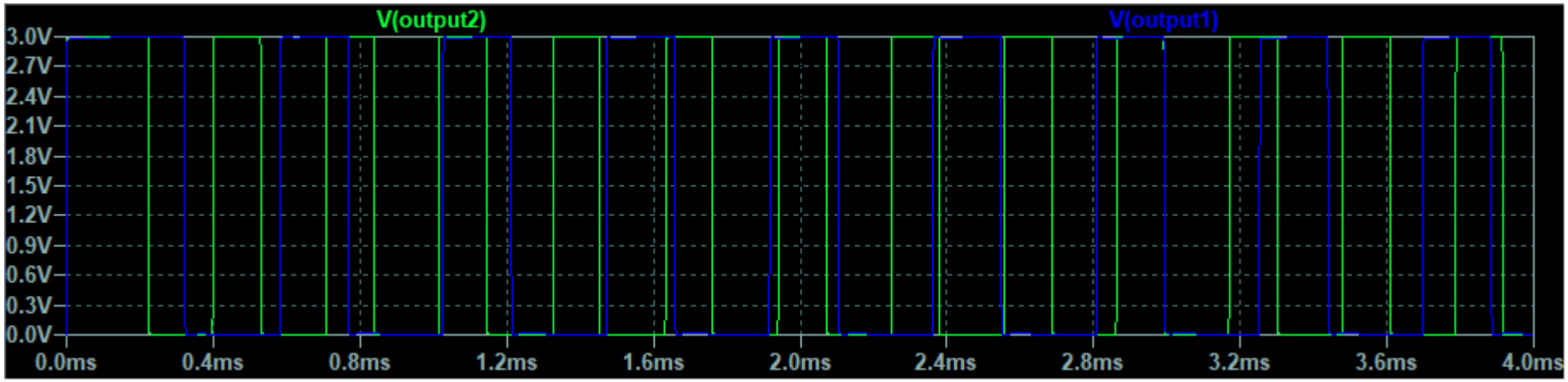


Figure 7D – Simulation 4. Output steady state

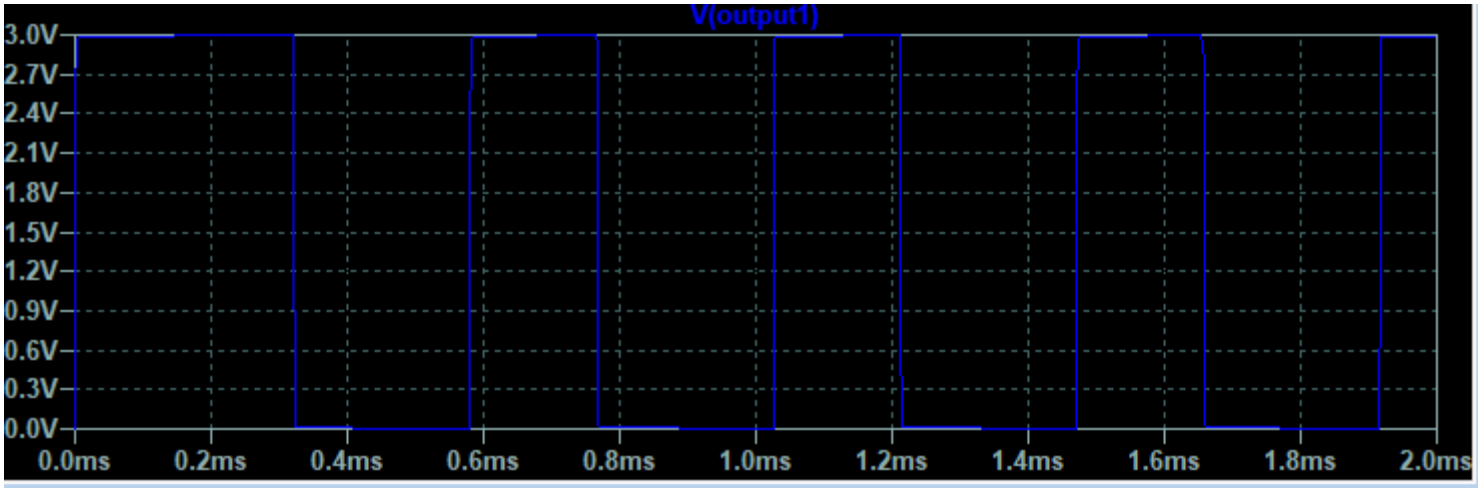


Figure 7E – Simulation 5. Idle to Tone 1

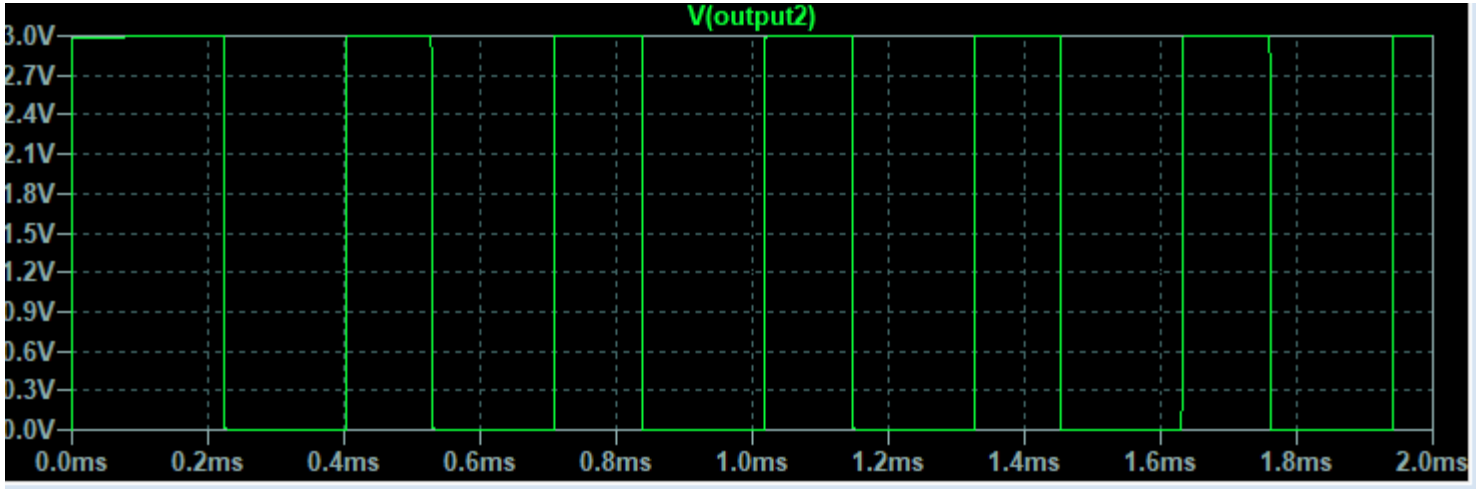


Figure 7F – Simulation 6. Idle to Tone 2

Simualtion mdeol netlist (LTspice)

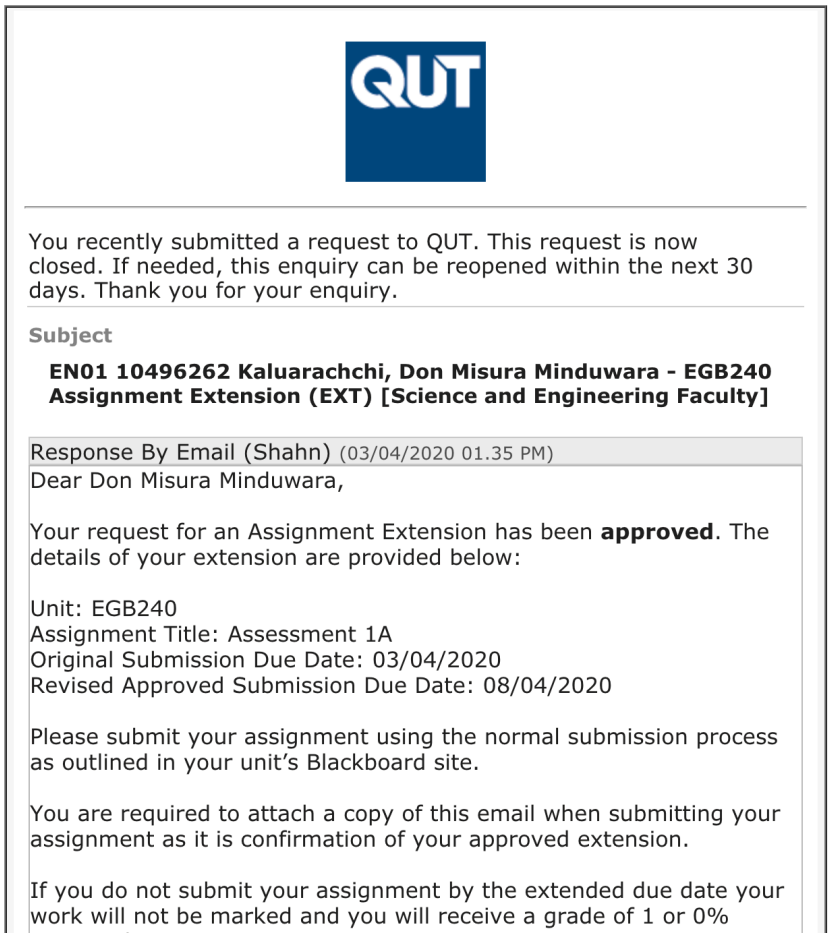
```
* C:\Users\ misurakaluarachchi\Documents\LTspice\misuras_simulation.asc

A1 N004 0 0 0 0 N003 0 0 SCHMITT Vhigh=3 Rhigh=34 Rlow=41 Cout=200p Vt=1.27 Vh=0.4 td=32n
A2 N002 0 0 0 0 Output1 0 0 SCHMITT Vhigh=3 Rhigh=34 Rlow=41 Cout=200p Vt=1.27 Vh=0.4 td=32n
A4 N005 0 0 0 0 Output2 0 0 SCHMITT Vhigh=3 Rhigh=34 Rlow=41 Cout=200p Vt=1.27 Vh=0.4 td=32n
R1 N003 N004 68k
R2 Output1 N002 10k
R3 Output2 N005 10k
D1 N005 N003 D
XX1 Output2 Output1 PS1720P02
C3 N004 0 10µ
C4 N005 0 27.3n
C2 N002 0 39.3n
D2 N003 N002 D
R4 P001 N003 100
R5 P002 0 100
D3 N003 P002 D
D4 N001 P001 D
V1 N001 0 3v

.model D D
.lib C:\Users\misurakaluarachchi\Documents\LTspice\lib\cmp\standard.dio
.include PS1720P02.sub
;tran 0 4m 1m 0.1m uic
.tran 0 4m 1m 0.2m uic
```

```
* Two-Tone Siren
* Simulation 1  -  Output steady state
* Simulation 2  -  Tone 1 steady state
* Simulation 3  -  Tone 2 steady state
* Simulation 4  -  Idle to Two-tone
* Uses external piezo buzzer model.\nSubcircuit must be placed on simulation path.


;tran 0 4m 1m 0.1m uic
;tran 0 4m 0m 0.2m uic

* Simulation 5  -  Idle to tone 1
* Simulation 6  -  Idle to tone 2

;tran 0 2m 0m 0.2m uic
;tran 0 2m 0m 0.2m uic

* Tone 1
* Tone 2
* Probe V(Output 1) and V(Output2) to visualize steady state operation
* Probe V(Output 1)  to visualize Tone 1 steady state operation
* Probe V(Output2) to visualize Tone 2 steady state operation
* Probe V(Output 2) to visualize Idle toTone 2 operation
* Probe V(Output 1) to visualize Idle toTone 1 operation
* Probe V(Output1) and V(Output2) to visualize Idle to Two-tone operation
.backanno
.end
```

8. Experimental results

EN01 10496262 Kaluarachchi, Don Misura Minduwara - EGB240 Assignment Extension (EXT) [Science and Engineering Faculty] [Incident: 200401-001549]

S sef.forms@qut.edu.au
Fri 03/04/2020 09:05
Don Misura Minduwara Kaluarachchi; mark.broadmeadow@qut.edu.au



You recently submitted a request to QUT. This request is now closed. If needed, this enquiry can be reopened within the next 30 days. Thank you for your enquiry.

Subject

EN01 10496262 Kaluarachchi, Don Misura Minduwara - EGB240 Assignment Extension (EXT) [Science and Engineering Faculty]

Response By Email (Shahn) (03/04/2020 01.35 PM)

Dear Don Misura Minduwara,

Your request for an Assignment Extension has been **approved**. The details of your extension are provided below:

Unit: EGB240
Assignment Title: Assessment 1A
Original Submission Due Date: 03/04/2020
Revised Approved Submission Due Date: 08/04/2020

Please submit your assignment using the normal submission process as outlined in your unit's Blackboard site.

You are required to attach a copy of this email when submitting your assignment as it is confirmation of your approved extension.

If you do not submit your assignment by the extended due date your work will not be marked and you will receive a grade of 1 or 0%

Proof of extension request Due to difficulty of current circumstances

You recently submitted a request to QUT. This request is now closed. If needed, this enquiry can be reopened within the next 30 days. Thank you for your enquiry.

Subject

EN01 10496262 Kaluarachchi, Don Misura Minduwara - EGB240 Assignment Extension (EXT) [Science and Engineering Faculty]

Response By Email (Shahn) (03/04/2020 01.35 PM)

Dear Don Misura Minduwara,

Your request for an Assignment Extension has been **approved**. The details of your extension are provided below:

Unit: EGB240
Assignment Title: Assessment 1A

Original Submission Due Date: 03/04/2020
Revised Approved Submission Due Date: 08/04/2020

Please submit your assignment using the normal submission process as outlined in your unit's Blackboard site.

You are required to attach a copy of this email when submitting your assignment as it is confirmation of your approved extension.

If you do not submit your assignment by the extended due date your work will not be marked and you will receive a grade of 1 or 0% against the assessment item.

Kind regards

Student Support Services

Science and Engineering Faculty/ Queensland University of Technology

O Block Podium, Level 3, Gardens Point Campus

Ph 3138 8822 / sef.enquiry@qut.edu.au / www.student.qut.edu.au

CRICOS number 00213J

Please make sure you check your study plan when any amendments or updates have been processed by SEF Student Services. Please inform the faculty immediately of any discrepancy or errors. Remember to check your QUT email address regularly for important faculty correspondence.

Auto-Response By (Administrator) (01/04/2020 08.02 PM)

Hi Don Misura Minduwara,

Thank you for your application for an Assignment Extension. Your enquiry reference number is 200401-001549. Please retain this number for your reference.

If you selected a COVID-19 reason for applying then you will receive a five day extension and do not need to supply any documentation.

If you selected a category other than COVID-19 your application will be processed as normal and will require supporting evidence.

We will aim to process your request within 5 business days.

IMPORTANT NOTE: If you do not receive an outcome from us prior to the assignment due date, please submit the work you have completed with a copy of this receipt attached.

We will not process your request unless supporting documentation is provided. If you did not attach your supporting documentation you have **3 business days** to do so. If no documentation is received after 3 business days your application will be refused.

When providing your supporting documents, please reply and attach to this acknowledgement email.

Information regarding special circumstances, examples of acceptable documentation and guidelines are available on the Special Circumstances page and Late Assignments and Extensions page on HiQ.

If you require further assistance, please contact HiQ .

Kind Regards,

QUT

Customer By CSS Email (Don Misura Minduwara Kaluarachchi) (01/04/2020 08.02 PM)

Assignment extension request

This email confirms the information you submitted online on Wednesday Apr 1 2020 at 20:00:19

Your service request

Student Id	10496262
Student given name	Don Misura Minduwara
Student family name	Kaluarachchi
Student email address	don.kaluarachchi@connect.qut.edu.au
Phone number	94 774424849

Request details

What course is this request for?	EN01 (2) - Bachelor of Engineering (Honours)
What unit is this request for?	EGB240 (2) - Electronic Design
Title of assessment	Assessment 1A Design Documentation and PCB Submission
Is this a group assessment?	No
Lecturer	Dr Mark Broadmeadow

Tutor	Tim Quelch
Due date	03-Apr-2020
Was the application submitted within three days of the assessment due date?	Yes
Reason for concession	COVID-19 self-isolation
Is there any additional information relevant to your request?	Difficulty in accessing resources to complete assessment on time given current circumstances

Declaration

YES, I accept the terms and conditions set out in the declaration on the online form.

Attachments

Supporting documentation

No Attachments

Question Reference # 200401-001549

Date Created: 01/04/2020 08.02 PM
Date Last Updated: 03/04/2020 01.35 PM
Status: Solved

GPO Box 2434 | Brisbane | QLD 4001

CRICOS No 00213J