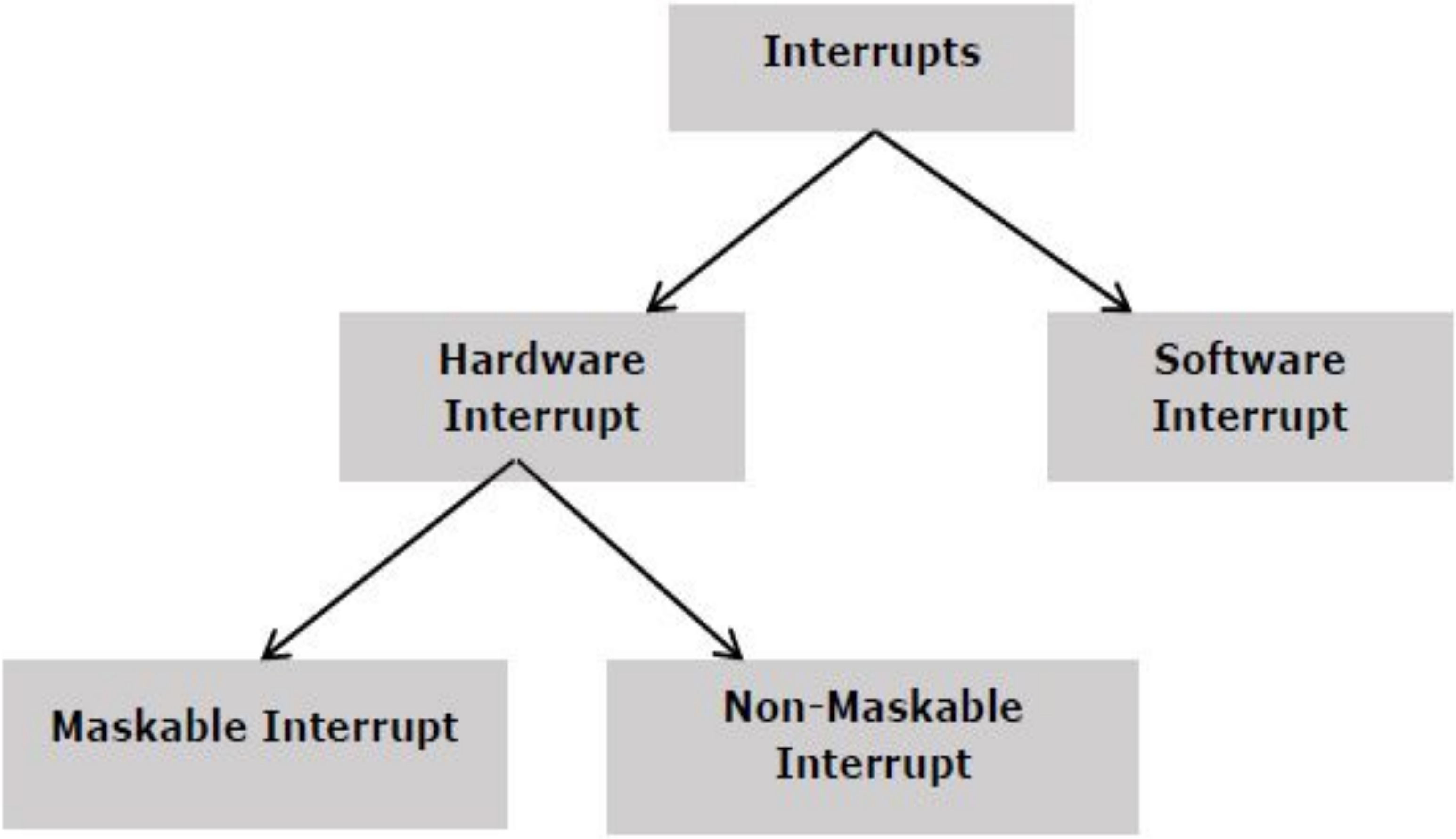
Interrupts

- **Interrupt** is the method of creating a temporary halt during program execution and allows peripheral devices to access the microprocessor.
- The microprocessor responds to that interrupt with an **ISR** (Interrupt Service Routine)

Types of interrupts in 8086 microprocessor



Interrupts

Hardware Interrupt

Software Interrupt

Maskable Interrupt

Non-Maskable Interrupt

Hardware Interrupts

- Caused by any peripheral device by sending a signal through a specified pin
- The 8086 has two hardware interrupt pins, i.e. NMI and INTR
- NMI is a non-maskable interrupt and INTR is a maskable interrupt having lower priority.
- INTA is called interrupt acknowledge.

Hardware Interrupts Contd..

NMI

- Non-maskable interrupt pin (NMI) having higher priority than the maskable interrupt request pin (INTR)

When this interrupt is activated, these actions take place −

- Completes the current instruction that is in progress.
- Pushes the Flag register values on to the stack.
- Pushes the CS (code segment) value and IP (instruction pointer) value of the return address on to the stack.
- IP is loaded from the contents of the word location 00008H.
- CS is loaded from the contents of the next word location 0000AH.
- Interrupt flag and trap flag are reset to 0.

INTR

The INTR is a maskable interrupt because the microprocessor will be interrupted only if interrupts are enabled using set interrupt flag instruction(STI)

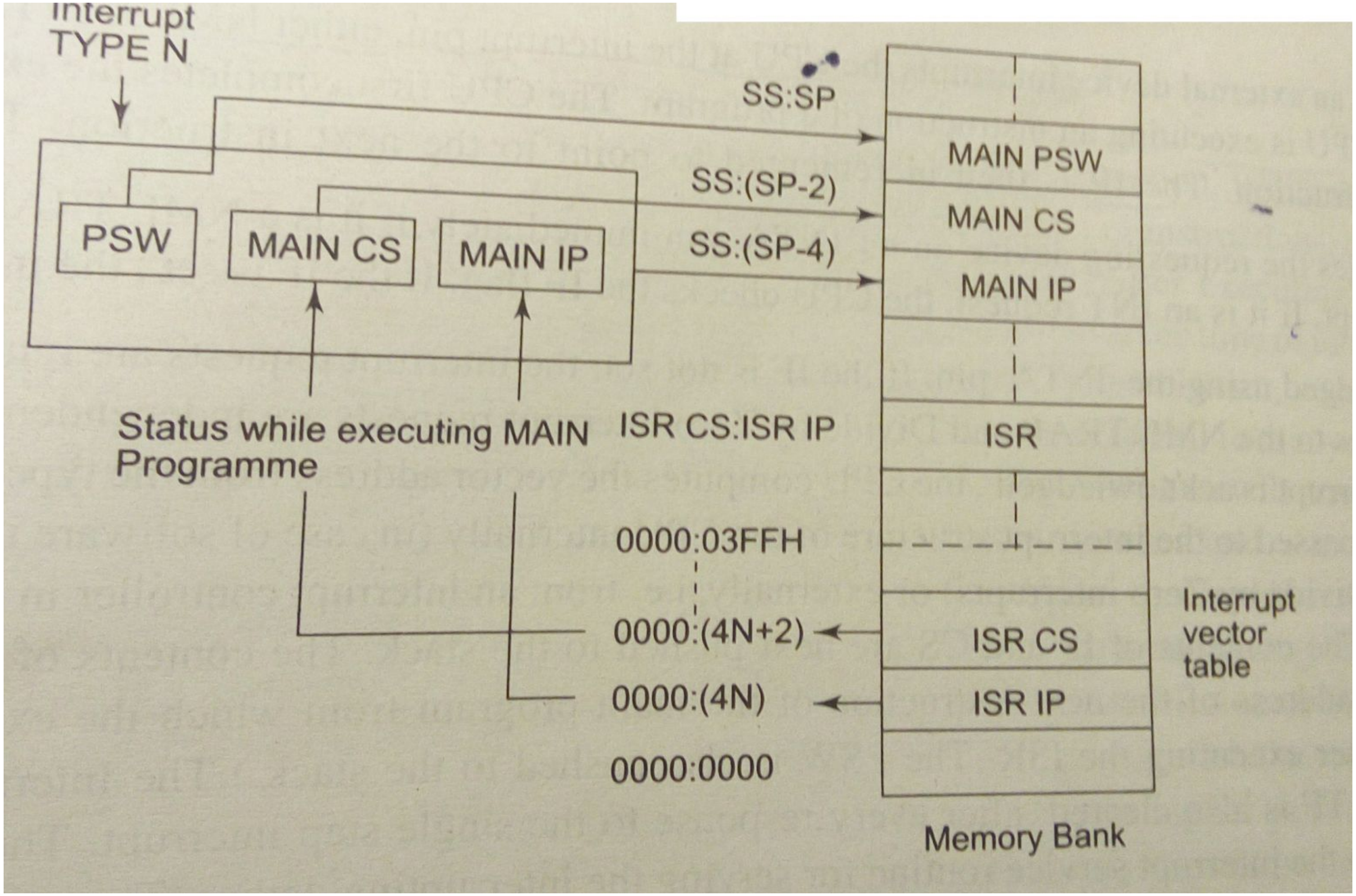
These actions are taken by the microprocessor −

- First completes the current instruction.
- Activates INTA output and receives the interrupt type, say X.
- Flag register value, CS value of the return address and IP value of the return address are pushed on to the stack.
- IP value is loaded from the contents of word location X × 4
- CS is loaded from the contents of the next word location 0000H
- Interrupt flag and trap flag is reset to 0

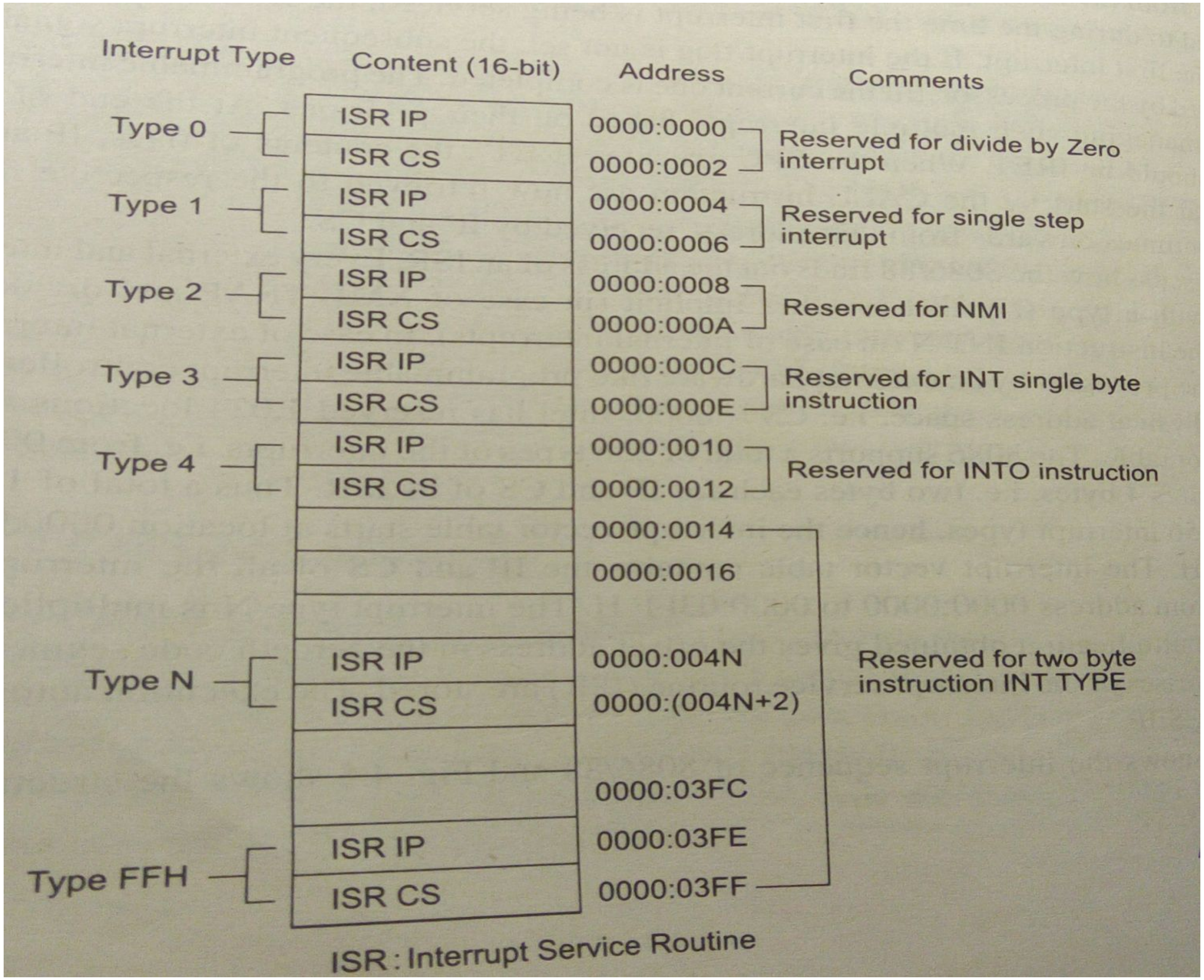
Software Interrupts

- Some instructions are inserted at the desired position into the program to create interrupts
- There are 256 interrupt types under this group.

Interrupt Response Sequence



Structure of Interrupt Vector Table



Interrupt Type	Content (16-bit)	Address	Comments
Type 0	ISR IP	0000:0000	Reserved for divide by Zero interrupt
	ISR CS	0000:0002	
Type 1	ISR IP	0000:0004	Reserved for single step interrupt
	ISR CS	0000:0006	
Type 2	ISR IP	0000:0008	Reserved for NMI
	ISR CS	0000:000A	
Type 3	ISR IP	0000:000C	Reserved for INT single byte instruction
	ISR CS	0000:000E	
Type 4	ISR IP	0000:0010	Reserved for INTO instruction
	ISR CS	0000:0012	
		0000:0014	Reserved for two byte instruction INT TYPE
		0000:0016	
Type N	ISR IP	0000:004N	
	ISR CS	0000:(004N+2)	
		0000:03FC	
Type FFH	ISR IP	0000:03FE	
	ISR CS	0000:03FF	

ISR: Interrupt Service Routine

Interrupts of 8086

- 8086 has 256 types of interrupts
- Type-0 to Type-4 are dedicated for specific functions by INTEL and they are called INTEL predefined interrupts
- Type-5 to Type-31 are reserved by INTEL
- Type-32 to Type-255 are available for the user as hardware or software interrupts

INTEL predefined or dedicated interrupts

1) Divide by zero interrupt(Type-0)

- Implemented as a part of divide instruction
- 8086 automatically do type-0 interrupt
- Non Maskable
- ISR should be stored in m/m
- Address of ISR is stored in IVT

2) Single step(Type-1) interrupt

- Generate when TF=1
- User can write ISR for Type-1 interrupt
- After execution of each instruction, user can halt processor and return control to user
- This feature will be useful to debug a program

- **3) NMI (Type-2) interrupt**

Automatically generate when it receives ***low-to high*** transition on its NMI pin

Used to save program data or status in case of system ac power failure

4) Break point(Type-3) interrupt

- Implement a break point function
- Execute a program partly or up to a desired point and then return control to user
- Useful to debug a program

5) Overflow (Type-4) interrupt

- This interrupt is initiated by the instruction INTO
- Overflow flag will be set

Interrupt priority(high to low)

1)Divide error, INT n, INTO

2)NMI

3)INTR

4)SINGLE STEP

Vectored and Non Vectored Interrupts

- If a program control automatically branches to a specified address when an interrupt signal is accepted by the processor. Such an interrupt is called vectored interrupt
- In non vectored interrupt the interrupting device should supply the address of the ISR to be executed in response to the interrupt
- All the 8086 interrupt are vectored

How 8086 find out the address of an ISR

- Total 1024 bytes are reserved for interrupt vector table
- Each interrupt requires 4 bytes
- IVT contains IP and CS of all interrupts stored sequentially from 0000:0000 to 0000:03FFH
- The interrupt type N is multiplied by 4 and hexadecimal multiplication obtained gives the offset address in the zero th code seg at which the IP and Cs addresses of ISR are stored.

- Question

1) Find out the address of the ISR(IP and CS) in an 8086 MP, if an interrupt occurs in the program like INT 21H.