Module1

CONTENTS

- 8086 Microprocessor

MICROPROCESSOR

- "The integrated circuit which contain all the function of the CPU (Central Processing Unit) of a computer is known as Microprocessor."

- Microprocessor is a multipurpose, clock driven, register based, programmable electronic device that accepts digital data or binary data as input, process it according to instructions stored in its memory and provides results as output

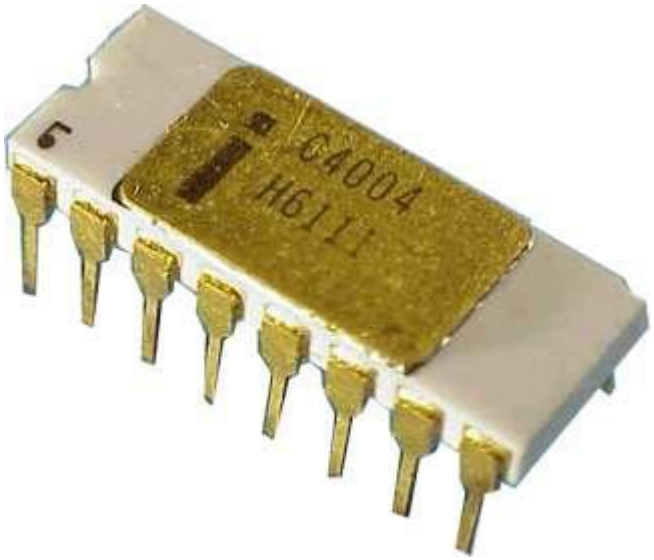
Manufacturers/Designers

- Intel.
- AMD.
- Qualcomm.
- NVIDIA.
- IBM.
- Samsung.
- Motorola.
- Hewlett-Packard (hp)

Evolution of microprocessors

- 4-Bit Microprocessors
- 8-Bit Microprocessors
- 16-Bit Microprocessors
- 32-Bit Microprocessors
- 64-Bit Microprocessors

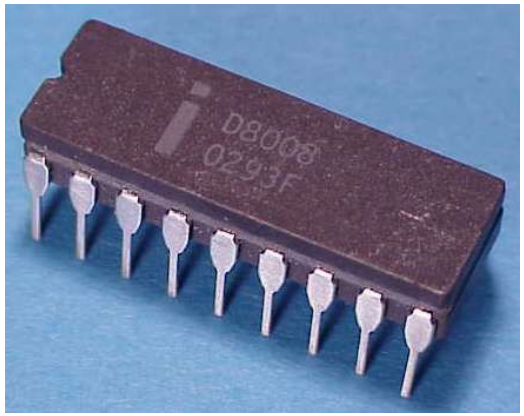
4-BIT MICROPROCESSOR



INTEL 4004

- Introduced in 1971.
- It was the first microprocessor by Intel.
- It was a 4-bit µP.
- Its clock speed was 740KHz.
- It had 2,300 transistors.
- It could execute around 60,000 instructions per second.
- Another eg: INTEL 4040

8-BIT MICROPROCESSOR



INTEL 8008

- Introduced in 1972,first 8-bit µP, clock speed was 500 KHz, could execute 50000 instructions per second.

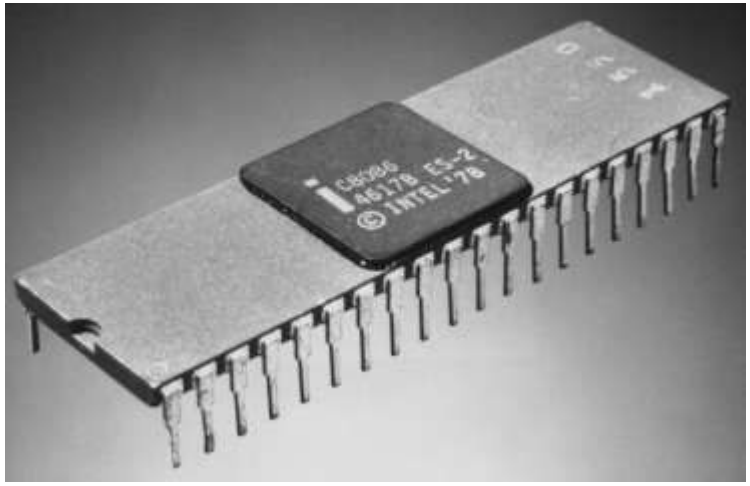
INTEL 8080

- Introduced in 1974,clock speed was 2MHz, 6,000 transistors,10 times faster than 8008. Could execute 5,00,000instructions per second.

INTEL 8085

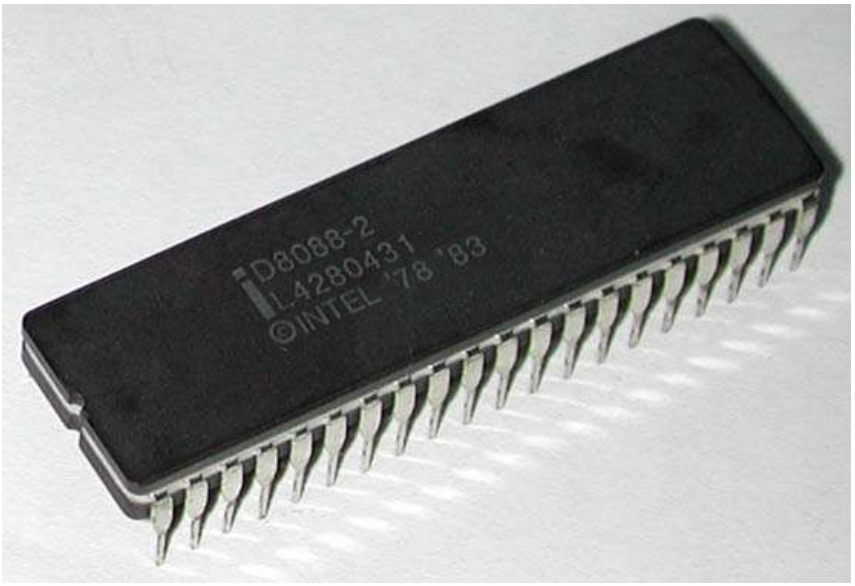
- Introduced in 1976, clock speed was 3 MHz. Its data bus is 8-bit and address bus is 16-bit.
- 6,500 transistors, execute 7,69,230 instructions per second.
- It could access 64 KB of memory.

16-BIT MICROPROCESSORS



INTEL 8086

- Introduced in 1978, clock speed is 4.77 MHz, 8 MHz and 10 MHz, depending on the version.
- Its data bus is 16-bit and address bus is 20-bit.
- It had 29,000 transistors, execute 2.5 million instructions per second.
- It could access 1 MB of memory.



INTEL 8088

- Introduced in 1979.
- It was created as a cheaper
- version of Intel's 8086.
- It was a 16-bit processor with an 8-bit external bus.
- Could execute 2.5 million
- instructions per second.
- This chip became the most popular in the computer industry when IBM used it for its first PC.
- Other eg:80186 & 80188,80286

32-BIT MICROPROCESSORS

INTEL 80386

- Introduced in 1986.
- 32-bit µP, data bus is 32-bit and address bus is 32-bit.
- It could address 4 GB of Memory, 2,75,000 transistors.
- Its clock speed varied from 16MHz to 33 MHz depending upon
- the various versions.
- Different versions:
  - 80386 DX
  - 80386 SX
  - 80386 SL

32-BIT MICROPROCESSORS Contd..

- INTEL 80486, INTEL PENTIUM, PENTIUM PRO, PENTIUM II,PENTIUM II XEON, PENTIUM III, PENTIUM IV, DUAL CORE,

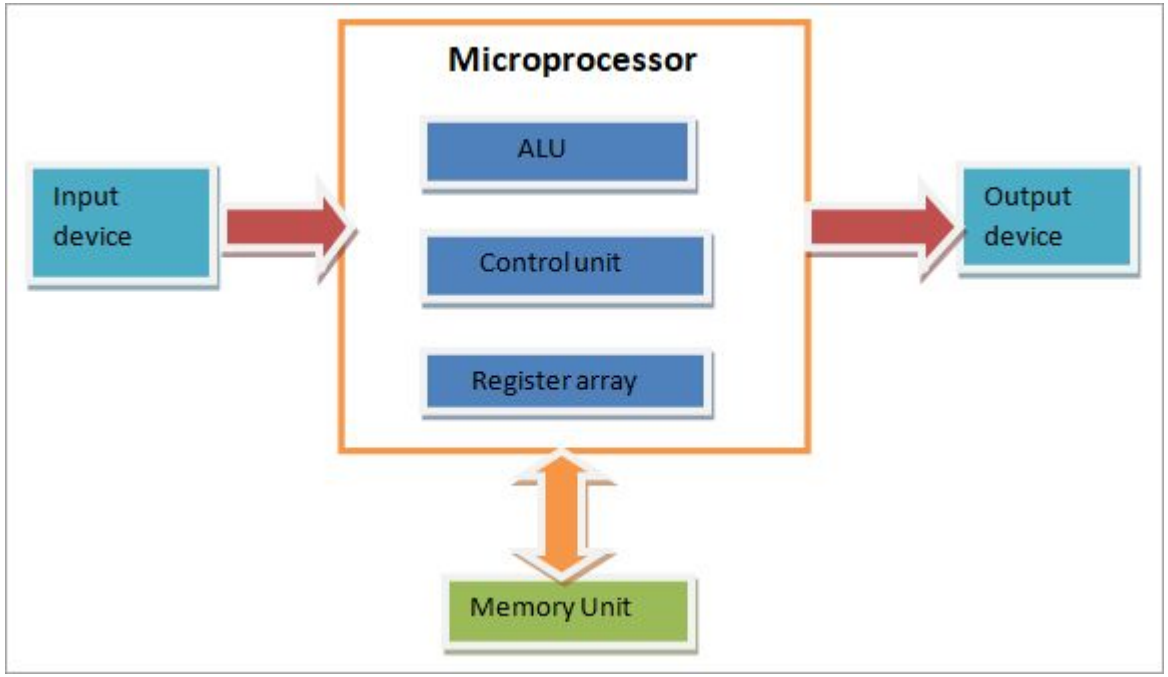
64-BIT MICROPROCESSORS

INTEL CORE 2

- Introduced in 2006.
- clock speed is from 1.2GHz to 3 GHz.
- It has 291 million transistors.
- It has 64 KB of L1 cache per core and 4 MB of L2 cache.
- It is launched in three different versions:
  - Intel Core 2 Duo
  - Intel Core 2 Quad
  - Intel Core 2 Extreme

  Other examples: INTEL CORE I3,I5,I7

Basic components of Microprocessor



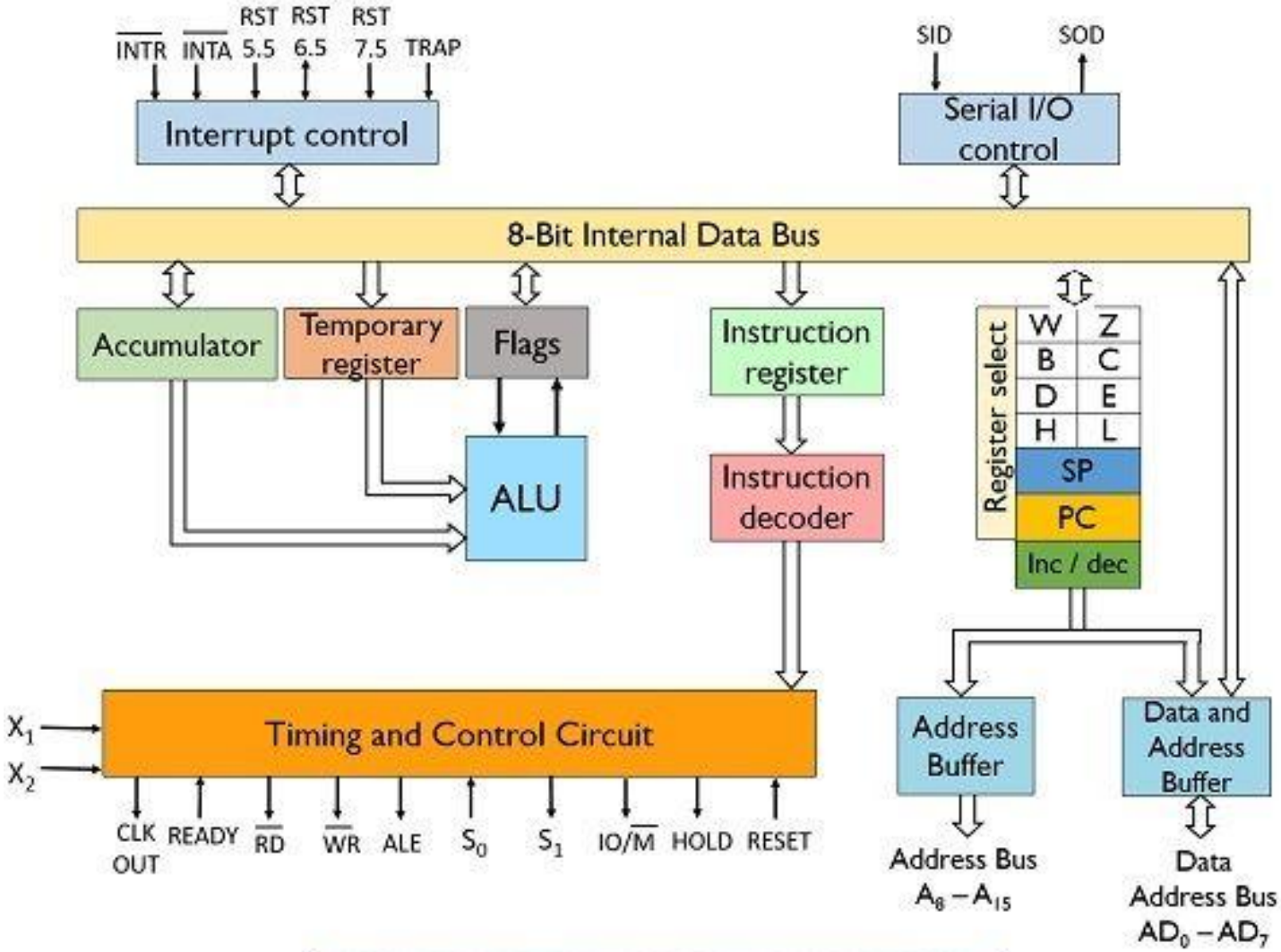
8085 Microprocessor

- It is an 8-bit microprocessor designed by Intel in 1977 using NMOS technology.

It has the following configuration −

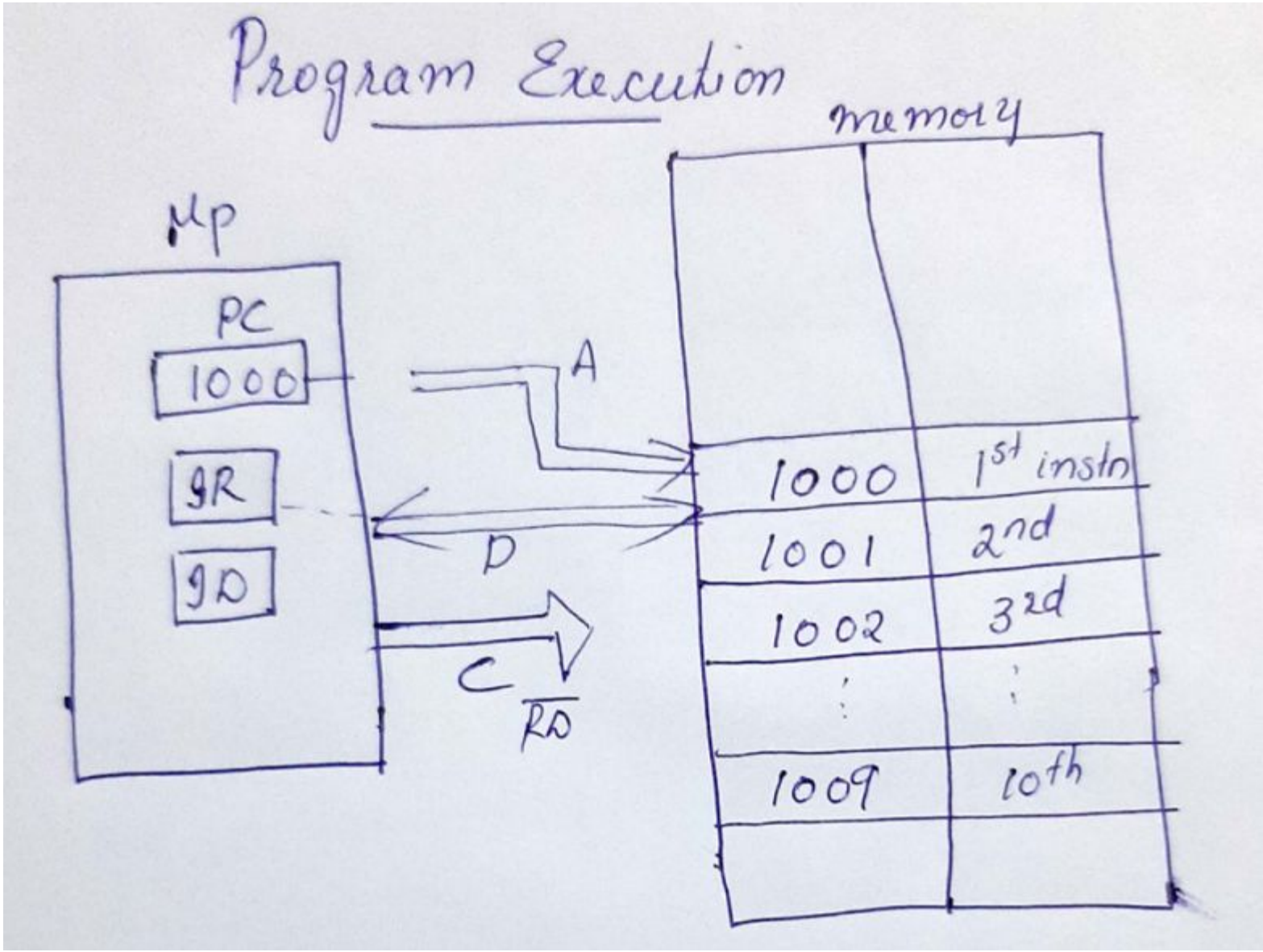
- 8-bit data bus
- 16-bit address bus, which can address upto 64KB
- A 16-bit program counter
- A 16-bit stack pointer
- Six 8-bit registers arranged in pairs: BC, DE, HL
- Requires +5V supply to operate at 3.2 MHZ single phase clock

- It was most commercially successful Processor
- It is used in washing machines, microwave ovens, mobile phones, etc.



Architecture of 8085 Microprocessor

Program Execution



8085 Microprocessor – Functional Units

Accumulator

- It is an 8-bit register used to perform arithmetic, logical, I/O & LOAD/STORE operations. It is connected to internal data bus & ALU.

Arithmetic and logic unit

- As the name suggests, it performs arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.

General purpose register

- There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data.
- These registers can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.

Functional Units (Contd…)

Program counter

- It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.

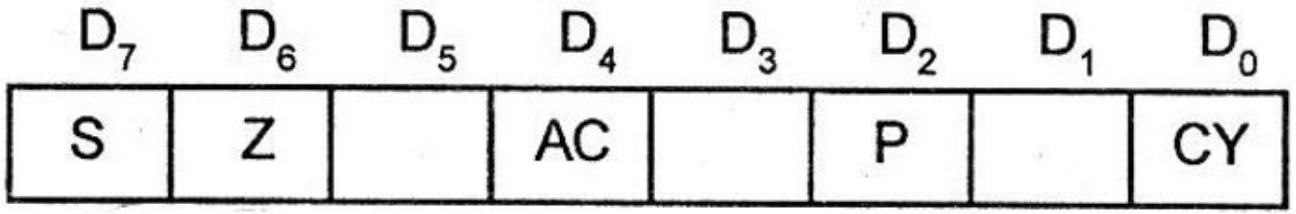
Stack pointer

- It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

Temporary register

- It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.

FLAG REGISTER OF 8085



Flag is an 8-bit register containing 5 1-bit flags:

Sign - set if the most significant bit of the result is set.

Zero - set if the result is zero.

Auxiliary carry - set if there was a carry out from bit 3 to bit 4 of the result.

Parity - set if the parity (the number of set bits in the result) is even.

Carry - set if there was a carry during addition, or borrow during subtraction/comparison.

Instruction register and decoder

- It is an 8-bit register. When an instruction is fetched from memory then it is stored in the Instruction register. Instruction decoder decodes the information present in the Instruction register.

Timing and control unit

- It provides timing and control signal to the microprocessor to perform operations. Following are the timing and control signals, which control external and internal circuits −

Control Signals: READY, RD', WR', ALE

Status Signals: S0, S1, IO/M'

DMA Signals: HOLD, HLDA

RESET Signals: RESET IN, RESET OUT

Interrupt control

- When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program.
- 5 interrupt signals in 8085 microprocessor: INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Serial Input/output control

- It controls the serial data communication by using these two instructions: SID (Serial input data) and SOD (Serial output data).

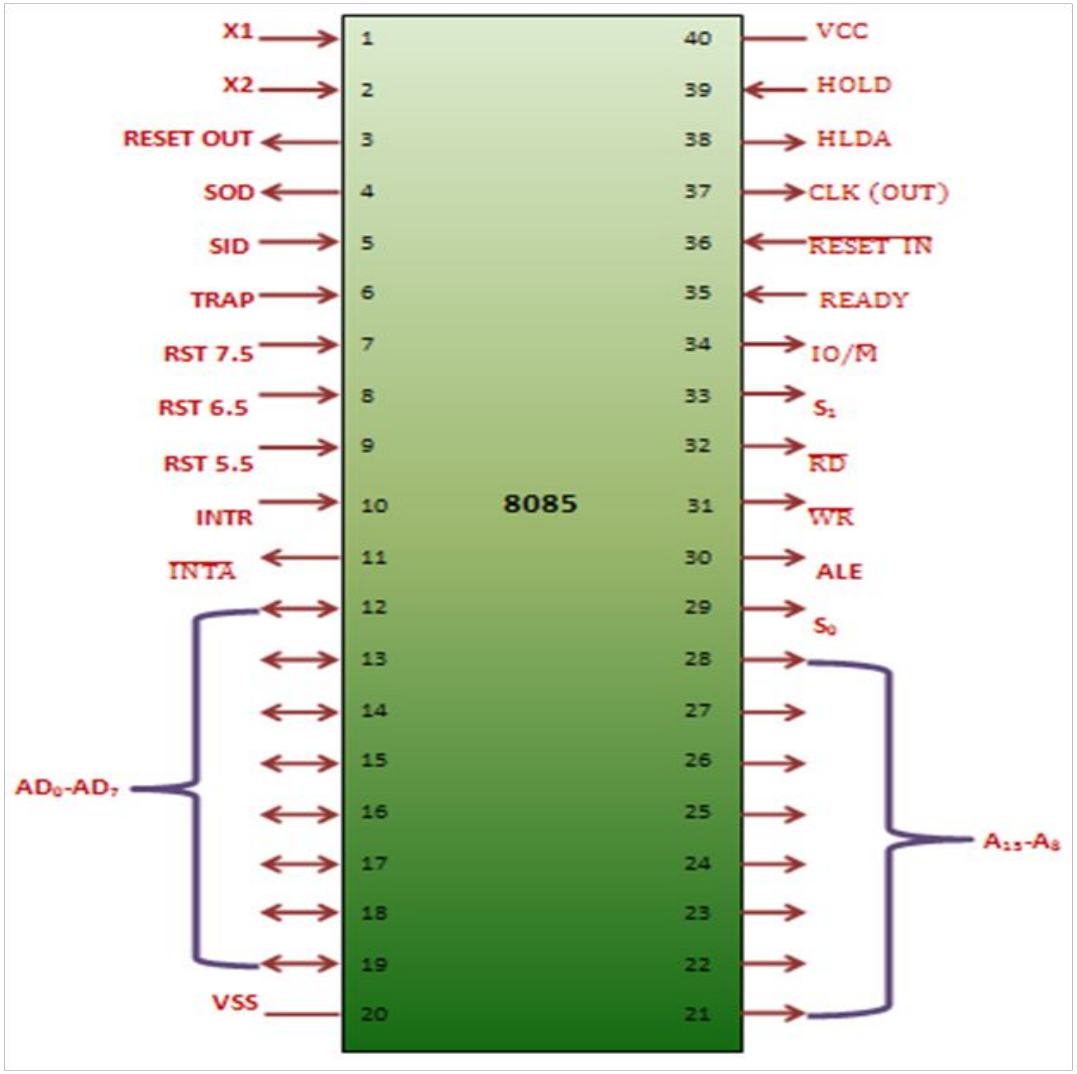
Address buffer and address-data buffer

- The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange the desired data with the memory and I/O chips.

Address bus and data bus

- Data bus carries the data to be stored. It is bidirectional, whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data & Address I/O devices.

8085-Pin diagram



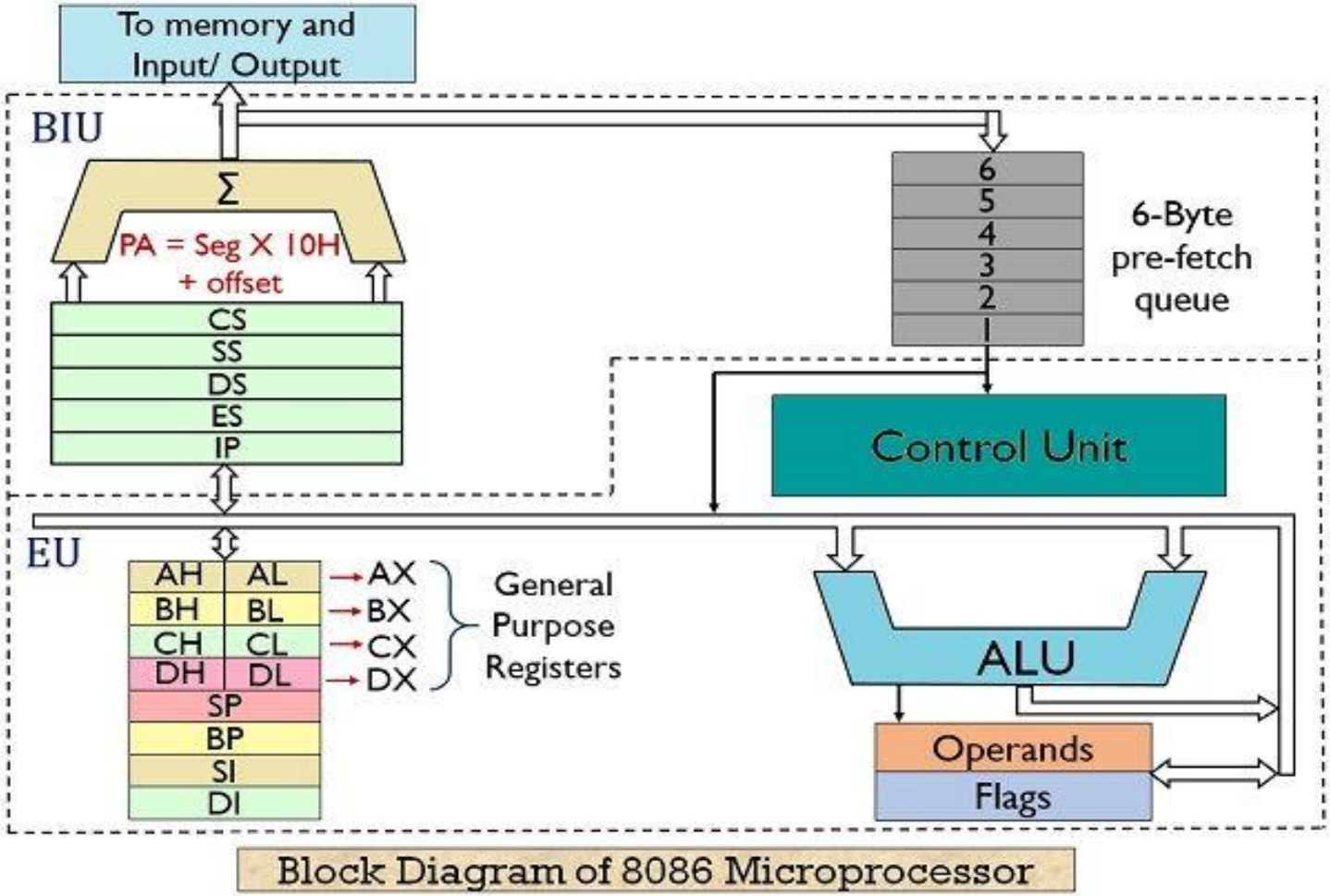
8086 Microprocessor

- 8086 Microprocessor is an enhanced version of 8085
- Designed by Intel in 1976.
- It is a 16-bit Microprocessor having 20 address lines and16 data lines that provides up to 1MB storage
- It consists of powerful instruction set, which provides operations like multiplication and division easily.
- It supports two modes of operation, i.e. Maximum mode and Minimum mode.
- Maximum mode is suitable for system having multiple processors and Minimum mode is suitable for system having a single processor.

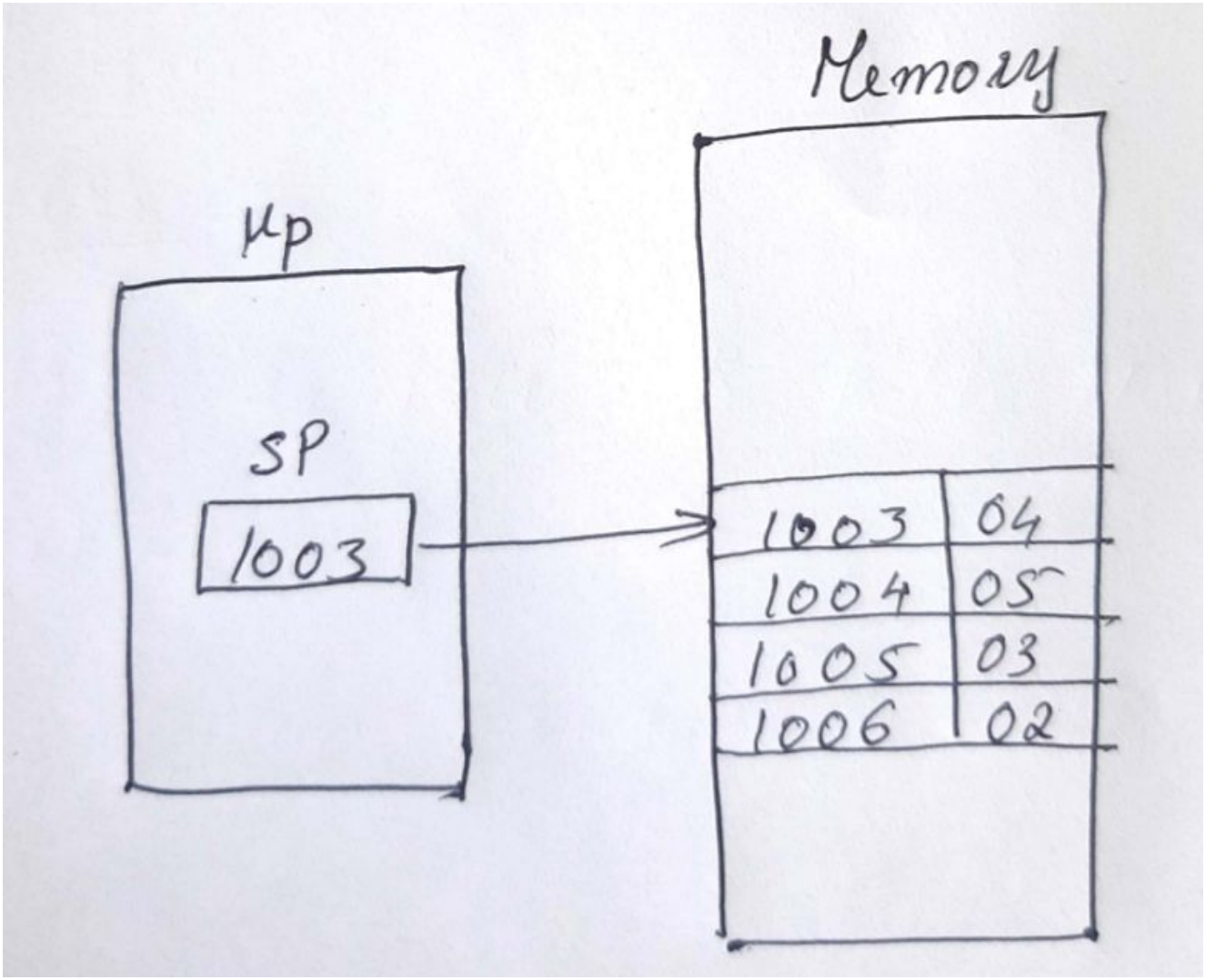
Features of 8086

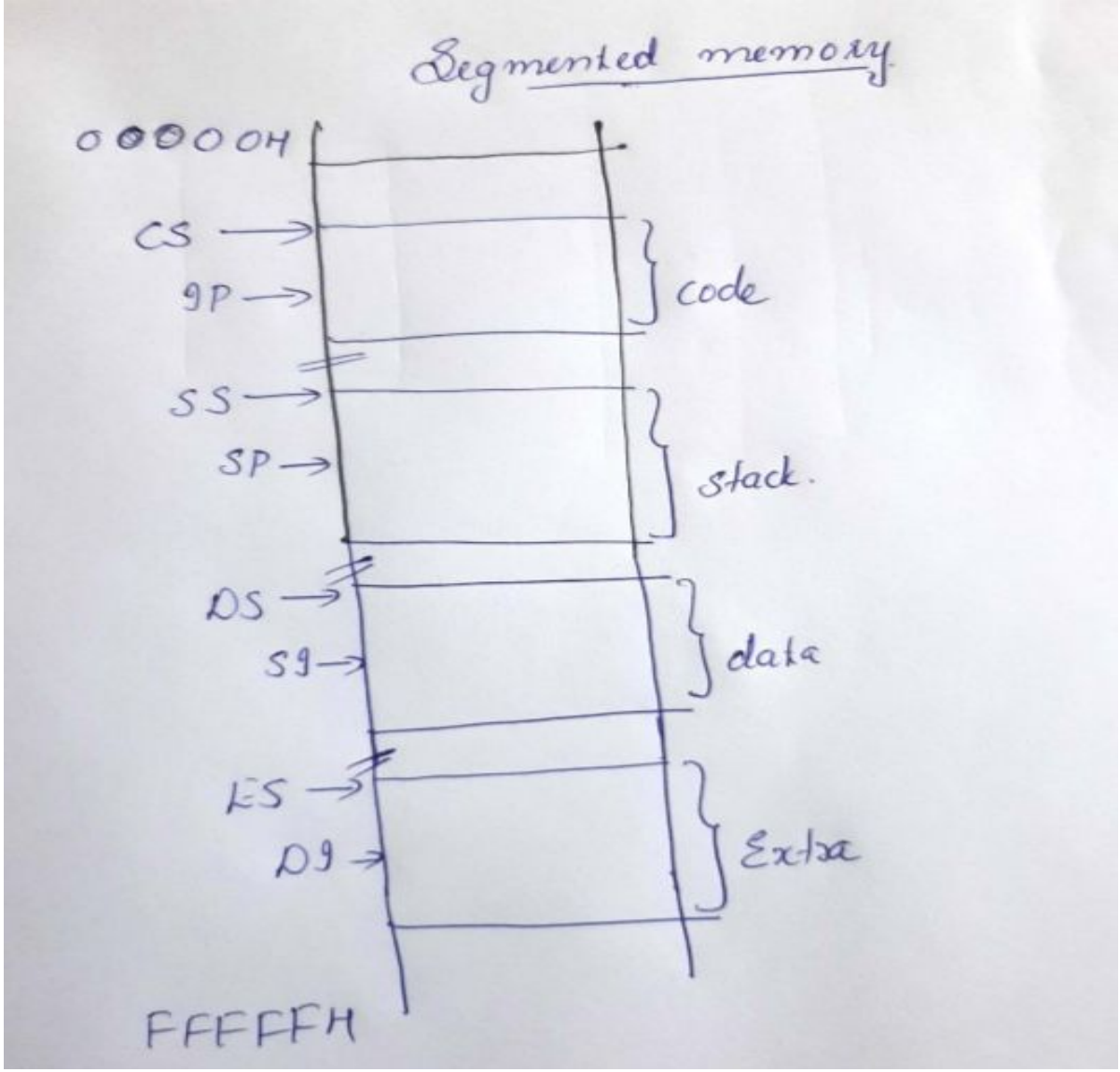
- It has an instruction queue, which is capable of storing six instruction bytes from the memory resulting in faster processing.
- It was the first 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, and 16-bit external data bus resulting in faster processing.
- It is available in 3 versions based on the frequency of operation −

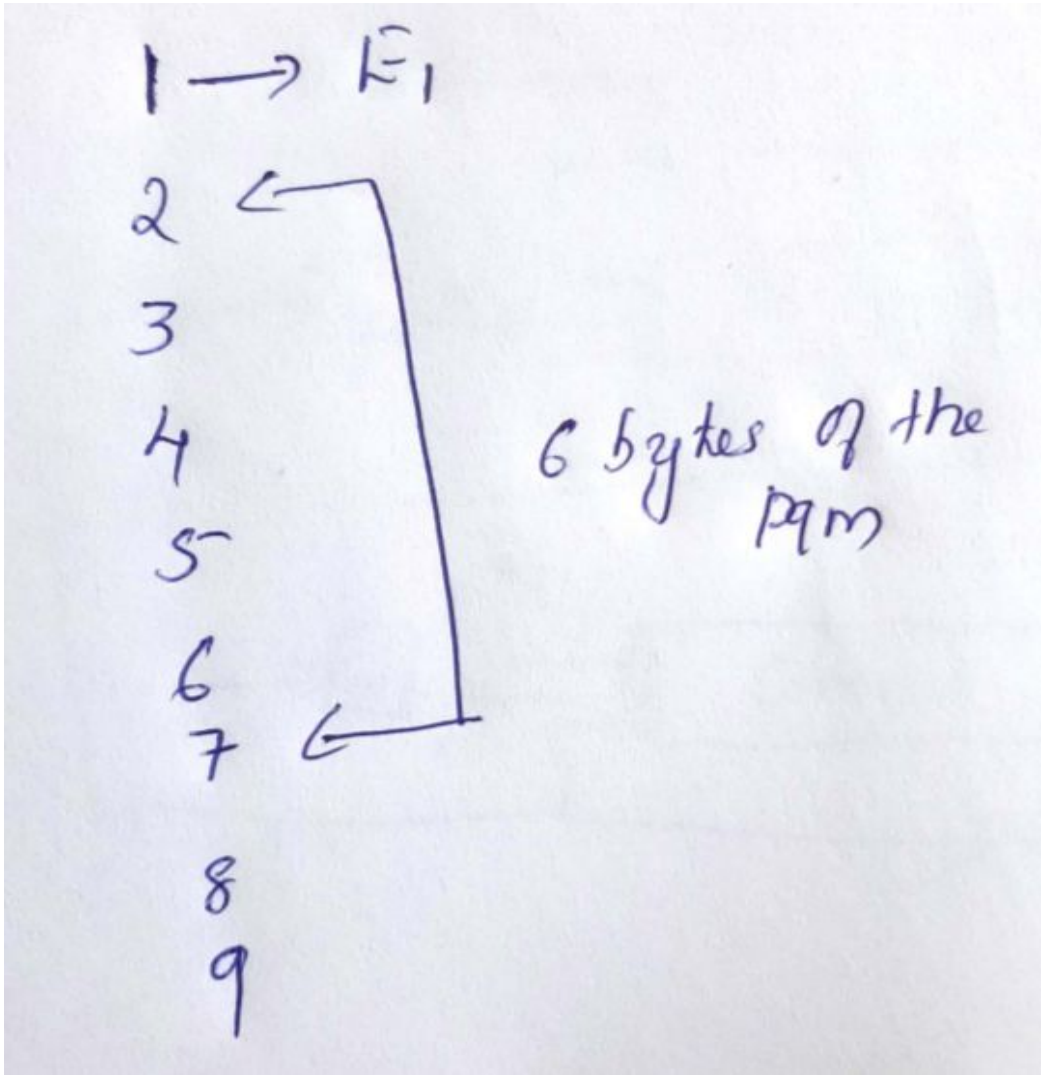
  5MHz,8MHz,10 MHz
- It has 256 vectored interrupts.
- It consists of 29,000 transistors.



Block Diagram of 8086 Microprocessor


Memory
μp
SP
1003
1003
04
1004
05
1005
03
1006
02


Segmented memory
00000H
CS
IP
code
SS
SP
stack.
DS
SI
data
ES
DI
Extra
FFFFFH


1 → E1
2
3
4
5
6
7
8
9
6 bytes of the PAM

Architecture of 8086

- 8086 Microprocessor is divided into two functional units, i.e., **EU** (Execution Unit) and **BIU** (Bus Interface Unit).

EU (Execution Unit)

- Execution unit gives instructions to BIU stating from where to fetch the data and then decode and execute those instructions. Its function is to control operations on data using the instruction decoder & ALU.
- EU has no direct connection with system buses as shown in the above figure, it performs operations over data through BIU.

Execution Unit

ALU

- It handles all arithmetic and logical operations, like +, −, ×, /, OR, AND, NOT operations.

Flag Register

- It is a 16-bit register that behaves like a flip-flop, i.e. it changes its status according to the result stored in the accumulator. It has 9 flags and they are divided into 2 groups − Conditional Flags and Control Flags.

Conditional Flags

- It represents the result of the last arithmetic or logical instruction executed.

Following is the list of conditional flags −

- Carry flag − This flag indicates an overflow condition for arithmetic operations.
- Auxiliary flag − When an operation is performed at ALU, it results in a carry/borrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), then this flag is set, i.e. carry given by D3 bit to D4 is AF flag
- Parity flag − This flag is used to indicate the parity of the result, i.e. when the lower order 8-bits of the result contains even number of 1's, then the Parity Flag is set. For odd number of 1's, the Parity Flag is reset.
- Zero flag − This flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0.
- Sign flag − This flag holds the sign of the result, i.e. when the result of the operation is negative, then the sign flag is set to 1 else set to 0.
- Overflow flag − This flag represents the result when the system capacity is exceeded.

Control Flags

- Control flags controls the operations of the execution unit. Following is the list of control flags −
- Trap flag − It is used for single step control and allows the user to execute one instruction at a time for debugging. If it is set, then the program can be run in a single step mode.
- Interrupt flag − It is an interrupt enable/disable flag, i.e. used to allow/prohibit the interruption of a program. It is set to 1 for interrupt enabled condition and set to 0 for interrupt disabled condition.
- Direction flag − It is used in string operation. As the name suggests when it is set then string bytes are accessed from the higher memory address to the lower memory address and vice-a-versa.

Flag Register

Auxiliary Carry Flag

This is set, if there is a carry from the lowest nibble, i.e, bit three during addition, or borrow for the lowest nibble, i.e, bit three, during subtraction.

Carry Flag

This flag is set, when there is a carry out of MSB in case of addition or a borrow in case of subtraction.

Sign Flag

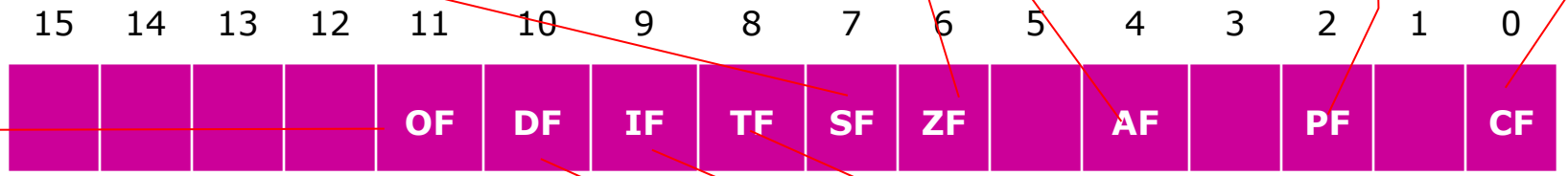
This flag is set, when the result of any computation is negative

Zero Flag

This flag is set, if the result of the computation or comparison performed by an instruction is zero

Parity Flag

This flag is set to 1, if the lower byte of the result contains even number of 1's ; for odd number of 1's set to zero.



Over flow Flag

This flag is set, if an overflow occurs, i.e, if the result of a signed operation is large enough to accommodate in a destination register. The result is of more than 7-bits in size in case of 8-bit signed operation and more than 15-bits in size in case of 16-bit sign operations, then the overflow will be set.

Tarp Flag

If this flag is set, the processor enters the single step execution mode by generating internal interrupts after the execution of each instruction

Direction Flag

This is used by string manipulation instructions. If this flag bit is '0', the string is processed beginning from the lowest address to the highest address, i.e., auto incrementing mode. Otherwise, the string is processed from the highest address towards the lowest address, i.e., auto incrementing mode.

Interrupt Flag

Causes the 8086 to recognize external mask interrupts; clearing IF disables these interrupts.

General purpose register

- There are 8 general purpose registers, i.e., AH, AL, BH, BL, CH, CL, DH, and DL. These registers can be used individually to store 8-bit data and can be used in pairs to store 16bit data. The valid register pairs are AH and AL, BH and BL, CH and CL, and DH and DL. It is referred to the AX, BX, CX, and DX respectively.
- AX register − It is also known as accumulator register. It is used to store operands for arithmetic operations.
- BX register − It is used as a base register. It is used to store the starting base address of the memory area within the data segment.
- CX register − It is referred to as counter. It is used in loop instruction to store the loop counter.
- DX register − This register is used to hold I/O port address for I/O instruction.

Stack pointer register

It is a 16-bit register, which holds the address from the start of the segment to the memory location, where a word was most recently stored on the stack.

BIU (Bus Interface Unit)

- BIU takes care of all data and addresses transfers on the buses for the EU like sending addresses, fetching instructions from the memory, reading data from the ports and the memory as well as writing data to the ports and the memory. EU has no direct connection with System Buses so this is possible with the BIU. EU and BIU are connected with the Internal Bus

BIU has the following functional parts

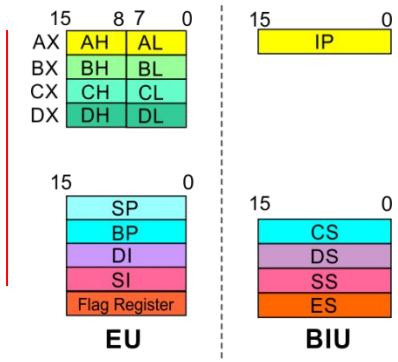
- **Instruction queue** − BIU gets upto 6 bytes of next instructions and stores them in the instruction queue. When EU executes instructions and is ready for its next instruction, then it simply reads the instruction from this instruction queue resulting in increased execution speed.
- Fetching the next instruction while the current instruction executes is called pipelining.

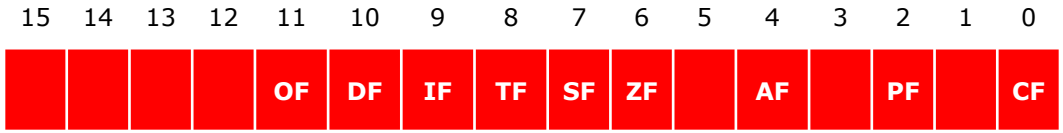
- Segment register − BIU has 4 segment registers i.e. CS, DS, SS& ES.
- CS − It stands for Code Segment. It is used for addressing a memory location in the code segment of the memory, where the executable program is stored.
- DS − It stands for Data Segment. It consists of data used by the program and is accessed in the data segment by an offset address or the content of other register that holds the offset address.
- SS − It stands for Stack Segment. It handles memory to store data and addresses during execution.

- ES − It stands for Extra Segment. ES is additional data segment, which is used by the string to hold the extra destination data.
- Instruction pointer(IP) − It is a 16-bit register used to hold the address of the next instruction to be executed.

Architecture

8086 registers categorized into 4 groups

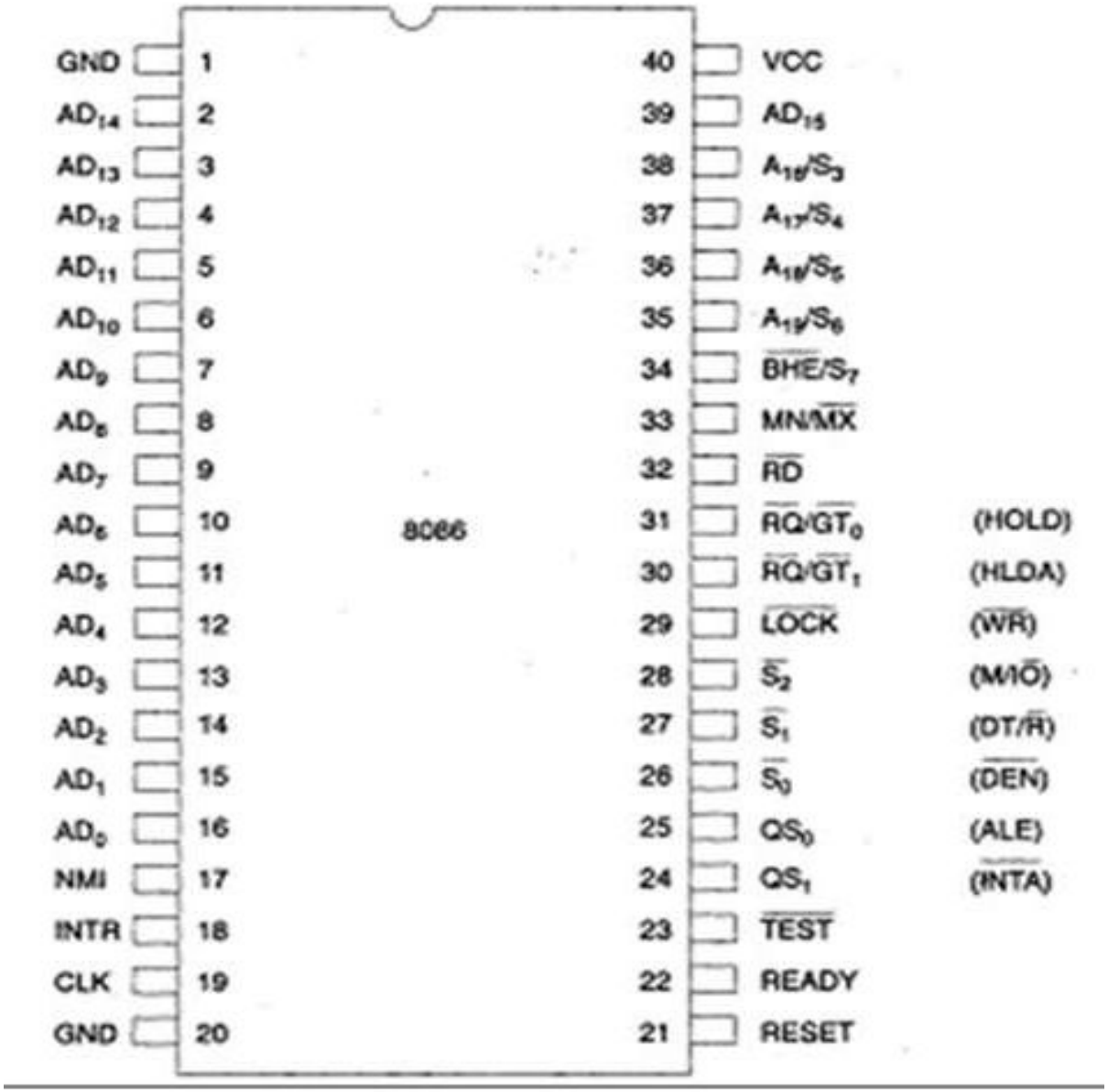




Sl.No.	Type	Register width	Name of register
1	General purpose register	16 bit	AX, BX, CX, DX
		8 bit	AL, AH, BL, BH, CL, CH, DL, DH
2	Pointer register	16 bit	SP, BP
3	Index register	16 bit	SI, DI
4	Instruction Pointer	16 bit	IP
5	Segment register	16 bit	CS, DS, SS, ES
6	Flag (PSW)	16 bit	Flag register

Register	Name of the Register	Special Function
AX	16-bit Accumulator	Stores the 16-bit results of arithmetic and logic operations
AL	8-bit Accumulator	Stores the 8-bit results of arithmetic and logic operations
BX	Base register	Used to hold base value in base addressing mode to access memory data
CX	Count Register	Used to hold the count value in SHIFT, ROTATE and LOOP instructions
DX	Data Register	Used to hold data for multiplication and division operations
SP	Stack Pointer	Used to hold the offset address of top stack memory
BP	Base Pointer	Used to hold the base value in base addressing using SS register to access data from stack memory
SI	Source Index	Used to hold index value of source operand (data) for string instructions
DI	Data Index	Used to hold the index value of destination operand (data) for string operations

8086 Pin Diagram



8086 signals

- **Power supply and frequency signals**

It uses 5V DC supply at V_{CC} pin 40, and uses ground at V_{SS} pin 1 and 20 for its operation.

- **Clock signal**

Clock signal is provided through Pin-19. It provides timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.

- **Address/data bus**

AD0-AD15. These are 16 address/data bus. AD0-AD7 carries low order byte data and AD8-AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.

- **Address/status bus**

A16-A19/S3-S6. These are the 4 address/status buses. During the first clock cycle, it carries 4-bit address and later it carries status signals.

S7/BHE

- BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15. This signal is low,whenever a byte is transferred thru higher byte of the data bus

- **S7/BHE**

BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15. This signal is low during the first clock cycle, thereafter it is active.

- **Read**

It is available at pin 32 and is used to read signal for Read operation.

- **Ready**

It is available at pin 22. It is an acknowledgement signal from I/O devices that data is transferred. It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

- **RESET**

It is available at pin 21 and is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high for the first 4 clock cycles to RESET the microprocessor.

$\overline{BHE}$	A_0	*Indication*
0	0	Whole word (2 bytes)
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address
1	1	None

- **INTR**

It is available at pin 18. It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine the availability of the request. If any interrupt occurs, then processor

NMI

It stands for non-maskable interrupt and is available at pin 17. It is an edge triggered input, which causes an interrupt request to the microprocessor.

TEST

This input is examined by a '**WAIT**' instruction and is available at pin 23. When this signal is high, then the processor remains in an IDLE state, else the execution continues.

MN/*MX*

- It stands for Minimum/Maximum and is available at pin 33. It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode and vice-versa.

- **INTA**

It is an interrupt acknowledgement signal and is available at pin 24. When it goes low ,means processor has accepted the interrupt. It goes active low during T2,T3,Tw of each interrupt ack cycle.

- **ALE**

It stands for address enable latch and is available at pin 25. A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.

- **DEN**

It stands for Data Enable and is available at pin 26. It is used to enable Transreceiver 8286. The transreceiver is a device used to separate data from the address/data bus.

- **DT/R**

It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the transreceiver. When it is high, data is transmitted out and vice-a-versa.

- **M/IO**

This signal is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low indicates the memory operation. It is available at pin 28.

- **WR**

It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

- **HLDA**

It stands for Hold Acknowledgement signal and is available at pin 30. This signal acknowledges the HOLD signal.

- **HOLD**

This signal indicates to the processor that another master is requesting to access the address/data buses. It is available at pin 31.

- **QS1 and QS0**

These are queue status signals and are available at pin 24 and 25. These signals provide the status of instruction queue. Their conditions are shown in the following table −

QS_0	QS_1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

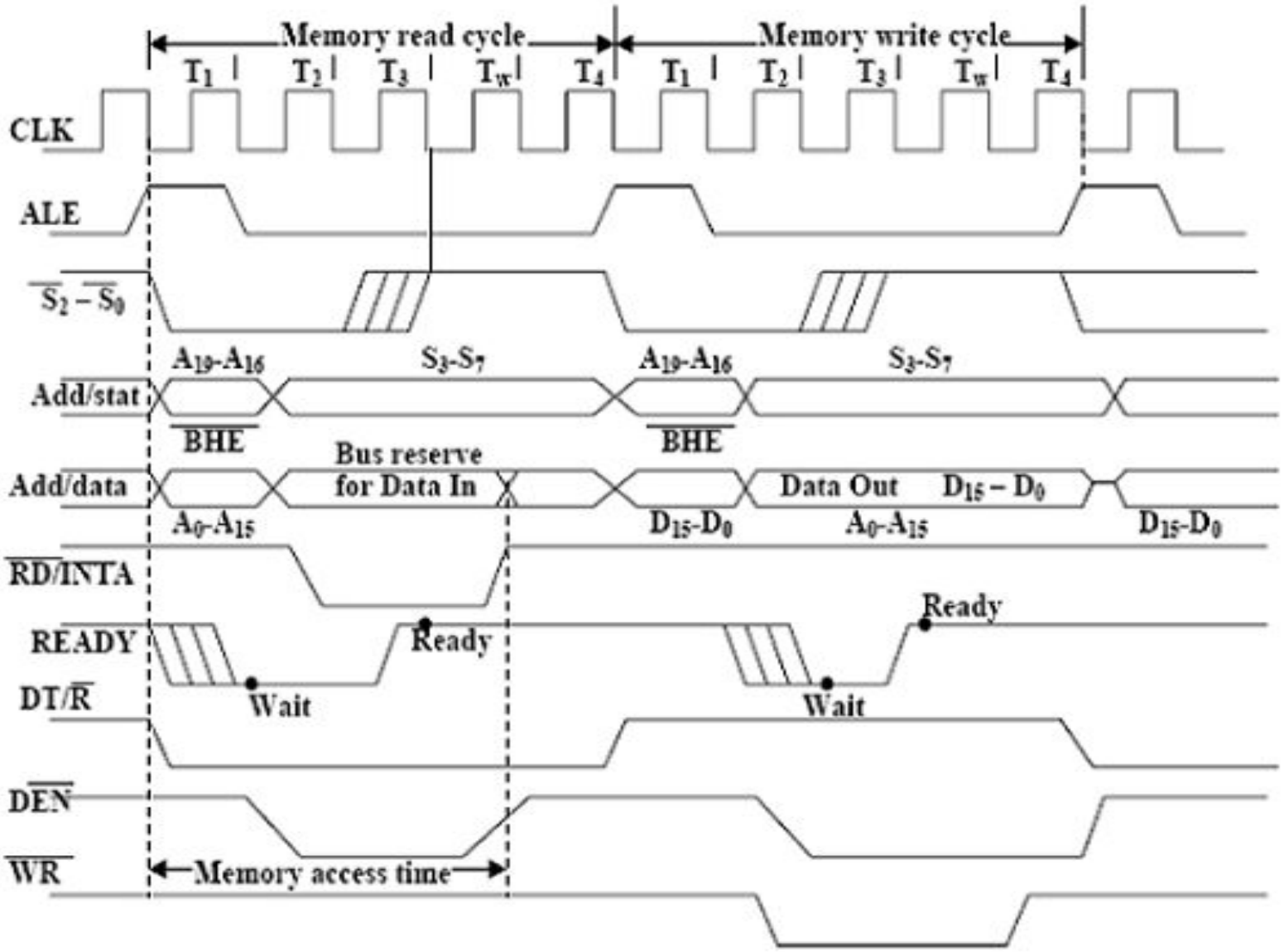
S_2	S_1	S_0	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

- **LOCK**

When this signal is active, it indicates that other system bus masters will be prevented from gaining access to system bus. It is activated by the 'LOCK' prefix instruction and remains active until the completion of next instruction

RQ/GT_1 and RQ/GT_0

These are the Request/Grant signals used by other local bus masters, in maximun mode requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT_0 has a higher priority than RQ/GT_1.

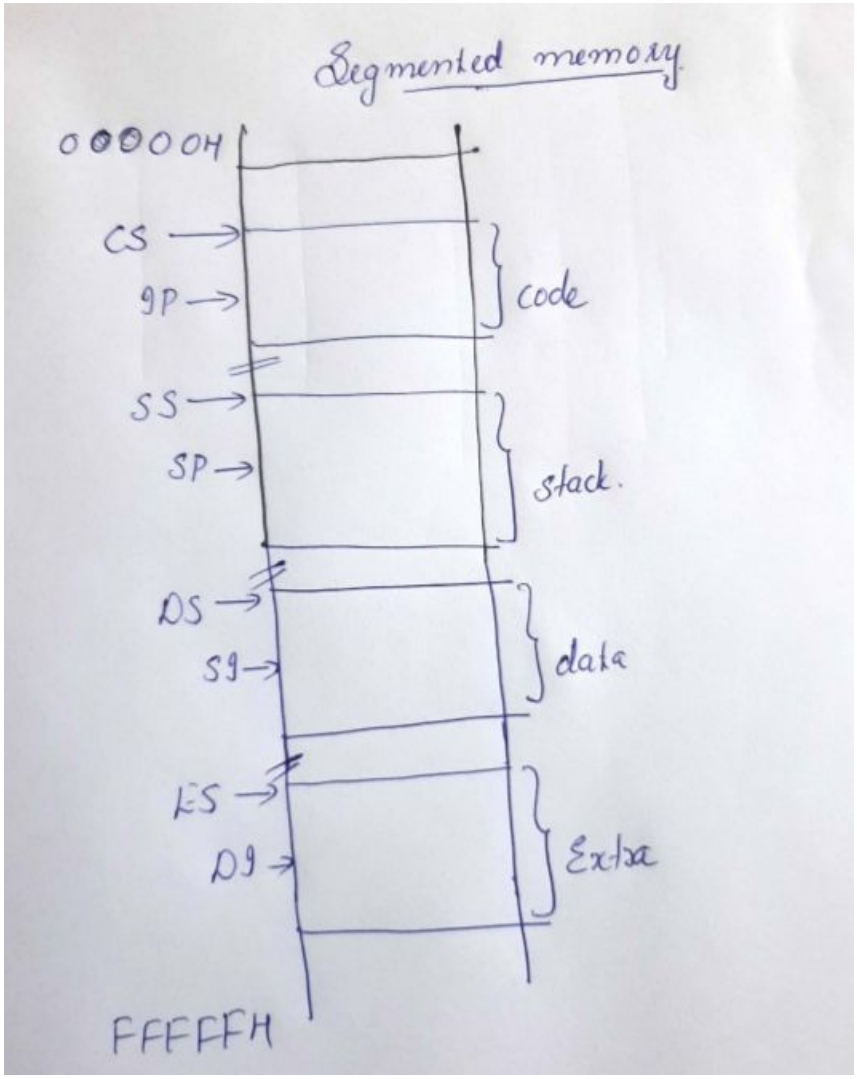

Memory read cycle
Memory write cycle
T1
T2
T3
Tw
T4
CLK
ALE
S2 – S0
A19-A16
S3-S7
Add/stat
BHE
Bus reserve
for Data In
Add/data
A0-A15
D15-D0
Data Out
D15 – D0
RD/INTA
READY
Ready
Wait
DT/R
DEN
WR
Memory access time

Memory Segmentation

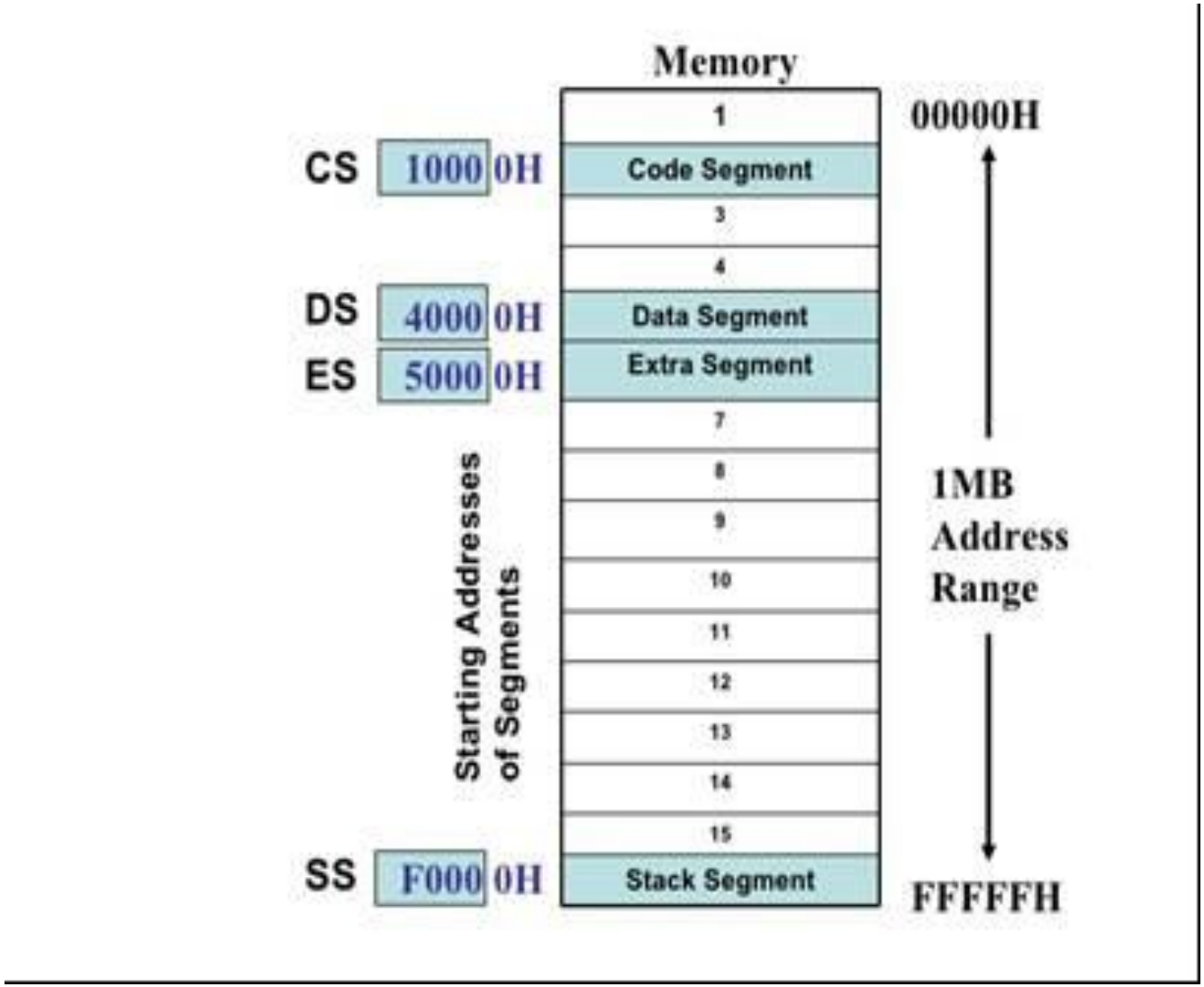
- Main memory is divided into different segments and each segment has its own base address.
- Increase the execution speed of computer system so that processor can able to fetch and execute the data from memory easy and fastly

Segmentation in 8086

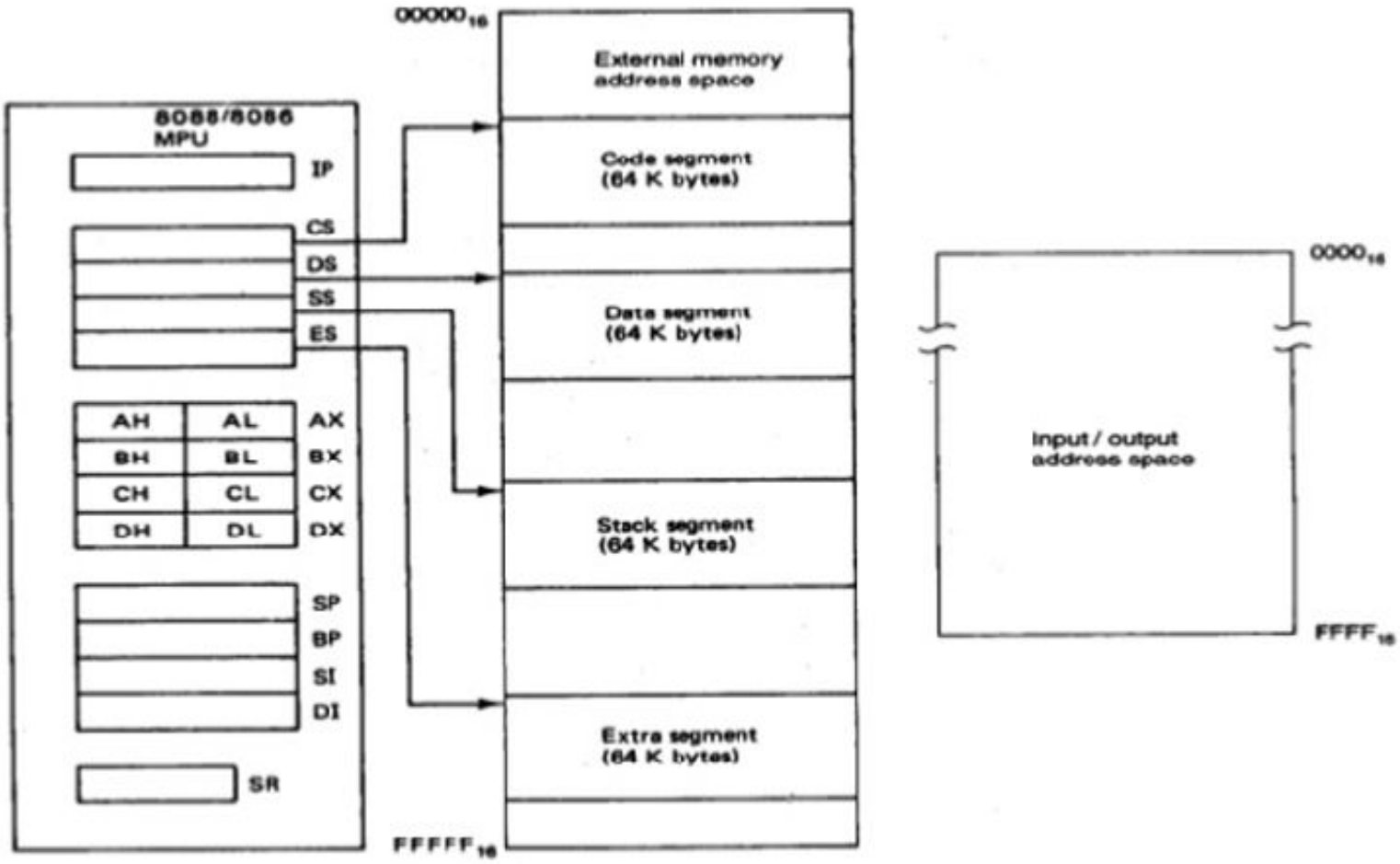
- The size of address bus of 8086 is 20 and is able to address 1 Mbytes of physical memory.
- The compete 1 Mbytes memory can be divided into 16 segments, each of 64 Kbytes size.
- Only four segments can be addressed at a time


Segmented memory
00000H
CS
IP
code
SS
SP
stack.
DS
SI
data
ES
DI
Extra
FFFFFH

Segmentation in 8086



Segmented Memory Representation



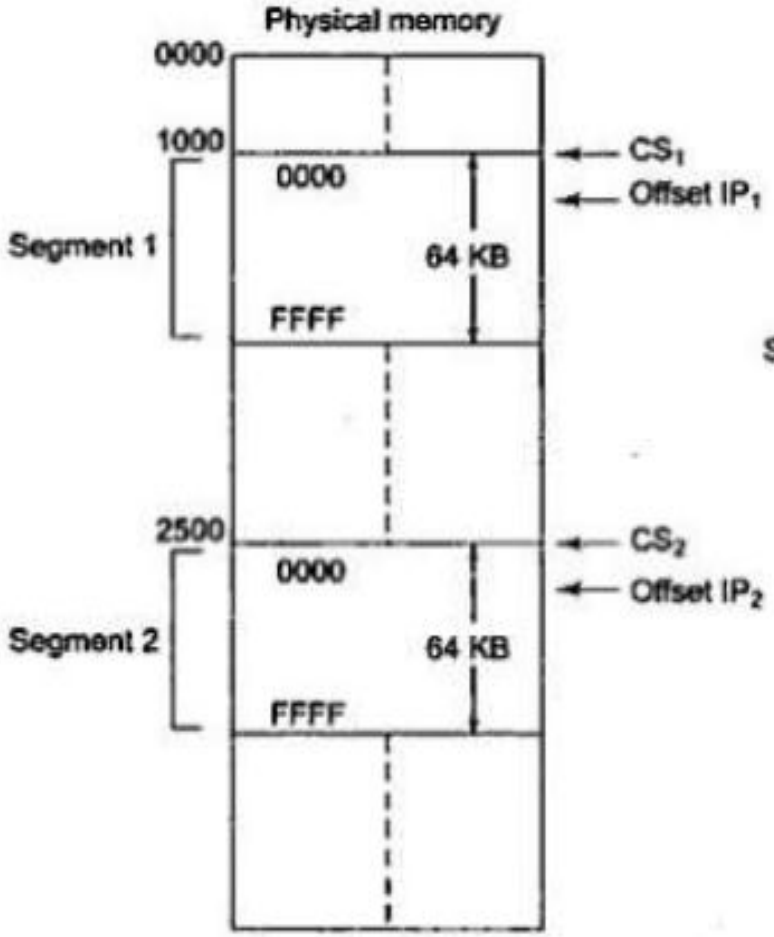
Types of Segmentation

Overlapping segment

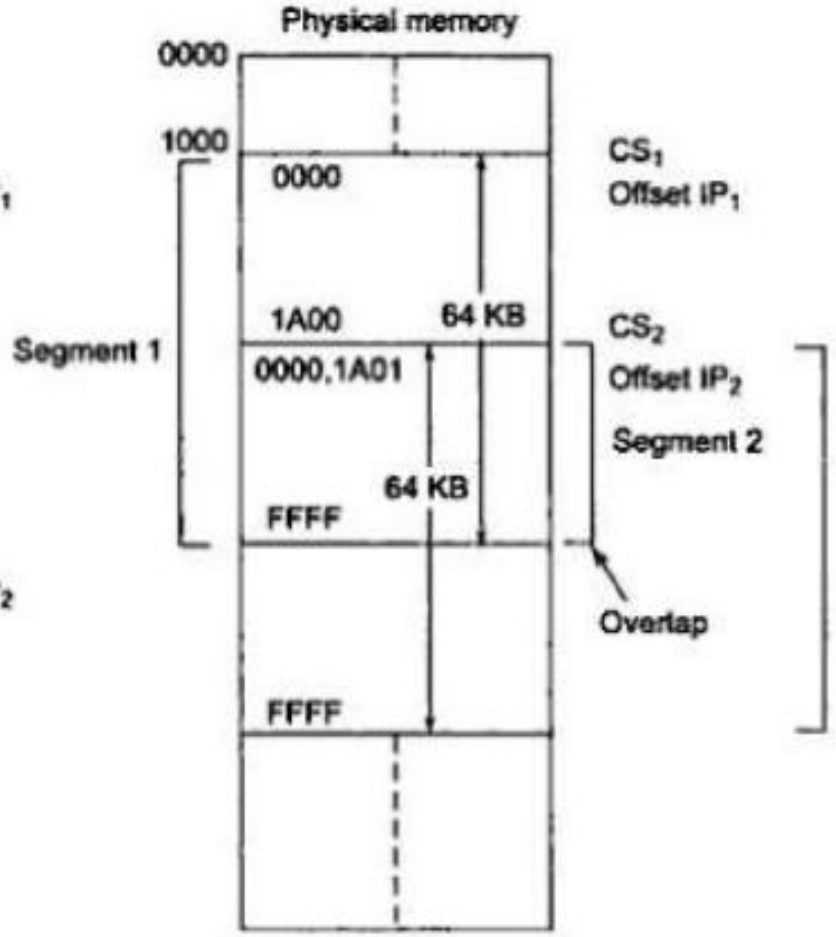
- A segment starts at a particular address and its maximum size can go up to 64 Kbytes. But if another segment starts along this 64 Kbytes location of the first segment, the two segments are said to be overlapping segment.
- The area of memory from the start of the second segment to the possible end of the first segment is called as overlapped segment.

Non Overlapped Segment

- A segment starts at a particular address and its maximum size can go up to 64 Kbytes. Another segment starts after this 64 Kbytes location of the first segment, then the two segments are said to be Non- overlapping segment.



Non-overlapping Segments



Overlapping Segments

Advantages of the Segmentation

1. Allows the memory capacity to be 1Mbytes although the actual addresses to be handled are of 16-bit size
2. Allows the placing of code, data and stack portions of the same program in different parts (segments) of memory, for data and code protection
3. Permits a program and/or its data to be put into different areas of memory each time the program is executed, i.e. provision for relocation is done.

Physical Address Calculation in 8086

- Segment address ----- 1005H
- Offset address -------5555H
- Segment address-----1005------ 0001 0000 0000 0101
- Shifted by 4 bit positions---- 0001 0000 0000 0101 0000

  +
- Offset address ---------- 0101 0101 0101 0101

- Physical address ---------- 0001 0101 0101 1010 0101

  1 5 5 A 5

Question

1) The value of Code Segment (CS) Register is 4042H and the value of offset is IP: 0580H.Calculate the effective address of the memory location pointed by the CS register.

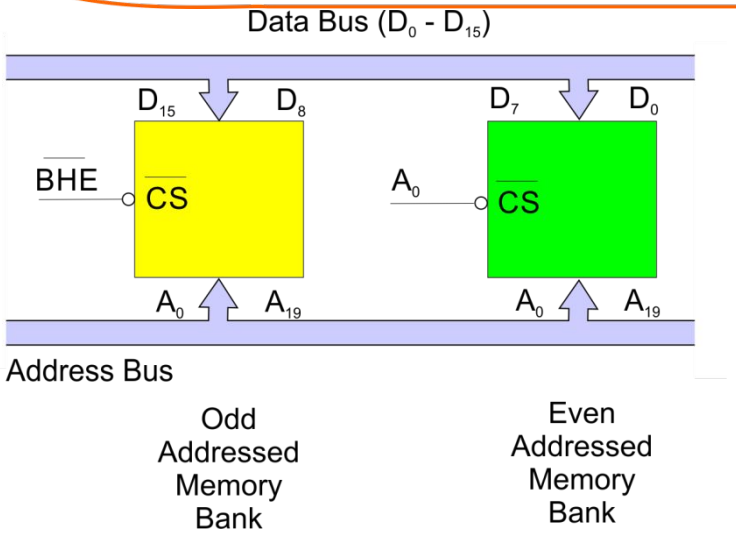
Ans: 409A0

Physical Memory Organization

- The total memory (1Mb) of 8086 is arranged in two banks. An odd bank and an even bank. Both the banks have equal no. of locations.
- The odd bank contains odd numbered memory locations. It is known as upper bank.
- The even bank contains only even numbered memory locations. It is known as lower bank.
- This arrangement is done in order to speed up the operation

- Byte data with even address is transferred on $D_{0\,-}\ D_7$ and byte data with odd address is transferred on $D_8 - D_{15}$

Memory organization in 8086



BHE	A_0	Function
0	0	Whole word
0	1	Upper byte/ odd address
1	0	Lower byte/even address
1	1	none

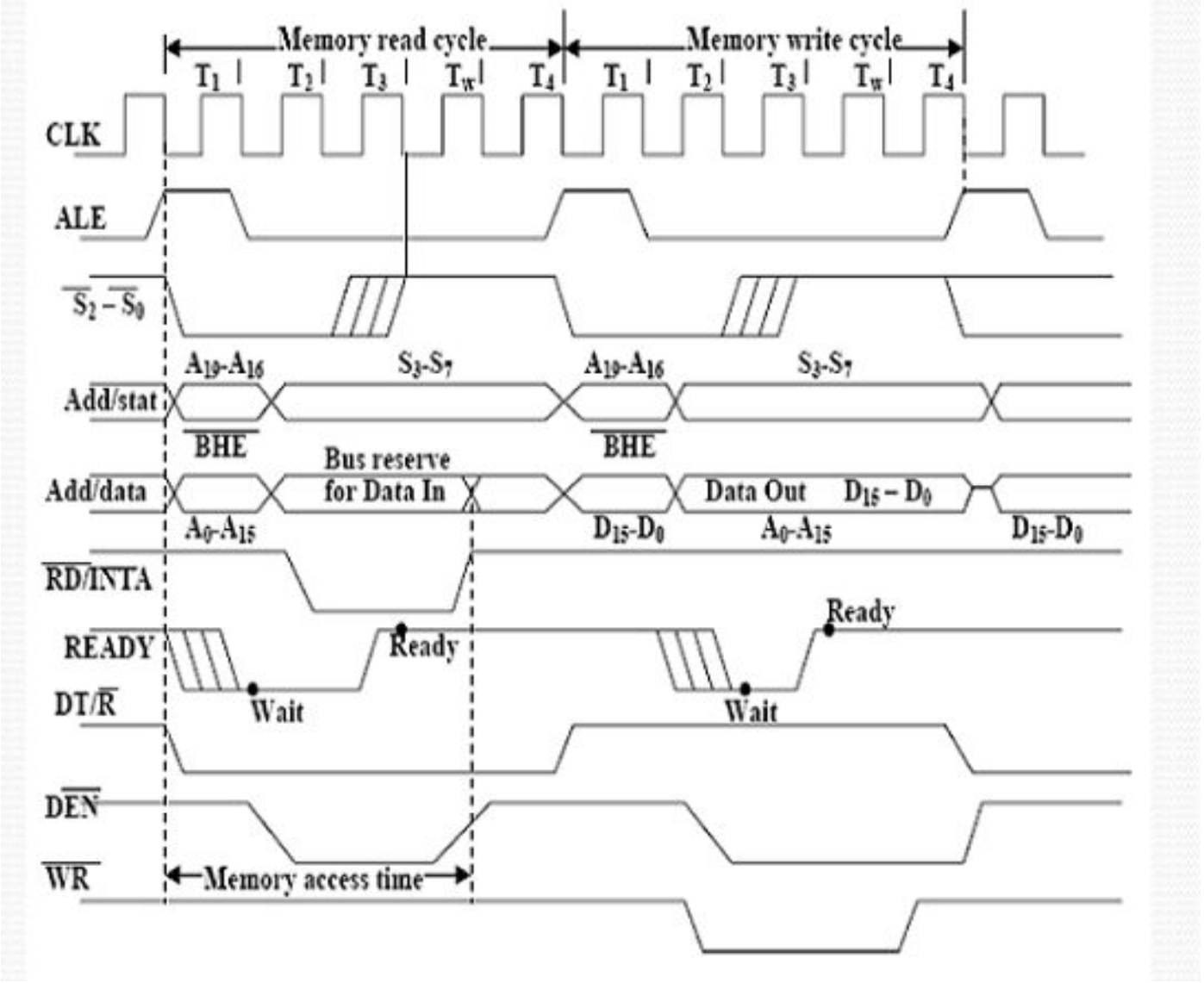
General Bus Operation

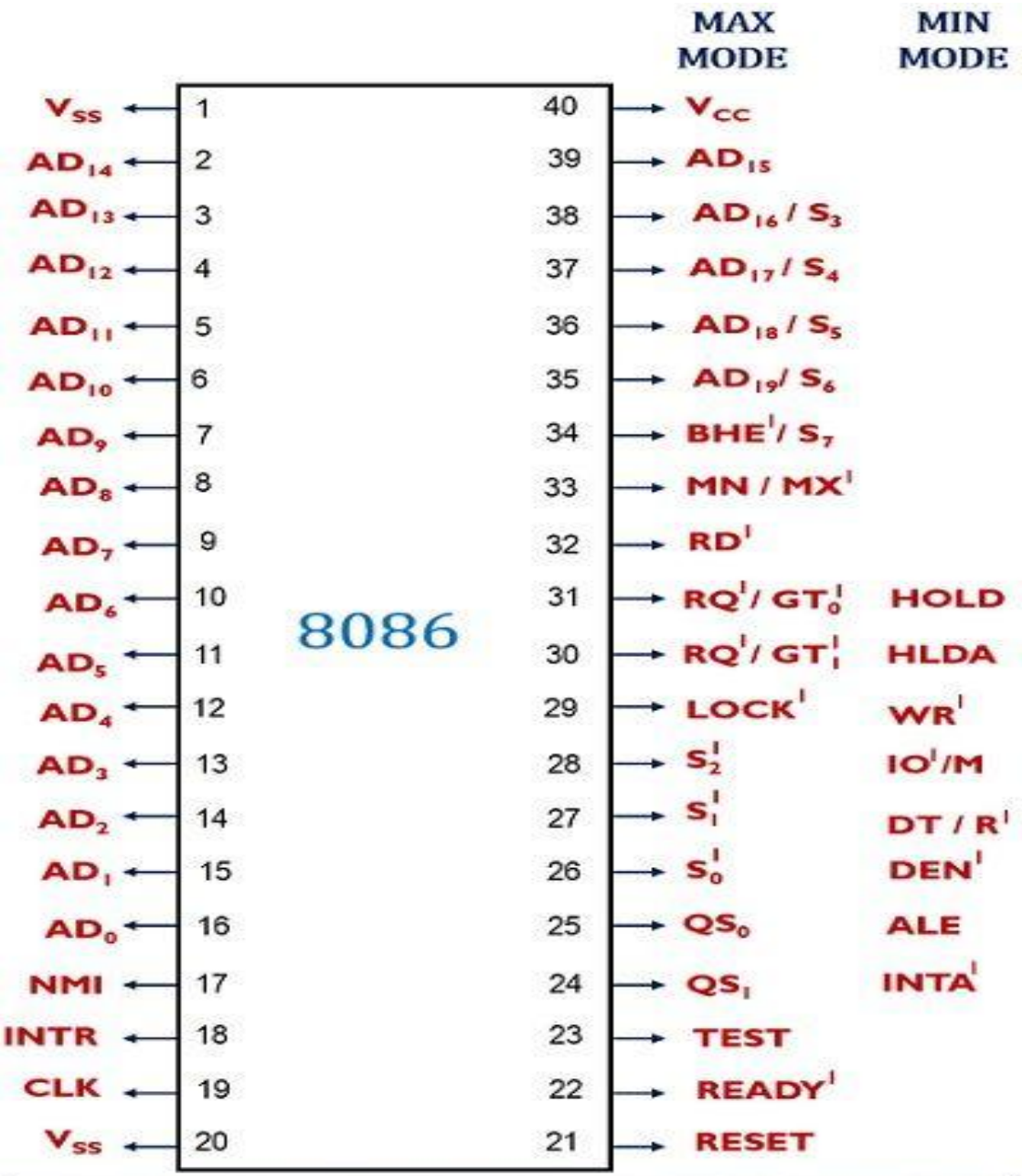
- All the processor bus cycles consist of at least four clock cycles -T1, T2, T3, T4.
- The 8086 has time multiplexed address and data bus. This is for maximum utilization of processor pins and it facilitates the use of 40 pin standard DIP package.
- The address is transmitted by the processor during T1.During T2, T3 and T4, data is transmitted over these lines. Tw is wait state , is introduced between T3 and T4.

•**ALE-** is emitted during T1 by the processor or bus controller. Used to separate address or data or status information.

- In maximum mode, the status lines **S0, S1 and S2** are used to indicate the type of operation.

General Bus Operation Cycle in Maximum Mode





Pin diagram of 8086 Microprocessor

Electronics Desk

	$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$
IOR	0	0	1
IOW	0	1	0
MEMR	1	0	1
MEMR	1	1	0

$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$
0	0	0
0	1	1
1	0	0
1	1	1

Minimum Mode 8086 System

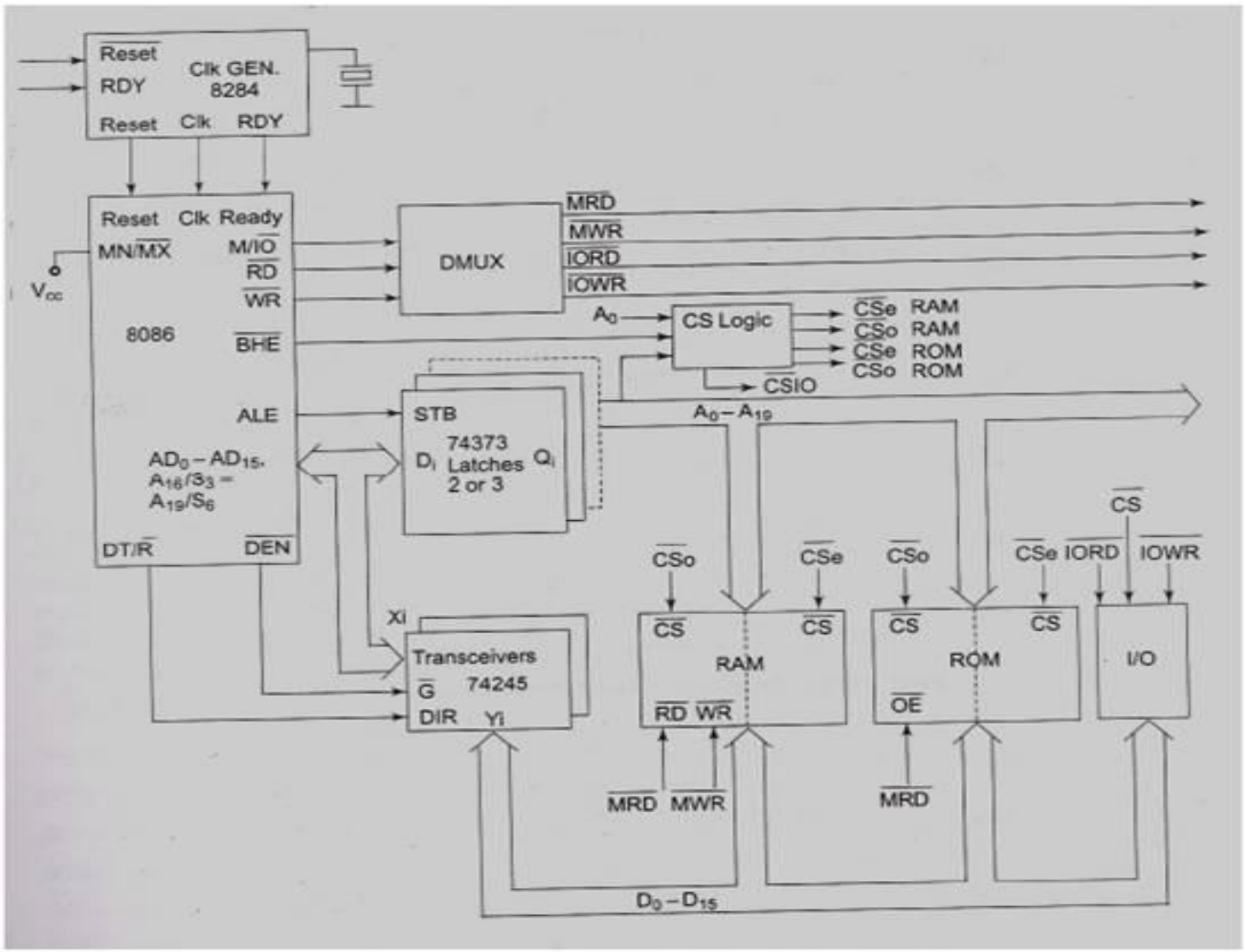
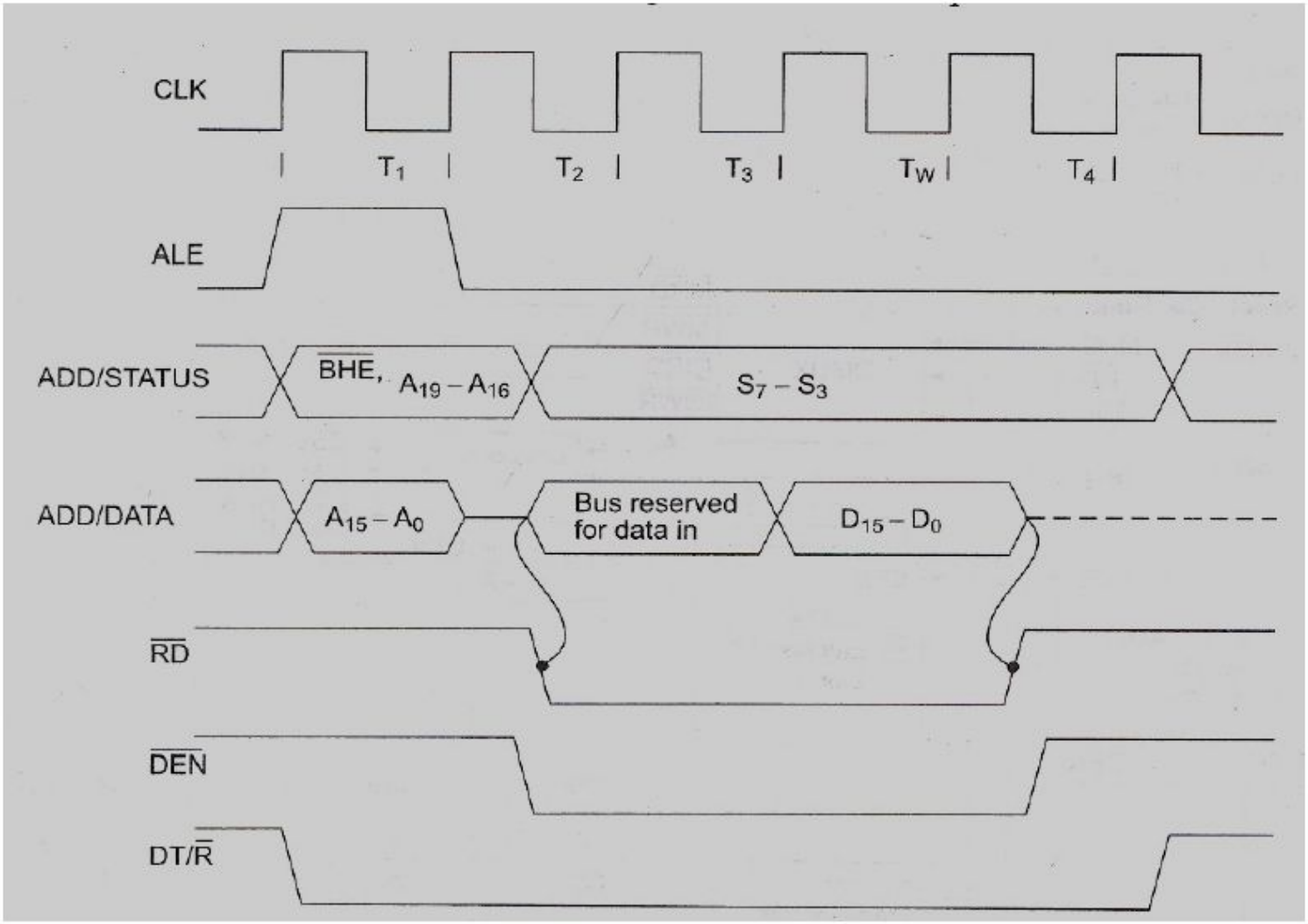
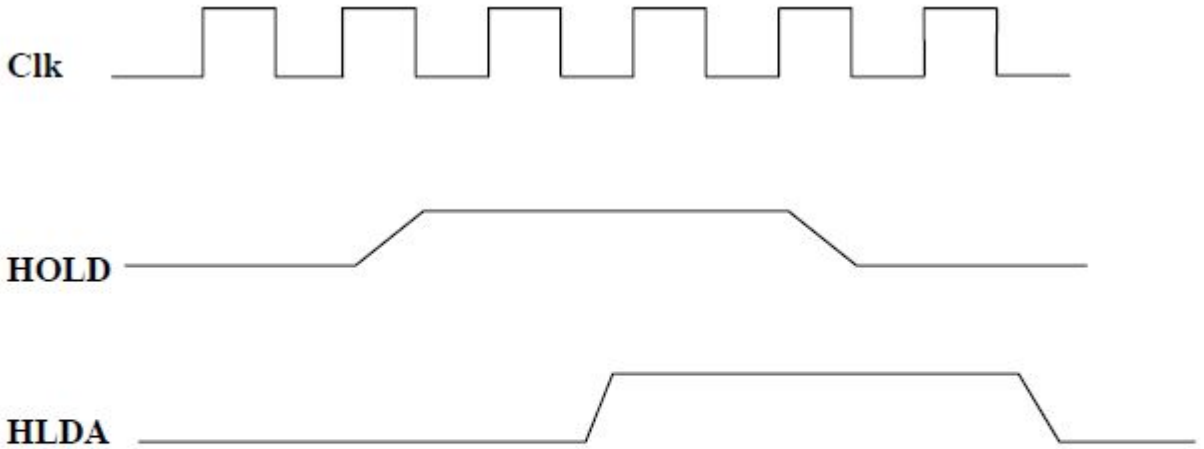


Fig 1.1. Minimum Mode 8086 System

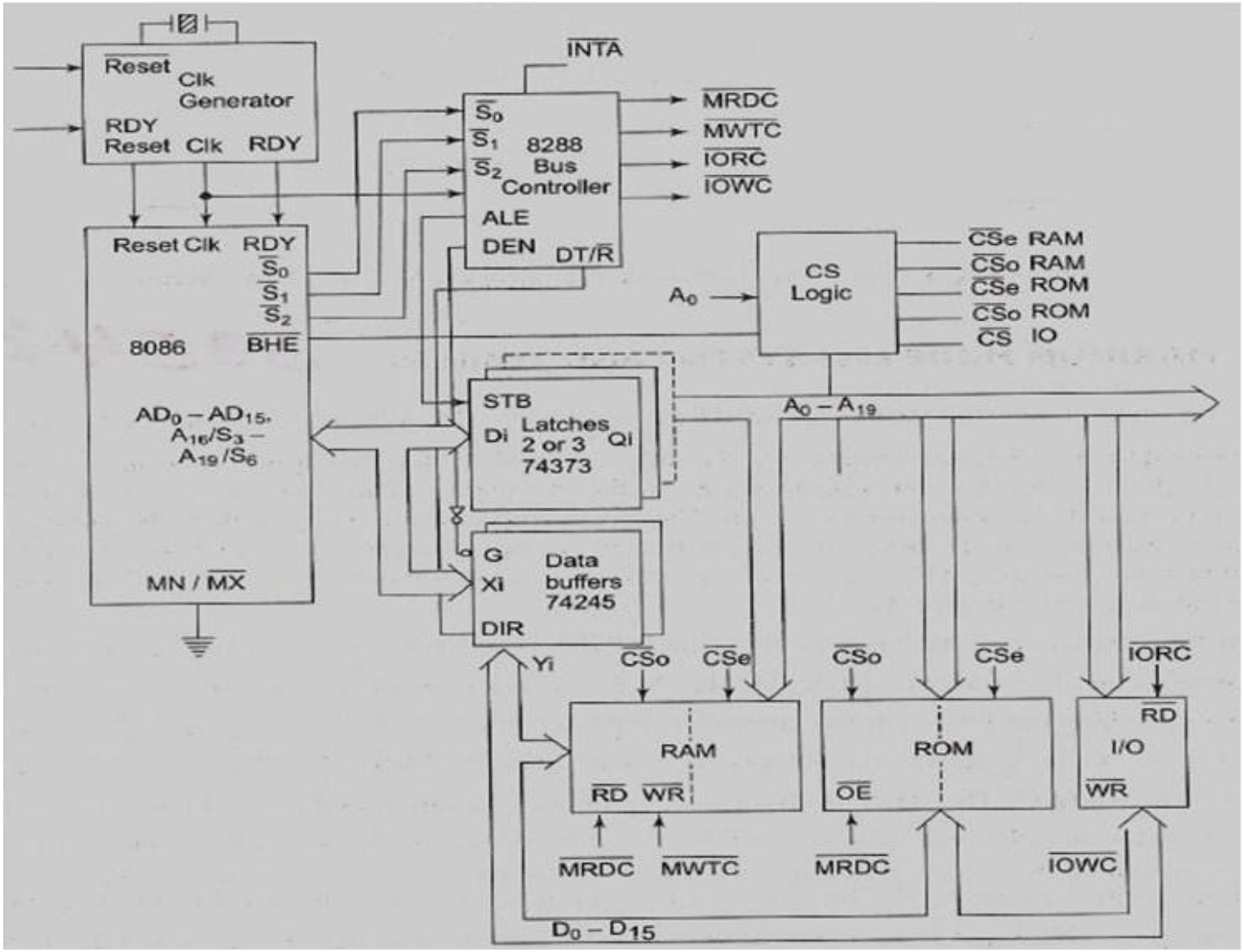
Read Cycle timing diagram for minimum mode



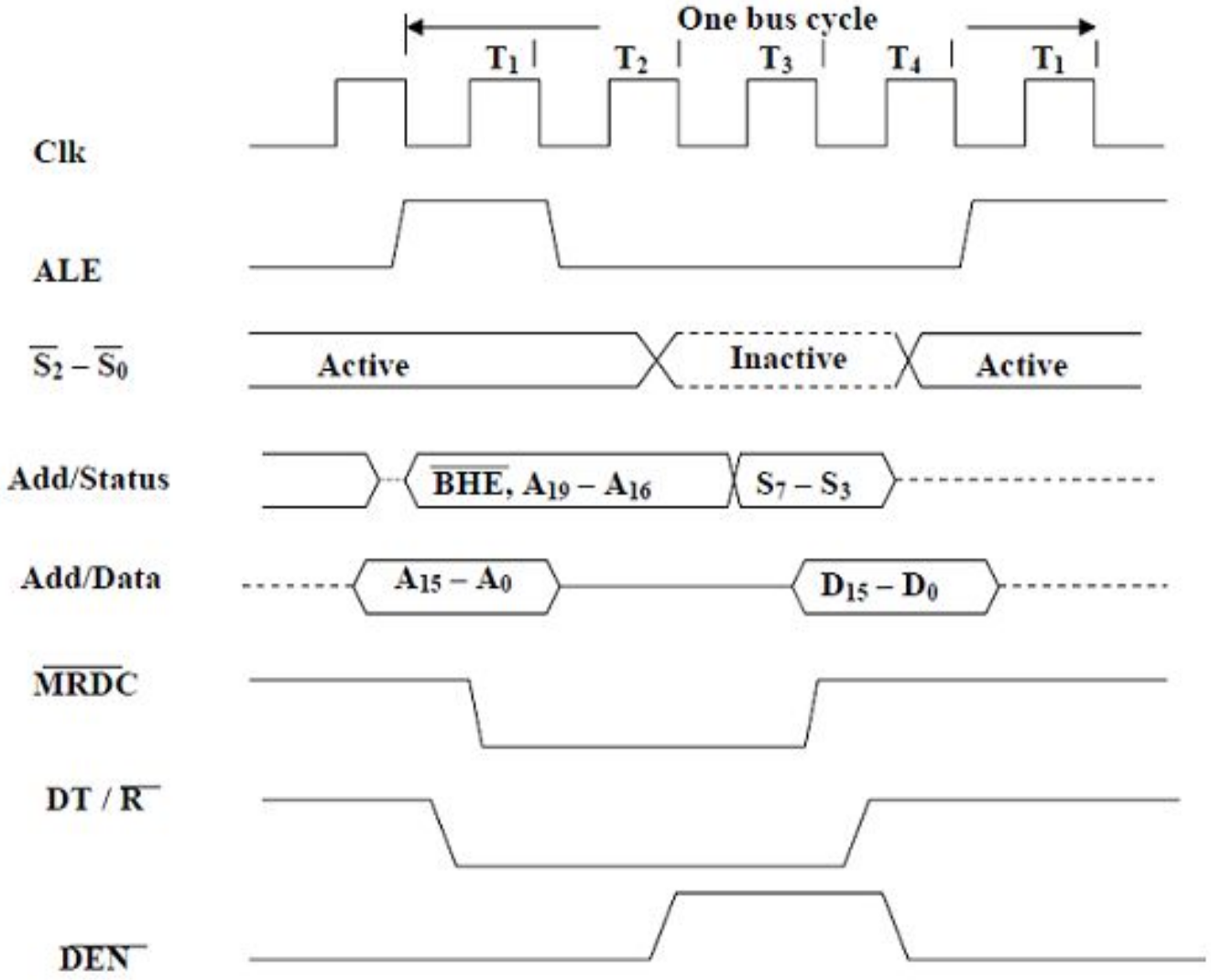


Bus Request and Bus Grant Timings in Minimum Mode System

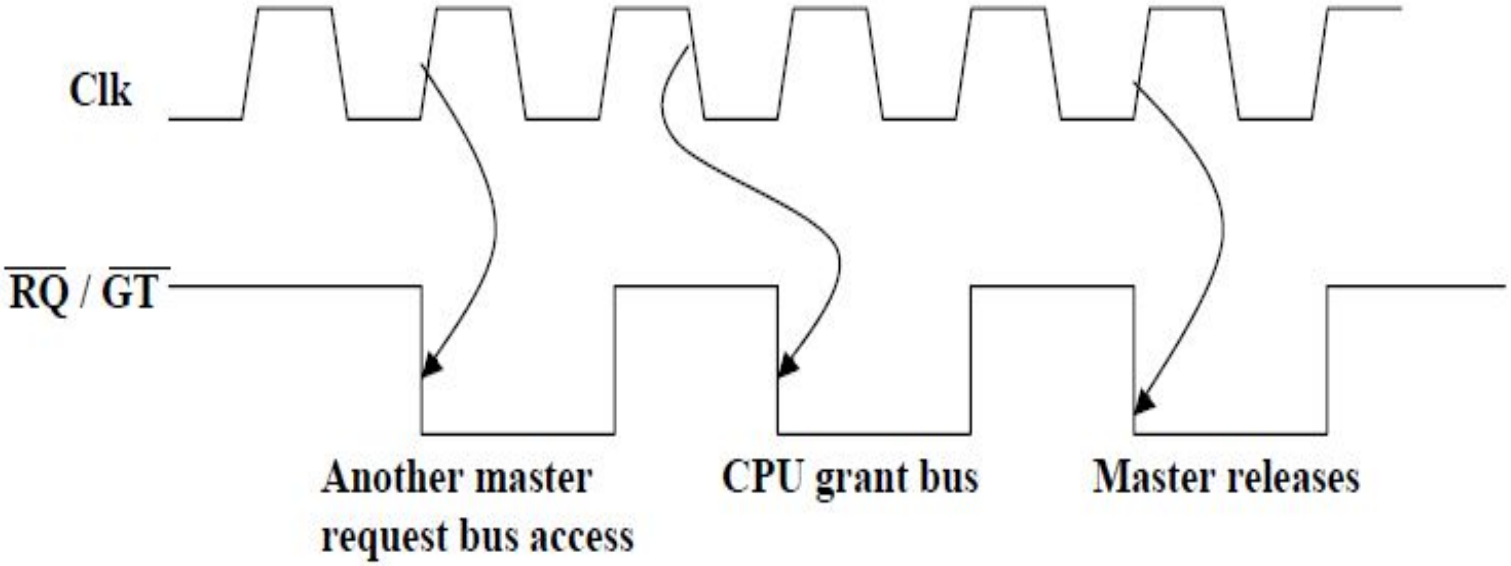
Maximum Mode 8086 System



Memory Read Timing in Maximum Mode



RQ/GT Timings in Maximum mode



Comparison of 8086 and 8088

8086 Microprocessor	8088 Microprocessor
8086 has 16-bit data lines.	8088 has 8-bit data lines.
8086 is available in three clock speed 5 MHz, 8 MHz and 10 MHz	Whereas 8088 is available in two clock speed 5 MHz and 8 MHz
The memory space of 8086 is organized as two 512KB banks.	The memory space of 8088 is implemented as single 1M*8 Memory bank.
8086 has 6-bit instruction queue.	8088 has4-bit instruction queue.
The 8086 has BHE (Bank high enable)	The 8088 has SSO status signal.
The 8086 can read or write 8-bit or 16-bit data at a time.	The 8088 can read/write 8-bit data at a time.
The I/O voltages level for 8086 is measured at 2.5 mA.	The I/O voltages level for 8086 is measured at 2 mA.
The 8086 draws maximum supply current of 360mA.	The 8086 draws maximum supply current of 340mA.