8-BIT DIGITAL TO ANALOG CONVERTER INTERFACE BOARD

(Model No :VBMB - 002)

Application Manual

Version 2.0

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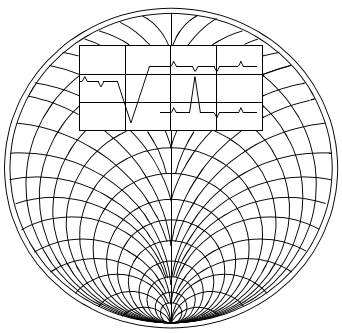

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CHAPTER -1

INTRODUCTION

In order to control medical instruments or automobiles or the machines in electronics factory, with a microprocessor based system, we need to determine the values of physical quantities such as temperature, pressure etc. These are represented by equivalent electrical quantities by means of transducers. These signals are called analog signals. Even though an analog signal may represent a real physical parameter with accuracy, it is difficult to process or store the analog signal for later use without introducing considerable error. Therefore in a microprocessor based control system, it is necessary to translate an analog signal into digital signal and vice versa. The electronic circuit that translates an analog signal into a digital signal is called an Analog-to-Digital or A/D Converter (ADC). Similarly the circuit that translates digital information to analog signal is called Digital-to-Analog converter or D/A Converter (DAC).

VBMB-002 contains two D/A converters using DAC0800. Using this add-on card you can learn in detail how to interface D/A converters with microprocessors. This card also consists of a comparator which can be used along with the D/A converter. Details about this is discussed later.

CHAPTER - 2

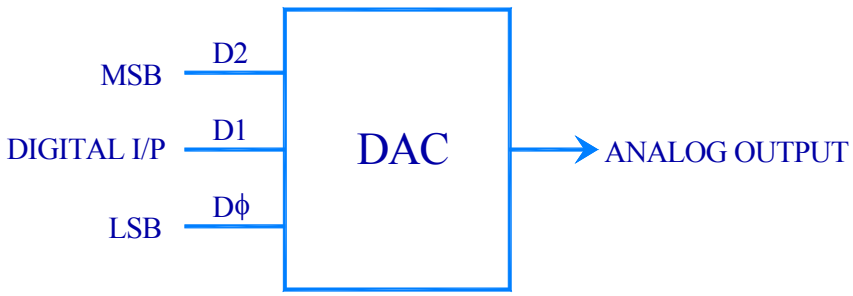
BASIC WORKING PRINCIPLE

2.1 D/A CONVERTERS - BASIC WORKING PRINCIPLE

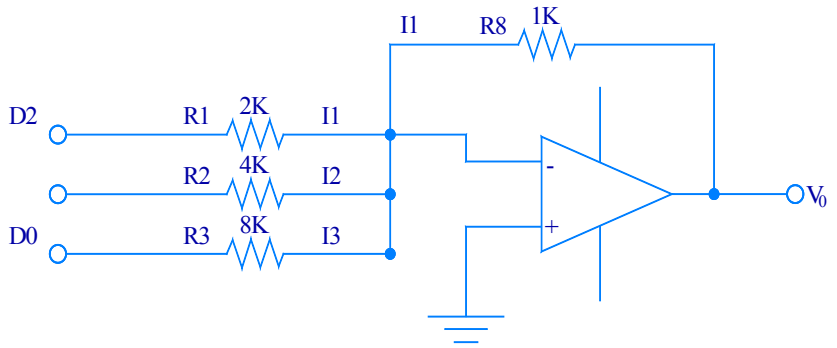
Digital-to-Analog converters can be classified as current output, voltage output and multiplying type. The current output DAC, provides current as the output signal. The voltage output DAC internally converters the current signal into voltage signal. The voltage output DAC is slower than the current output DAC because of the delay in converting the current signal in to voltage signal. The voltage output DAC is slower than the current signal into the voltage signal.

The multiplying DAC is similar to the other 2 types except its output represents the product of input signal and the reference source and the product is linear over a board range. Conceptually there is no difference between these three types; (i.e) any DAC can be viewed as a multiplying DAC. DACS specially designed to be compatible with microprocessors are available. Our add-on card uses one such DAC 0800, an 8-bit Digital-to-Analog Converter. Typical applications of DACS include digital voltmeters, peak detectors, panel meters, programmable gain and attenuation and stepping motor drive.

Figure-1 shows a simple 3 bit D/A converter. It has 3 digital input lines (D2,D1 and D0) and one output line for the analog signal. The 3 input signals can assume 8 combinations from 000 to 111. If the input ranges from 0 to 1 V it can be divided into 8 equal parts (1/8V) and each successive input is 1/8 V higher than the previous combination. Thus if the full-scale analog voltage is 1V, the smaller unit (LSB) or 001 is equivalent to 1/8 of 1V. The 100 (MSB) represents half of the full-scale value. For maximum input signal 111, the output signal is equal to the value of the full-scale input signal minus the value of the 1 LSB. So for a full scale voltage 1V, it will be 7/8V in the above example.



Input signals representing appropriate binary values can be simulated by an operational amplifier with a summing network as shown in Figure-2. If all the inputs are 1, the total current is 0.875 (7/8)mA or the voltage is 7/8 V.



$IT = I1+I2+I3$

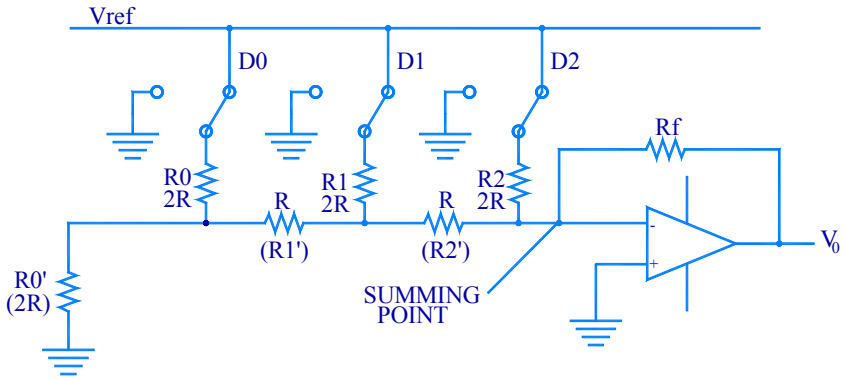
$= \frac{VIN}{1K}(1/2 + 1/4 + 1/8)$

$= 0.875(7/8)mA$ or $7/8mA$

$V0 = IT+Rf$

$= 0.875(7/8)V$ or $7/8V$

One major drawback of the above is the requirement for various precision resistors. Another method is to employ an R/2R ladder network as shown in fig.3.



Our board VBMB-002 is based on DAC 0800. Internally it consists of an R/2R ladder network. Details about the features of this IC and the interfacing of DAC with microprocessor is dealt in detail in the following chapter.

2.2 A/D CONVERSION METHODS

The A/D conversion is the process in which an analog signal is represented by equivalent binary states. Analog-to Digital converters can be classified into two general groups based on the conversion technique. One technique involves comparing a given analog signal with the internally generated equivalent signal. This group involves successive approximation, counter and flash-type converters. The second technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes integrator converters and voltage to frequency converters. The trade-off between the two techniques is based on accuracy Vs speed. The successive approximation and the flash type are faster but generally less accurate than the integrator and the voltage-to-frequency type converters. Furthermore, the flash type is expensive and difficult to design for high accuracy.

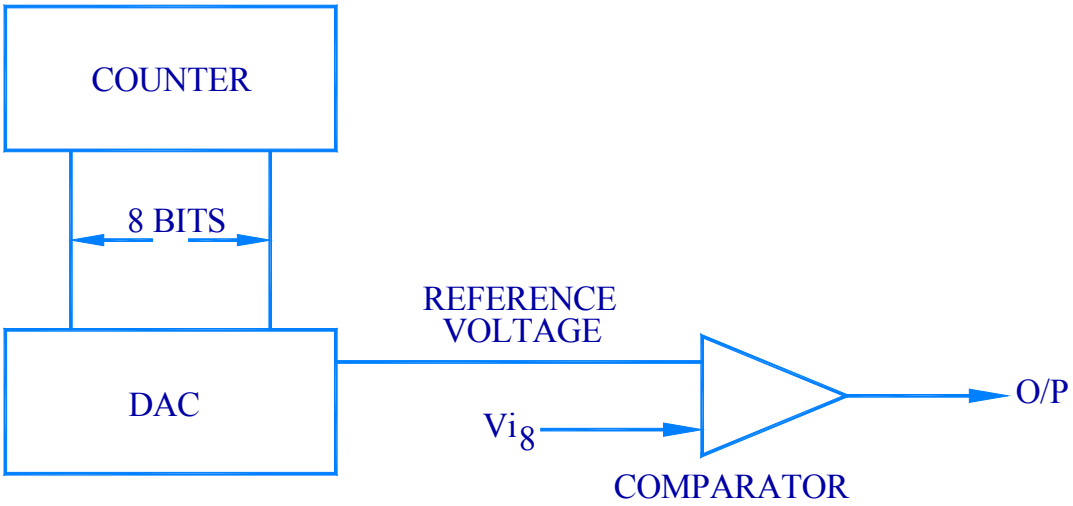
We will brief our discussion here on counter method and successive approximation method. Students are requested to refer to the suggested references in Appendix for more details.

2.2.1. A/D CONVERTER - COUNTER METHOD

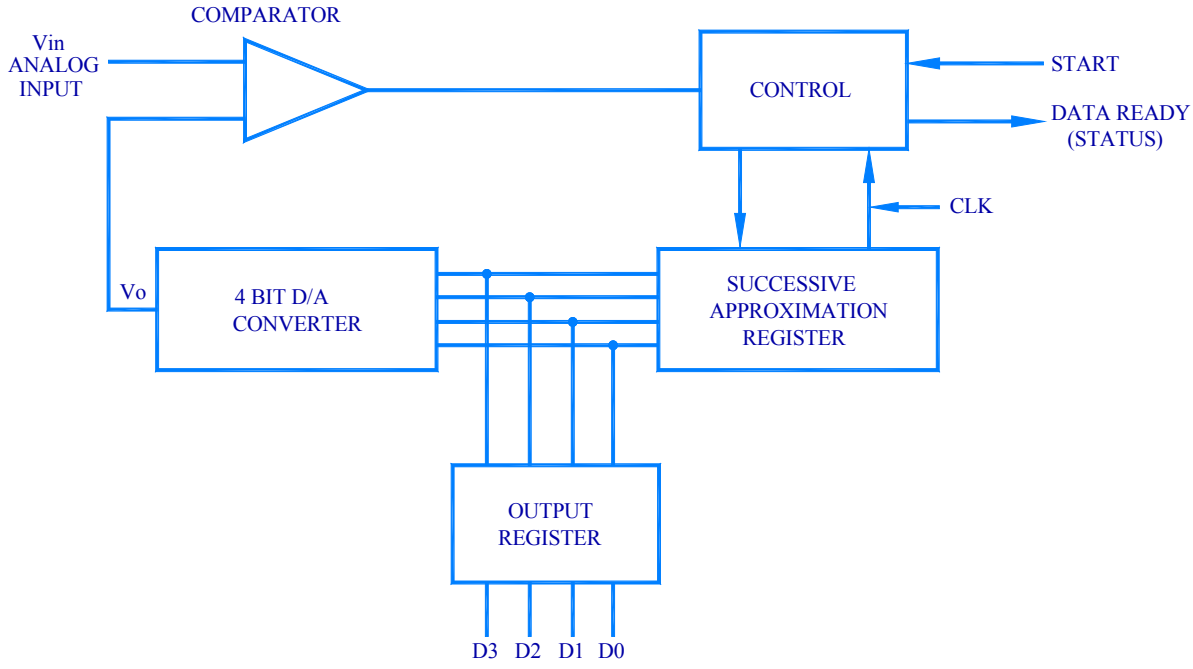
A high resolution A/D converter using a single comparator could be constructed with a variable reference voltage. This reference voltage could be applied to the comparator and when it become equals to the analog input voltage, the conversion would be complete. A counter can be used to generate the required reference voltage. The counter value is incremented until the DAC output is equal to the measured value. The content of the counter gives the equivalent binary for the measured voltage, refer Figure-4.

2.2.2. SUCCESSIVE APPROXIMATION TECHNIQUE

The disadvantage of the counter technique is the difference in time taken for conversion. When the measured voltage increases conversion becomes slower. Successive approximation technique is much faster. Block diagram for successive approximation ADC is shown in Figure-4.

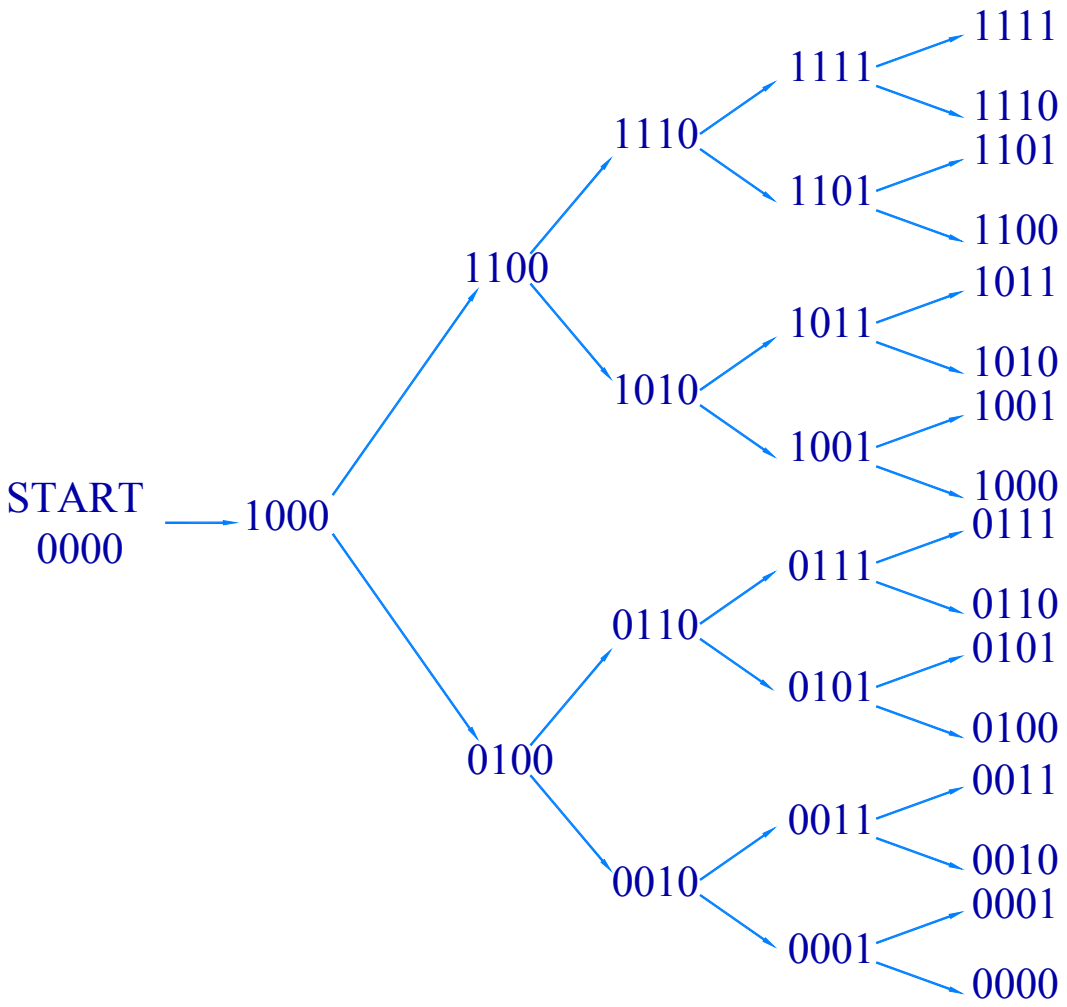


COUNTER TYPE A/D CONVERTER



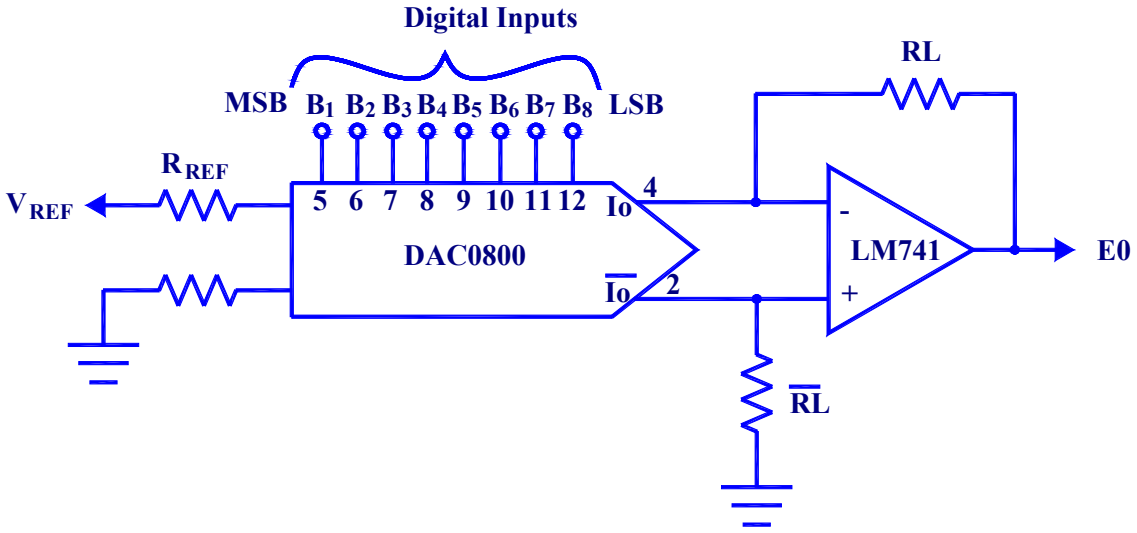
SUCCESSIVE APPROXIMATION A/D CONVERTER

This method similar to the counter method in that the measured voltage is compared with an internally generated reference voltage. But the method of creating the reference voltage is different. In this case for a 4 bit ADC shown in Figure-4, bit D3 is turned on first and the output of the DAC is compared with an analog signal. If the comparator changes state, indicating that the output generated by D3 is larger than the analog signal, bit D3 is turned off in the SAR and the bit D2 is turned on. The process continues until the input reaches bit D0. Figure-5 shows the chain.



Successive approximation process can be accomplished through either software or hardware approach. In the software approach, an A/D converter is designed using a D/A converter and the microprocessor plays the role of the counter and the SAR.

In our VBMB - 002 board we can design DAC0800 IC as shown in below figure.



Where as output can be expressed as,

$$E_0 = V_{REF}\left(\frac{-256}{256} \times \frac{2X}{256}\right)$$

X = Input code.

$$R_L = \overline{R_L} = R_{REF}$$

The output can be obtained from the following inputs,

	B1	B2	B3	B4	B5	B6	B7	B8	EO
Positive Full scale	1	1	1	1	1	1	1	1	+9.960
Positive full scale -LSB	1	1	1	1	1	1	1	0	+9.880
(+) zero scale	1	0	0	0	0	0	0	0	+0.040
(-) Zero scale	0	1	1	1	1	1	1	1	-0.040
Negative full scale +LSB	0	0	0	0	0	0	0	1	-9.880
Negative full scale	0	0	0	0	0	0	0	0	-9.960

CHAPTER - 3

CIRCUIT IMPLEMENTATION

The basic microprocessor board, VBMB-002, incorporates two 8-bit Digital-to-Analog converters, DAC 0800.

DAC 0800 is a monolithic, high speed, current output Digital to Analog converter. It's unique features are:

* Typical settling time of 100 Nanoseconds.
* Complementary current outputs.
* Differential output voltages of 20V peak-to-peak with simple resistor loads.
* 2-quadrant wide range multiplying capability.

The DAC interface section comprises of

i. I/O decoding

ii. D/A conversion circuit

3.1 I/O DECODING

The IC's 74LS138 and 74LS00 form the address decoding logic in this interface board. The address lines A3, A4 and A5 are tied to pin 1, pin 2 and pin 3 of 74LS138 respectively. The address lines A6 and A7 are NANDed together and the NAND gate output is connected to pin 5 of 74LS138. Similarly IOW and IOR signals are NANDed and the NAND gate output is connected to pin 6 of 74LS138. (Refer the circuit diagram in Appendix-A). Pin 4 is grounded.

Thus with

A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	1	X	X	X	= C8 (Hex)

DAC 1 is selected, and with

A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	0	X	X	X	= C0 (Hex)

3.2 D/A CONVERSION CIRCUIT

The design comprises of the latch 74LS273, DAC 0800 and the current to voltage converting circuitry using OP AMP 741. DAC 0800 is configured for bipolar output operation.

IC 74LS273 latches the 8-bit data on the data bus. The data latched by 74LS273 is input to DAC 0800. The DAC 0800 converters the 8-bit input and gives equivalent complementary current outputs.

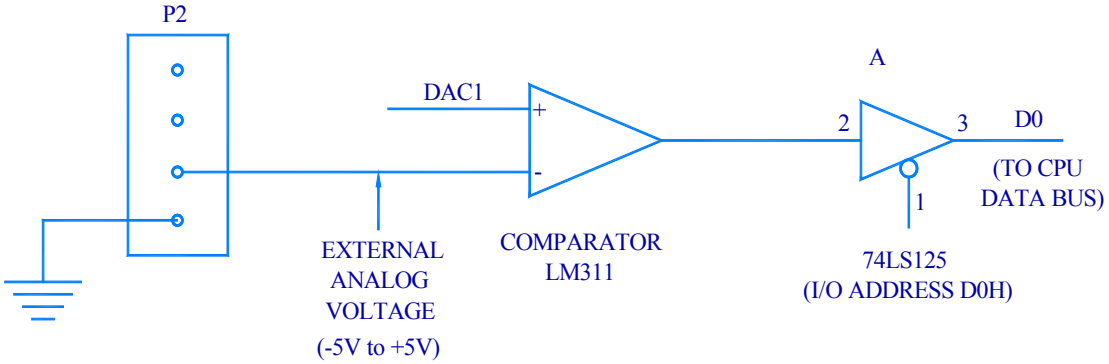
Current to voltage conversion circuit is designed using OP AMP 741. This circuit converters the current output of DAC 0800 into equivalent analog voltage. Complementary current outputs Iout, Iout are connected to inverting and non-inverting inputs of OP AMP 741. In order to have the output voltage variation from -5 to +5V, a 2.2K feed back resistor has been selected.

The DAC outputs are available at the 4 pin J801 connector (p1). DAC 1 and DAC 2 outputs are terminated at pin 1 and pin 2 respectively. Pin 4 is connected to the ground.

The circuit diagram with connector pinout details and the component layout are given at the end of this application note.

3.3 A/D CONVERSION CIRCUIT

As you are now aware it is possible to construct an ADC using DAC if you have a register (Successive Approximation Register) or a counter and a comparator. We have also mentioned that in the software based A/D converter microprocessor can act as a counter or successive provided a comparator LM-311 in our card VBMB-002. The output of DAC channel 1 is given to one of the inputs of the comparator. You can given an analog voltage, between -5 to +5V to be converted to digital forms the other input. Figure-6 illustrates the arrangement in our card.



The comparator's output goes high when DAC 1 and the analog voltage are approximately equal. To check the buffer (U10) the output of which is connected to D0 line. The 74125 address is decoded as follows.

3.4 TEMPERATURE MEASUREMENT USING VBMB-002 AND ITB-005

A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	0	0	0	0	= D0H

In application of VBMB-002 is temperature measurement using ITB-005 is basically signal conditioning board with a thermocouple and AD-590 module. The AD-590 module gives a voltage from 0V to 5V for a rang of 0 to 100°C. For supplying power to ITB-005 board, +12V, -12V and +5V are taken out and terminated at connector P3 of ITB-002. You can connect this signal to the ADC input of connector P2 in VBMB-002. By writing appropriate software you can find out the equivalent hex value proportional to the temperature and display it. Example-6 in the following chapter illustrates this.

CHAPTER - 4

SOFTWARE EXAMPLES

After going through the software examples you can learn how to control the DAC using 8085 and generate sine wave, sawtooth wave etc by means of software. Same function can be done by using other microprocessors also. This is achieved simply by changing the software for corresponding CPU. The program for other micro processes are listed in the appendices.

4.1 EXAMPLE - 1

AIM To obtain a output of 0 volts at DAC1.

Since DAC 0800 is an 8-bit DAC and the output voltage variation is between -5V and +5V. The output voltage varies in steps of 10/256 = 0.04 (approx). The digital data input and the corresponding output voltages are presented in the following table.

Input Data in Hex	Output Voltage
00	-5.00
01	-4.96
02	-4.92
.	
.	
7F	0.00
.	
.	
.	
FD	4.92
FE	4.96
FF	5.00

Execute the following program and observe that the output voltage at DAC 1 is 0 Volts.

```
                    ORG     4100H
4100 3E     7F      MVI     A,7F
4102 D3     C0      OUT     0C0H
4104 76
```

4.2 EXAMPLE - 2

AIM

To generate square-wave at the DAC2 output.

The basic idea behind the generation of waveforms is the continuous generation of analog output of DAC.

With 00 (Hex) as input to DAC 2, the analog output is -5V. Similarly with FF (Hex) as input the output is +5V. Outputting digital data 00 and FF at regular intervals, to DAC2, results in a square wave of amplitude 15 Volts.

```
4100 3E    00        START: MVI    4100H
4102 D3    C8               OUT    0C8H
4104 CD    11 41            CALL   DELAY
4107 3E    FF               MVI    A, 0FF
4109 D3    C8               OUT    0C8H
410BCD     11 41            CALL   DELAY
410EC3     00 41            JMP    START
4111 06    05               MVI    B, 05
4113 0E    FF               MVI    C,0FF
4115 0D                     DCR    C
4116 C2    15 41            JNZ    L2
4119 05                     DCR    B
411AC2     13 41            JNZ    L1
411DC9                      RET
```

Execute the program and using a CRO, verify that the waveform at the DAC2 output is a square-wave. Modify the frequency of the square-wave, by varying the time delay.

4.3 EXAMPLE - 3

AIM

To create a Saw-Tooth wave at the output of DAC-1.

Output digital data from 00 to FF in constant steps of 01 to DAC 1. Repeat this sequence again and again. As a result a saw-tooth wave will be generated at DAC1 output.

```
4100                    ORG 4100H
4100              START:
4100  3E 00              MVI  A,00H
4102              L1:
4102  D3 C0              OUT  0C0H
4104  3C                 INR  A
4105  C2 02 41           JNZ  L1
4108  C3 00 41           JMP  START
```

4.4 EXAMPLE - 4

AIM

To generate Triangular waveform at DAC-2 output.

The following program will generate a triangular wave at DAC2 output. The program is self explanatory.

```
4100                    ORG 4100H
4100              START:
4100  2E 00              MVI  L,00H
4102              L1:
4102  7D                 MOV A,L
4103  D3 C8              OUT  0C8H
4105  2C                 INR  L
4106  C2 02 41           JNZ  L1
4109  2E FF              MVI  L,0FFH
410B              L2:
410B  7D                 MOV A,L
410C  D3 C8              OUT  0C8H
410E  2D                 DCR  L
410F  C2 0B 41           JNZ  L2
4112  C3 00 41           JMP  START
```

4.5 EXAMPLE - 5

AIM

To generate sine - wave at DAC-1 output.

A lookup table is provided in the program for sine-wave generation. Output data continuously to DAC1 from this lookup table. Verify using an CRO at DAC 1 output, that the waveform is a sine-wave. The data for lookup task is arrived by experiments.

```
4100                              ORG 4100H
4100                        START:
4100 21    10      41             LXI   H,4110H
4103 0E    46                     MVI   C,46H
4105                        LOP:
4105 7E                           MOV A,M
4106 D3    C0                     OUT   0C0H
4108 23                           INX   H
4109 0D                           DCR   C
410AC2     05    41               JNZ   LOP
410DC3     00    41               JMP   START
4110 7F    8A    95    A0
4114 AA     B5   BF    C8
4118 D1     D9   E0    E7
411CED      F2   F7    FA
4120 FC     FE   FF    FE
4124 FC     FA   F7    F2
4128 ED     E7   E0    D9
412CD1      C8   BF    B5
4130 AA     A0   95    8A
4134 7F     74   69    5F
4138 53     49   3F    36
413C2D      25   1D    17
4140 10     0B   01    04
4144 07     0B   10    17
4148 1D     25   2D    36
4150 3F     49   53    5F
4154 69     74
```

EXAMPLE-6 This Program optional one for Temperature controller unit

AIM

To write a program to control temperature for given set point using ON-OFF controller unit.

As explained in the earlier chapter you can interface VBMB-002 and ITB-005. Connect power connector of ITB-005 to connector P3 of VBMB-002. Connect the output of ITB 005 at P2 to ADC input (Pin no.3 of P2) in VBMB-002. Execute the following program. We are using simple counter method, to convert Analog signal to Digital signal.

PROGRAM

```
            DAC1        EQU  0C0H
            OUTPUT      EQU  0D0H

4100                INIT:
4100  3E FF                MVI  A,0FFH
4102  D3 C8               OUT   0C8H
4104                START:
4104  3E 00                MVI   A,00H
4106                REPEAT:
4106  47                   MOV B,A
4107  D3 C0                OUT  C0H
4109  DB D0                IN   D0H
410B  E6 01                ANI  01H
410D  C2 15 41             JNZ  FINAL
4110  78                   MOV A,B
4111  3C                   INR  A
4112  C3 06 41             JMP  REPEAT
4115                FINAL:
4115  78                   MOV A,B
4116  32 00 50             STA  5000H
4119  E6 0F                 ANI  0FH
411B  32 02 50             STA  5002H
```

```
411E   78          MOV A,B
411F   E6 F0          ANI   0F0H
4121   0F          RRC
4122   0F          RRC
4123   0F          RRC
4124   0F          RRC
4125   32 01 50    STA  5001H
4128   21 01 50    LXI   H,5001H
412B   3E 03       MVI   A,03H
412D   0E 08       MVI   C,08H
412F   CD 05 00    CALL0005
4132   3A 00 50    LDA  5000H
4135   FE C0       CPI   C0H
4137   DA 00 41    JC    INIT
413A   3E 7F       MVI   A,7FH
413C   D3 C8       OUT  0C8H
413E   C3 04 41    JMP  START
4141                END
```

[For the digital data 80 to FF equals to temperature 0 to 100 degree. Since Digital to analog converter is Bipolar one, we can add 80 (hexa decimal value) forgetting digital data corresponds to temperature.]

I.e. -5 Volt 0Volt +5Volt

00(hex) 80 FF

0 deg.C 100deg.C

The digital data to be outputted is configured as

$$Digital\ data\ for\ required\ voltage = \frac{80H + (RV * 7FH)}{5}$$

Rv = Required voltage corresponds to temperature.

Digital data to be outputted for required temperature,

Digital data for required temp = 80H+(Rt*7FH)/100

Rt = Required temperature in Deg.C

For example, for required 50 deg.C

Digital data = 80H+50*7FH/100

Formula for obtaining the temperature corresponds to the digital data displayed in the trainer kit is:

Temperature = (Hex data - 7F)*100/128[displayed in the trainer kit].

The characteristic of LM 311 is such that it goes high only when the I/P is a little bit higher than reference voltage. At the time the comparator output goes high, the actual digital input for DAC and the digital equivalent of measured voltage are not equal and they differ by one bit. So to get an error free result the count in DAC input is decremented, by one.

4.7 EXERCISES

1. Generate sine-waves at DAC 1 and DAC 2 output with different frequencies, simultaneously.

2. The two DAC's outputs can be used to control the X and Y deflection of an CRO. With the CRO in X-Y mode, can you create alphabets in the CRO screen ? And numerals? And messages? And if possible some figures?.

3. Give a voltage between -5V and +5V at pin 3 of P2. Write a program to find out the equivalent hex value by successive approximation method.

CHAPTER - 5

TESTING POINTS

Testing points have been provided to enable you to see the nature of the signals.

In this board (refer circuit diagram in Appendix-A), the two testing points T1 and T2 represent, the chip select signals derived from 3 to 8 decoder 74 LS138.

T1 - $\overline{CS\ 1}$ ▸ Clocks the latch 74LS273 (U5)

T2 - $\overline{CS\ 2}$ ▸ Clocks the latch 74LS273 (U6)

$\overline{CS\ 1}$ Signal becomes active when I/O read or write operation is performed on the device with the address C0H.

$\overline{CS\ 2}$ Signal becomes active when I/O read or write operation is performed on the device with the address C8H.

Execute the software examples presented in the previous section and simultaneously observe signals at the testing points T1 and T2 using a CRO.

Please refer to the Circuit Diagram (Appendix-A) and the Component Layout (Appendix-B) for more details.

APPENDIX - A

IC DATA SHEETS

National Semiconductor

September 2006

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications, while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs will accept a variety of logic levels. The performance and characteristics of the device are essentially unchanged over the ±4.5V to ±18V power supply range and power consumption at only 33 mW with ±5V supplies is independent of logic input levels.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively. For single supply operation, refer to AN-1525.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Application

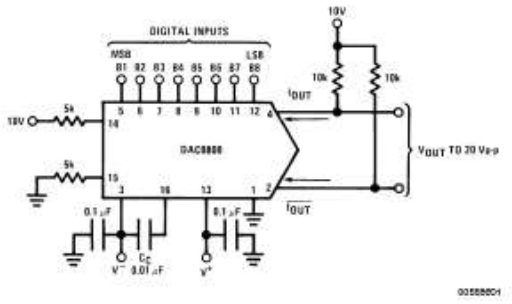


FIGURE 1. ±20 V_{p-p} Output Digital-to-Analog Converter (Note 4)

Ordering Information

Non-Linearity	Temperature Range (T_A)	Order Numbers				
		J Package (J16A) *		N Package (N16E) *		SO Package (M16A)
±0.1% FS	0°C to +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C to +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C to +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

* Devices may be ordered by using either order number.

 DS006686 www.national.com

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 2)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs ($V_{S^-} = -15V$)	4.25 mA
ESD Susceptibility (Note 3)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Note 1)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0802LC	0	+70	°C
V^+	$(V^-) + 10$	$(V^-) + 30$	V
V_-	−15	−5	V
I_{REF} ($V^- = -5V$)	1	2	mA
I_{REF} ($V^- = -15V$)	1	4	mA

Electrical Characteristics

The following specifications apply for $V_S = \pm15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25°C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A=25°C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ, Typical	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = R15 = 5.000 kΩ, T_A=25°C	1.984	1.992	2.00	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0	µA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	µA
I_{FSR}	Output Current Range	$V^- = -5V$	0	2.0	2.1	0	2.0	2.1	mA
		$V^- = -8V$ to $-18V$	0	2.0	4.2	0	2.0	4.2	

Electrical Characteristics (Continued)

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Logic Input Levels	$V_{LC} = 0V$							
V_{IL}	Logic "0"				0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	$V_{LC} = 0V$							
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	$V^- = -15V$	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	(*Figure 11*)	4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Positive Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$	Negative Power Supply Sensitivity	$-4.5V \le V^- \le 18V$, I_{REF} = 1mA		0.0001	0.01		0.0001	0.01	%/%
I+	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1$ mA		2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8	mA
I+	Power Supply Current	$V_S = +5V, -15V$, $I_{REF} = 2$ mA		2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8	mA
I+	Power Supply Current	$V_S = \pm 15V$, $I_{REF} = 2$ mA		2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Consumption	±5V, $I_{REF} = 1$ mA		33	48		33	48	mW
		+5V, −15V, $I_{REF} = 2$ mA		108	136		108	136	mW
		±15V, $I_{REF} = 2$ mA		135	174		135	174	mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

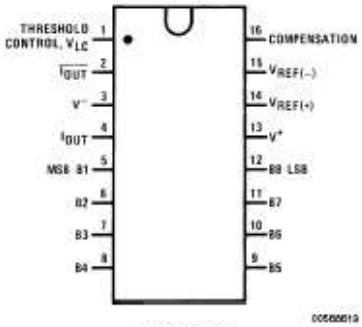
Note 2: The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 4: Pin numbers represent the Dual-In-Line package. The Small Outline package pin numbers differ from from that of the Dual-In-Line package.

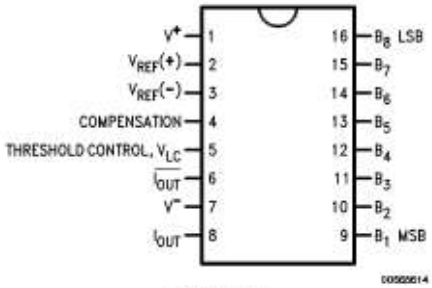
Connection Diagrams

Dual-In-Line Package



Top View

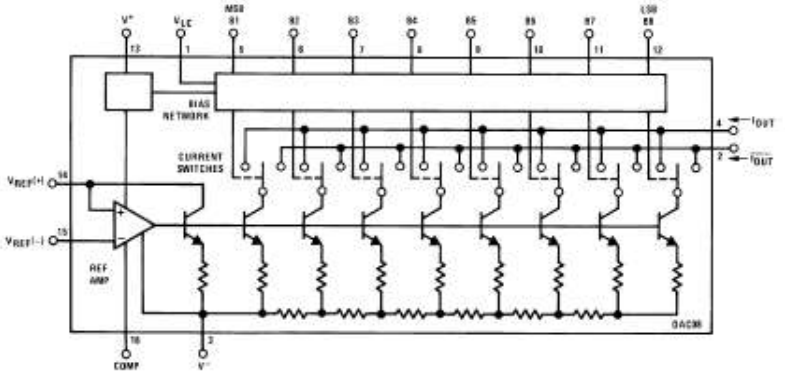
Small Outline Package



Top View

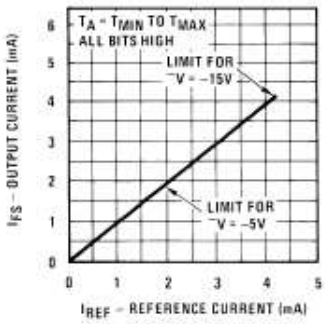
See Ordering Information

Block Diagram (Note 4)

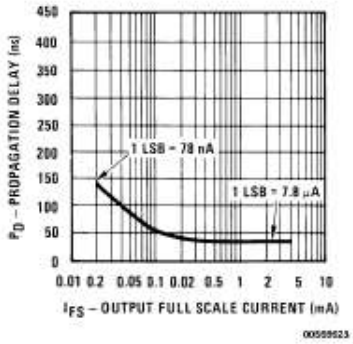


Typical Performance Characteristics

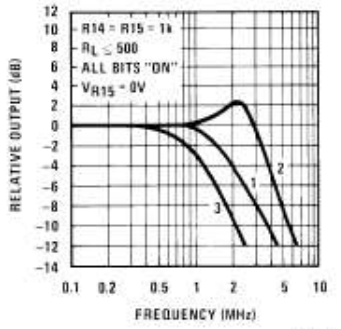
Full Scale Current vs. Reference Current



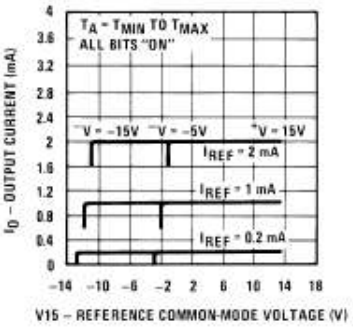
LSB Propagation Delay vs. I_{FS}



Reference Input Frequency Response



Reference Amp Common-Mode Range



Curve 1: C_C=15 pF, V_{IN}=2 Vp-p centered at 1V.

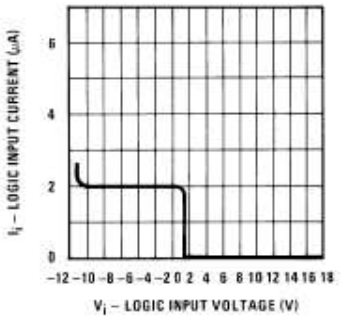
Curve 2: C_C=15 pF, V_{IN}=50 mVp-p centered at 200 mV.

Curve 3: C_C=0 pF, V_{IN}=100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

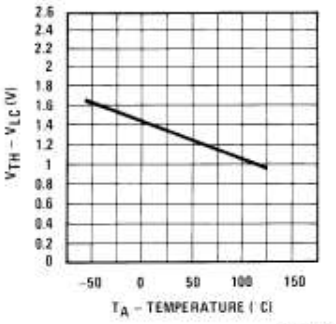
Note. Positive common-mode range is always (V+) – 1.5V.

Typical Performance Characteristics (Continued)

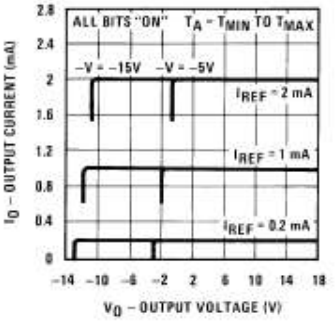
Logic Input Current vs. Input Voltage



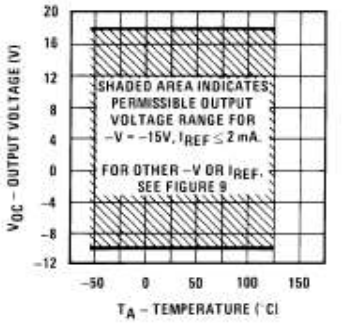
V_{TH} — V_{LC} vs. Temperature



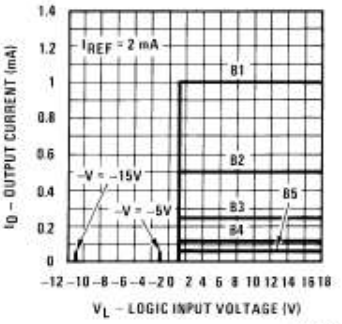
Output Current vs. Output Voltage (Output Voltage Compliance)



Output Voltage Compliance vs. Temperature

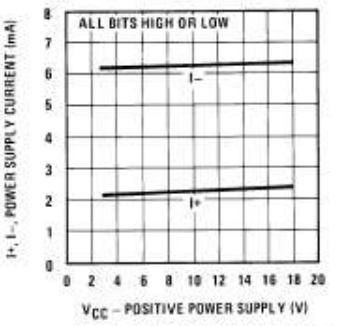


Bit Transfer Characteristics



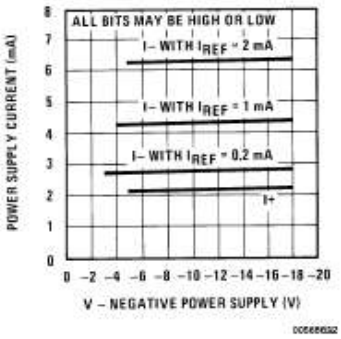
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Power Supply Current vs. +V

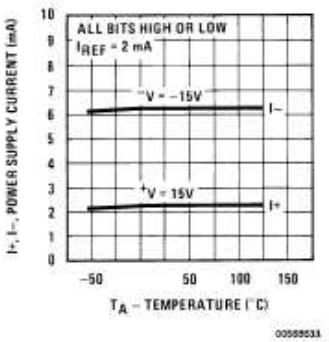


Typical Performance Characteristics (Continued)

Power Supply Current vs. –V



Power Supply Current vs. Temperature



Equivalent Circuit

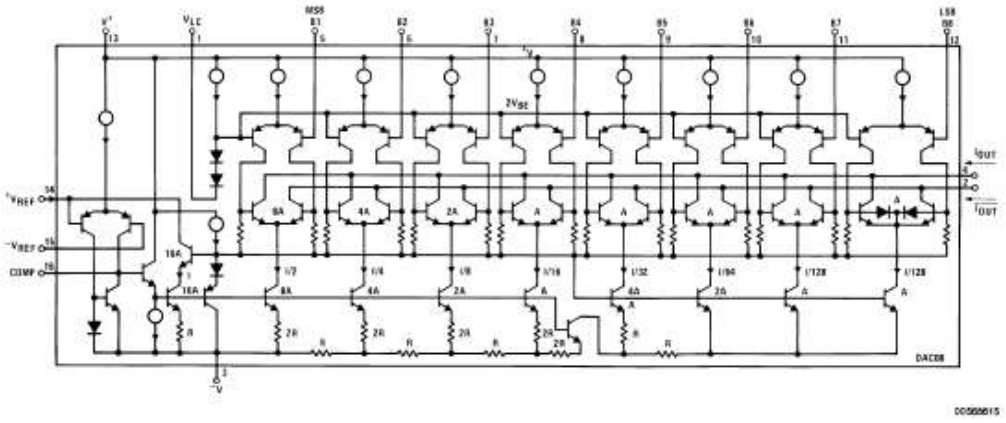
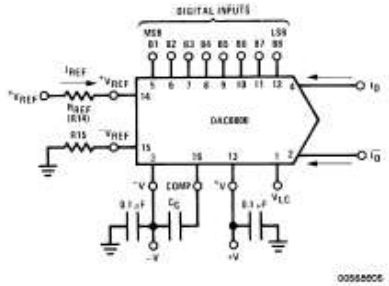


FIGURE 2. Equivalent Circuit

Typical Applications



$$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \bar{I}_O = I_{FS}$ for all logic states
For fixed reference, TTL operation, typical values are:
$V_{REF} = 10.000V$
$R_{REF} = 5.000k$
$R15 = R_{REF}$
$C_C = 0.01\ \mu F$
$V_{LC} = 0V$ (Ground)

FIGURE 3. Basic Positive Reference Operation (Note 4)

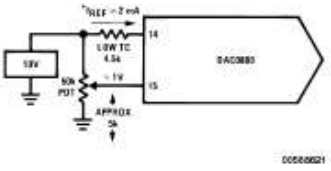


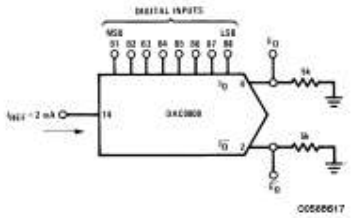
FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 4)

$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

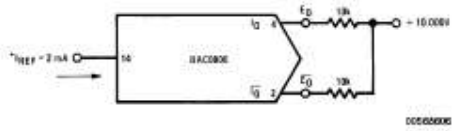
FIGURE 5. Basic Negative Reference Operation (Note 4)

Typical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I}_O$mA	E_O	$\overline{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

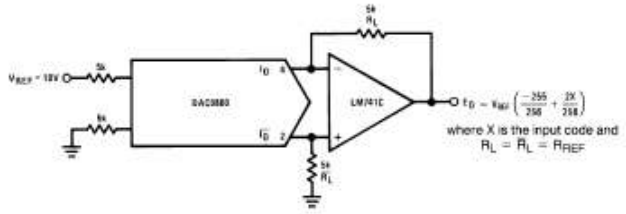
FIGURE 6. Basic Unipolar Negative Operation (Note 4)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

FIGURE 7. Basic Bipolar Output Operation (Note 4)

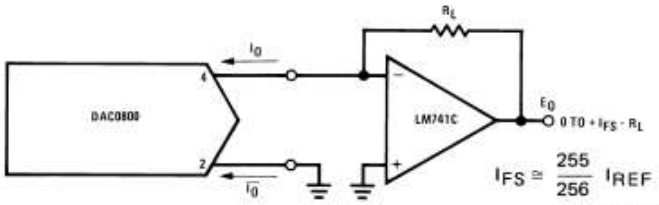
Typical Applications (Continued)



If $R_L = \overline{R}_L$ within ±0.05%, output is symmetrical about ground

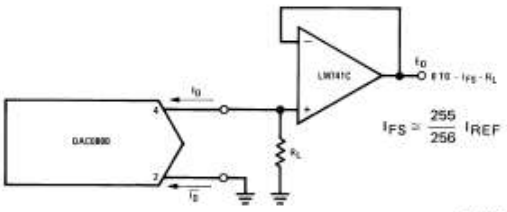
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale–LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(–)Zero Scale	0	1	1	1	1	1	1	1	–0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	–9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	–9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 4)



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I}_O$ (pin 2), connect I_O (pin 4) to ground.

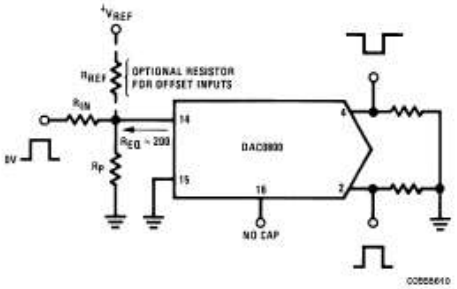
FIGURE 9. Positive Low Impedance Output Operation (Note 4)



For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to $\overline{I}_O$ (pin 2); connect I_O (pin 4) to ground.

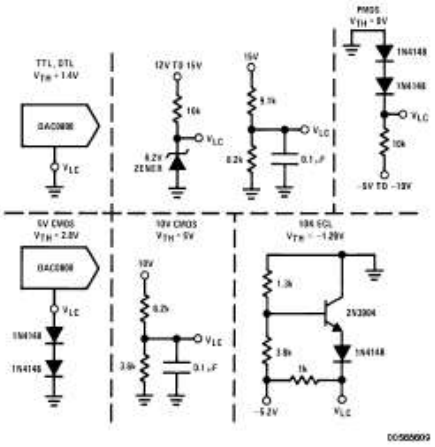
FIGURE 10. Low Impedance Negative Output Operation (Note 4)

Typical Applications (Continued)



Typical values: R_{IN}=5k, V_{IN}=10V

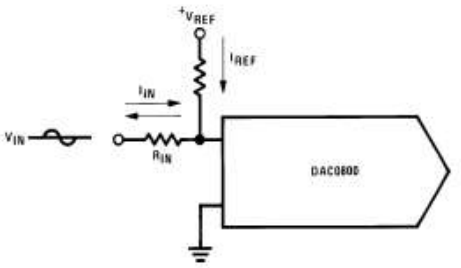
FIGURE 11. Pulsed Reference Operation (Note 4)



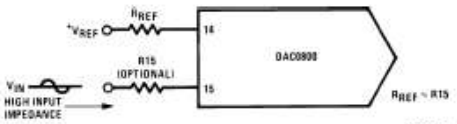
$V_{TH} = V_{LC} + 1.4V$
15V CMOS, HTL, HNIL
$V_{TH} = 7.6V$
Note. Do not exceed negative logic input range of DAC.

FIGURE 12. Interfacing with Various Logic Families

Typical Applications (Continued)



(a) $I_{REF} \geq$ peak negative swing of I_{IN}



(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

FIGURE 13. Accommodating Bipolar References (Note 4)

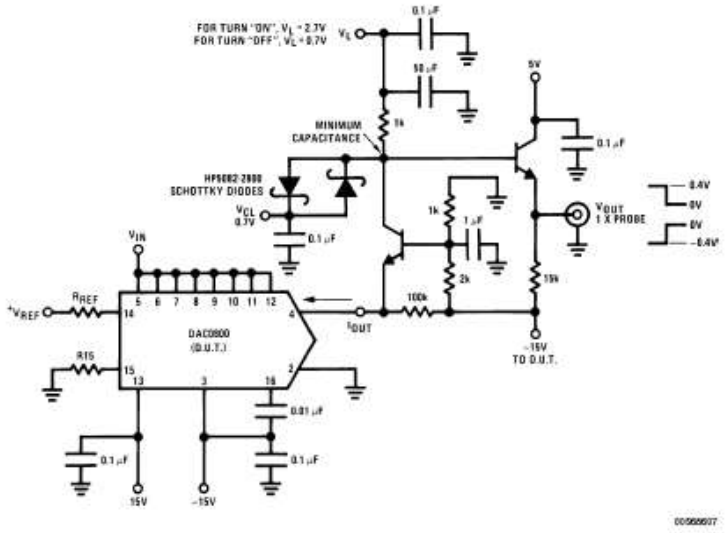
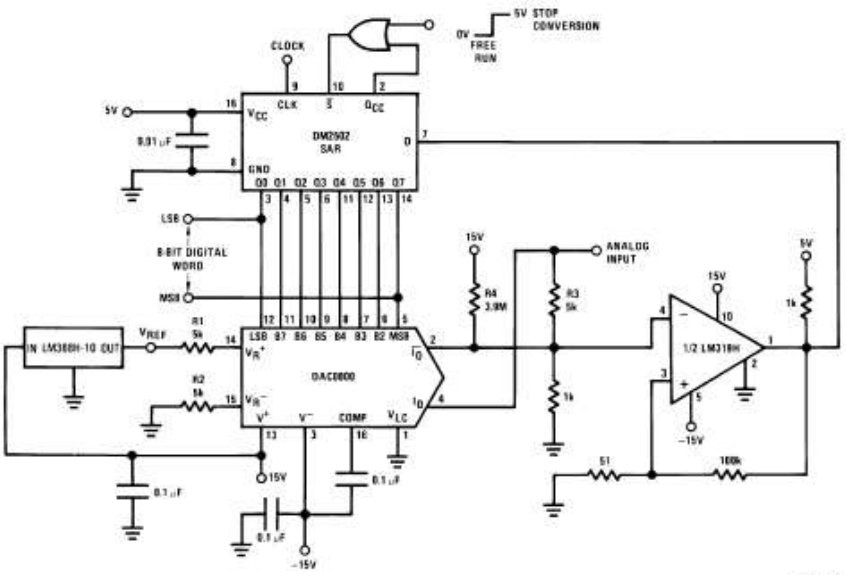


FIGURE 14. Settling Time Measurement (Note 4)

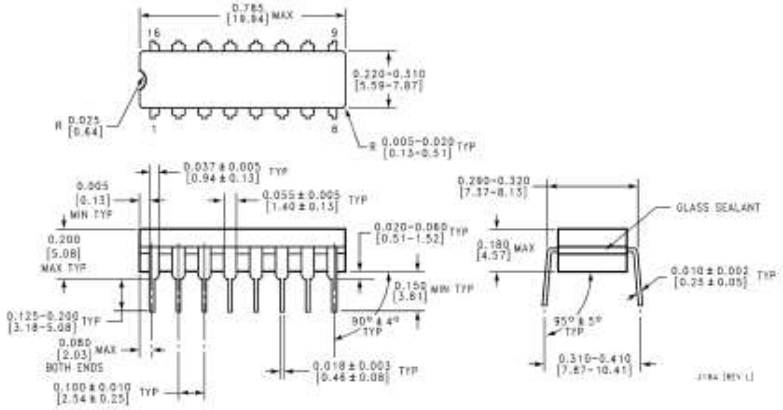
Typical Applications (Continued)



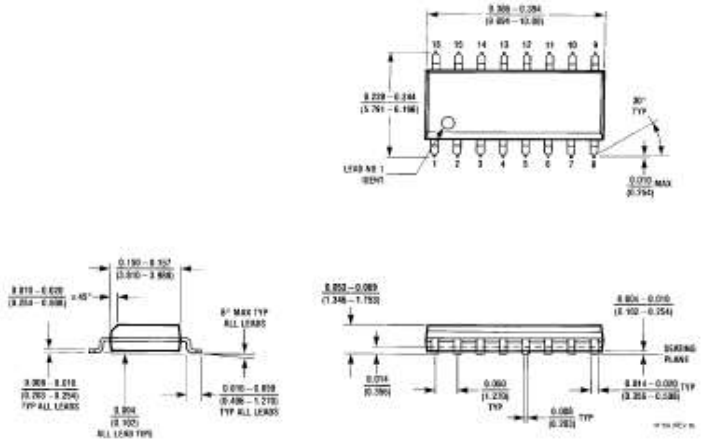
Note. For 1 µs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 15. A Complete 2 µs Conversion Time, 8-Bit A/D Converter (Note 4)

Physical Dimensions inches (millimeters) unless otherwise noted

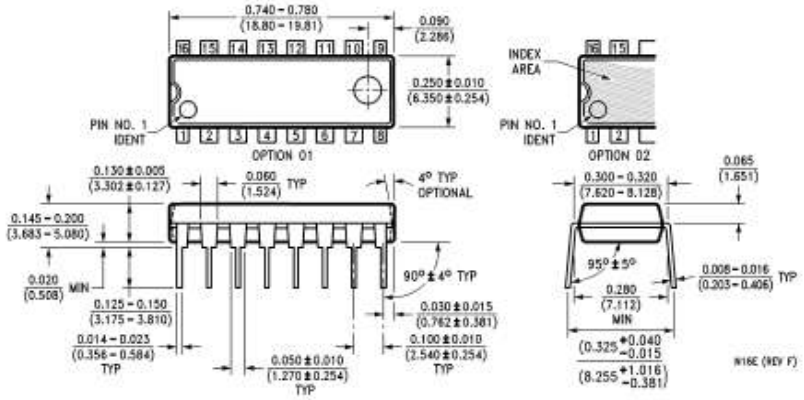


Molded Small Outline Package (SO)
Order Numbers DAC0800LCM,
or DAC0802LCM
NS Package Number M16A



Molded Small Outline Package (SO)
Order Numbers DAC0800LCM,
or DAC0802LCM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



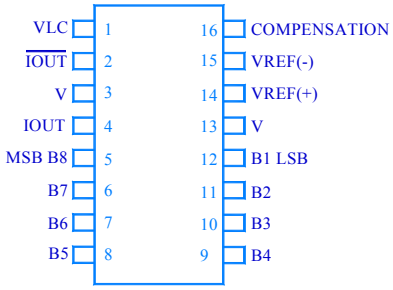
Molded Dual-In-Line Package
Order Numbers DAC0800, DAC0802
NS Package Number N16E

APPENDIX - B

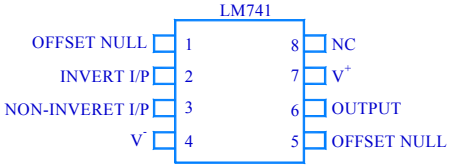
IC PINOUTS

DAC0800 - DIGITAL TO ANALOG CONVERTER

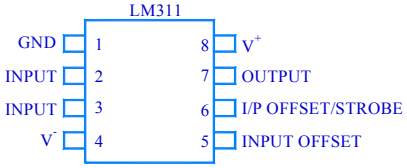
SIGNAL	INPUT/ OUTPUT	DESCRIPTION
B1-B8	I	DIGITAL INPUTS
VLC	I	THRESHOLD CONTROL
VREF(-) VREF(+)	I	REFERANCE VOLTAGES
IOUT $\overline{\text{IOUT}}$	O	COMPLEMENTARY CURRENT OUTPUTS
V^+		+12V POWER SUPPLY
V^-		-12V POWER SUPPLY



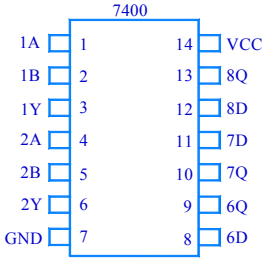
OPERATIONAL AMPLIFIER LM741



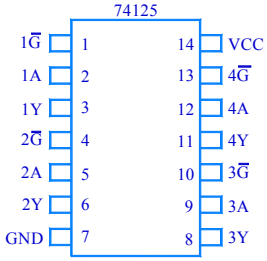
VOLTAGE COMPARATOR LM311



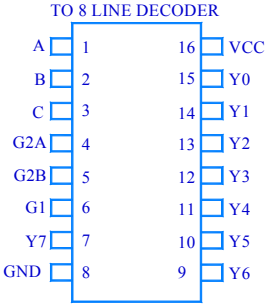
NAND GATE 7400



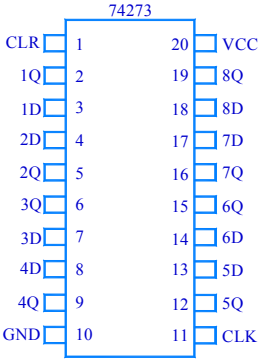
NAND GATE 74125



TO 8 LINE DECODER

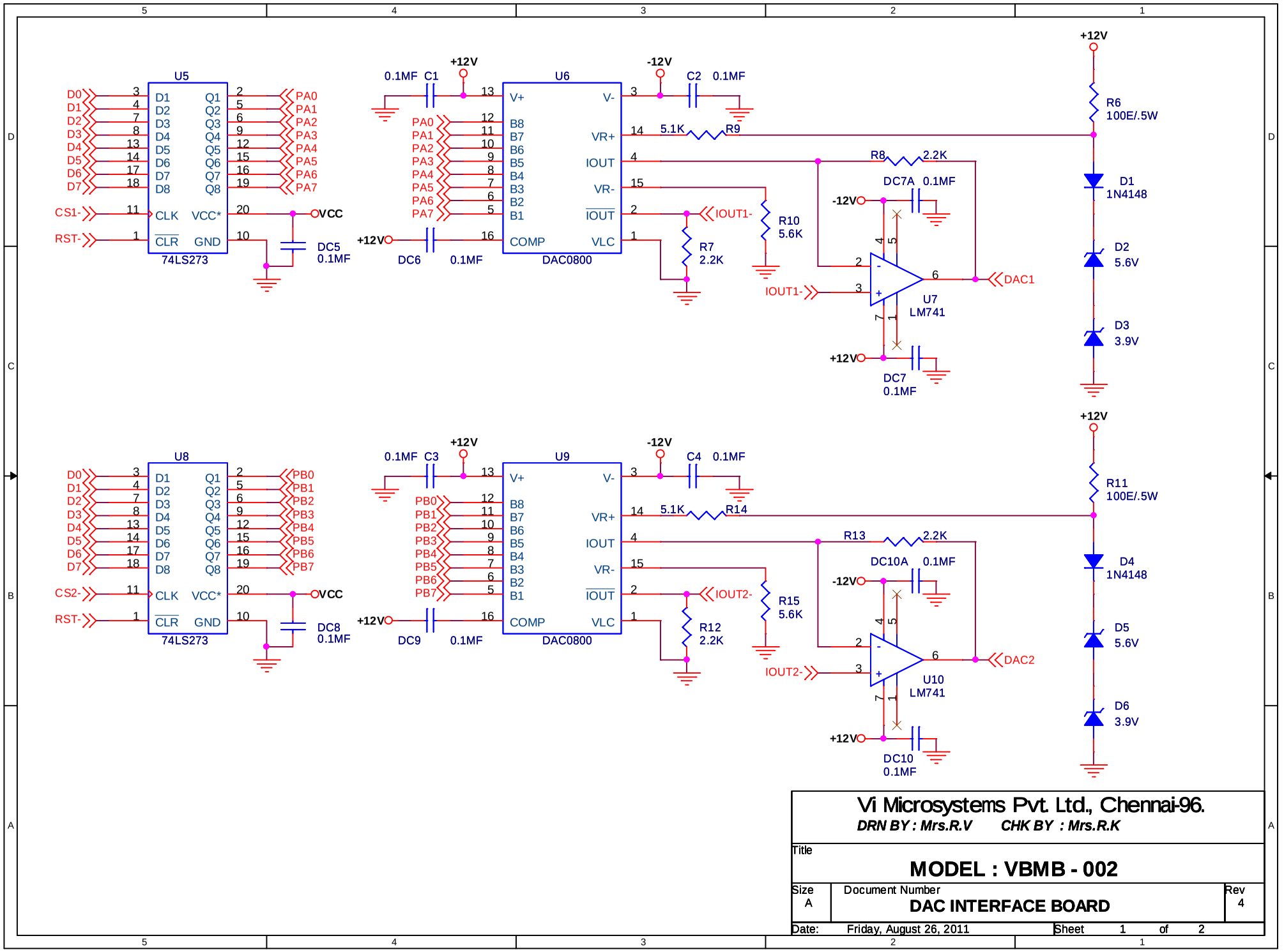


Quad-3-State Buffer 74273

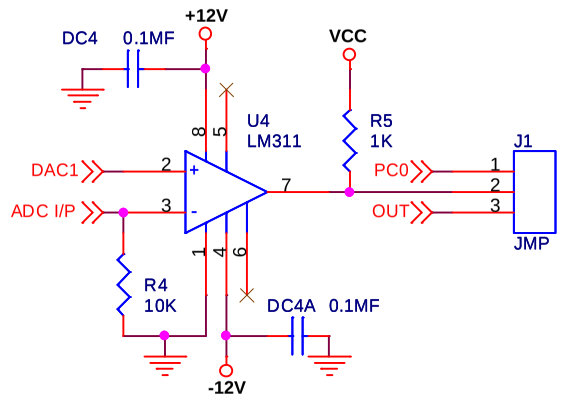


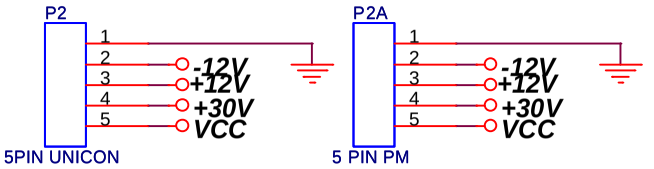
APPENDIX - C

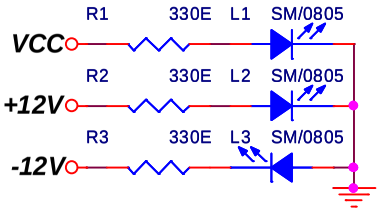
CIRCUIT DIAGRAM

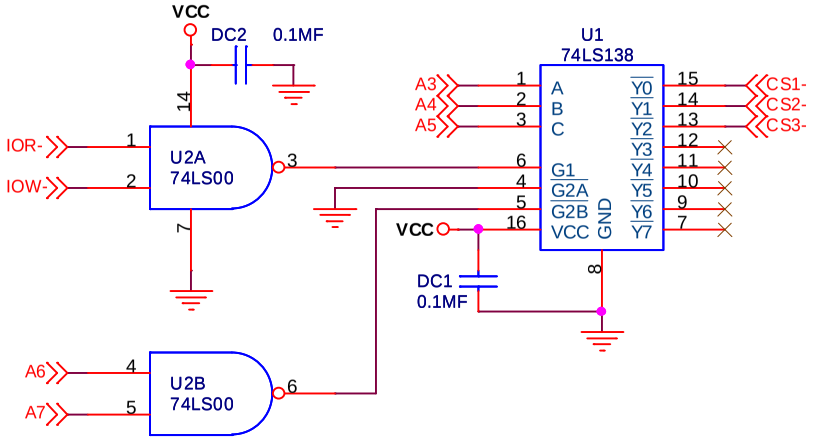


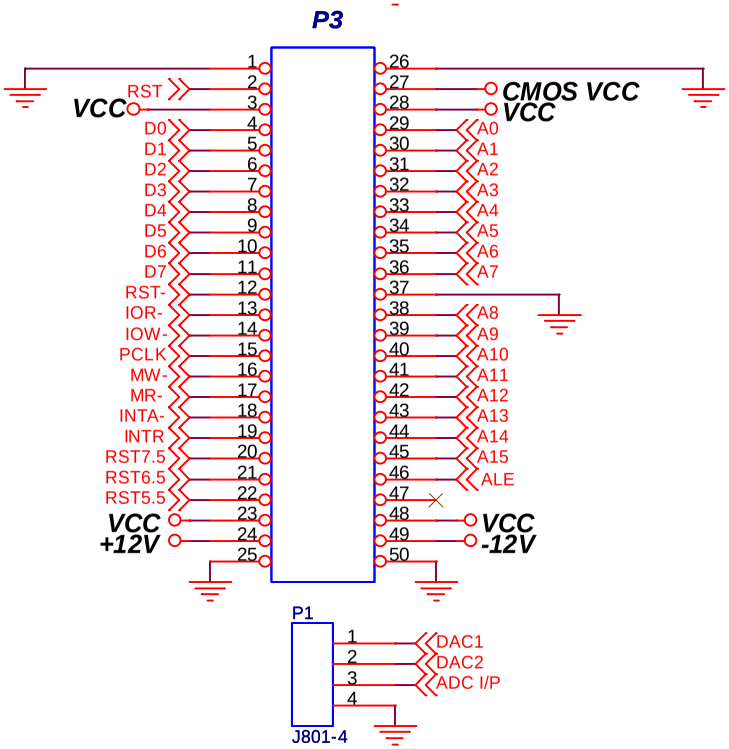
Vi Microsystems Pvt. Ltd., Chennai-96.		
DRN BY : Mrs.R.V	*CHK BY : Mrs.R.K*	
Title	**MODEL : VBMB - 002**	
Size A	Document Number **DAC INTERFACE BOARD**	Rev 4
Date: Friday, August 26, 2011	Sheet 1 of 2	

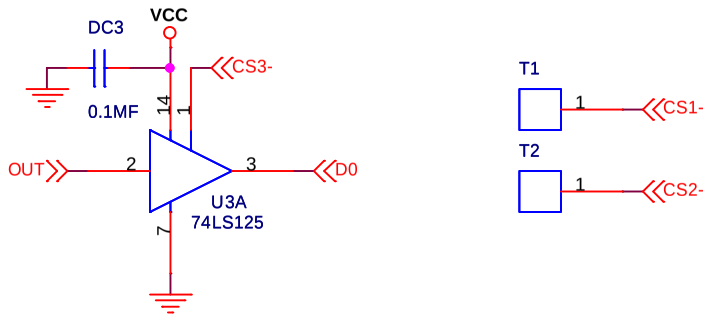








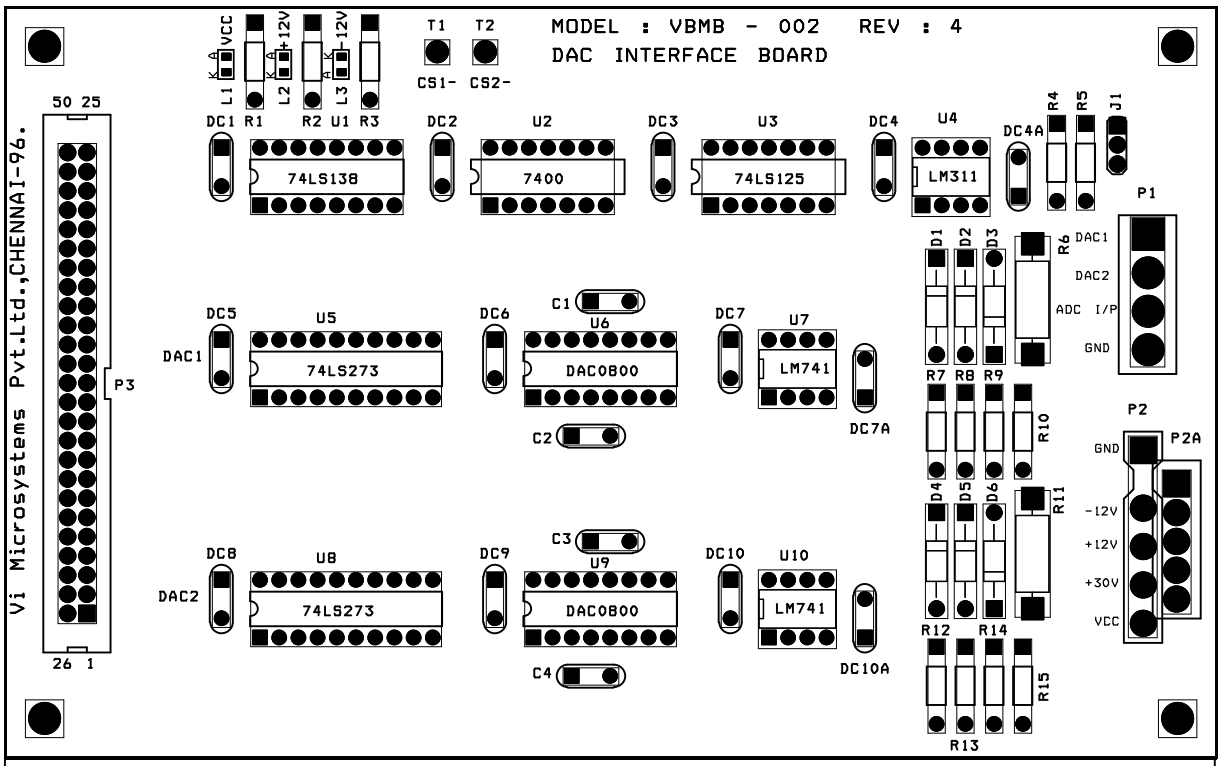




Vi Microsystems Pvt. Ltd., Chennai-96.		
DRN BY : Mrs.R.V *CHK BY : Mrs.R.K*		
Title: **MODEL : VBMB - 002**		
Size: A	Document Number: **DAC INTERFACE BOARD**	Rev: 4
Date: Thursday, August 25, 2011	Sheet 2 of 2	

APPENDIX - D

COMPONENT LAYOUT



LIST OF COMPONENT'S :-

IC'S : -

U1 - 74LS138(16PIN BASE)
U2 - 74LS00(14PIN BASE)
U3 - 74LS125(14PIN BASE)
U4 - LM311(8PIN BASE)
U5,U8 - 74LS273(20PIN BASE)
U6,U9 - DAC0800(16PIN BASE)
U7,U10 - LM741(8PIN BASE)

CONNECTOR'S :-

P1 - J801 4 PIN
P2 - 5PIN UNICON MALE
P2A - 5PIN POWER MATE
P3 - 50PIN FRC CONNECTOR

RESISTOR'S :-

R1,R2,R3 - 330E
R4 - 10K
R5 - 1K
R6,R11 - 100E/.5W
R7,R8,R12,R13 - 2.2K
R9,R14 - 5.1K
R10,R15 - 5.6K

CAPACITOR'S :-

C1,C2,C3,C4 - 0.1MF DISC
DC1-DC10,DC4A,DC7A,DC10A - 0.1MF DISC

OTHER COMPONENT'S :-

D1,D4 - 1N4148 DIODE
D2,D5 - 5.6V ZENER DIODE
D3,D6 - 3.9V ZENER DIODE
J1 - 3 PIN JUMPER
L1,L2,L3 - 0805 SMD SINGLE LED
T1,T2 - P8000 CONNECTOR

Vi Microsystems Pvt.Ltd.,CHENNAI-96.	
MODEL : VBMB - 002 DAC INTERFACE BOARD	
REV : 4 DATE : 26/08/11	COMPONENT LAYOUT SHEET 1 OF 1
DRN BY : Mrs.R.V	CHK BY : Mrs.R.K

APPENDIX - E

SOFTWARE EXAMPLES IN 8031 ASSEMBLY LANGUAGE

This appendix gives 6 experiments in 8031 assembly language to be done with VBMB-002 Revision 2. Port address specified in the examples are for Micro-51. For example port address for DAC 1 is given as EOCO. The same should be replaced by AOCO in MP-i with piggyback and FFCO in micro-31 eb. The ports and their addresses in the respective kits is shown in the table below.

PORT	MICRO-51	MICROPOWER -I	MICRO-31 eb
DAC 1 DAC 2	EOCO EOC8	AOCO AOC8	FFCO FFC8

1. To Obtain an Output of 0 Volts at DAC-1.

```
4100 74    3F              MOV    A,#3FH
4102 90 00 00              MOV    DPTR,#0E0C0
4105 F0                    MOVX   @DPTR,A
4106 80 FE          HERE:  SJMP   HERE
```

2. To Generate Square Waveform at DAC-2 Output.

```
4100 90 FF C8              MOV    DPTR,#0FFC8H
4103 74 00          START: MOV    A,#00H
4105  F0                   MOVX   @DPTR,A
4106 12 41 12              LCALL  DELAY
4109 74 FF                 MOV    A,#0FFH
410B    F0                 MOVX   @DPTR,A
410C    12 41 12           LCALL  DELAY
410F 02 41 03              LJMP   START
4112 79 05       DELAY:    MOV    R1,#05H
4114 7A FF       LOOP:     MOV    R2,#0FFH
```

```
4116 DA FE    HERE:    DJNZ    R2,HERE
4118 D9 FA             DJNZ    R1,LOOP
411A    22             RET
411B    80 E6          SJMP    START
```

3. To Create a Saw-tooth Waveform at the DAC-1 Output .

```
4100   90 FF C0          MOV     DPTR,#0FFC0H
4103   74 00               MOV     A,#00H
4105   F0         LOOP:   MOVX    @DPTR,A
4106   04                 INC     A
4107   80 FC              SJMP    LOOP
```

4. To Generate Triangular Waveform at DAC-2 Output.

```
4100   90 FF C8          MOV     DPTR,#0FFC8H
4103   74 00     START:   MOV     A,#00H
4105   F0         LOOP1:MOVX    @DPTR,A
4106   04                 INC     A
4107   70 FC              JNZ     LOOP1
4109   74 FF              MOV     A,#0FFH
410B   F0         LOOP2:MOVX    @DPTR,A
410C  14                  DEC     A
410D   70 FC               JNZ     LOOP2
410F 02 41 03              LJMP    START
```

5. To Generate Sine Wave at DAC-1 OUTPUT

```
4100   79 00      START:  MOV     R1,#00H
4102   7A 42              MOV     R2,#42H
4104   7B 46              MOV     R3,#46H
4106   89 82      LOOP:   MOV     DPL,R1
4108   8A 83              MOV     DPH,R2
410A   E0                 MOVX    A,@DPTR
410B   90 FF C0 LOOP2:  MOV     DPTR,#0FFC0H
410E   F0                 MOVX    @DPTR,A
410F   09          INC     R1
4110   DB F4              DJNZ    R3,LOOP
4112 02 41 00             LJMP    START
```

```
4200 7F 8A 95 A0
4204 AA B5 BF C8
4208 D1 D9 E0 E7
420C ED F2 F7 FA
4210 FC FE FF FE
4214 FC FA F7 F2
4218 ED E7 E0 D9
421C D1 C8 BF B5
4220 AA A0 95 8A
4224 7F 74 69 5F
4228 53 49 3F 36
422C 2D 25 1D 17
4230 10 0B 01 04
4234 07 0B 10 17
4238 1D 25 2D 36
423C 3F 49 53 5F
4240 69 74
4244 69 74
```

6.to Measure Temperature Using ITB-005 and VBMB-002.

```
4100   74 00          START:    MOV     A,#00H
4102   F8             REPT:   MOV     R0,A
4103   90 E0 C0                MOV     DPTR,#0E0C0H
4106   F0             LOOP:   MOVX    @DPTR,A
4107   90 00 00                MOV     DPTR,#0E0D0
410A   E0                      MOVX    A,@DPTR
410B   20 E0 04       LOOP2:    JB        ACC.0,FINAL
410E   E8                      MOV     A,R0
410F   04                      INC     A
4110   80 F0                   SJMP    REPT
4112   18             FINAL:  DEC     R0
4113   88 82                     MOV     DPL,R0
4115   74 02                     MOV     A,#02H
4117   79 02                     MOV     R1,#02H
4119   12 00 14                LCALL   0020
411C   80 E2                   SJMP    START
```

7. To Write a Program to Control Temperature for a Given Set Point Using On-off Controller Unit.

As explained in the earlier chapter you can interface VBMB-002 and ITB-005. Convert power connector of ITB-005 to connector P3 of VBMB-002. Connect the output ITB-005 at P2 to ADC input (pin no.3 of P2) in VBMB-002. Execute the following program. To display the data in the micro controller(LED) trainer Kit. This program utilized the function call facility available in the Monitor program. We are using simple counter method, to cover Analog Signal to Digital Signal.

```
        SYSTEM          EQU     4100H
        DAC1            EQU     0020H
        OUTPUT          EQU     0FFD0H
        DAC2            EQU     0FFC8H
        STORE           EQU     5000H
4100            INT:
4100  74 FF      INIT:     MOV     A,#0FFH
4102  90 FF C8              MOV     DPTR,#0FFC8H
4105  F0                    MOVX    @DPTR,A
4106  74 00      START:       MOV     A,#00H
4108  F5 F0      REPEAT:   MOV     B,A
410A  90 FF C0              MOV     DPTR,#0FFC0H
410D  F0                    MOVX    @DPTR,A
410E  90  FF D0             MOV     DPTR,#0FFD0H
4111  E0                    MOVX    A,@DPTR
4112  54 01                   ANL     A,#01H
4114  70 05                   JNZ     FINAL
4116  E5 F0                 MOV     A,B
4118  04                    INC     A
4119  80 ED                 SJMP    REPEAT
411B  E5 F0      FINAL:    MOV     A,B
411D  90 50 00              MOV     DPTR,#5000H
4120  F0                    MOVX    @DPTR,A
4121  54 0F                 ANL     A,#0FH
4123  90 50 01              MOV     DPTR,#5000+1H
4126  F0                    MOVX    @DPTR,A
4127  E5 F0                 MOV     A,B
4129  54 F0                 ANL     A,#0F0H
```

```
412B  C4          SWAP  A
412C  90 50 02    MOV   DPTR,#5000+2H
412F  F0          MOVX  @DPTR,A
4130  74 02           MOV   A,#02H
4132  79 00           MOV   R1,#00H
4134  75 F0 00    MOV   B,#00H
4137  90 50 00    MOV   DPTR,#5000H
413A  12 00 20    LCALL 0020H
413D  C3          CLR   C
413E  90 50 00    MOV   DPTR,#5000H
4141  E0          MOVX  A,@DPTR
4142  94 C0       SUBB  A,#0C0H
4144  40 BA       JC    INIT
4146  74 7F       MOV   A,#7FH
4148  90 FF C8    MOV   DPTR,#0FFC8H
414B  F0          MOVX  @DPTR,A
414C  80 B8       SJMP  .START
                  END
```

APPENDIX – F

SOFTWARE EXAMPLES IN 8086 ASSEMBLY LANGUAGE

1. To Obtain the Output of 0 Volts at DAC-1.

```
1000 B0   7F          MOV     AL,7FH
1002 E6   C0          OUT     0C0H,AL
1004 F4               HLT
```

2. To Generate Square Waveform at DAC-2 Output.

```
1000                START:
1000 B0 00                  MOV    AL,00H
1002 E6 C8                  OUT    0C8H,AL
1004 E8 09 00               CALL   DELAY
1007 B0 FF                  MOV    AL,0FFH
1009 E6 C8                    OUT    0C8H,AL
100BE8 02 00                CALL   DELAY
100EEB F0                   JMP    START
1010                DELAY:
1010 B9  FF 05               MOV    CX,05FFH
1013                LOP:
1013 E2  FE                 LOOP   LOP
1015 C3                      RET
```

3. To Create a Saw-tooth Waveform at the DAC-1 Output.

```
1000            START:
1000 B0 00                  MOV    AL,00H
1002            LOP:
1002 E6 C0                  OUT    0C0H,AL
1004 FE C0                  INC    AL
1006 75  FA                 JNZ    LOP
1008 EB F6                  JMP    START
```

4. To Generate Triangular Waveform at DAC-2 Output.

```
1000            START:
1000 B3 00                  MOV     BL,00H
1002            LOP:
1002 88 D8                  MOV     AL,BL
1004 E6 C8                  OUT      0C8H,AL
1006 FE C3                  INC     BL
1008 75 F8                  JNZ     LOP
100AB3 FF                   MOV     BL,0FFH
100C                LOPP:
100C8A C3                   MOV     AL,BL
100EE6 C8                   OUT     0C8H,AL
1010 FE CB                  DEC     BL
1012 75 F8                  JNZ     LOPP
1014 EB EA                  JMP      START
```

5. To Generate Sine Wave at DAC-1 Output

```
1000            START:
1000 BB 00 11               MOV     BX,1100H
1003 B1 46                  MOV     CL,46H
1005            LOOP:
1005 8A 07                  MOV     AL,[BX]
1007 E6 C0                  OUT     0C0H,AL
1009 43                     INC     BX
100AE2 F9                   LOOP    LOP
100CEB F2                   JMP      START
1100 7F 8A 95 A0
1104 AA B5 BF C8
1108 D1 D9 E0 E7
110CED F2 F7 FA
1110 FC FE FF FE
1114 FC FA F7 F2
1118 ED E7 E0 D9
111CD1 C8 BF B5
1120 AA A0 95 8A
1124 7F 74 69 5F
1128 53 49 3F 36
```

```
112C 2D 25 1D 17
1130 10 0B 01 04
1134 07 0B 10 17
1138 1D 25 2D 36
1140 3F 49 53 5F
1144 69 74
```

6. To Measure Temperature Using ITB-005 and VBMB-002 and Measure the Proportional Hex Value at Location

```
1000                START:
1000  B0 00                 MOV     AL,00H
1002                LOP:
1002  88 C3                 MOV     BL,AL
1004  E6 C0                 OUT     0C0H,AL
1006  E4 D0                 IN      AL,0D0H
1008  24 01                 AND     AL,01H
100A  75 06                 JNZ     LOP1
100C  88 D8                 MOV     AL,BL
100E  FE C0                 INC     AL
1010  EB F0                    JMP     LOP
1012                LOP1:
1012  88 D8                 MOV     AL,BL
1014  BB 00 11              MOV     BX,1100H
1017  88 07                 MOV     [BX],AL
1019  F4                       HLT
```

APPENDIX – G

SOFTWARE EXAMPLES IN 86/88EB LCD ASSEMBLY LANGUAGE

1. To Obtain the output of 0 volts at DAC-1.

```
1000  C6 C0 7F          MOV    AL,7FH
1003  E6 C0             OUT    0C0H,AL
1005  F4                HLT
```

2. To Generate Square Waveform at Dac-2 Output.

```
1000                START:
1000  C6 C0 00              MOV    AL,00H
1003  E6 C8                 OUT    0C8H,AL
1005  E8 0B 00              CALL   DELAY
1008  C6 C0 FF              MOV    AL,0FFH
100B  E6 C8                 OUT    0C8H,AL
100D  E8 03 00              CALL   DELAY
1010  E9 ED FF              JMP    START
1013                DELAY:
1013  C7 C1 FF 05           MOV    CX,05FFH
1017                 LOP:
1017  E2 FE                  LOOP   LOP
1019  C3                    RET
```

3.To create a saw-tooth waveform at the DAC-1 output.

```
1000            START:
1000  C8 C0 00          MOV AL,00H
1003            LOP:
1003  E6 00             OUT 0C0H,AL
1005  FE C0             IN  CAL
1007  75 FA             JNZ LOP
1009  E9 F4 FF          JMP START
```

4.To generate triangular waveform at DAC-2 output.

```
1000              START:
1000  C6 C3 00             MOV BL,00H
1003              LOP:
1003  88 D8                MOV AL,BL
1005  E6 C8                OUT  0C8H,AL
1007  FE C3                INC   BL
1009  75 F8                JNZ   LOP
100B  C6 C3 FF                MOV BL,0FFH
100E                LOPP:
100E  88 D8                MOV AL,BL
1010  E6 C8                OUT  0C8H,AL
1012  FE CB                DEC  BL
1014  75 F8                JNZ   LOPP
1016  E9 E7 FF             JMP  START
```

5. To generate sine wave at DAC-1 output

```
1000              START:
1000  C7 C3 00 11          MOV   BX,1100H
1004  C6 C1 46             MOV   CL,46H
1007              LOP:
1007  8A 07                MOV   AL,[BX]
1009  E6 C0                OUT   0C0H,AL
100B  43                   INC    BX
100C  E2 F9                LOOP LOP
100E  E9 EF FF             JMP    START

1100 7F 8A 95 A0
1104 AA B5 BF C8
1108 D1 D9 E0 E7
110C ED F2 F7 FA
1110 FC FE FF FE
1114 FC FA F7 F2
118   ED E7 E0 D9
111C D1 C8 BF B5
1120 AA A0 95 8A
1124 7F 74 69 5F
```

```
1128 53 49 3F 36
112C 2D 25 1D 17
1130 10 0B 01 04
1134 07 0B 10 17
1138 1D 25 2D 36
1140 3F 49 53 5F
1144 69 74
```

6. To measure temperature using ITB-005 and VBMB-002 and measure the proportional hex value at Location

```
1000                START:
1000  C6 C0 00             MOV     AL,00H
1003                LOP:
1003  88 C3               MOV     BL,AL
1005  E6 C0               OUT     0C0H,AL
1007  E4 D0               IN      AL,0D0H
1009  80 E0 01            AND     AL,01H
100C  75 07               JNZ     LOP1
100E  88 D8               MOV     AL,BL
1010  FE C0               INC     AL
1012  E9 EE FF                JMP     LOP
1015                LOP1:
1015  88 D8               MOV     AL,BL
1017  C7 C3 00 11         MOV     BX,1100H
101B  88 07               MOV     [BX],AL
101D  F4                    HLT
```

APPENDIX - H

SOFTWARE EXAMPLES IN 8097 ASSEMBLY LANGUAGE

This appendix gives the software examples in 8097 assembly language. The I/O addresses in 8097 based kits is given below.

EXAMPLE-1

To Obtain a output 0 Volts at DAC-1.

```
9000    A1 C0 FF 50          LD      50,#0FFC0H
9004    B1 7F 52             LDB     52,#7FH
9007    C6 50 52             STB     52,[50]
900A    27 FE          HERE: SJMP    HERE
```

EXAMPLE-2

To generate square waveform at DAC-2 output

```
                     START:
9000    A1 C8 FF 50          LD      50,#0FFC8H
9004    B1 00 52             LDB     52,#00H
9007    C6 50 52             STB     52,[50]
900A    EF 0C 00             LCALL   LOP
900D    A1 FF 00 54          LD      54,#00FFH
9011    C6 50 54             ST      54,[50]
9014    EF 02 00             LCALL   LOP
9017    27 E7                SJMP    START
                     LOP:
9019    B1 05 53             LDB     53,#05H
                     LOP1:
901C    A1 FF 00 56          LD      56,#00FFH
                     LOP2:
9020    05 56                DEC     56
9022    D7 FC                JNE     LOP2
9024    15 53                DECB    53
9026    D7 F4                JNE     LOP1
9028    F0                   RET
```

EXAMPLE - 3

To generate SAW-TOOTH waveform at DAC-1 output

```
                        START:
9000    A1 C0 FF 50             LD      50,#0FF50H
                        LOP1:
9004    B1 00 52                LDB     52,#00H
                        LOP:
9007    C6 50 52                STB     52,[50]
900A    17 52                   INCB    52
900C    D7 F9                   JNE     LOP
9000    DF F4                   JE      LOP1
```

EXAMPLE-4

To generate Triangular waveform at DAC-2 output.

```
                        START:
9000    A1 C8 FF 50             LD      50,#0FFC8H
                        LOP:
9004    B1 00 52                LDB     52,#00H
                        LOP1:
9007    B0 52 53                LDB     53,52
900A    C6 50 53                STB     53,[50]
900D    17 52                   DECB    52
900F    D7 F6                   JNE     LOP1
9011    A1 FF 00 52             LD      52,#0FFH
                        LOP2:
9015    A0 52 54                LD      54,52
9018    C6 50 54                STB     54,[50]
901B    05 52                   DEC     52
901D    D7 F6                   JNE     LOP2
901F    27 E3                   SJMP    LOP
```

EXAMPLE-5

To generate sine waveform at DAC-1 output

```
                    START:
9000    A1 00 91 50         LD      50,#9100H
9004    A1 C0 52            LD      52,#0FFC0H
9008    B1 46 54            LDB     54,#46H
                    LOP:
900B    B2 51 55            LDB     55,[50]+
900E    C6 52 55            STB     55,[52]
9011    15 54               DECB    54
9013    D7 F6               JNE     LOP
9015    27 E9               SJMP    START

 9100   7F 8A 95 A0
 9104   AA B5 BF C8
 9108   D1 D9 E0 E7
 910C   ED F2 F7 FA
 9210   FC FE FF FE
 9214   FC FA F7 F2
 9218   ED E7 E0 D9
 921C   D1 C8 BF B5
 9320   AA A0 95 8A
 9324   7F 74 69 5F
 9328   53 49 3F 36
 932C   2D 25 1D 17
 9430   10 0B 01 04
 9434   07 0B 10 17
 9438   1D 25 2D 36
 9540   3F 49 53 5F
 9544   69 74
```

APPENDIX - I

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