Computer Architecture

Lab #4

Luis Santos

Eberardo Sanchez

Kevin Valdez

Donato Kava

“GEFORCE MIPS CPU”

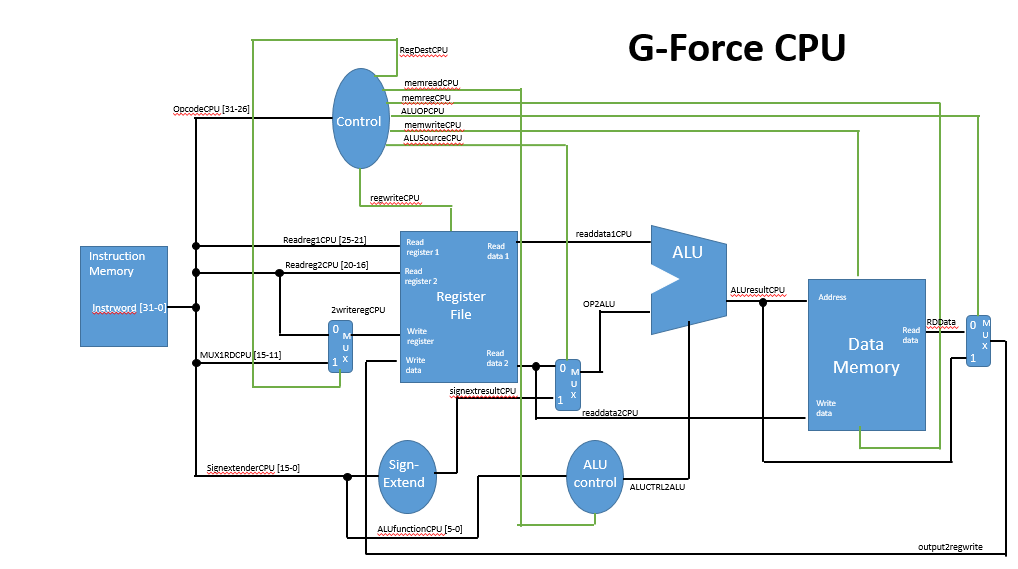
Inside the computer, the processor is the brain, and the CPU data path is the nervous system, the network of nerve cells and fibers that transmits impulses between parts of the body. Both brain and the nerve network are part of the same system and they work together to accomplish a goal, the same happens on the CPU, the data and control path work together so the necessary to process the data. We have to remember that the data path is “a collection of functional units, such as arithmetic logic units or multipliers, that perform data processing operations, registers, and buses. Along with the control unit it composes the central processing unit (CPU).”, so inside of the data path there is some other parts that work together, and we are going to refer to those parts as modules.

One of the modules that we were talking about is the arithmetic logic unit (ALU) in this project designed by Luis Santos, the ALU is a complex digital circuit that performs bitwise and mathematical operations on binary number and it’s the last component to perform calculations in the processor. The ALU uses operands and code that tells it which operation to perform for input data.

After the information, has been processed in this module, the data would be sent to the computer’s memory module made by Eberardo Sanchez. The memory register module its the part in the data path that holds of the memory location where the next instruction is to be executed. While the first instruction is being executed, the address of the next memory location is held by it.

Kevin Valdez was in charge of the register file and the sign extend. The register file is a collection of registers in which any register can be read or written by specifying the number of the register in the file. The register file contains the register state of the computer. The sign extend module takes the 16-bit offset field in the instruction and modify it to a 32-bit signed value by repeating the most significant bit until it completes the 32 bits.

The instruction memory was designed by Donato Kava, the instruction memory lets you define the test to be performed, or the test data register to be accessed, or both during boundary scan test. Each Instruction Register cell comprises a shift-register flip-flop and a parallel output latch. The shift registers hold the instruction bits moving through the Instruction Register. The latches hold the current instruction.



We also have the control unit that is responsible for setting all the control signals so that each instruction is executed properly, it directs the operation of the other units by providing timing and control signals.Most computer resources are managed by the CU. It directs the flow of data between the CPU and the other devices.  And also coordinates the sequence of data movements into, out of, and between a processor's many sub-units. The result of these routed data movements through various digital circuits (sub-units) within the processor produces the manipulated data expected by a software instruction.

The first step on the data path is the instruction fetch from the memory to know which instruction is next we need to decode it Part of the decoding process fetches the input operands. For example, if you have an add instruction that adds the contents of register 1 and 2, and places the result in register, then the values of register 1 and 2 need to be fetched to perform the addition. Then we move the data to the ALU that controls the sequential instruction, regulates and controls processor timing and sends and receives control signals from other computer devices. After this comes the memory that in terms for this design where we store data, the instruction memory takes address and supplies instructions, the data memory takes address and supplies data or takes address to write in the memory, this in a general aspect it’s how our single cycle CPU data path works.