

CSC258 lab4
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PRA0105

Truth table for SR latch

Initial state Q = HIGH, notQ = LOW

C	S	R	NotQ	Q
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1(forbidden)	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1(forbidden)	0	0

Initial state Q = LOW, notQ = HIGH

C	S	R	NotQ	Q
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1(forbidden)	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1(forbidden)	0	0

The diagram illustrates a 2-bit shift register implemented with two D flip-flops, labeled 'Dlatch'. The first flip-flop has inputs D₀ and C₀, both connected to a constant logic 0. Its Q output is connected to the D input of the second flip-flop. The clock input (C) of the second flip-flop is connected to the Q output of the first flip-flop through an inverter. The Q output of the second flip-flop is labeled Q₁.

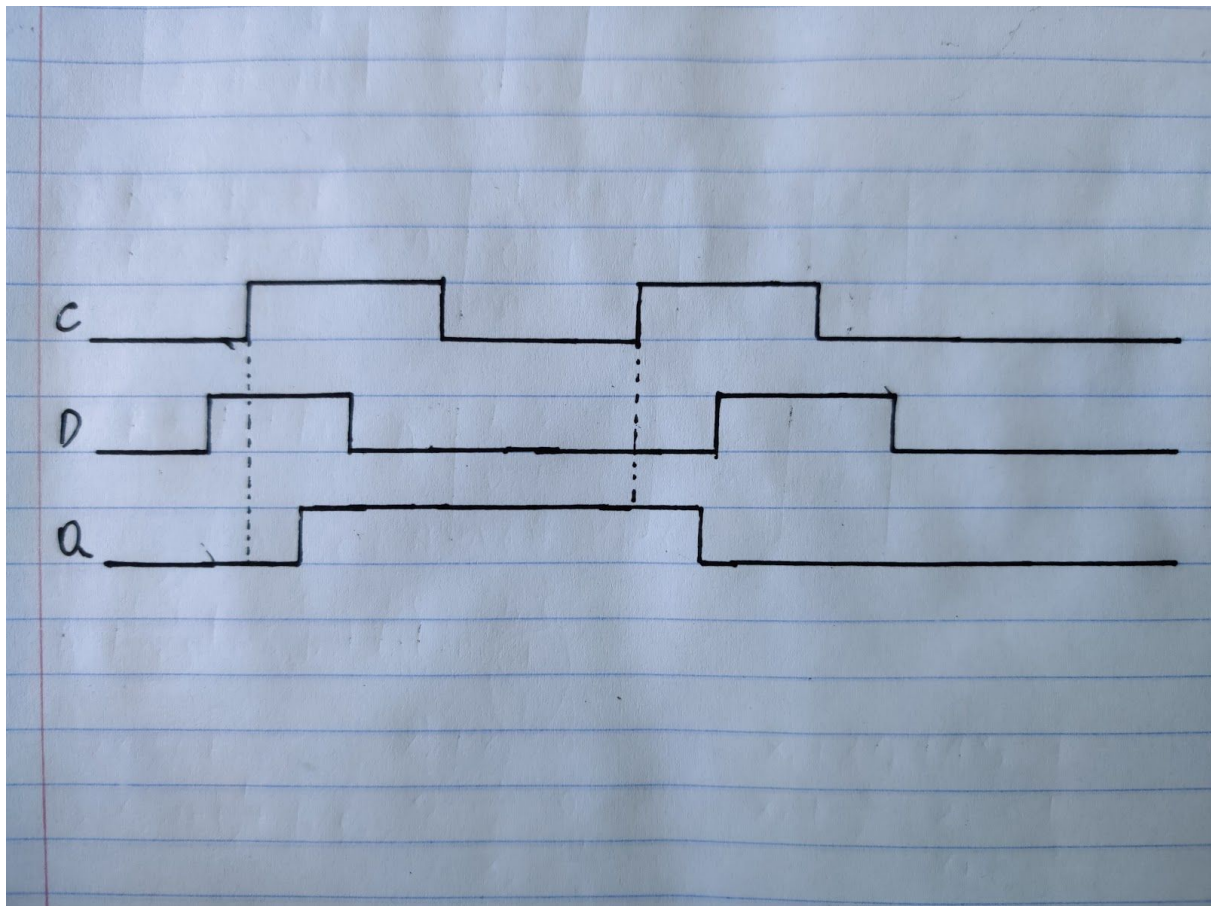
The timing diagram illustrates the operation of a 4-bit ripple-carry adder. The signals are:

- C**: Carry-in signal, which transitions from low to high at the start of the first clock cycle.
- S**: Sum signal, which is high during the first two clock cycles and low during the next two.
- R**: Ripple carry signal, which is high during the first two clock cycles and low during the next two.
- a**: Carry-out signal, which is high during the first two clock cycles and low during the next two.

The diagram shows the propagation of a carry through the stages of the adder, with the carry-in (C) and carry-out (a) signals being high during the first two clock cycles and low during the next two. The sum (S) and ripple carry (R) signals are high during the first two clock cycles and low during the next two.

When the clock signal is low, the output Q is not affected by the set S and reset R signal pulse. When the clock signal is high, the output Q is high when the set S pulse arrives, and the output is low when the reset R pulse arrives.

Waveform for D flip-flop



In this implementation of D flip-flop, the output Q is only triggered by the positive-edge of the clock signal. We can see that neither the positive-edge nor the negative-edge of D changes the output. It is whenever the positive-edge of C occurs and then the D signal is sampled to reflect on the output.