CSC258 lab4
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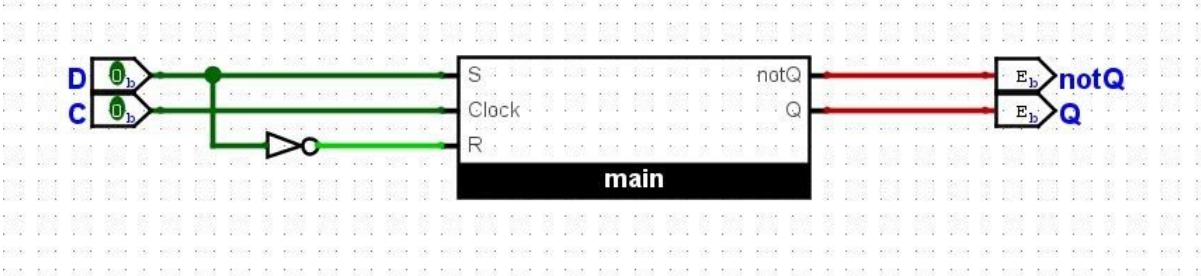
Truth table for SR latch
Initial state Q = HIGH, notQ = LOW

C	S	R	NotQ	Q
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1(forbidden)	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1(forbidden)	0	0

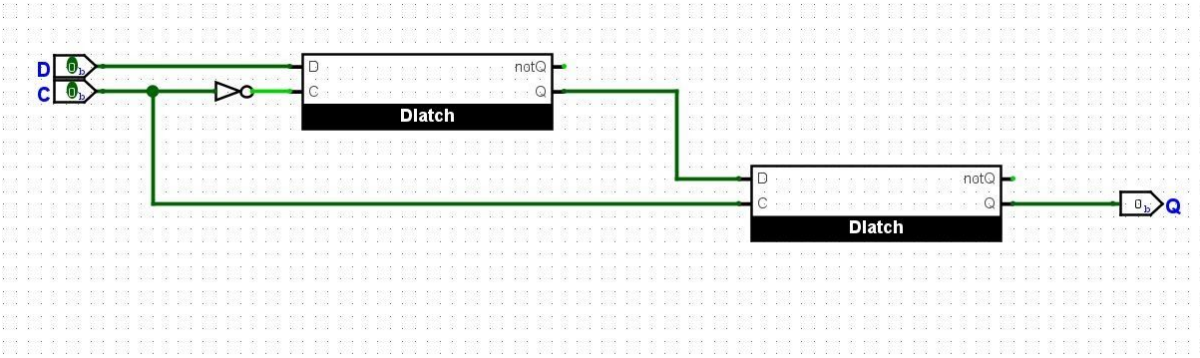
Initial state Q = LOW, notQ = HIGH

C	S	R	NotQ	Q
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1(forbidden)	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1(forbidden)	0	0

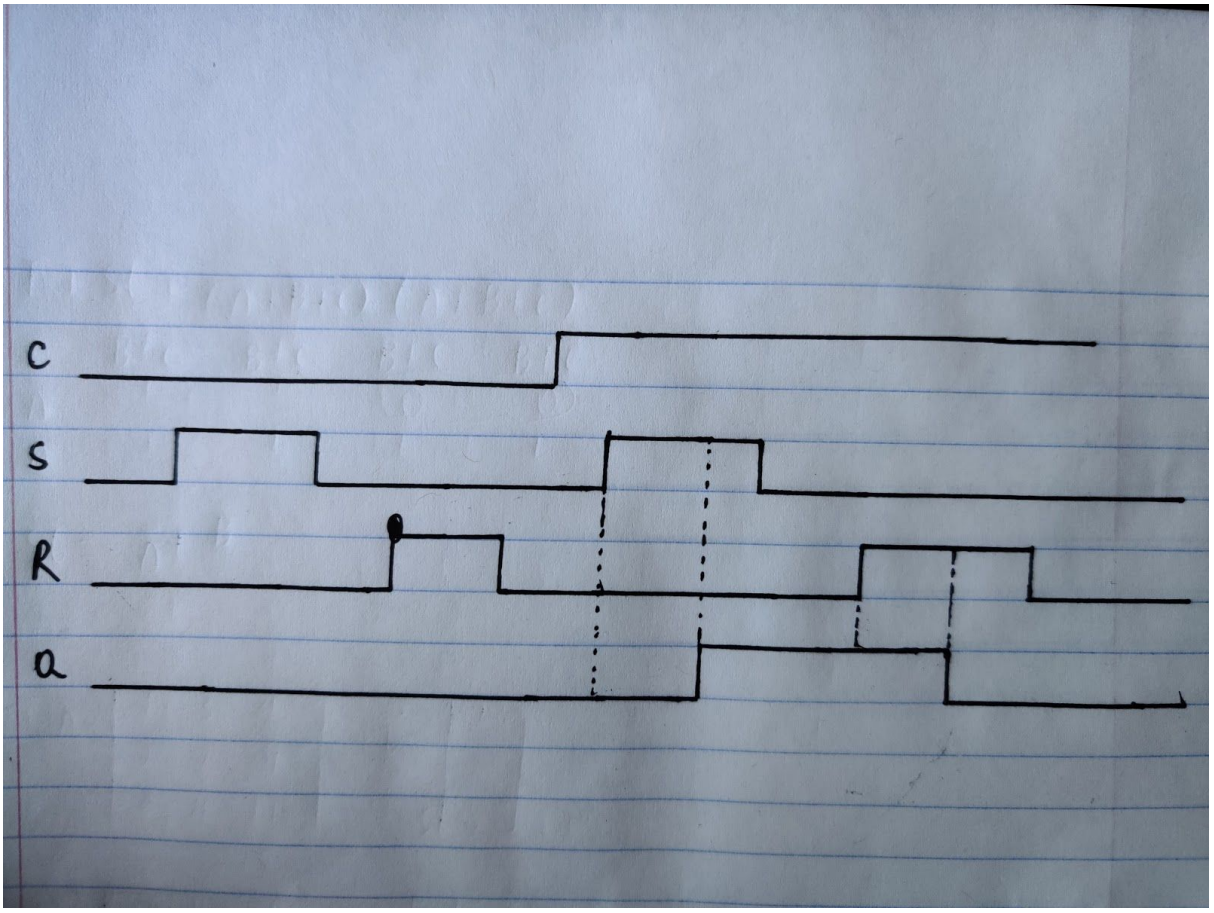
D-latch



D flip-flop

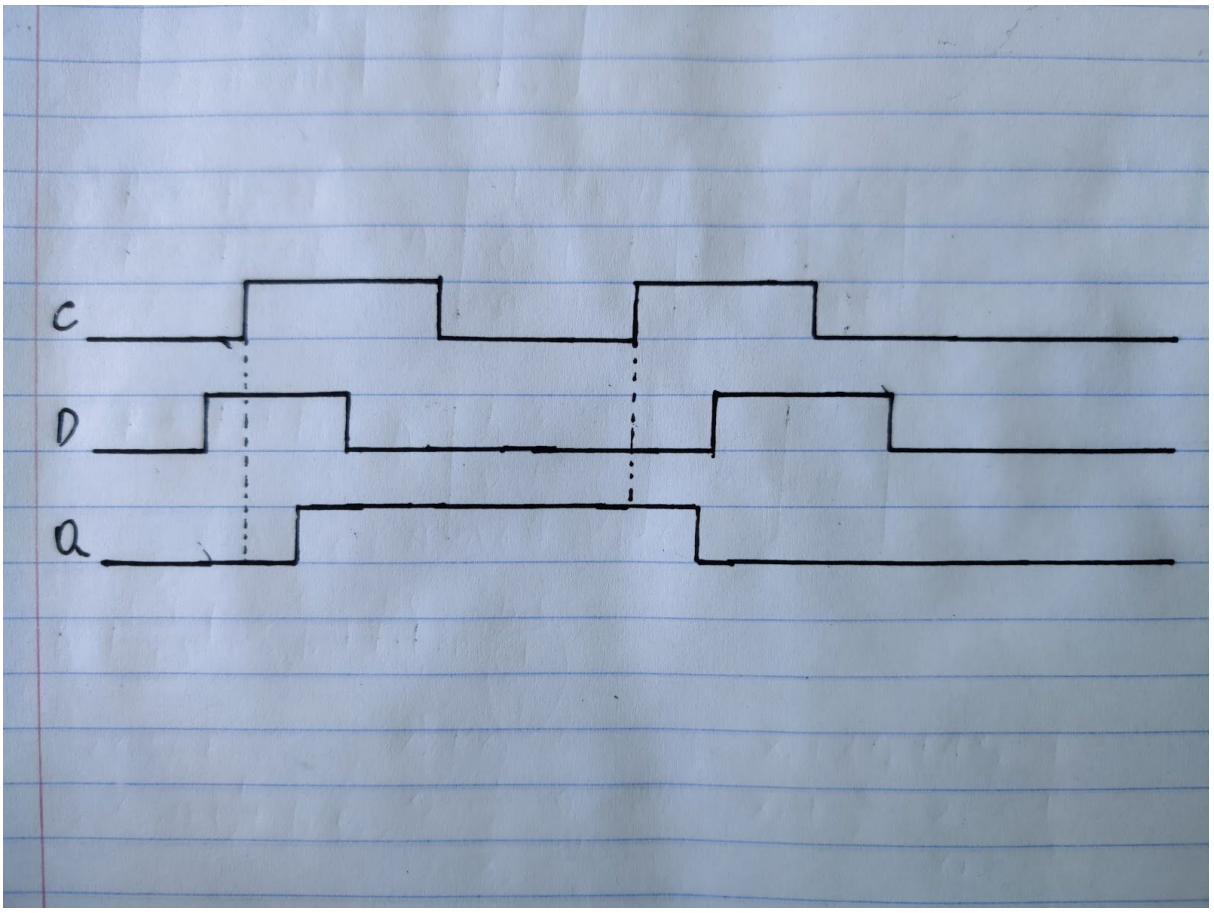


Waveform for SR latch



When the clock signal is low, the output Q is not affected by the set S and reset R signal pulse. When the clock signal is high, the output Q is high when the set S pulse arrives, and the output is low when the reset R pulse arrives.

Waveform for D flip-flop



In this implementation of D flip-flop, the output Q is only triggered by the positive-edge of the clock signal. We can see that neither the positive-edge nor the negative-edge of D changes the output. It is whenever the positive-edge of C occurs and then the D signal is sampled to reflect on the output.