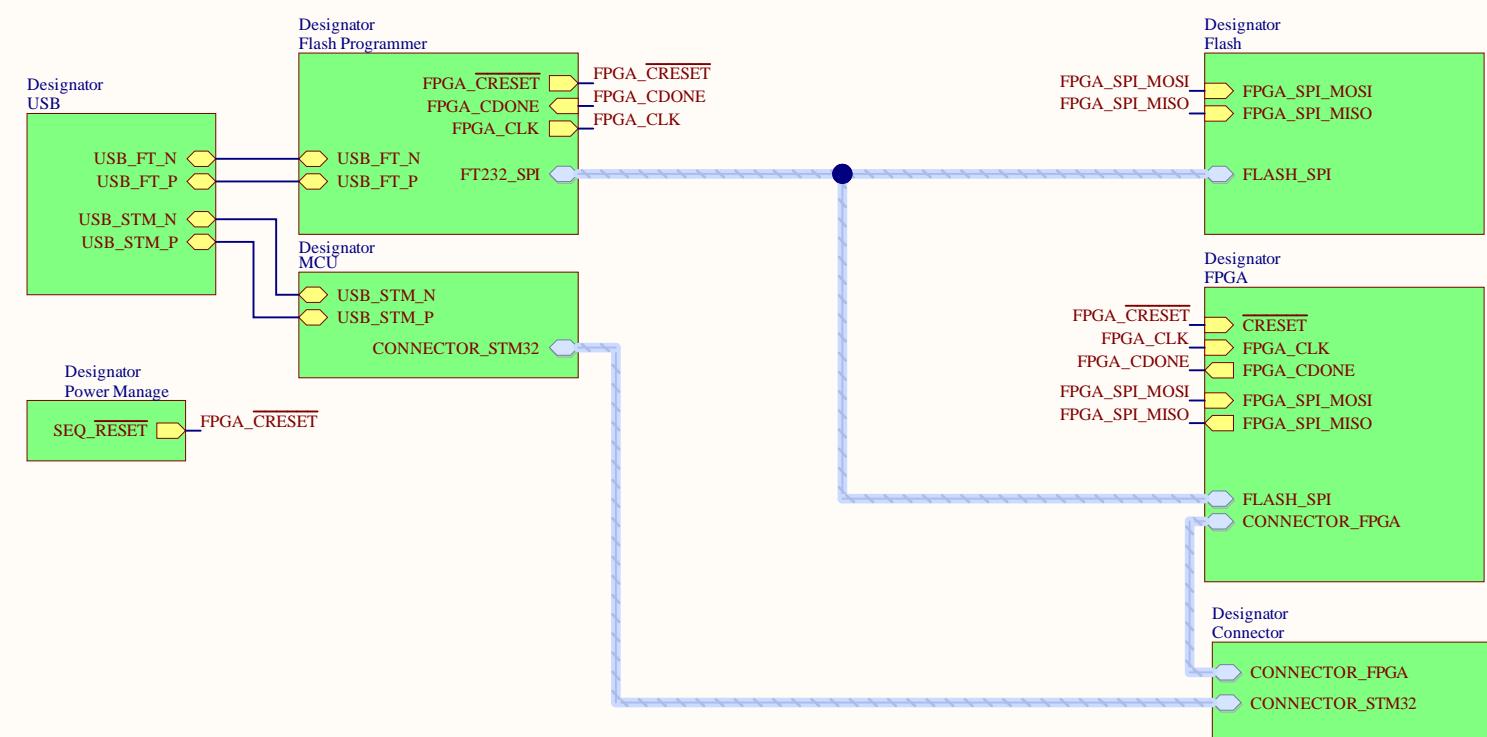


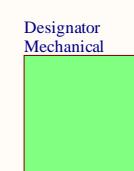
A

A



B

B



Warsaw University of Technology		
Project:	Control BoardPrjPcb.PrjPcb	
Page Contents:	Main.SchDoc	
Size:	DWG NO: -	

Variant
[No Variations]

Checked by:

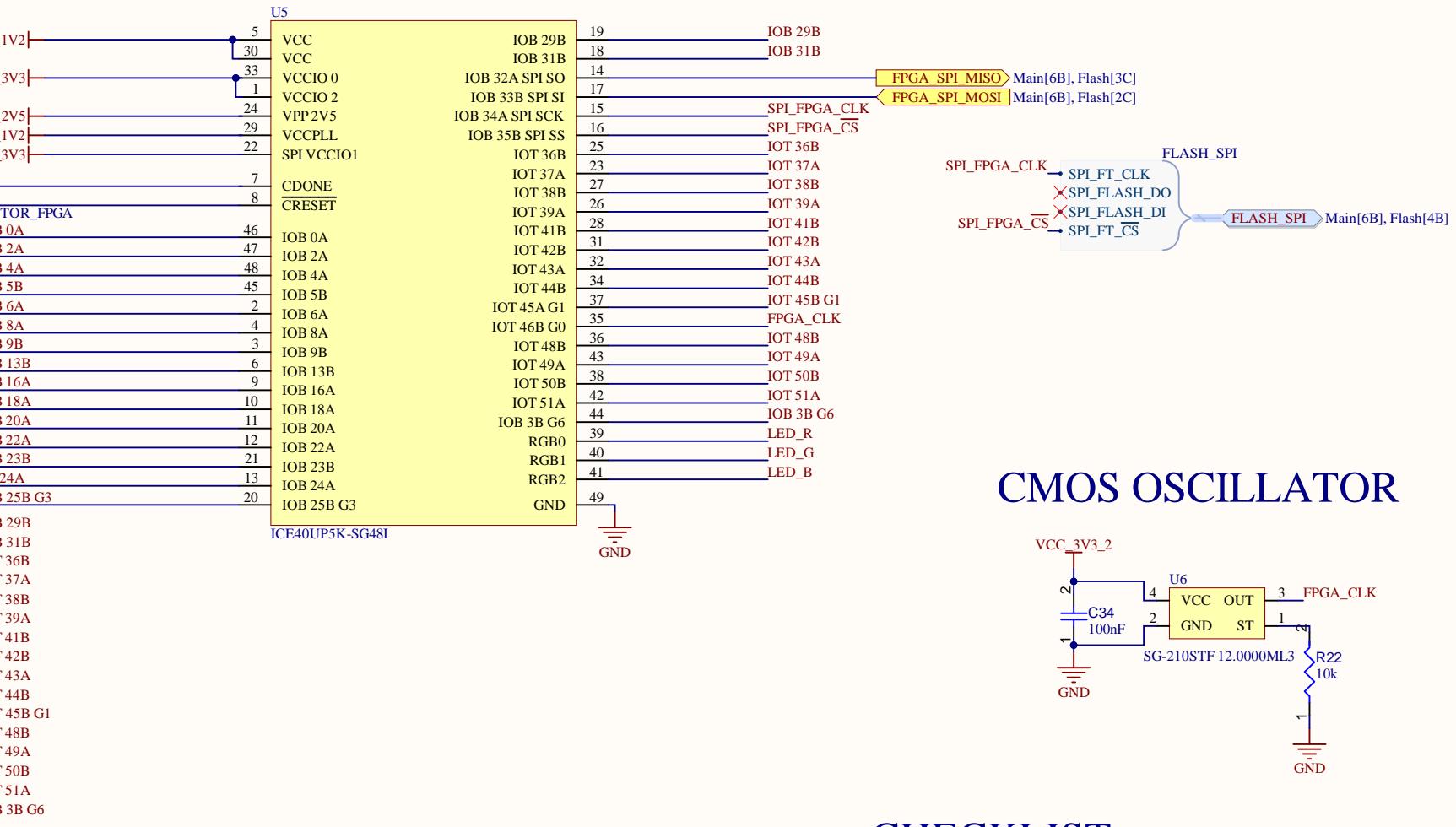
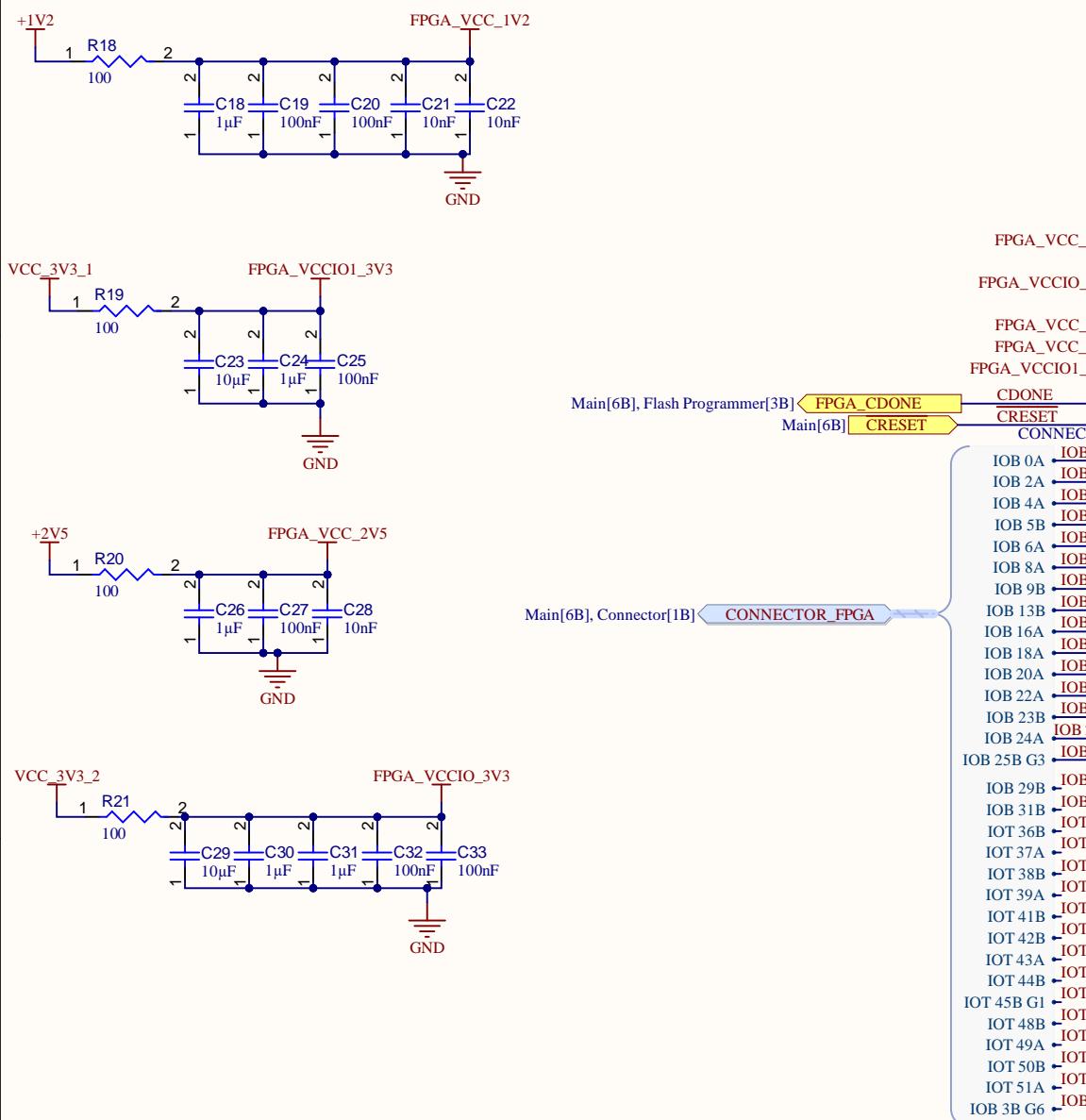
Revision:

Date: 18.09.2023 Design by: Michal Karas Sheet 1 of 9

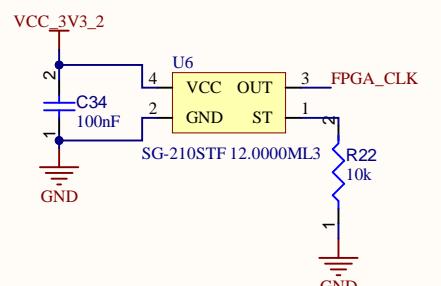
FILTER&DECOUPLING

FPGA

ICE40



CMOS OSCILLATOR



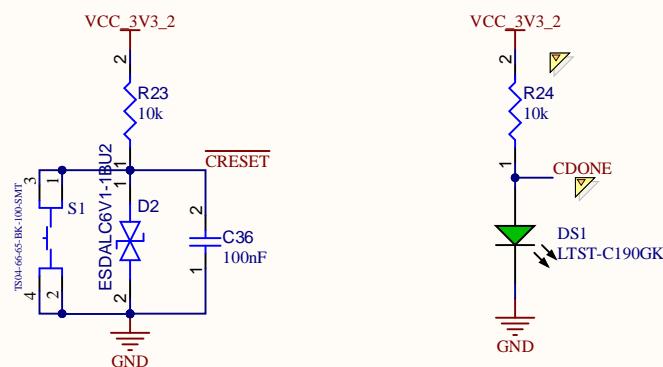
CHECKLIST

Table 5.1. ICE40 Hardware Checklist

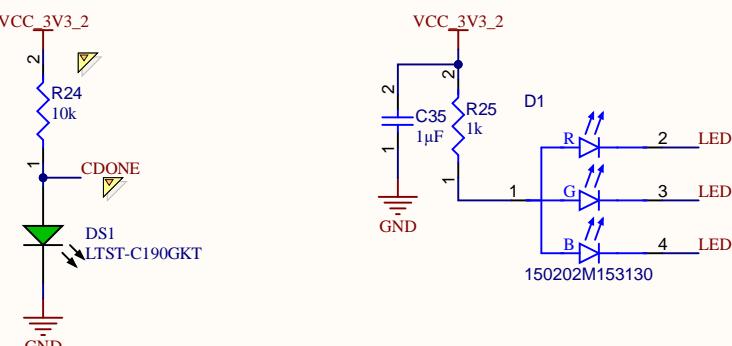
iCE40 Hardware Checklist Item	OK	N/A
1 Power Supply		
1.1 Core supply VCC at 1.2 V	X	
1.2 I/O power supply VCCIO 0-3 at 1.5 V to 3.3 V	X	
1.3 SPI_VCC at 1.8 V to 3.3 V	X	
1.4 VCCPLL pulled to VCC even if PLL not used	X	
1.5 Power supply filter for VCCPLL and GNDPLL	X	
1.6 GNDPLL must NOT be connected to the board*	X	
1.7 Power-up supply sequence and Ramp Rate requirements are met	X	
1.8 VPP_2V5 should not exceed 3.0V during NVCM programming	X	
2 Power-on-Reset (POR) inputs		
2.1 VCC	X	
2.2 SPI_VCC	X	
2.3 VCCIO_0-3	X	
2.4 VPP_2V5	X	
2.5 VPP_FAST	X	
3 Configuration		
3.1 Configuration mode based on SPI_SS_B	X	
3.2 Pull-up on CRESET_B_CDONE pin	X	
3.3 TRST_B is kept low for normal operation	X	
4 I/O pin assignment		
4.1 LVDS pin assignment considerations	X	



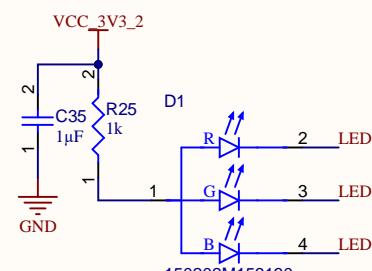
RESET



CDONE



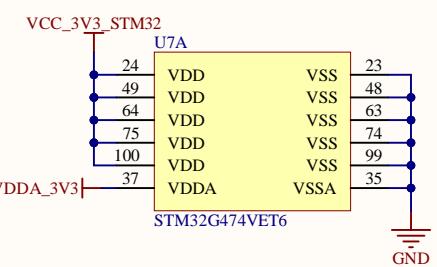
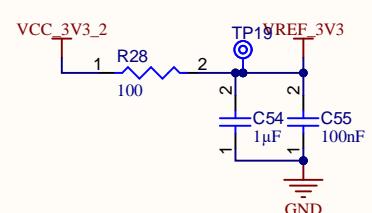
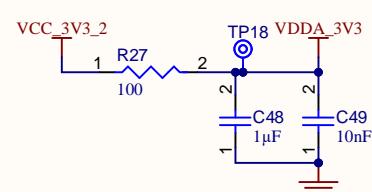
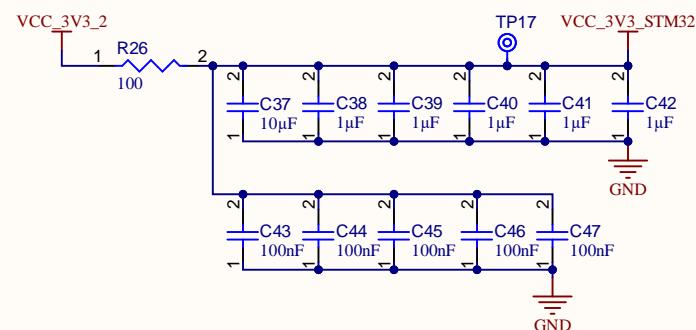
LED



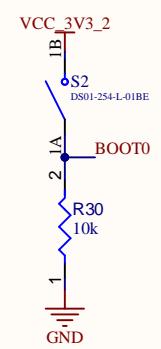
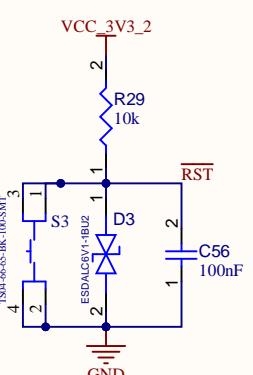
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Variant:	[No Variations]	
Checked by:		
Page Contents:	FPGA.SchDoc	
Size:	DWG NO: -	
Revision:	-	
Date:	18.09.2023	Design by:
Sheet 2	of 9	

MCU

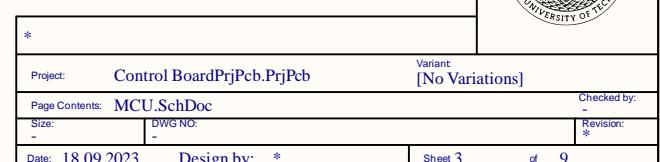
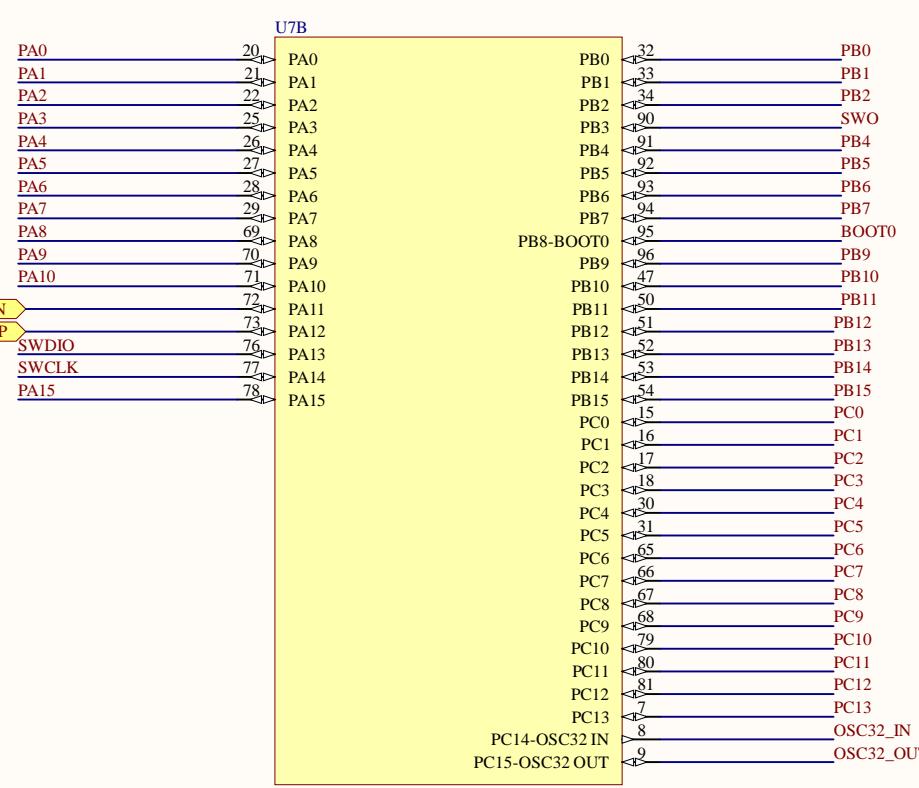
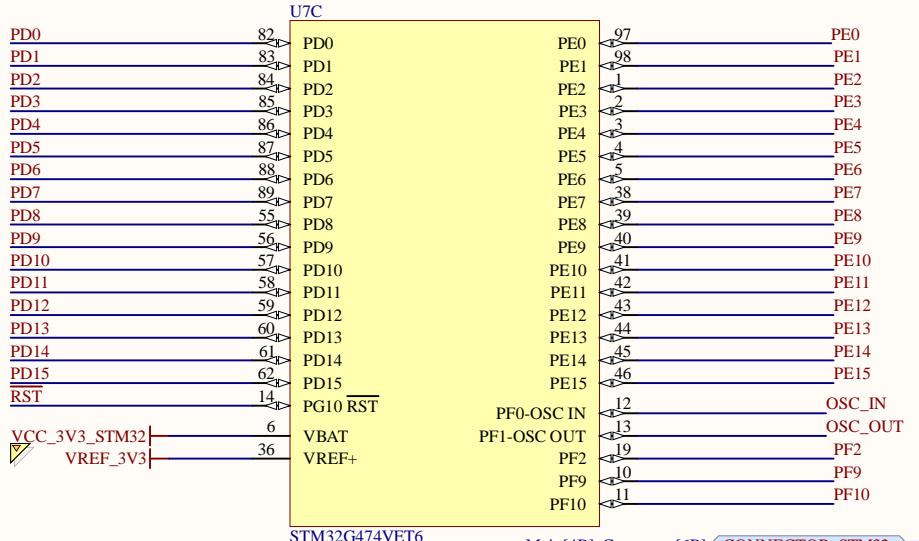
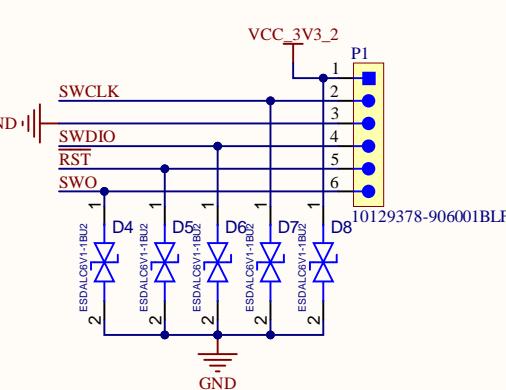
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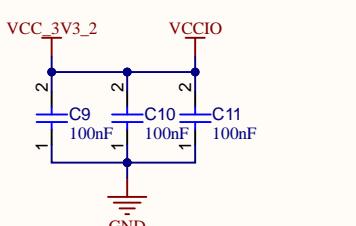
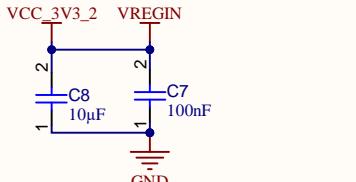
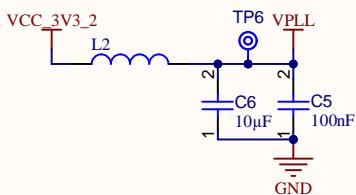
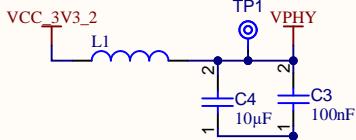
RESET



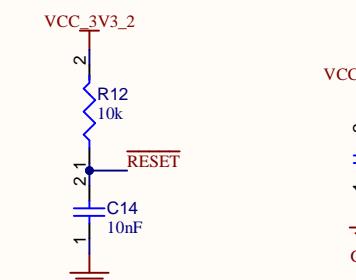
SWD&BOOT0



FILTER&DECOUPLING



RESET



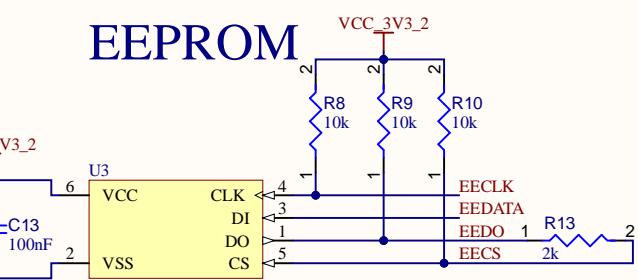
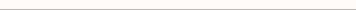
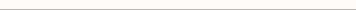
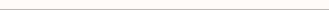
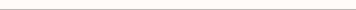
EEPROM



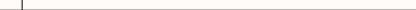
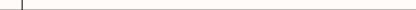
TP13 \ominus EECLK
TP14 \ominus FEDATA
TP15 \ominus EECS
TP16 \ominus EEDO



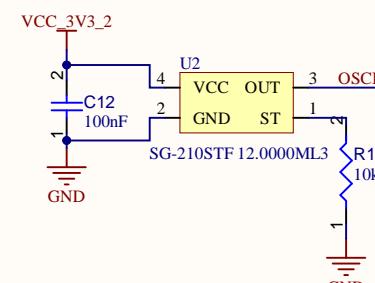
USB->SPI



TP13 \ominus EECLK
TP14 \ominus FEDATA
TP15 \ominus EECS
TP16 \ominus EEDO



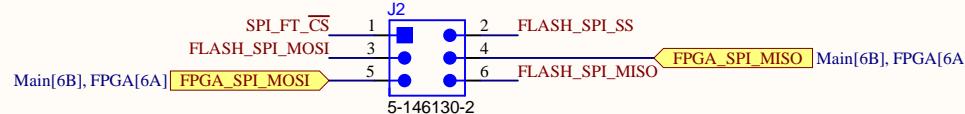
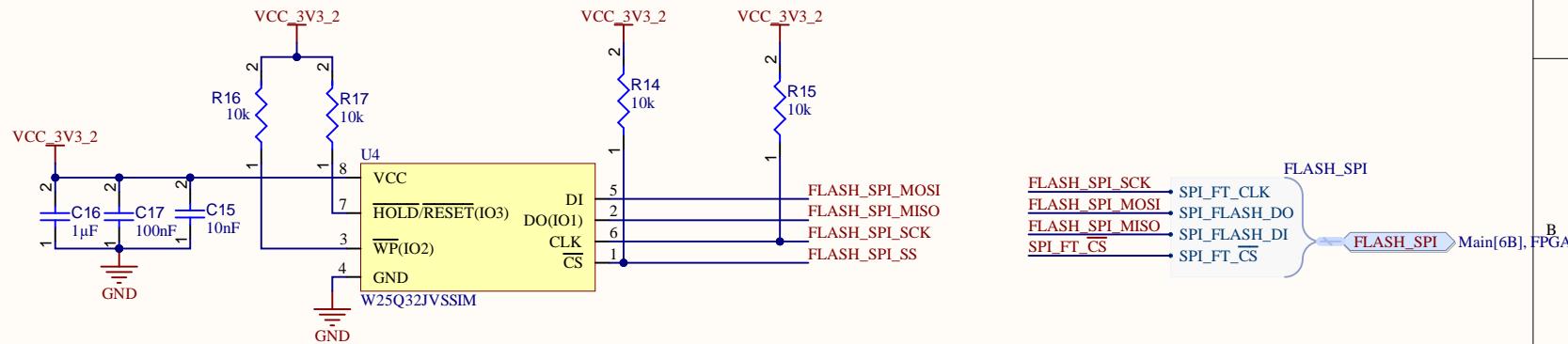
CMOS OSCILLATOR



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Page Contents: Flash Programmer.SchDoc				
Size: - DWG NO: -				
Date: 18.09.2023 Design by: *		Sheet 4 of 9		



FLASH



Shunt 1,2 for programming flash and normal operation.
 Remove shunt for programming FPGA

For programming Flash - shunt 3,4 and 5,6

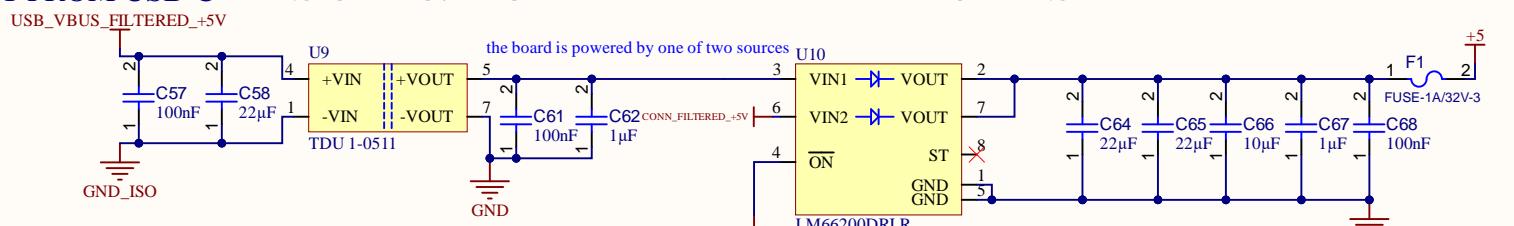
For programming FPGA directly - shunt 3,5 and 4,6

*		
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Page Contents:	Flash.SchDoc	Checked by:
Size:	DWG NO:	Revision:
-	-	-
Date: 18.09.2023	Design by: *	Sheet 5 of 9

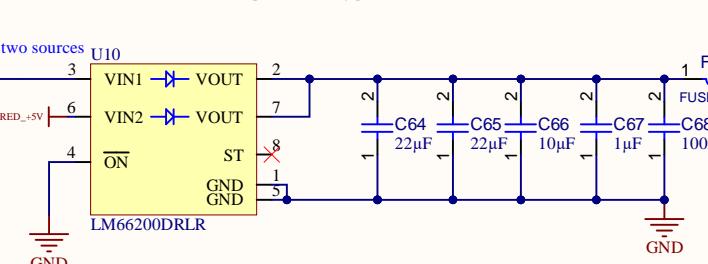


POWER MANAGE

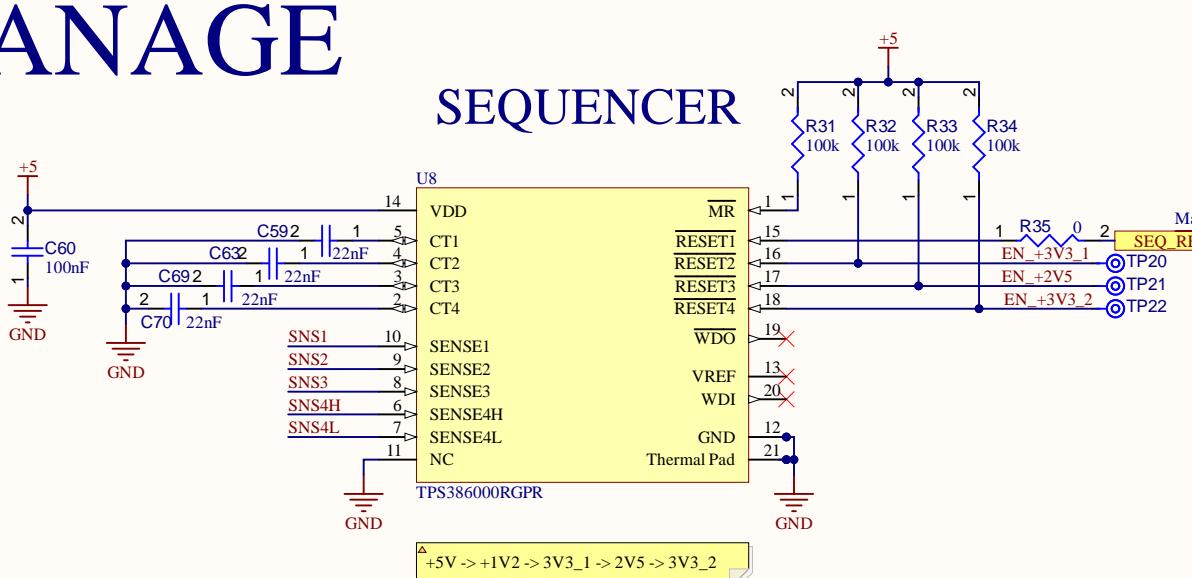
SUPPLY FROM USB-C ISO DC/DC



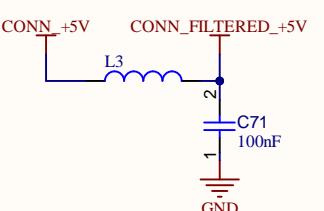
IDEAL DIODES



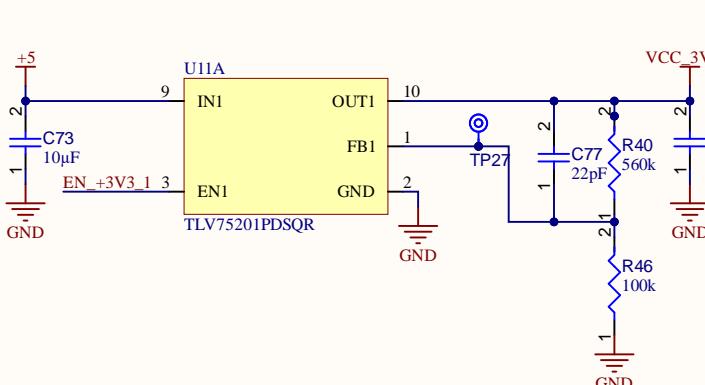
SEQUENCER



SUPPLU FROM CONNECTOR



5V->3V3



5V->2.5V

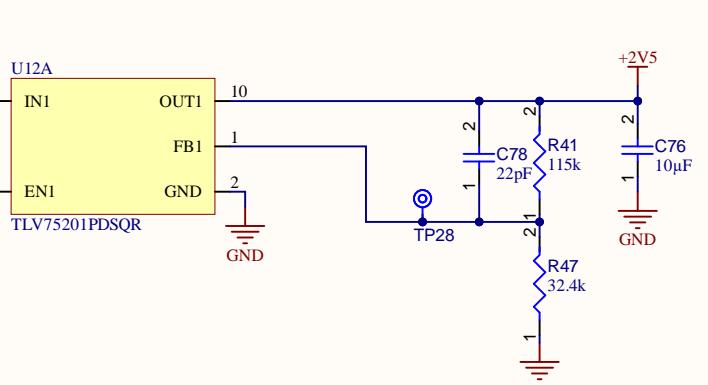


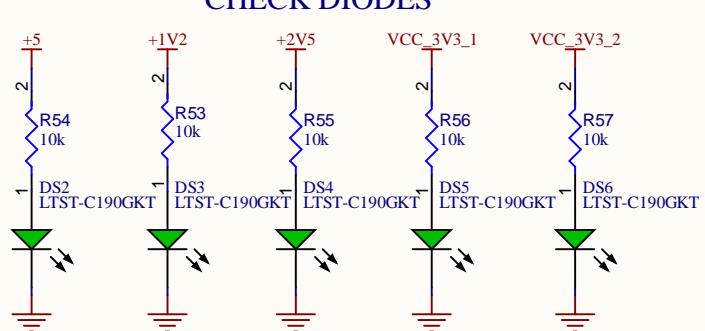
Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
$V_{CC}^{1,2}$	Core Supply Voltage	1.14	1.26	V	
V_{PP_2V5}	Slave SPI Configuration	1.71 ⁴	3.46	V	
	Master SPI Configuration	2.30	3.46	V	
	Configuration from NVCM	2.30	3.46	V	
$V_{CCIO}^{1,2,3}$	I/O Driver Supply Voltage	$V_{CCIO_0}, V_{CCIO_1}, V_{CCIO_2}$	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V	
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C	
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C	
t_{PROG}	Junction Temperature NVCM Programming	10.00	30.00	°C	

Notes:

- Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
- See recommended voltages by I/O standard in subsequent table.
- V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
- V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

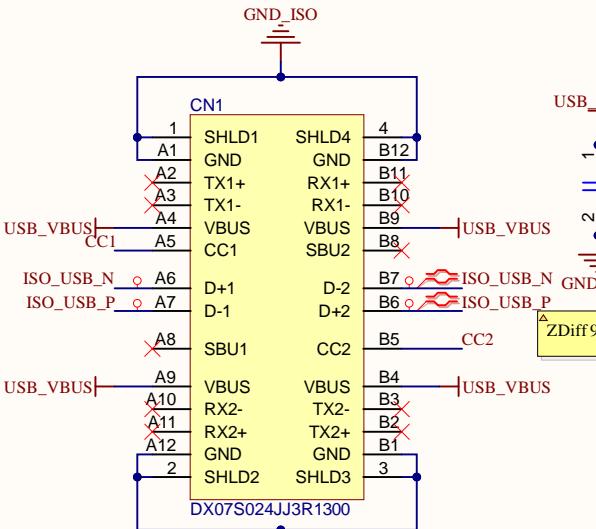
CHECK DIODES



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Variant:	[No Variations]	
Page Contents:	Power Manage.SchDoc	
Size:	DWG NO: -	
Date:	18.09.2023	
Design by:	* Sheet 6 of 9	

USB

USB-C CONNECTOR



CC1, CC2, GND_ISO

11 Layout

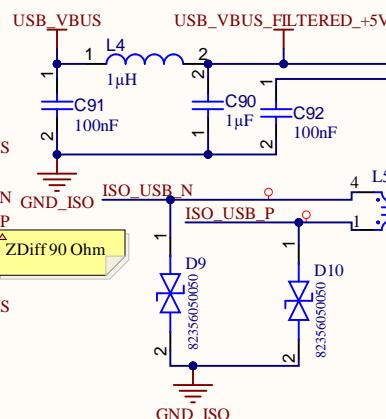
11.1 Layout Guidelines

- Two layers are sufficient to accomplish a low EMI PCB design.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90Ω differential impedance and as close to 45Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2 .
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- ESD structures must be placed on the top layer, close to the connector, and right on the D+/D- traces without vias. Ground routing for the ESD structures must be made in the top layer if possible, else must have a strong connection to the ground plane with multiple vias.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

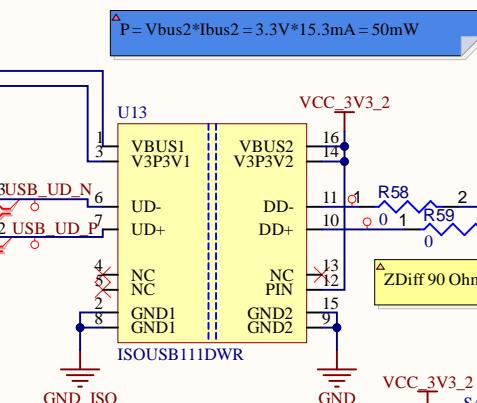
HOST

DS7
LTST-C190GKT

GND_ISO



ISOLATED USB REPEATER



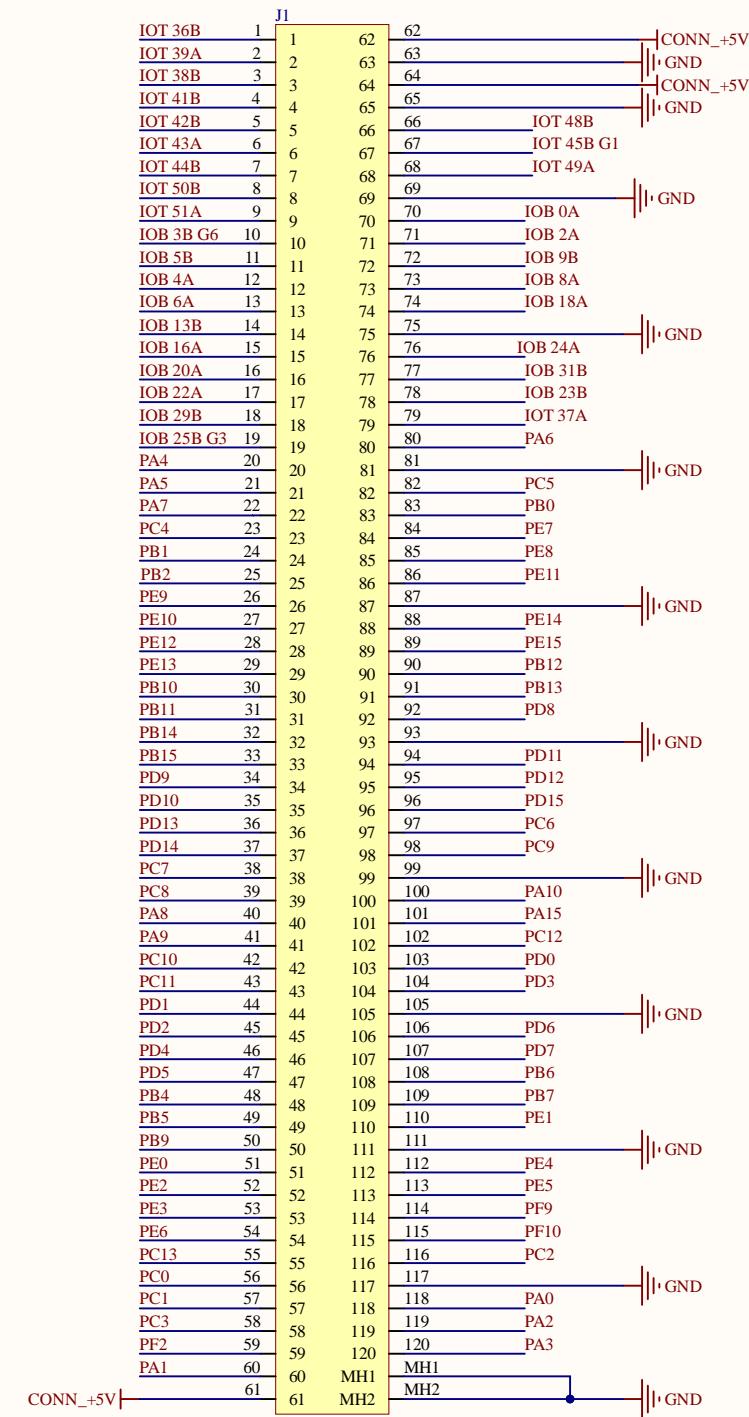
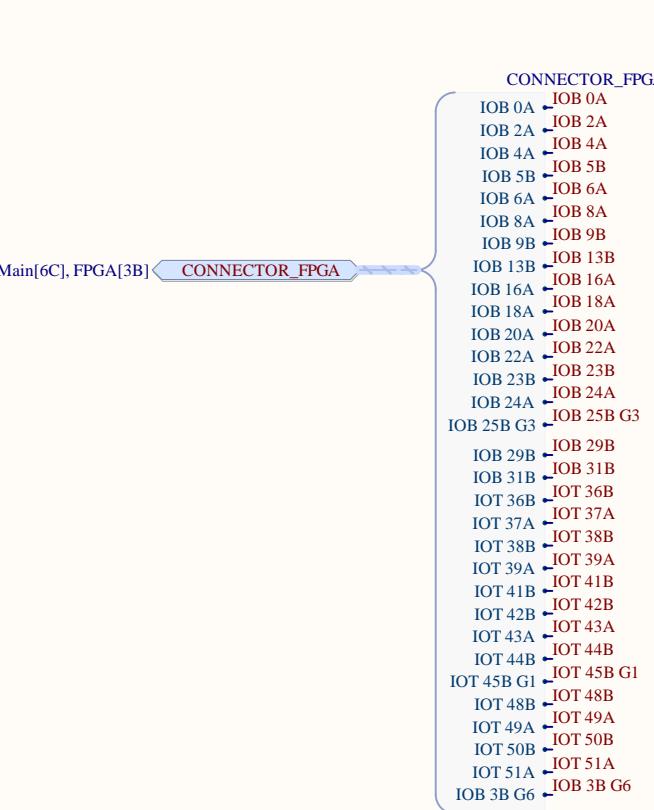
PARAMETER	TEST CONDITIONS	SPECIFICATIONS	DW-16	DW-16	UNIT
IEC 60664-1					
CLR External clearance ^[1]	Side 1 to side 2 distance through air	>8 mm			mm
CPG External Creepage ^[2]	Side 1 to side 2 distance across package surface	>1.2 mm			mm
DTI Dielectric strength of the insulation	Minimum dielectric strength (internal clearance):	>2100 V			μm
CTI Comparative tracking index	IEC 60112, UL 746A	>4000			V
Material Group	According to IEC 60664-1	I			
Overvoltage category	Rated mains voltage < 600 V _{AC}	I-IV	I-IV	I-IV	
	Rated mains voltage ≥ 600 V _{AC}	I-III	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-11) ^[3]					
V _{com} Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	V _{DC}	
V _{com} Maximum repetitive peak isolation voltage	AC voltage (sine wave), sine-dependent dielectric breakdown (SDB) test;	1500	1500	V _{DC}	
V _{com} Maximum repetitive peak isolation voltage	DC voltage (bipolar)	2121	2121	V _{DC}	
V _{com} Maximum transient isolation voltage	$V_{trans} + V_{com} = 1.60 \pm 0.05$ (qualification); $V_{trans} = 1.2 \times V_{com}$, $t = 1.5 \text{ ms}$ (100% production)	7071	7071	V _{DC}	
V _{imp} Maximum impulse voltage ^[4]	Tested in air, 1.250-ns rise time waveform per IEC 62305-2	8000	8000	V _{DC}	
V _{surge} Maximum surge isolation voltage ^[5]	Tested in air (qualification test), 1.250-μs rise time waveform per IEC 62305-2	12800	12800	V _{DC}	
	Method 2: After 100 safety test subgroups 2/3, $V_{surge} = V_{com} + t_{surge} \cdot 60 \text{ mV}$; $V_{com} = 1.2 \times V_{com_t_0} + 10 \text{ mV}$	± 5	± 5		
R _{qd} Apparent charge ^[6]	Method 3: After 100 supplemental tests subgroup 1, $V_{surge} = V_{com} + t_{surge} \cdot 60 \text{ mV}$; $V_{com} = 1.2 \times V_{com_t_0} + 10 \text{ mV}$	± 5	± 5	pC	
C _{qd} Barrier capacitance, input to output ^[7]	Method 4: After 100 supplemental tests subgroup 2, $V_{surge} = V_{com} + t_{surge} \cdot 60 \text{ mV}$; $V_{com} = 1.2 \times V_{com_t_0} + 10 \text{ mV}$	0.8	0.7	pF	
R _{io} Insulation resistance, input to output ^[8]	$V_{surge} = 0.4 \times V_{com}$; $f = 1 \text{ MHz}$	$> 10^{12}$	$> 10^{12}$		W
	$V_{surge} = 500 \text{ V}$; $T_x = 25^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$		
	$V_{surge} = 500 \text{ V}$; $T_x = 100^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$		
	$V_{surge} = 500 \text{ V}$; $T_x = 125^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$		
Pollution degree	2	2			
Climatic category	40/125/21/40/125/21				
UL 1577					
V _{iso} Withstand isolation voltage	$V_{test} = V_{iso} + 10 \text{ %}$ (qualification); $V_{test} = 1.2 \times V_{com}$, $t = 1.5 \text{ ms}$ (100% production)	5000	5000	V _{DC}	

*		
Project:	Control BoardPrjPcb.PrbPcb	
Variant:	[No Variations]	
Page Contents:	USB.SchDoc	
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CONNECTOR

A



CONNECTOR STM32

- PE0
- PE1
- PE2
- PE3
- PE4
- PE5
- PE6
- PE7
- PE8
- PE9
- PE10
- PE11
- PE12
- PE13
- PE14
- PE15
- PF2
- PF9
- PF10
- PD0
- PD1
- PD2
- PD3
- PD4
- PD5
- PD6
- PD7
- PD8
- PD9
- PD10
- PD11
- PD12
- PD13
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- PD58
- PD59
- PD60
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- PC1
- PC2
- PC3
- PC4
- PC5
- PC6
- PC7
- PC8
- PC9
- PC10
- PC11
- PC12
- PC13
- PA0
- PA1
- PA2
- PA3
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- PA12
- PA13
- PA14
- PA15

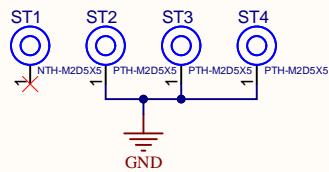
Main[6C], MCU[7B] CONNECTOR STM32

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Page Contents:	Connector.SchDoc	Checked by:		
Size:	DWG NO:	Revision:		
Date: 18.09.2023 Design by: *				Sheet 8 of 9



Mechanicals

Mouting Holes



Fiducials



*	Variant [No Variations]	
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Page Contents:	Mechanical.SchDoc	
Size:	DWG NO:	Revision:
-	-	*
Date: 18.09.2023	Design by: *	Sheet 9 of 9

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THE POLISH UNIVERSITY OF TECHNOLOGY**

