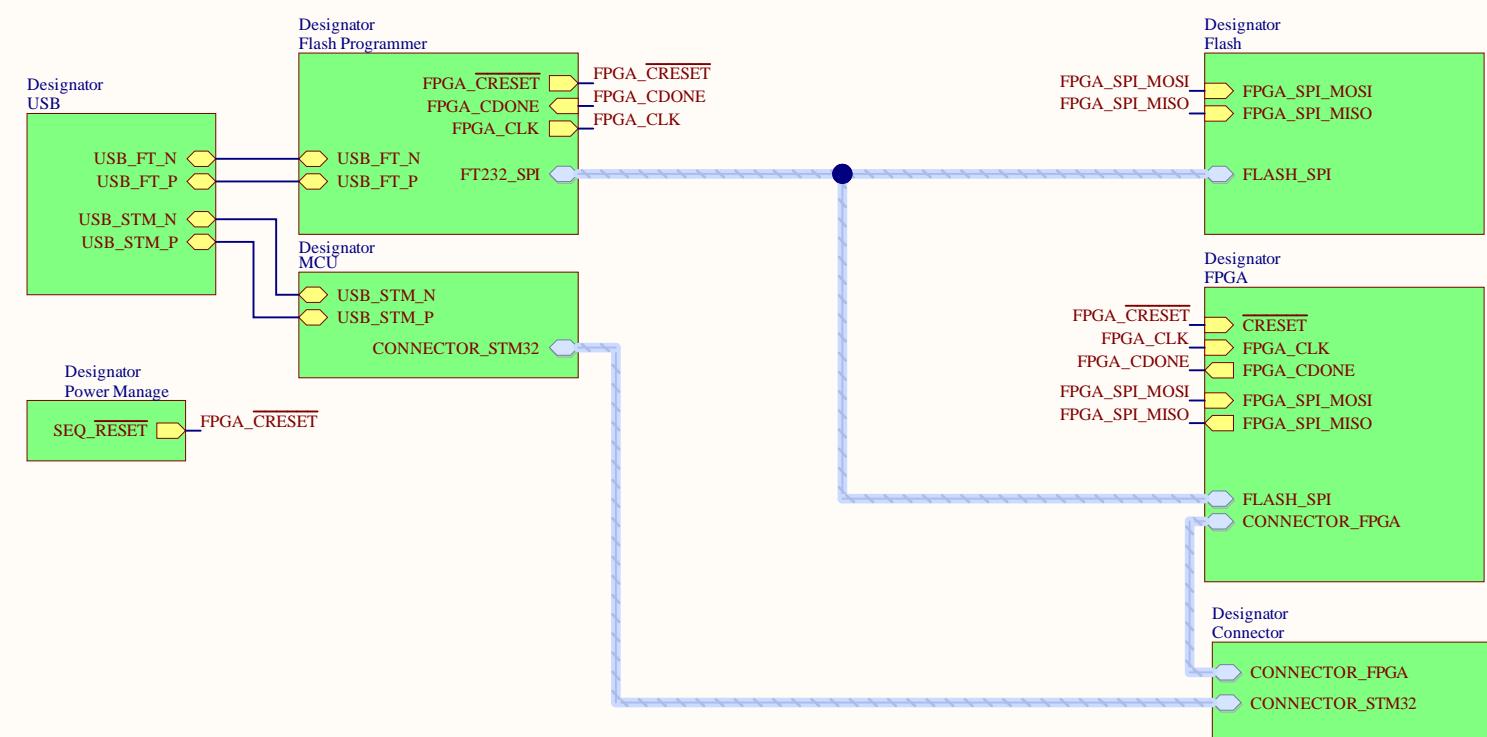


A

A



B

B

C

C

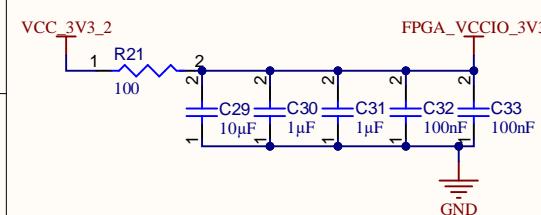
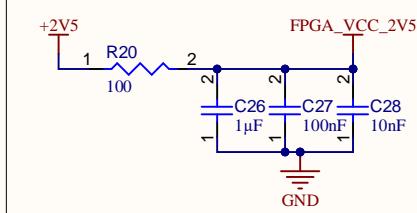
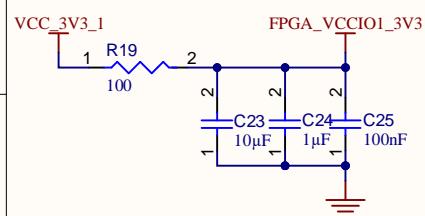
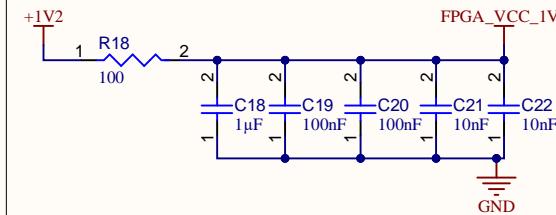
D

D



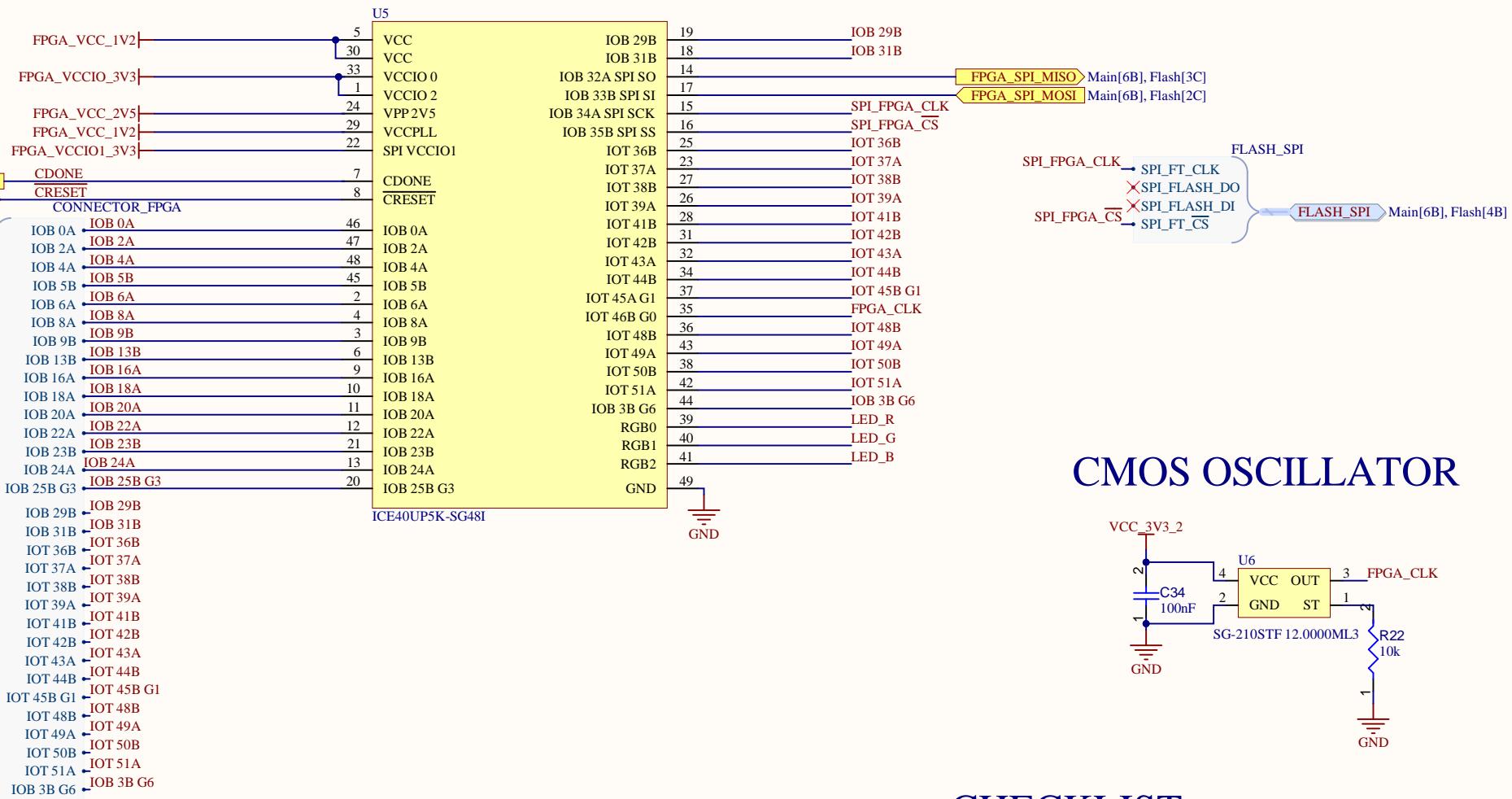
Warsaw University of Technology			
Project: Control BoardPrjPcb.PrjPcb			
Variant: [No Variations]			
Page Contents: Main.SchDoc			
Size:	DWG NO:	Checked by:	
-	-	Michał Karas	
Date: 16.09.2023	Design by:	Sheet 1 of 9	

FILTER&DECOUPLING

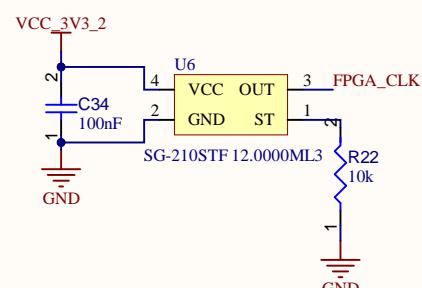


FPGA

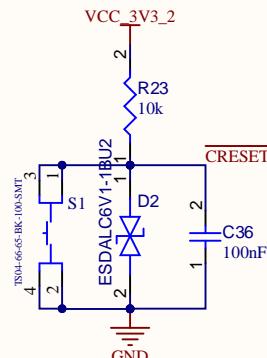
ICE40



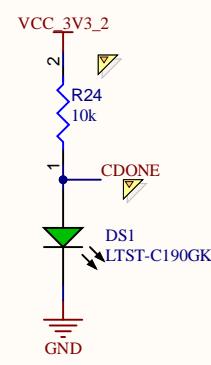
CMOS OSCILLATOR



RESET



CDONE



LED

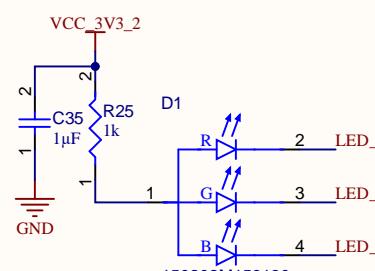


Table 5.1. ICE40 Hardware Checklist

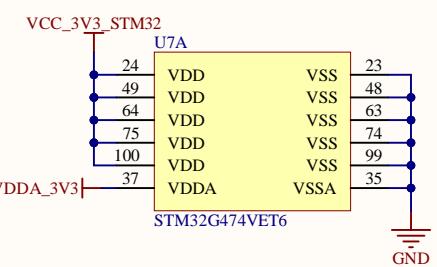
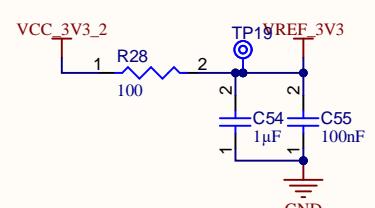
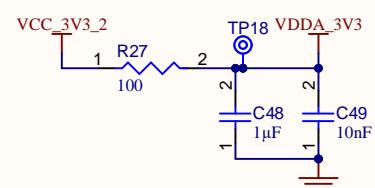
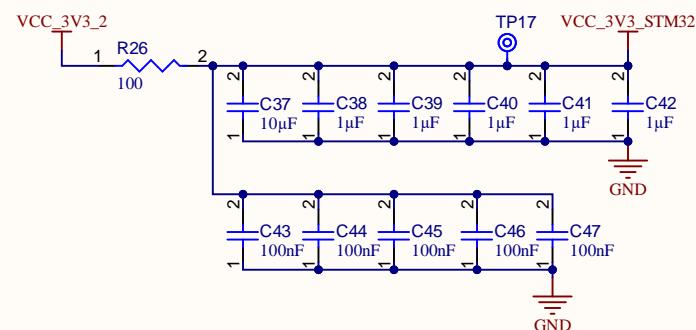
iCE40 Hardware Checklist Item	OK	N/A
1 Power Supply		
1.1 Core supply VCC at 1.2 V	X	
1.2 I/O power supply VCCIO 0-3 at 1.5 V to 3.3 V	X	
1.3 SPI_VCC at 1.8 V to 3.3 V	X	
1.4 VCCPLL pulled to VCC even if PLL not used	X	
1.5 Power supply filter for VCCPLL and GNDPLL	X	
1.6 GNDPLL must NOT be connected to the board*	X	
1.7 Power-up supply sequence and Ramp Rate requirements are met	X	
1.8 VPP_2V5 should not exceed 3.0V during NVCM programming	X	
2 Power-on-Reset (POR) inputs		
2.1 VCC	X	
2.2 SPI_VCC	X	
2.3 VCCIO_0-3	X	
2.4 VPP_2V5	X	
2.5 VPP_FAST	X	
3 Configuration		
3.1 Configuration mode based on SPI_SS_B	X	
3.2 Pull-up on CRESET_B_CDONE pin	X	
3.3 TRST_B is kept low for normal operation	X	
4 I/O pin assignment		
4.1 LVDS pin assignment considerations	X	

*		
Project:	Control BoardPrjPcb.PrjPcb	
Variant:	[No Variations]	
Checked by:		
Page Contents:	FPGA.SchDoc	
Size:	DWG NO: -	
Revision:	-	
Date:	16.09.2023	Design by:
Sheet 2	of 9	

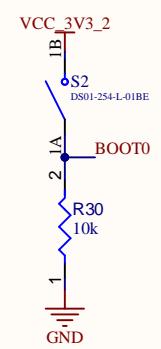
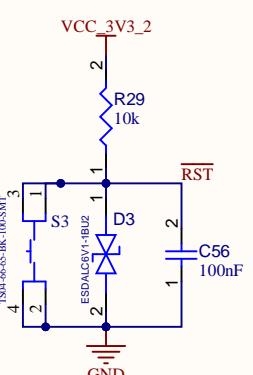


MCU

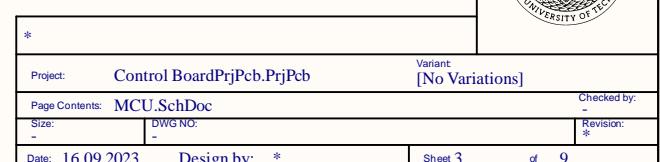
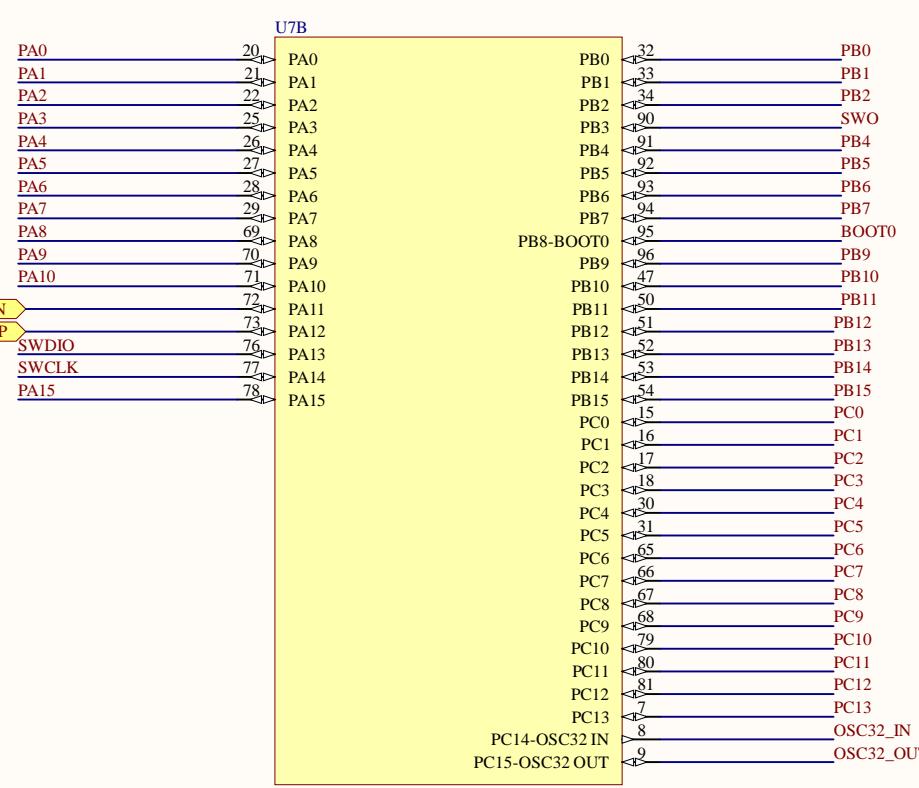
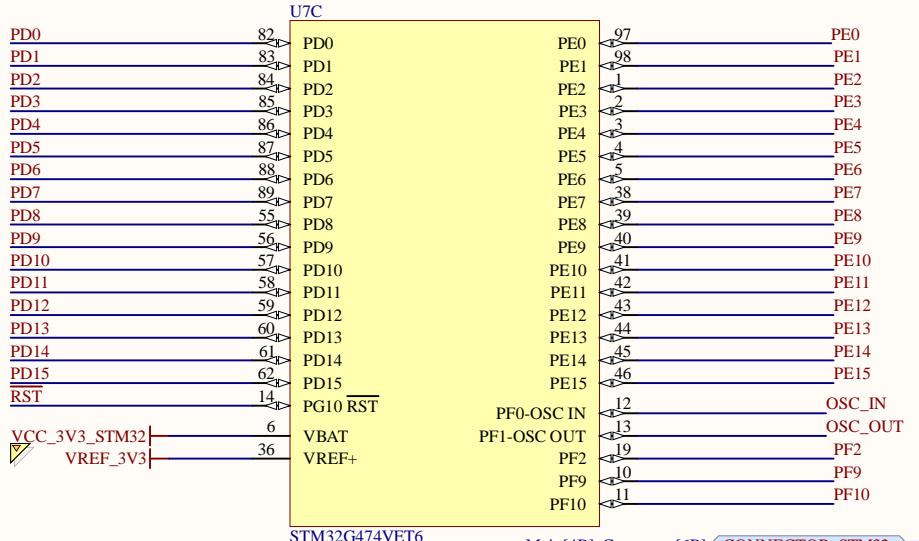
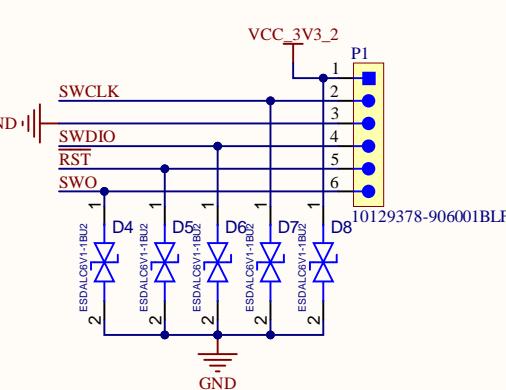
FILTER & DECOUPLING



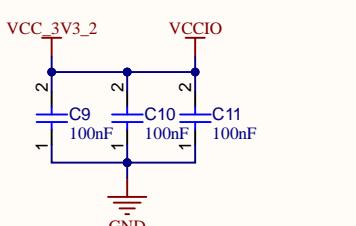
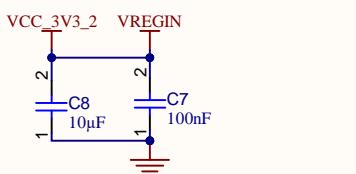
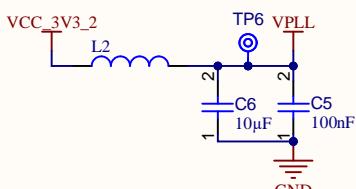
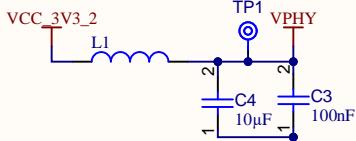
RESET



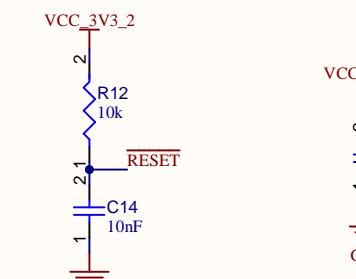
SWD&BOOT0



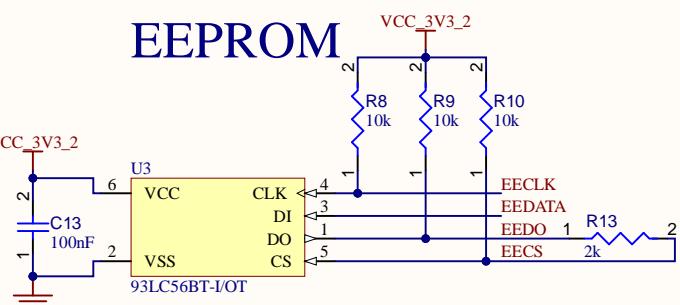
FILTER&DECOUPLING



RESET

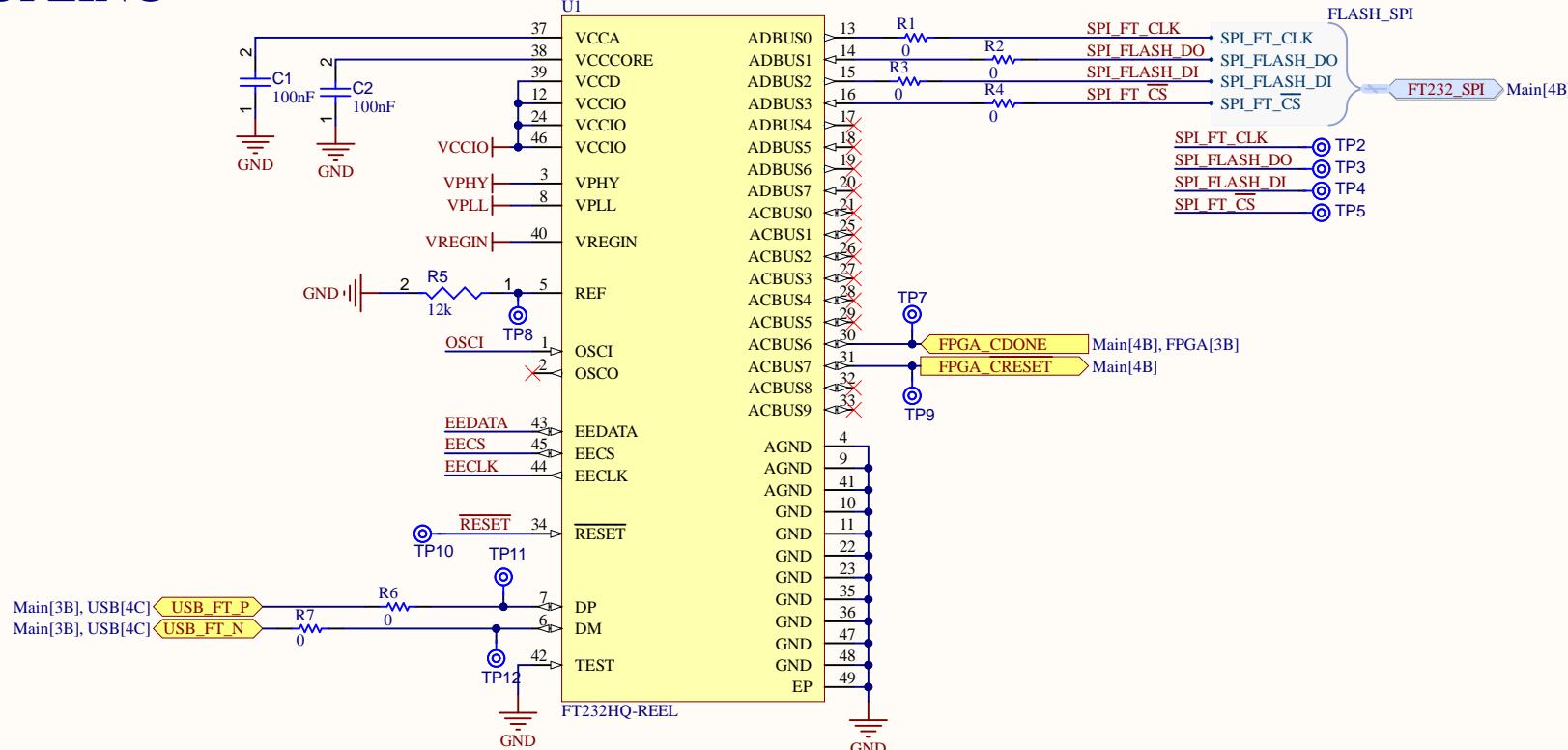


EEPROM

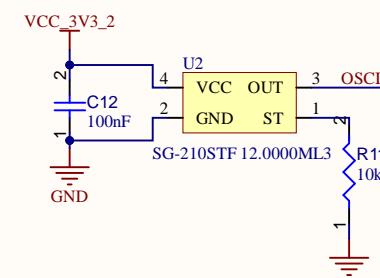


EECLK
EEDATA
EECS
EEDO

USB->SPI

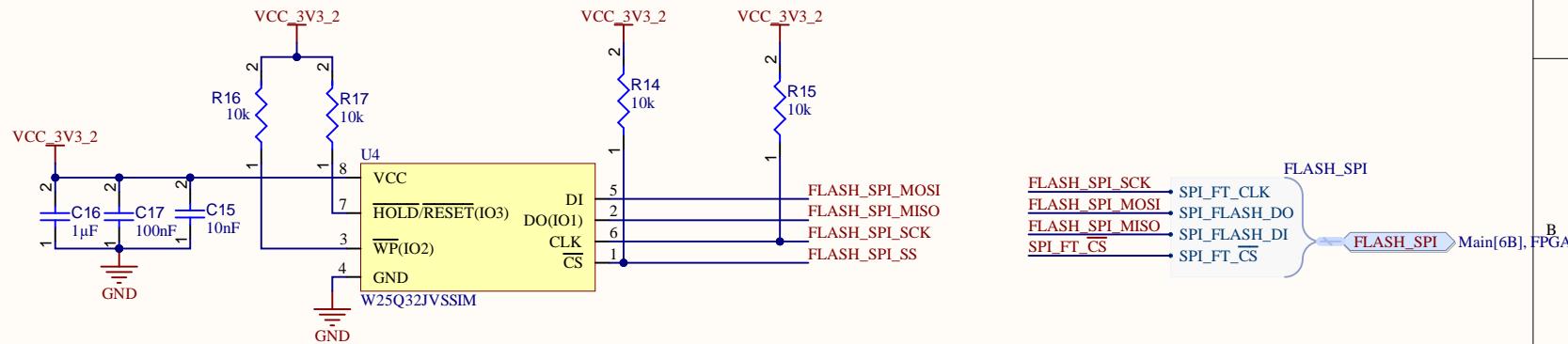


CMOS OSCILLATOR



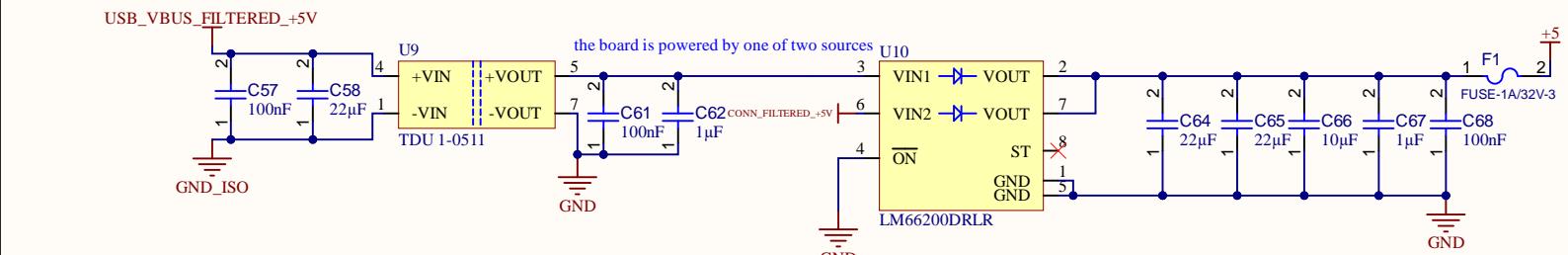
* 	
Project: Control BoardPrjPcb.PrjPcb Variant [No Variations]	
Page Contents: Flash Programmer.SchDoc Checked by: Size: - DWG NO: - Revision: *	
Date: 16.09.2023 Design by: * Sheet 4 of 9	

FLASH

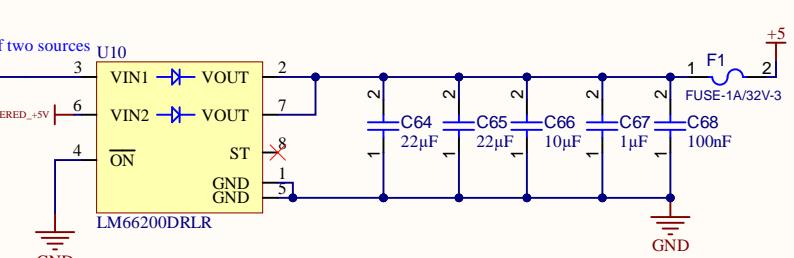


POWER MANAGE

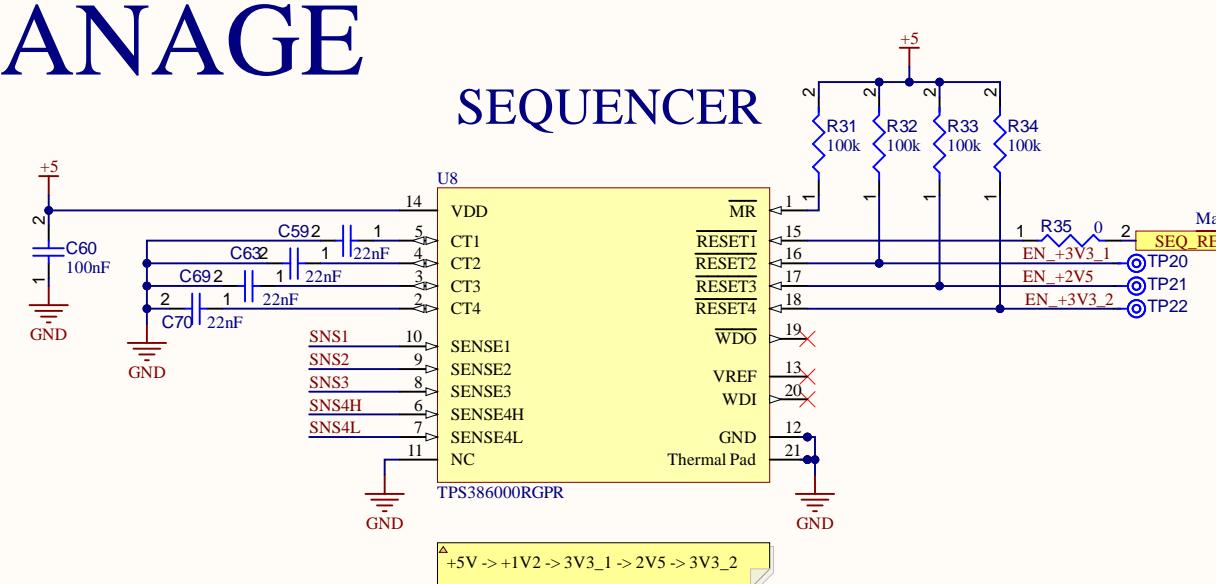
SUPPLY FROM USB-C ISO DC/DC



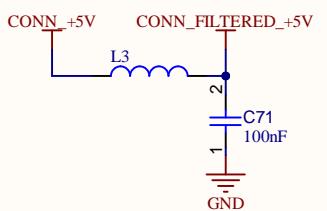
IDEAL DIODES



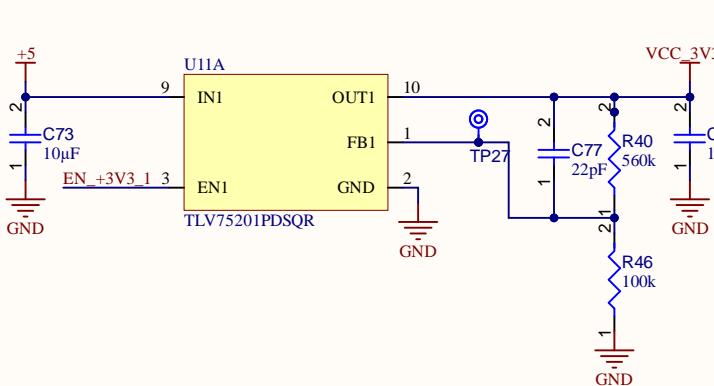
SEQUENCER



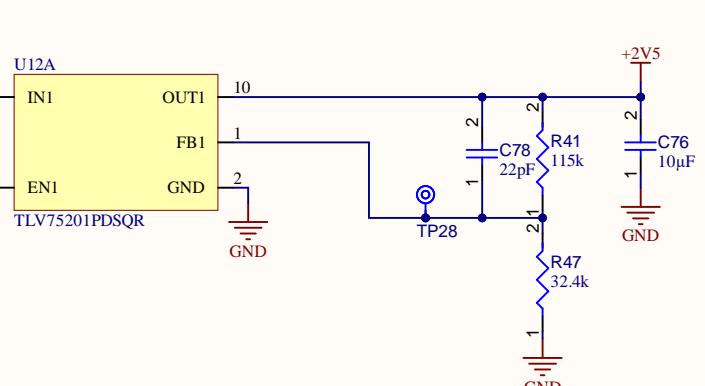
SUPPLI FROM CONNECTOR



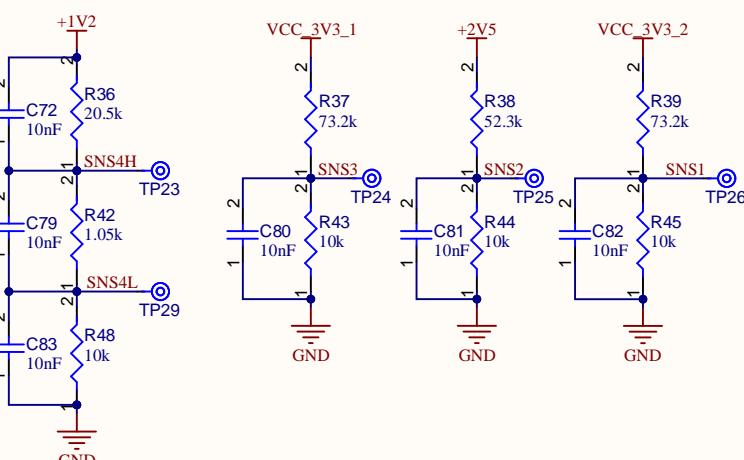
5V->3V3



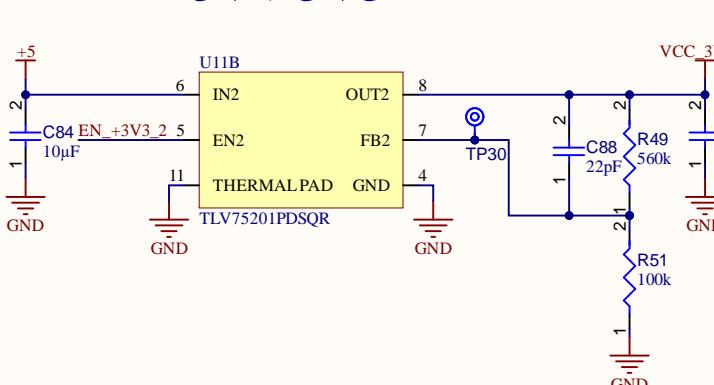
5V->2.5V



$V_h = 1.26V$ $V_l = 1.14V$



5V->3V3



5V->1.2V

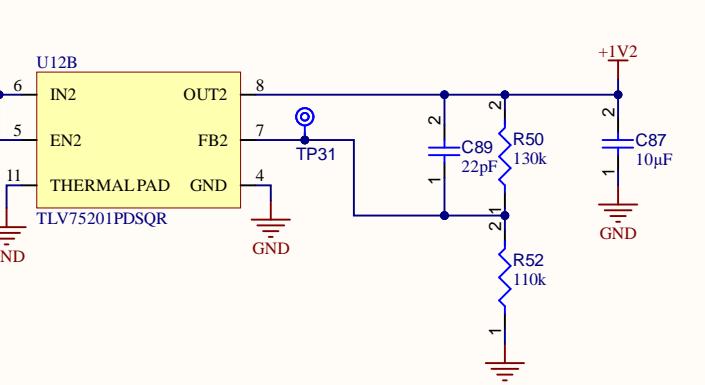


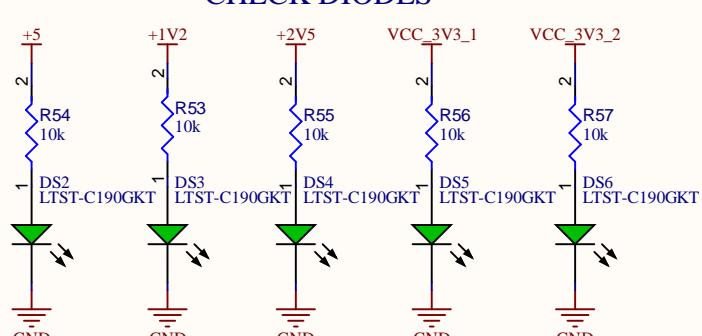
Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{cc}^{-1}	Core Supply Voltage	1.14	1.26	V
V_{pp_2v5}	Slave SPI Configuration Master SPI Configuration Configuration from NVCM NVCM Programming	1.71 ⁴ 2.30 2.30	3.46 3.46 3.46	V
$V_{ccio}^{1,2,3}$	I/O Driver Supply Voltage $V_{ccio_0}, SPI_Vccio_1, Vccio_2$	1.71	3.46	V
V_{ccpl}	PLL Supply Voltage	1.14	1.26	V
t_{jcom}	Junction Temperature Commercial Operation	0	85	°C
t_{jind}	Junction Temperature, Industrial Operation	-40	100	°C
t_{prog}	Junction Temperature NVCM Programming	10.00	30.00	°C

Notes:

- Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{cc} and V_{ccpl} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
- See recommended voltages by I/O standard in subsequent table.
- V_{ccio} pins of unused I/O banks should be connected to the V_{cc} power supply on boards.
- V_{pp_2v5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{pp_2v5} must be connected to a power supply with a minimum 2.30 V level.

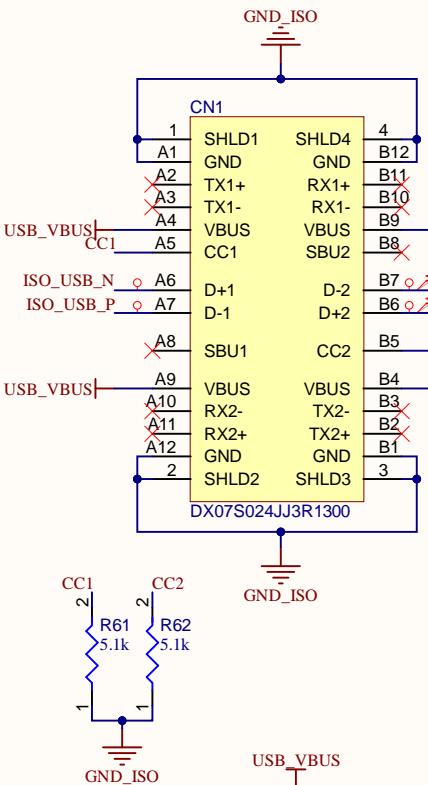
CHECK DIODES



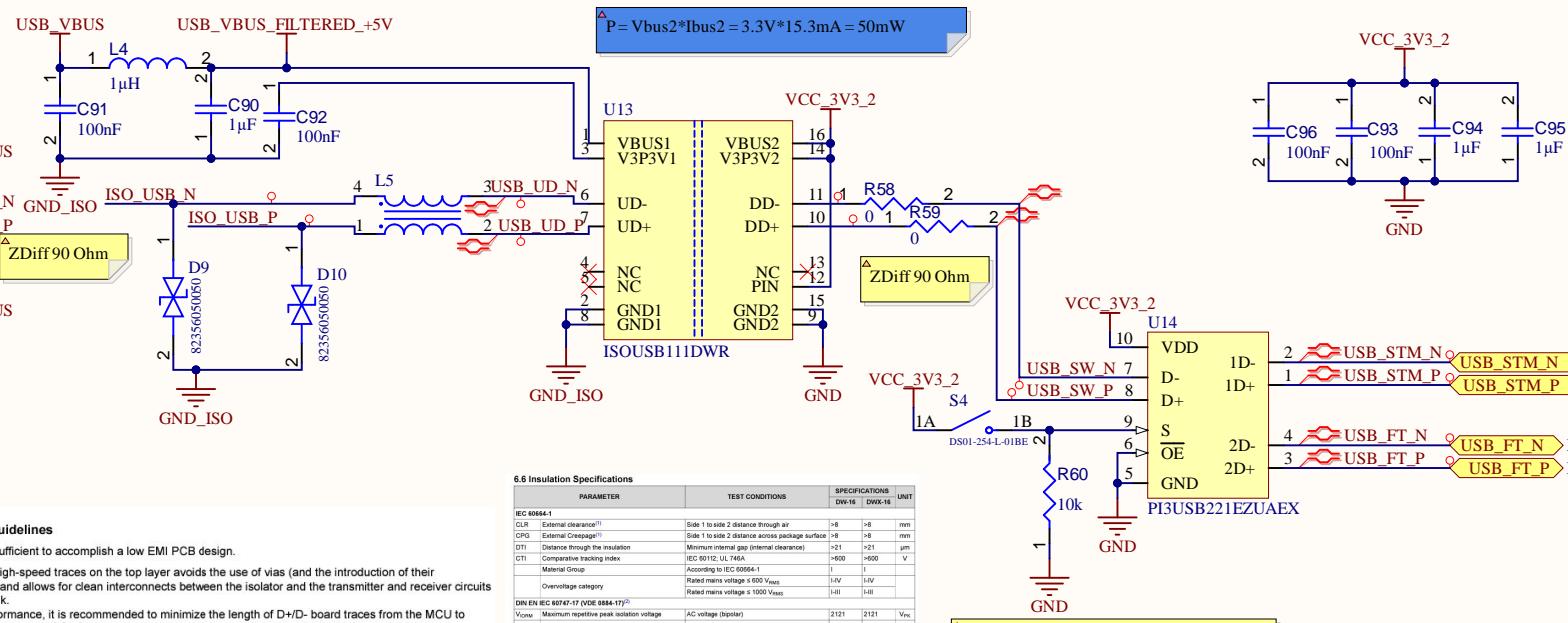
*	Project: Control BoardPrjPcb.PrjPcb		Variant: [No Variations]	Checked by:
Page Contents: Power Manage.SchDoc		DWG NO:		
Size: -				
Date: 16.09.2023 Design by: *		Sheet 6 of 9		

USB

USB-C CONNECTOR



ISOLATED USB REPEATER



Project: Control BoardPrjPcb.PrjPcb		Variant: [No Variations]	Checked by:
Page Contents: USB.SchDoc		DWG NO:	Revision:
Size:	-	-	-
Date: 16.09.2023	Design by: *	Sheet 7	d 9



CONNECTOR

A

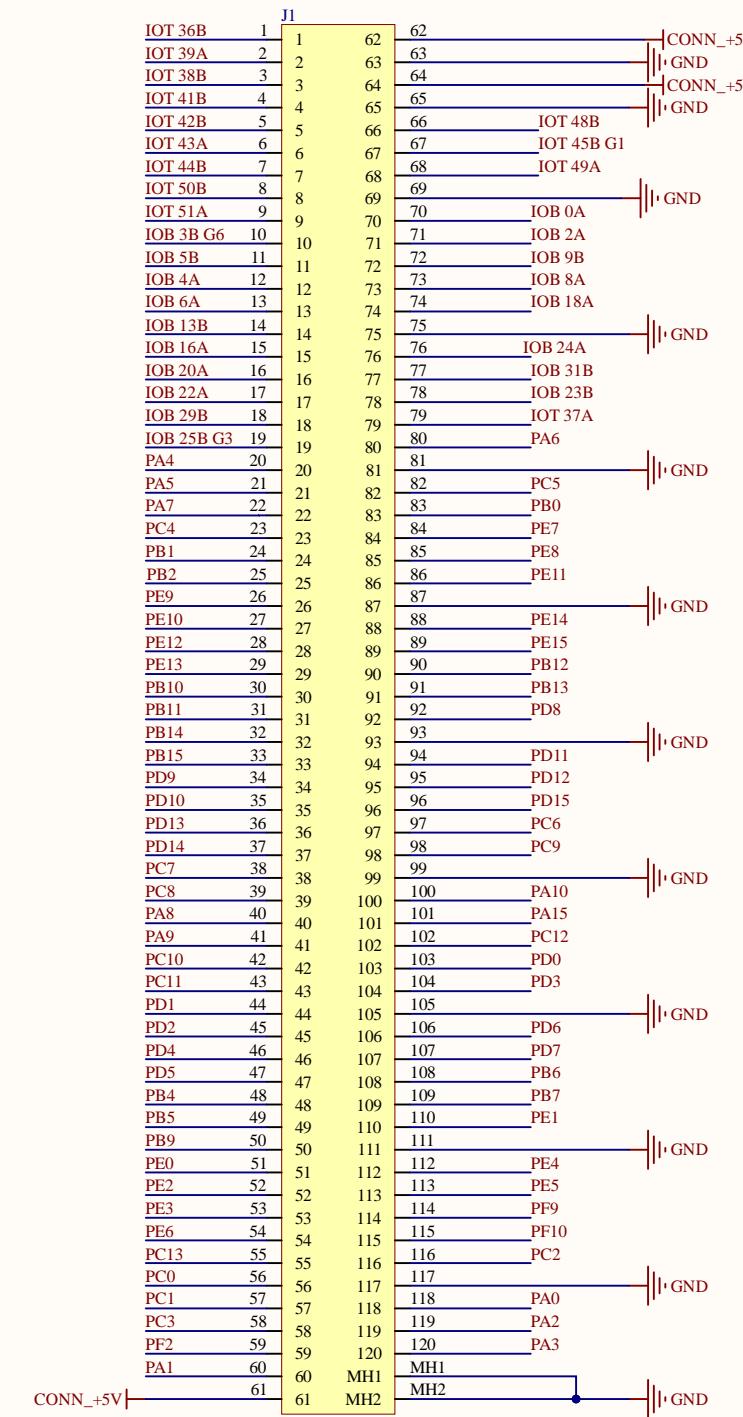
B

C

D

CONNECTOR_FPGA

- IOT 36B 1 J1
- IOT 39A 2 62 CONN_+5V
- IOT 38B 3 63 GND
- IOT 41B 4 64 CONN_+5V
- IOT 42B 5 65 GND
- IOT 43A 6 66 IOT 48B
- IOT 44B 7 67 IOT 45B G1
- IOT 50B 8 68 IOT 49A
- IOT 51A 9 69 GND
- IOB 0A 10 70 IOB 0A
- IOB 2A 11 71 IOB 2A
- IOB 4A 12 72 IOB 9B
- IOB 5B 13 73 IOB 8A
- IOB 6A 14 74 IOB 18A
- IOB 13B 15 75 GND
- IOB 16A 16 76 IOB 24A
- IOB 20A 17 77 IOB 31B
- IOB 22A 18 78 IOB 23B
- IOB 24A 19 79 IOT 37A
- IOB 25B G3 20 80 PA6
- PA4 21 81 GND
- PA5 22 82 PC5
- PA7 23 83 PB0
- PC4 24 84 PE7
- PB1 25 85 PE8
- PB2 26 86 PE11
- PE9 27 87 GND
- PE10 28 88 PE14
- PE12 29 89 PE15
- PE13 30 90 PB12
- PB10 31 91 PB13
- PB11 32 92 PD8
- PB14 33 93 GND
- PB15 34 94 PD11
- PD9 35 95 PD12
- PD10 36 96 PD15
- PD13 37 97 PC6
- PD14 38 98 PC9
- PC7 39 99 GND
- PC8 40 100 PA10
- PA8 41 101 PA15
- PA9 42 102 PC12
- PC10 43 103 PD0
- PC11 44 104 PD3
- PD1 45 105 GND
- PD2 46 106 PD6
- PD4 47 107 PD7
- PD5 48 108 PB6
- PB4 49 109 PB7
- PB5 50 110 PE1
- PB9 51 111 GND
- PE0 52 112 PE4
- PE2 53 113 PE5
- PE3 54 114 PF9
- PE6 55 115 PF10
- PC13 56 116 PC2
- PC0 57 117 GND
- PC1 58 118 PA0
- PC3 59 119 PA2
- PF2 60 120 PA3
- PA1 61 MH1
- CONN_+5V 61 MH2

**CONNECTOR STM32**

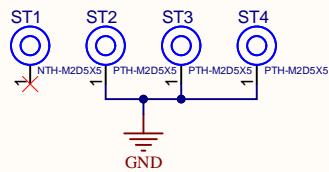
PE0	PE0
PE1	PE1
PE2	PE2
PE3	PE3
PE4	PE4
PE5	PE5
PE6	PE6
PE7	PE7
PE8	PE8
PE9	PE9
PE10	PE10
PE11	PE11
PE12	PE12
PE13	PE13
PE14	PE14
PE15	PE15
PF2	PF2
PF9	PF9
PF10	PF10
PD0	PD0
PD1	PD1
PD2	PD2
PD3	PD3
PD4	PD4
PD5	PD5
PD6	PD6
PD7	PD7
PD8	PD8
PD9	PD9
PD10	PD10
PD11	PD11
PD12	PD12
PD13	PD13
PD14	PD14
PD15	PD15
PB0	PB0
PB1	PB1
PB2	PB2
PB4	PB4
PB5	PB5
PB6	PB6
PB7	PB7
PB9	PB9
PB10	PB10
PB11	PB11
PB12	PB12
PB13	PB13
PB14	PB14
PB15	PB15
PC0	PC0
PC1	PC1
PC2	PC2
PC3	PC3
PC4	PC4
PC5	PC5
PC6	PC6
PC7	PC7
PC8	PC8
PC9	PC9
PC10	PC10
PC11	PC11
PC12	PC12
PC13	PC13
PC14	PC14
PC15	PC15
PA0	PA0
PA1	PA1
PA2	PA2
PA3	PA3
PA4	PA4
PA5	PA5
PA6	PA6
PA7	PA7
PA8	PA8
PA9	PA9
PA10	PA10
PA11	PA11

*	Project: Control BoardPrjPcb.PrjPcb	Variant: [No Variations]	Checked by:
Page Contents: Connector.SchDoc			
Size: -	DWG NO: -		Revision: *
Date: 16.09.2023	Design by: *		Sheet 8 of 9



Mechanicals

Mouting Holes

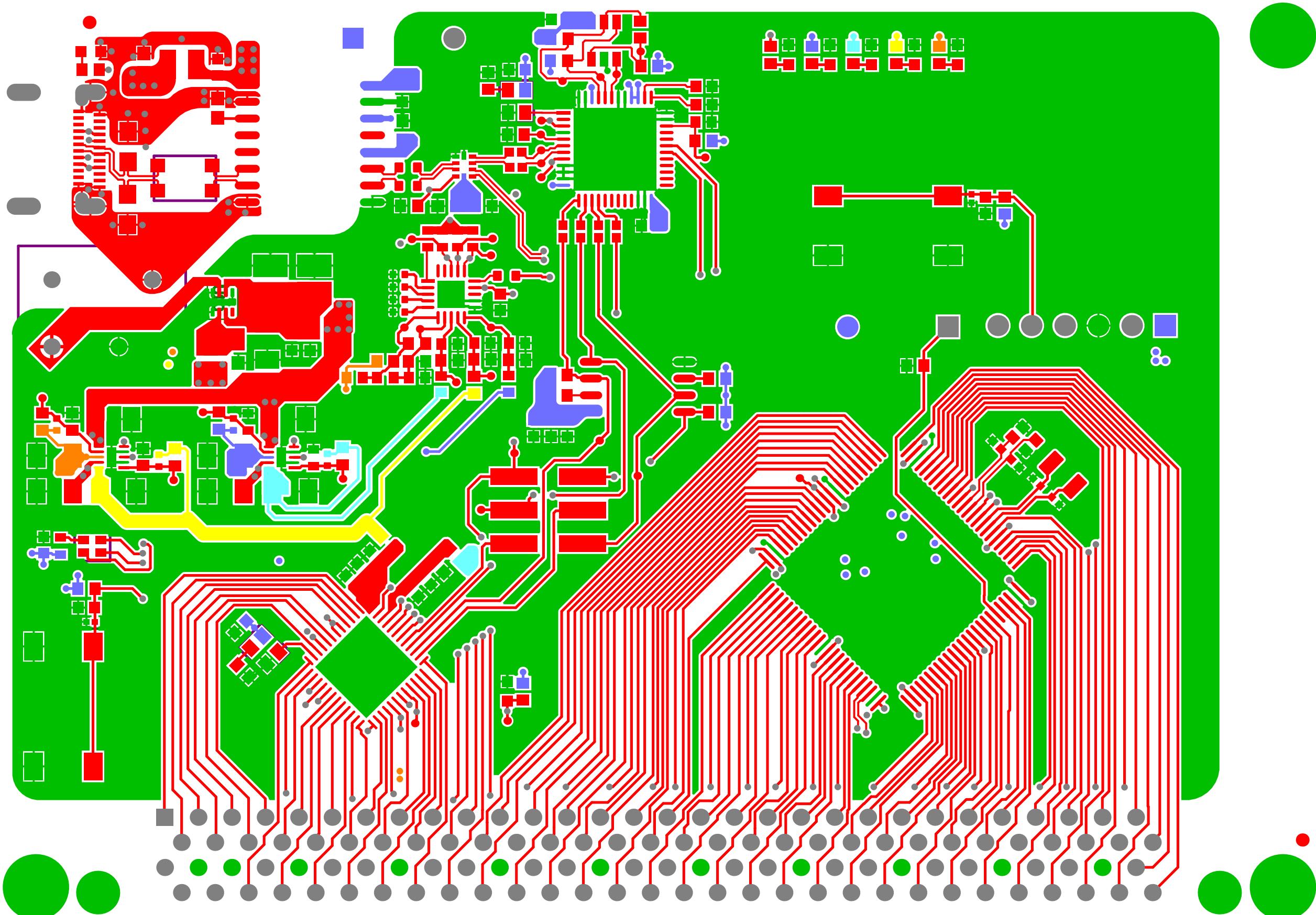


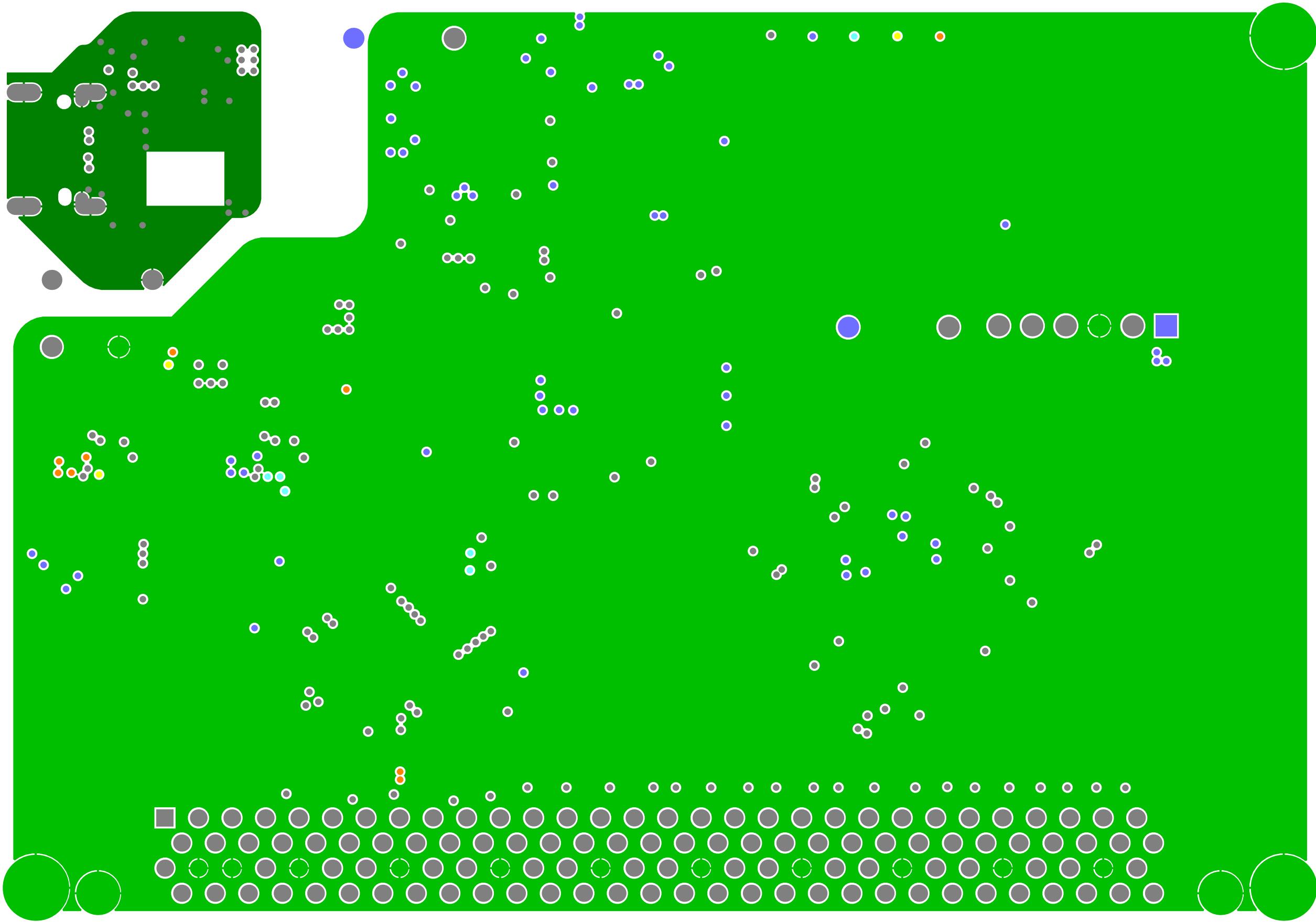
Fiducials

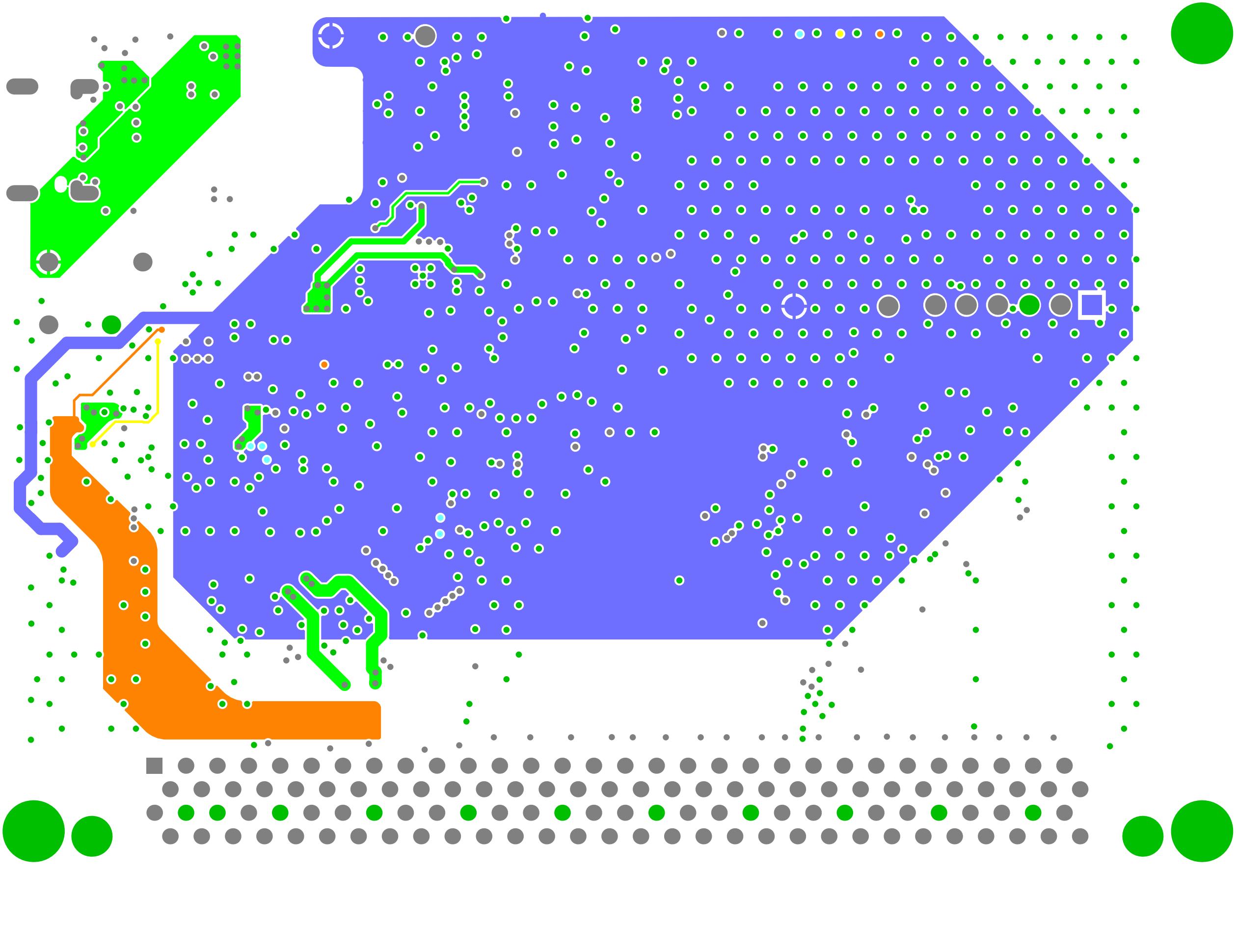


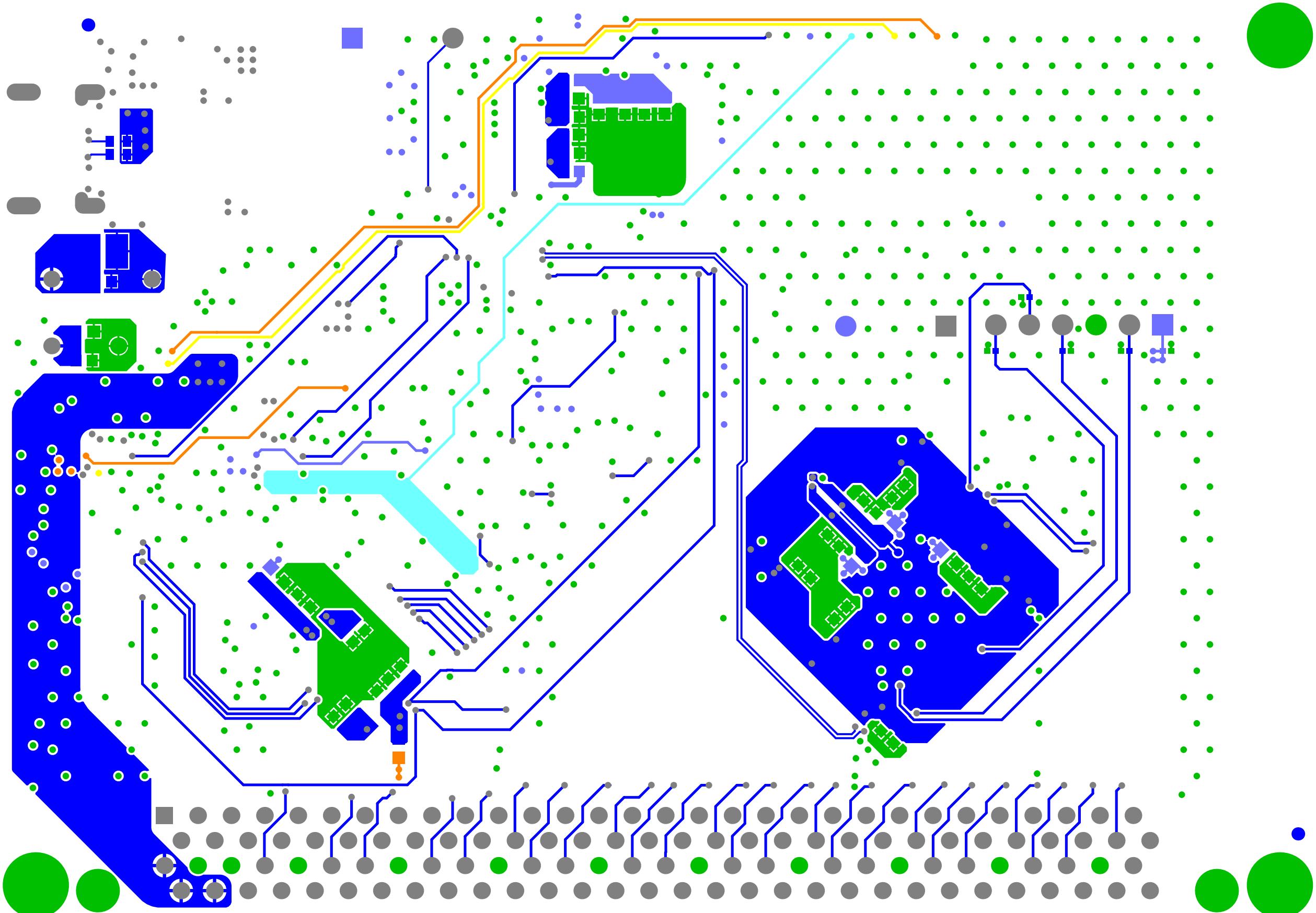
*	Variant [No Variations]	
Project:	Control BoardPrjPcb.PrjPcb	
Page Contents:	Mechanical.SchDoc	
Size:	DWG NO:	Revision:
-	-	* %
Date: 16.09.2023	Design by: *	Sheet 9 of 9

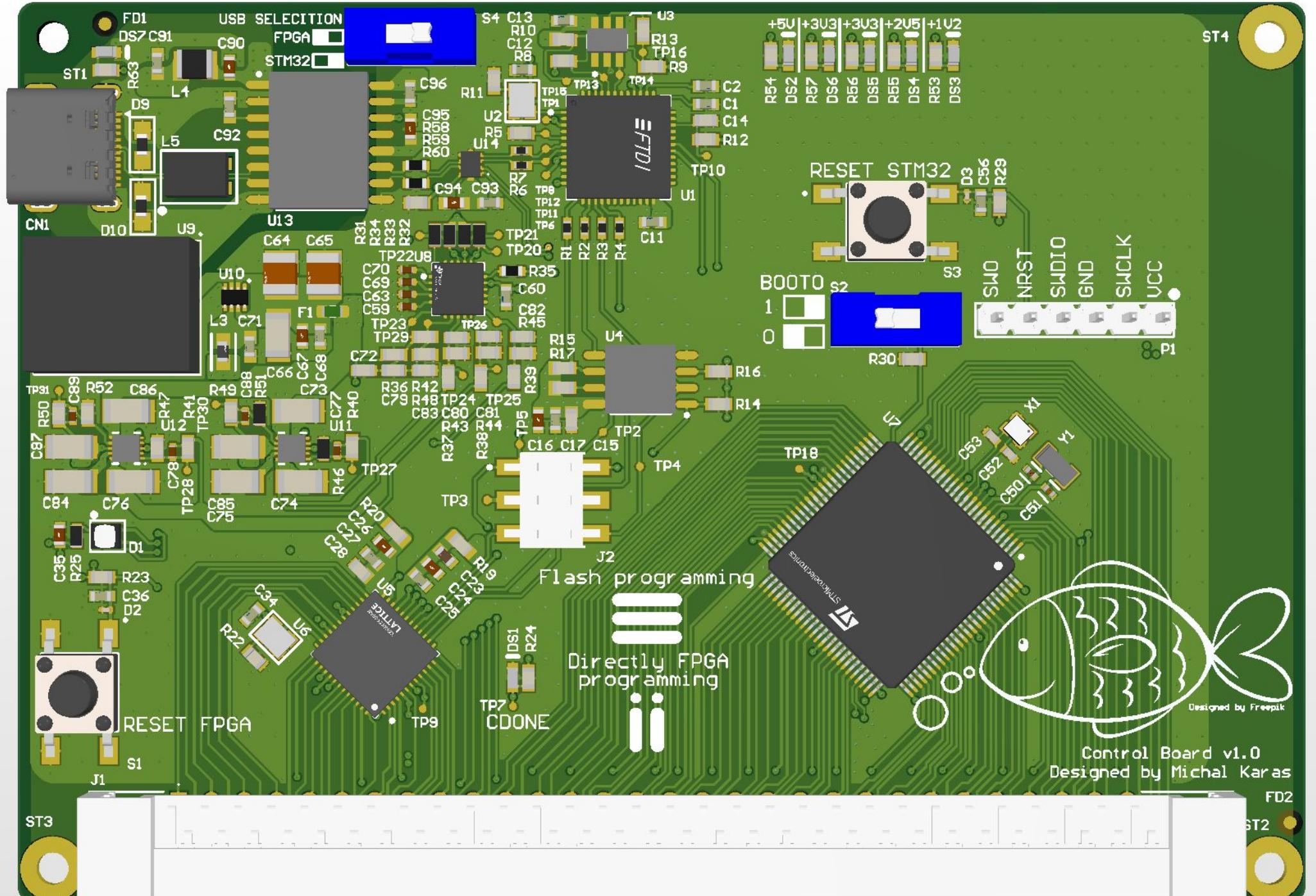
**POLITECHNIKA WARSZAWSKA
THE POLISH UNIVERSITY OF TECHNOLOGY**











Control Board v1.0
Designed by Michal Karas

ST4

FD2

ST2

FD1

Designed by Freepik

