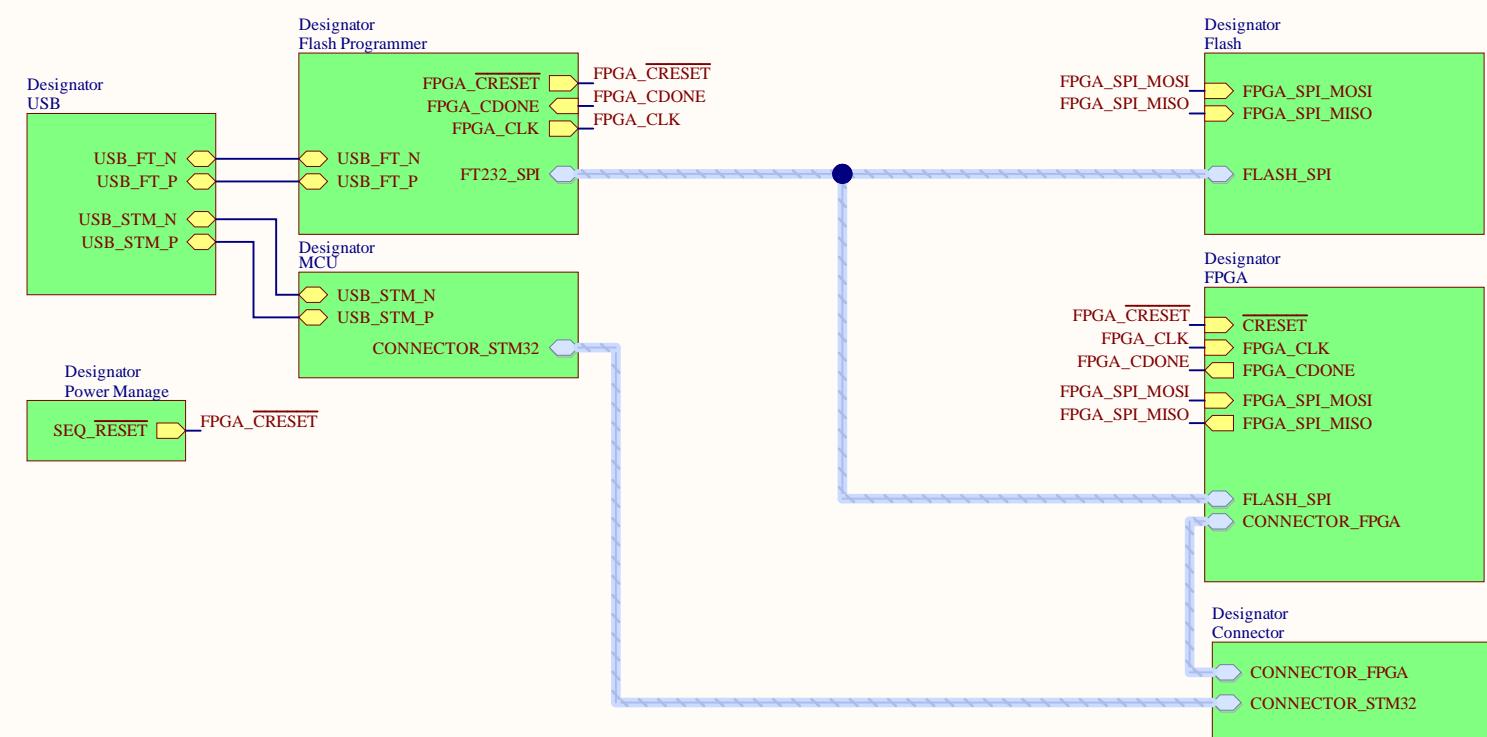


A

A



B

B

C

C

D

D

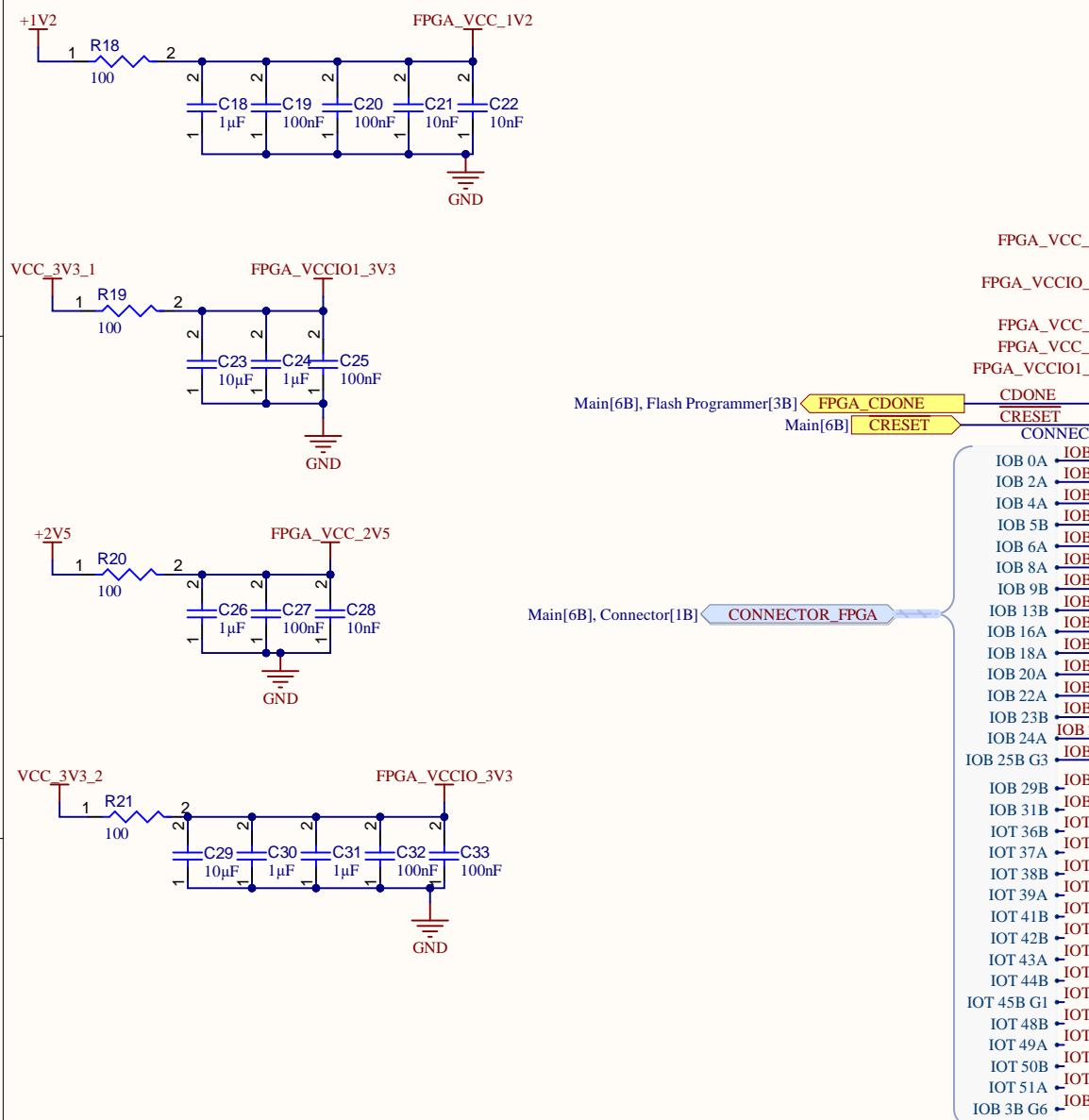


Warsaw University of Technology			
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Variant: [No Variations]			
Checked by:			
Page Contents: Main.SchDoc			
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Date: 19.09.2023	Design by: Michal Karas	Sheet 1 of 9	

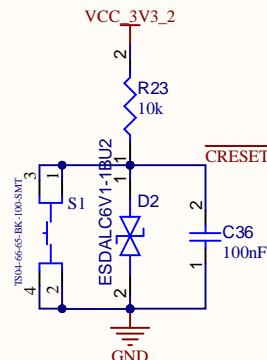
# FILTER&DECOUPLING

# FPGA

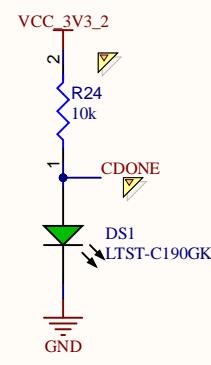
## ICE40



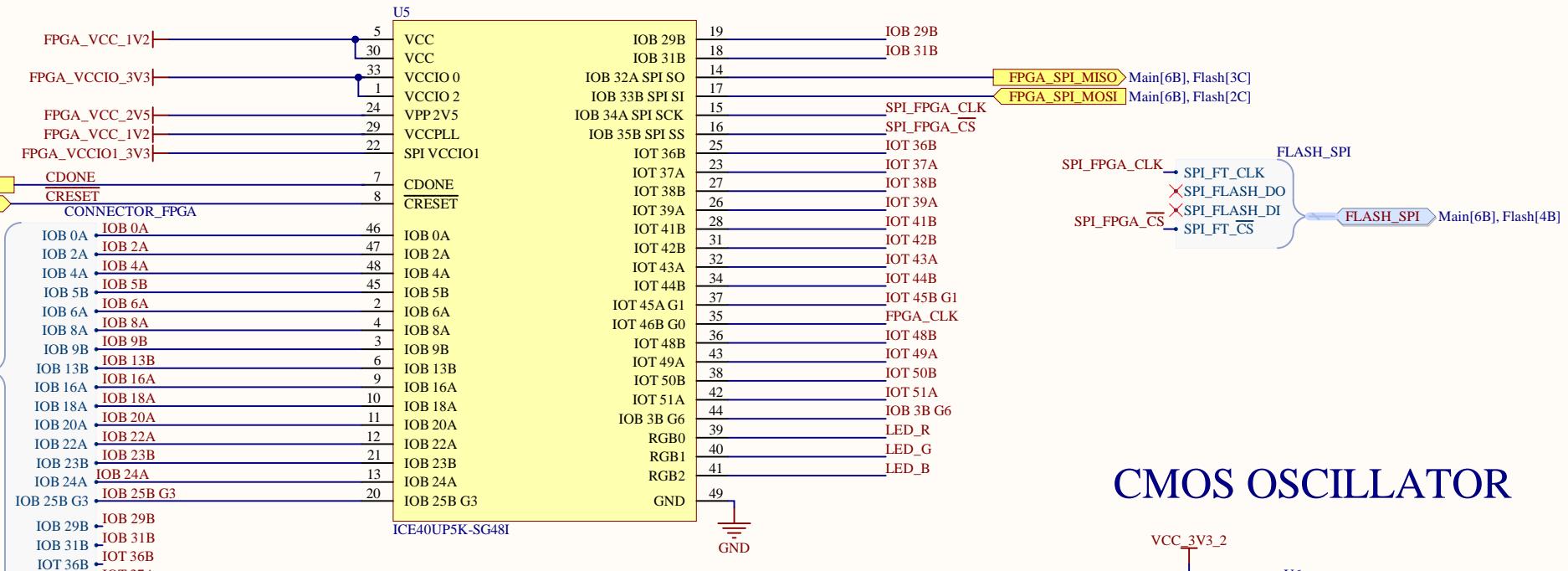
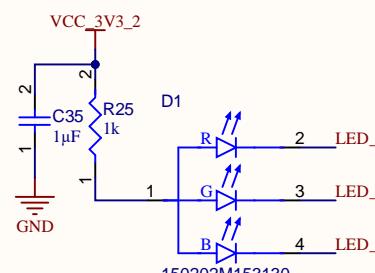
## RESET



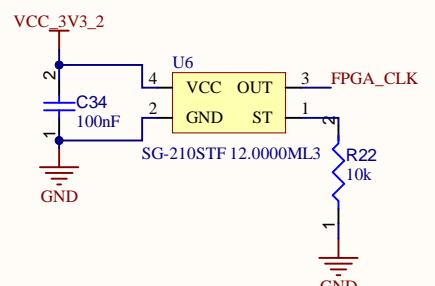
## CDONE



## LED



## CMOS OSCILLATOR



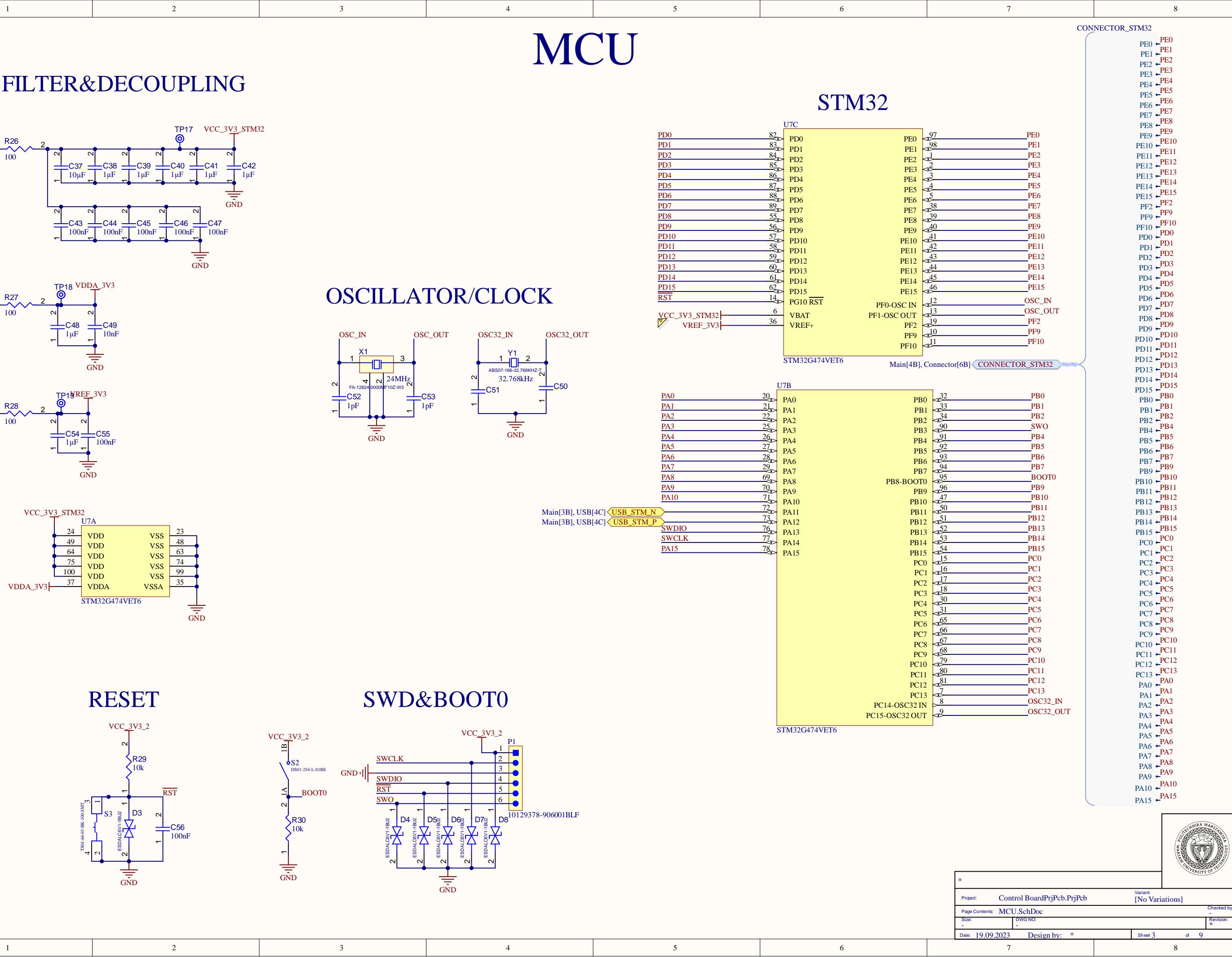
## CHECKLIST

Table 5.1. iCE40 Hardware Checklist

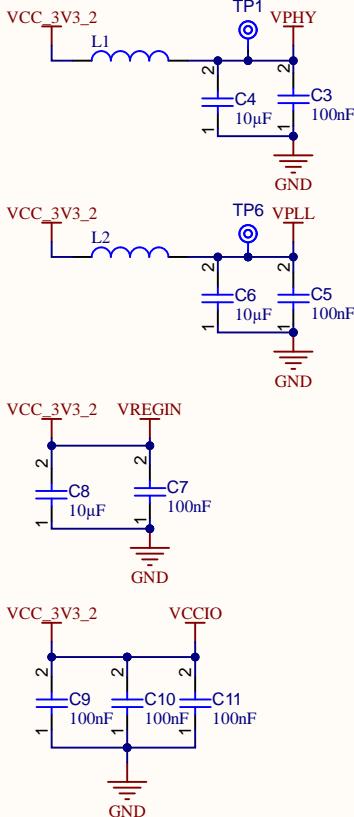
iCE40 Hardware Checklist Item	OK	N/A
1 Power Supply		
1.1 Core supply VCC at 1.2 V		
1.2 I/O power supply VCCIO 0-3 at 1.5 V to 3.3 V	X	
1.3 SPI_VCC at 1.8 V to 3.3 V	X	
1.4 VCCPLL pulled to VCC even if PLL not used	X	
1.5 Power supply filter for VCCPLL and GNDPLL	X	
1.6 GNDPLL must NOT be connected to the board*	X	
1.7 Power-up supply sequence and Ramp Rate requirements are met	X	
1.8 VPP_2V5 should not exceed 3.0V during NVCM programming	X	
2 Power-on-Reset (POR) inputs		
2.1 VCC	X	
2.2 SPI_VCC	X	
2.3 VCCIO_0-3	X	
2.4 VPP_2V5	X	
2.5 VPP_FAST	X	
3 Configuration		
3.1 Configuration mode based on SPI_SS_B	X	
3.2 Pull-up on CRESET_B_CDONE pin	X	
3.3 TRST_B is kept low for normal operation	X	
4 I/O pin assignment		
4.1 LVDS pin assignment considerations		X



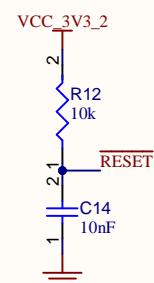
*			
Project:	Control BoardPrjPcb.PrjPcb	Variant:	[No Variations]
Page Contents:	FPGA.SchDoc	Checked by:	
Size:	-	DWG NO:	-
Date:	19.09.2023	Design by:	*
Revision:	#	Sheet 2 of 9	



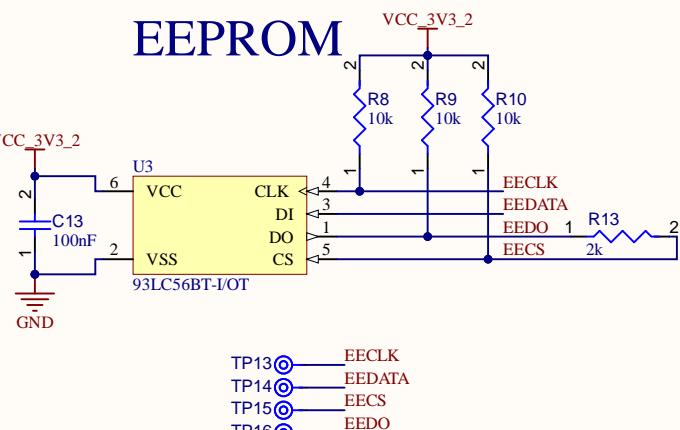
## FILTER&DECOUPLING



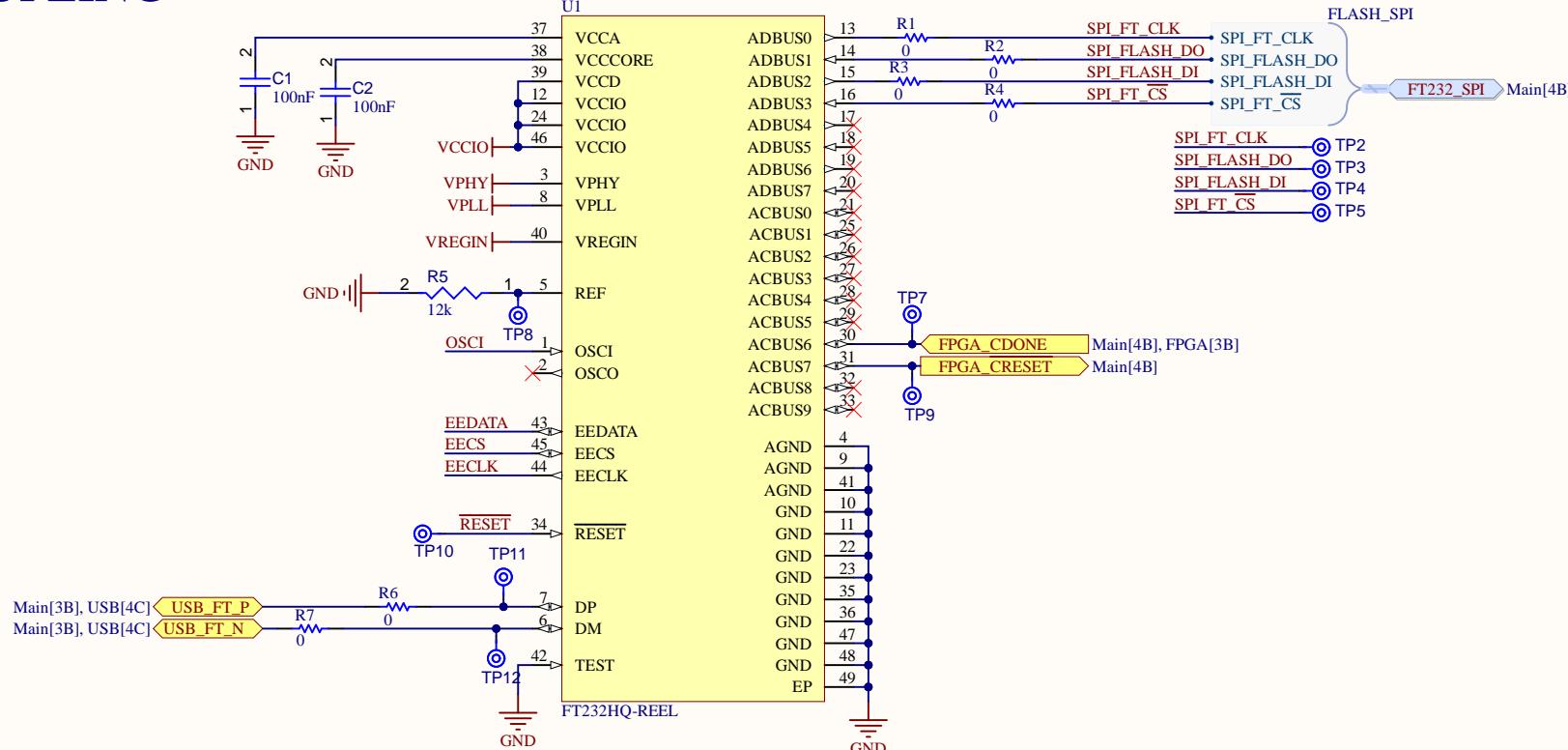
## RESET



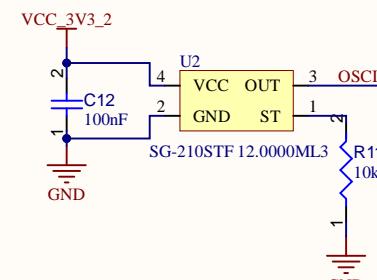
## EEPROM



# USB->SPI

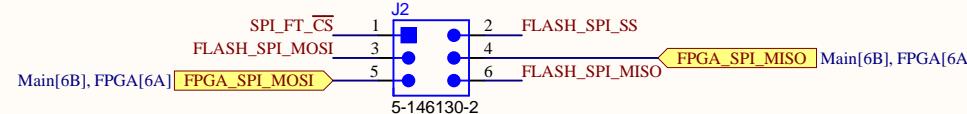
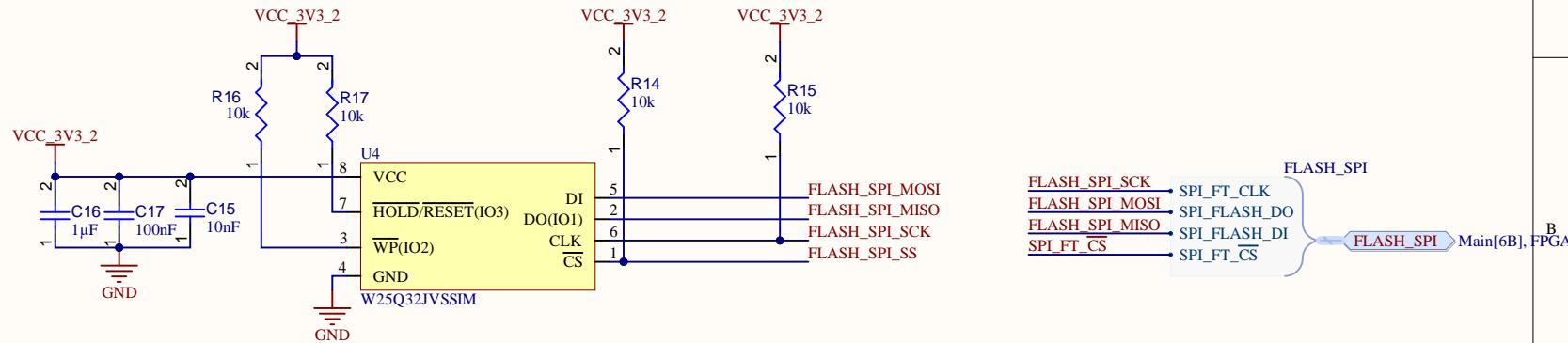


## CMOS OSCILLATOR



*	Project: Control BoardPrjPcb.PrbPcb		Variant: [No Variations]	Checked by:
Page Contents: Flash Programmer.SchDoc		DWG NO:	Revision:	
Size: -		1	1	
Date: 19.09.2023		Design by: *	Sheet 4	d 9

# FLASH



Shunt 1,2 for programming flash and normal operation.  
Remove shunt for programming FPGA

For programming Flash - shunt 3,4 and 5,6

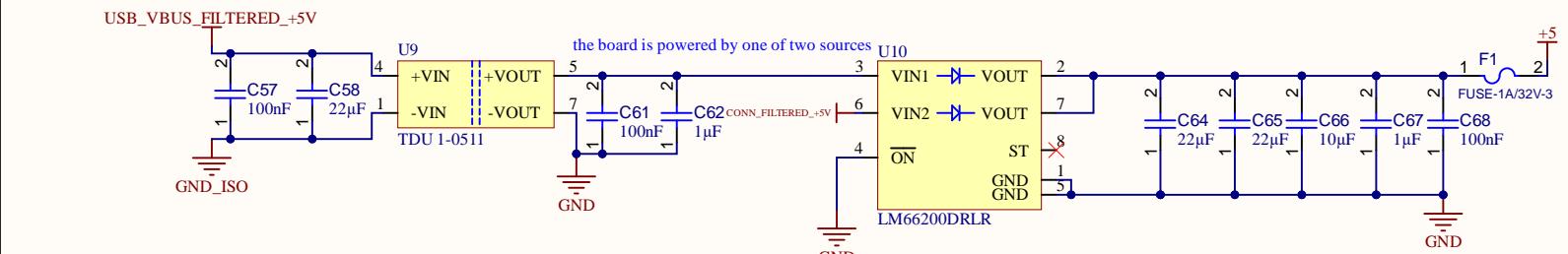
For programming FPGA directly - shunt 3,5 and 4,6

*	Variant [No Variations]	
Project:	Control BoardPrjPcb.PrjPcb	Checked by:
Page Contents:	Flash.SchDoc	DWG NO:
Size:	-	Revision:
Date:	19.09.2023	Design by: *
	Sheet 5	of 9

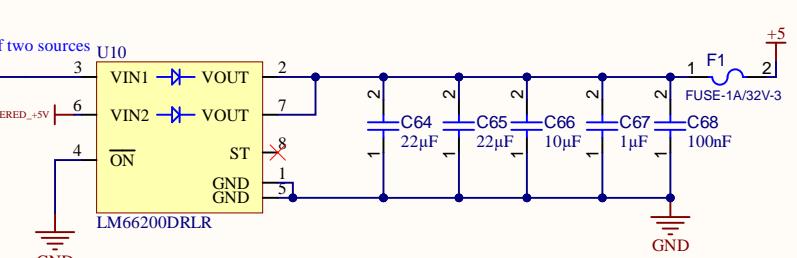


# POWER MANAGE

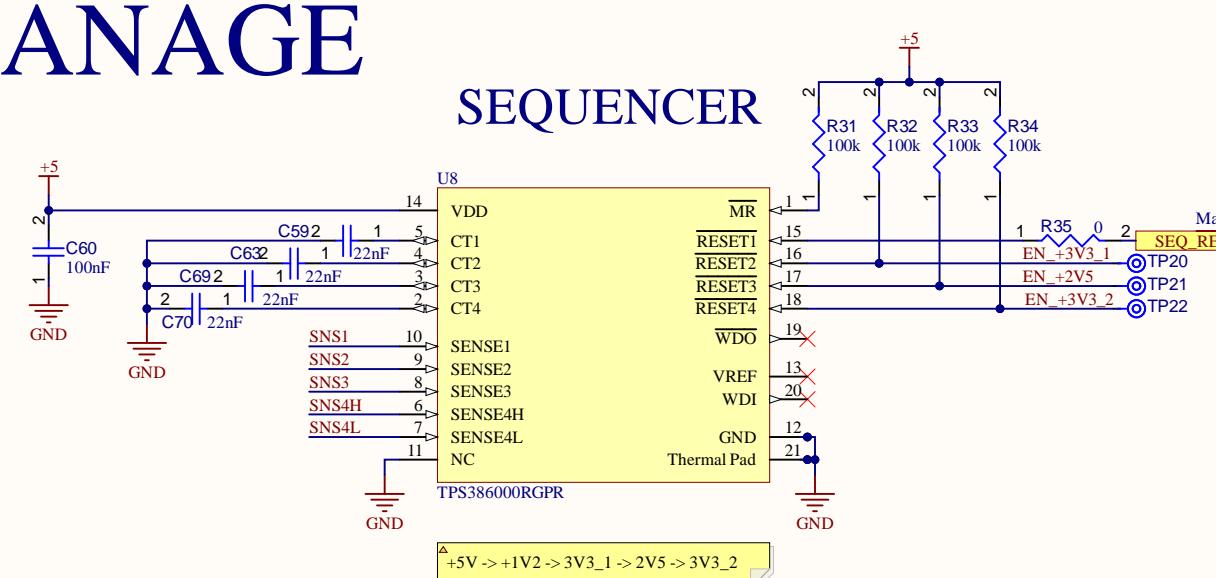
## SUPPLY FROM USB-C ISO DC/DC



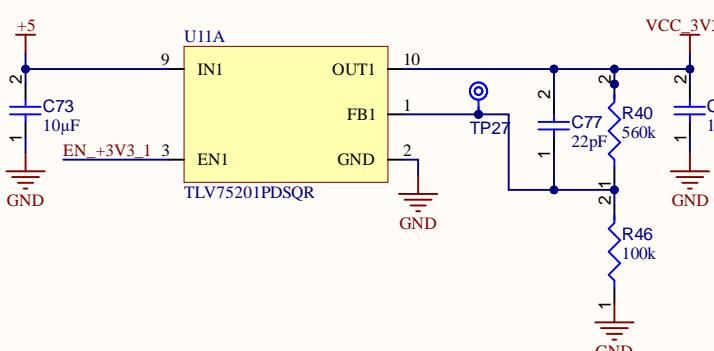
## IDEAL DIODES



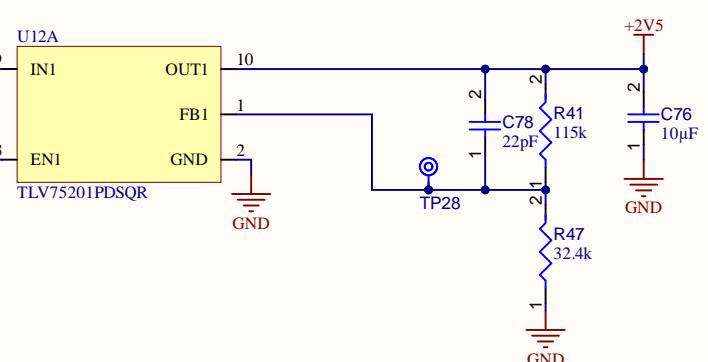
## SEQUENCER



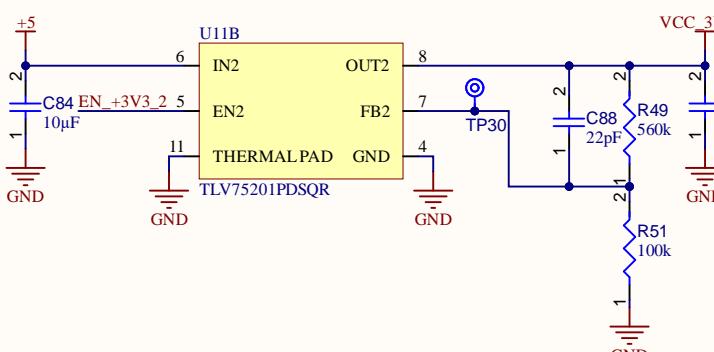
## 5V->3V3



## 5V->2.5V



## 5V->3V3



## 5V->1.2V

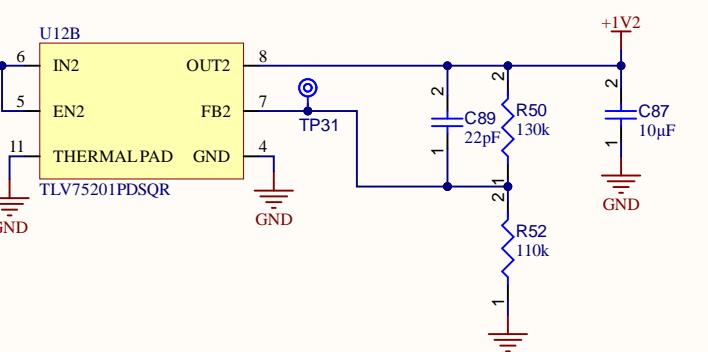


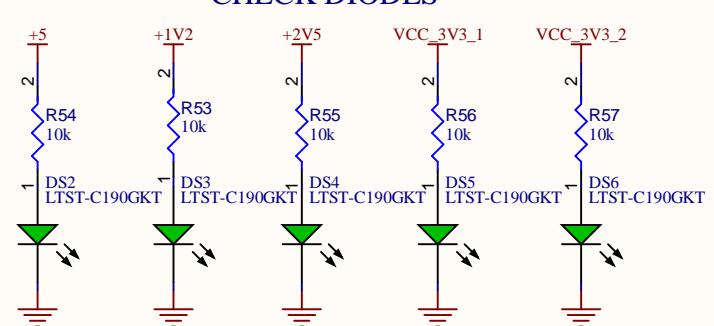
Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
$V_{cc}^{-1}$	Core Supply Voltage	1.14	1.26	V	
$V_{pp\_2v5}$	Slave SPI Configuration	1.71 <sup>4</sup>	3.46	V	
	Master SPI Configuration	2.30	3.46	V	
	Configuration from NVCM	2.30	3.46	V	
$V_{ccio}^{1,2,3}$	I/O Driver Supply Voltage	$V_{ccio\_0}, V_{ccio\_1}, V_{ccio\_2}$	1.71	3.46	V
$V_{ccpl}$	PLL Supply Voltage	1.14	1.26	V	
$t_{jcom}$	Junction Temperature Commercial Operation	0	85	°C	
$t_{jind}$	Junction Temperature, Industrial Operation	-40	100	°C	
$t_{prog}$	Junction Temperature NVCM Programming	10.00	30.00	°C	

Notes:

- Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section.  $V_{cc}$  and  $V_{ccpl}$  are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
- See recommended voltages by I/O standard in subsequent table.
- $V_{ccio}$  pins of unused I/O banks should be connected to the  $V_{cc}$  power supply on boards.
- $V_{pp\_2v5}$  can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise,  $V_{pp\_2v5}$  must be connected to a power supply with a minimum 2.30 V level.

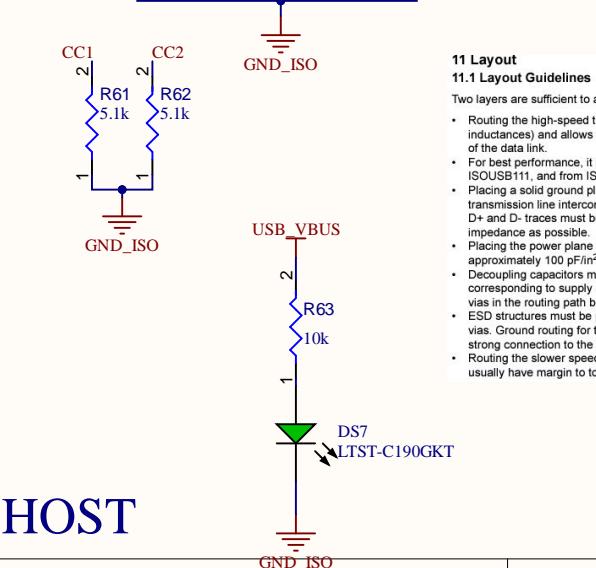
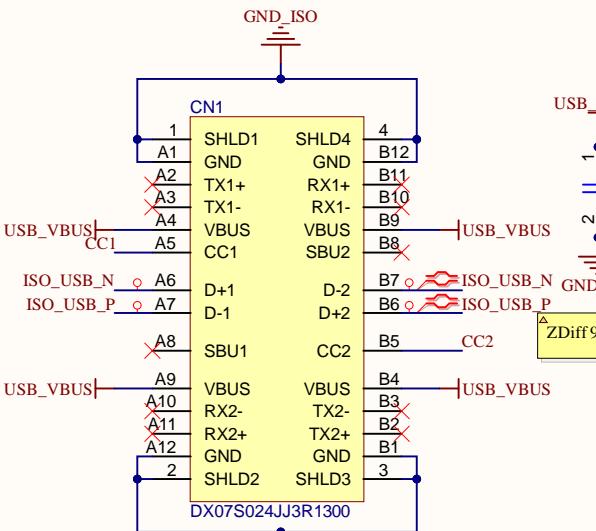
## CHECK DIODES



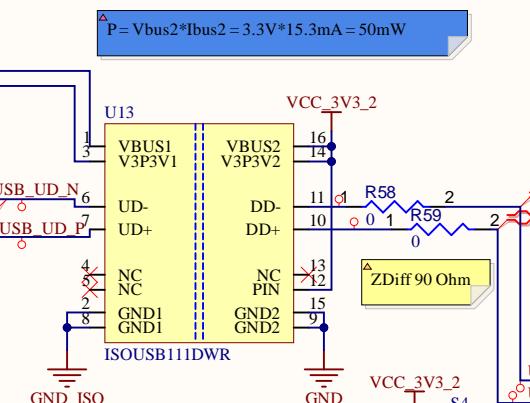
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Page Contents:	Power Manage.SchDoc		Checked by:
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# USB

## USB-C CONNECTOR

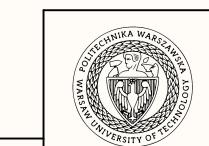


## ISOLATED USB REPEATER



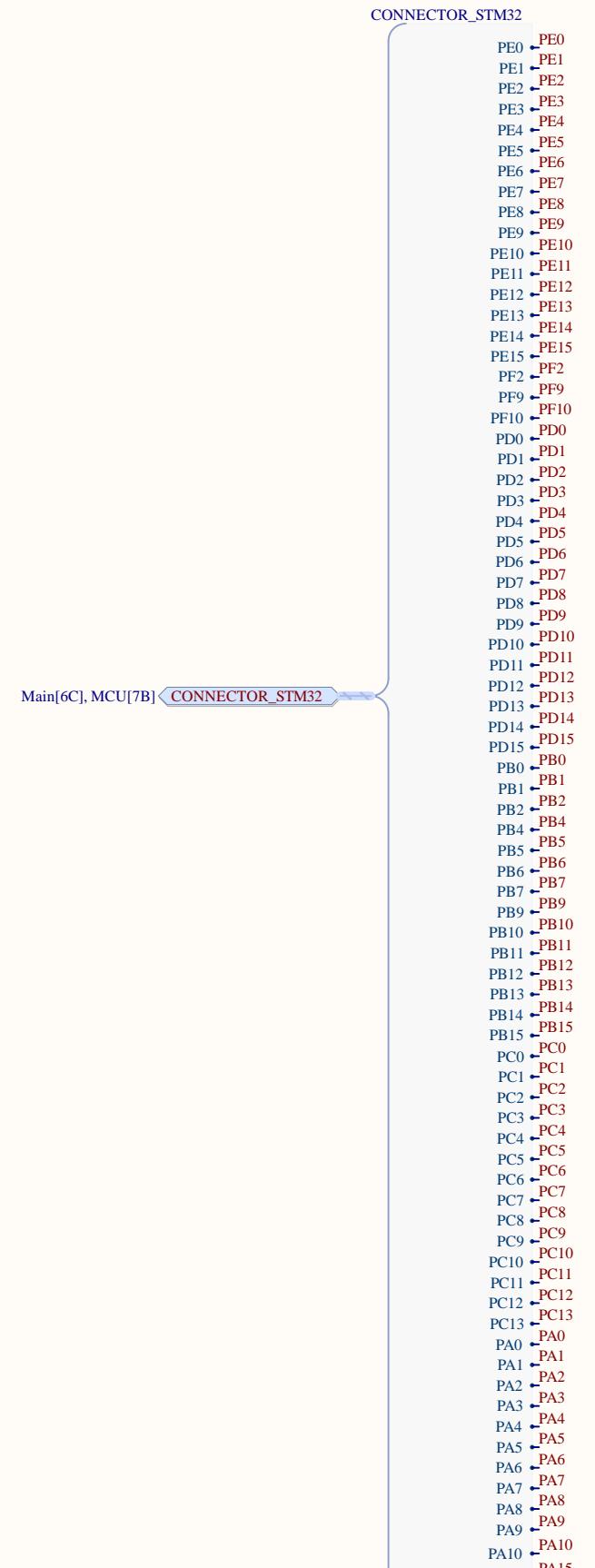
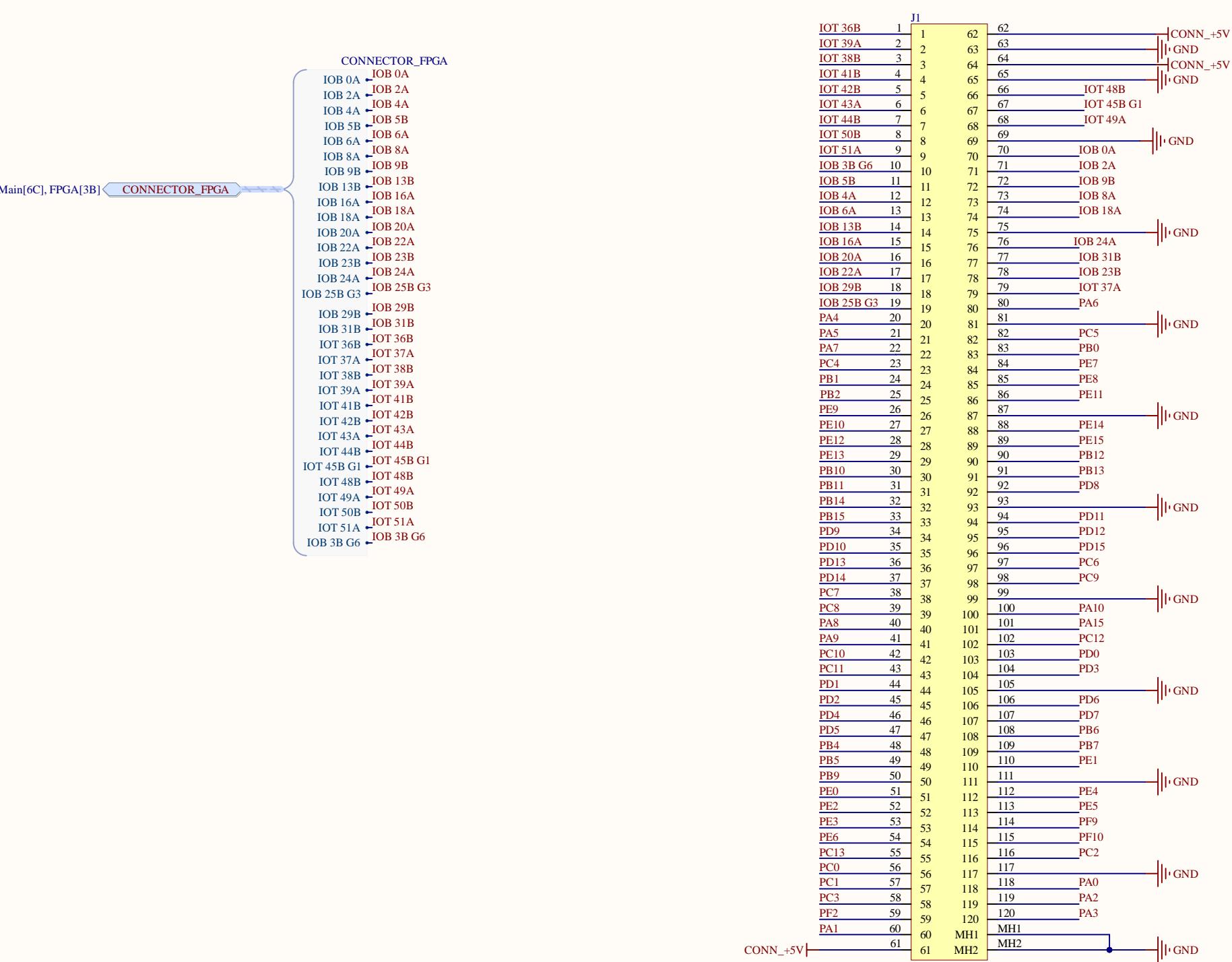
6.6 Insulation Specifications			
PARAMETER	TEST CONDITIONS	SPECIFICATIONS	DWY-16 DWY-18 UNIT
IEC 60664-1			
CLR External clearance <sup>[1]</sup>	Side 1 to side 2 distance through air	>8 mm	
CPI External Creepage <sup>[2]</sup>	Side 1 to side 2 distance across package surface	>8 mm	
DTI Dielectric strength of the insulation	Minimum dielectric strength (internal clearance)	>2100 µm	
CTI Comparative tracking index	IEC 60112, UL 746A	>6000 V	
Material Group	According to IEC 60664-1	I	
Overvoltage category	Rated mains voltage ≤ 600 V <sub>AC</sub>	II-V	
Rated mains voltage ≥ 600 V <sub>AC</sub>	III-IV		
DIN EN IEC 60747-17 (VDE 0884-11) <sup>[3]</sup>			
V <sub>com</sub> Maximum repetitive peak isolating voltage	AC voltage ( bipolar)	2121 2121 V <sub>DC</sub>	
V <sub>com</sub> Maximum repetitive peak isolating voltage	AC voltage ( sine wave); sine-dependent dielectric breakdown test (DBOT) test;	1500 1500 V <sub>DC</sub>	
V <sub>com</sub> Maximum repetitive peak isolating voltage	DC voltage ( bipolar)	2121 2121 V <sub>DC</sub>	
V <sub>com</sub> Maximum transient isolating voltage	V <sub>trans</sub> = V <sub>com</sub> + 1.60 ± 0.05 (qualification); V <sub>trans</sub> = 1.2 × V <sub>com</sub> , I = 1.5 (100% production)	7071 7071 V <sub>DC</sub>	
V <sub>imp</sub> Maximum impulse voltage <sup>[4]</sup>	Tested in air, 1.250-ns rise time waveform per IEC 62305-2	8000 8000 V <sub>DC</sub>	
V <sub>imp</sub> Maximum surge isolating voltage <sup>[5]</sup>	Tested in air (qualification test), 1.250-µs rise time waveform per IEC 62305-2	12800 12800 V <sub>DC</sub>	
R <sub>qd</sub> Apparent charge <sup>[6]</sup>	Method 4. After 100 safety test subgroups 2/3, V <sub>com</sub> = V <sub>com</sub> + 1.60 ± 0.05 V; V <sub>com</sub> = 1.2 × V <sub>com</sub> , I = 10 s	≤ 5 pC	
R <sub>qd</sub> Apparent charge <sup>[6]</sup>	Method 5. After 100 supplemental tests subgroup 1, V <sub>com</sub> = V <sub>com</sub> + 1.60 ± 0.05 V; V <sub>com</sub> = 1.2 × V <sub>com</sub> , I = 10 s	≤ 5 pC	
C <sub>qd</sub> Barrier capacitance, input to output <sup>[7]</sup>	Method 6. After 100 supplemental tests (qualification) and preconditioning (type test); V <sub>com</sub> = 1.2 × V <sub>com</sub> , I = 1 mA (method 5); or V <sub>com</sub> = V <sub>com</sub> , I = 10 mA (method 6)	≤ 5 pF	pF
R <sub>qd</sub> Insulation resistance, input to output <sup>[8]</sup>	V <sub>com</sub> = 0.4 × sin (2 π f); f = 1 MHz	0.8	Ω
R <sub>qd</sub> Insulation resistance, input to output <sup>[8]</sup>	V <sub>com</sub> = 500 V, T <sub>ext</sub> = -20 °C	> 10 <sup>12</sup>	Ω
R <sub>qd</sub> Insulation resistance, input to output <sup>[8]</sup>	V <sub>com</sub> = 500 V, T <sub>ext</sub> = 100 °C	> 10 <sup>12</sup>	Ω
Pollution degree	2	2	
Climatic category	40/125/21/40/125/21		
UL 1577			
V <sub>iso</sub> Withstand isolation voltage	V <sub>test</sub> = V <sub>iso</sub> + 1.60 ± 0.05 (qualification); V <sub>test</sub> = 1.2 × V <sub>iso</sub> ; I = 1.5 (100% production)	5000 5000 V <sub>DC</sub>	

Depend on selected IC shall be switch ON or OFF  
ON FPGA/FLASH(2D)  
OFF STM32(1D)



Project: Control BoardPrjPcb.PrjPcb		Variant [No Variations]	Checked by:
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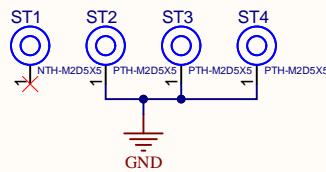
# CONNECTOR



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Sheet <b>8</b> of <b>Q</b>	

# Mechanicals

## Mouting Holes



## Fiducials



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Date: 19.09.2023	Design by: *	Sheet 9 of 9

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