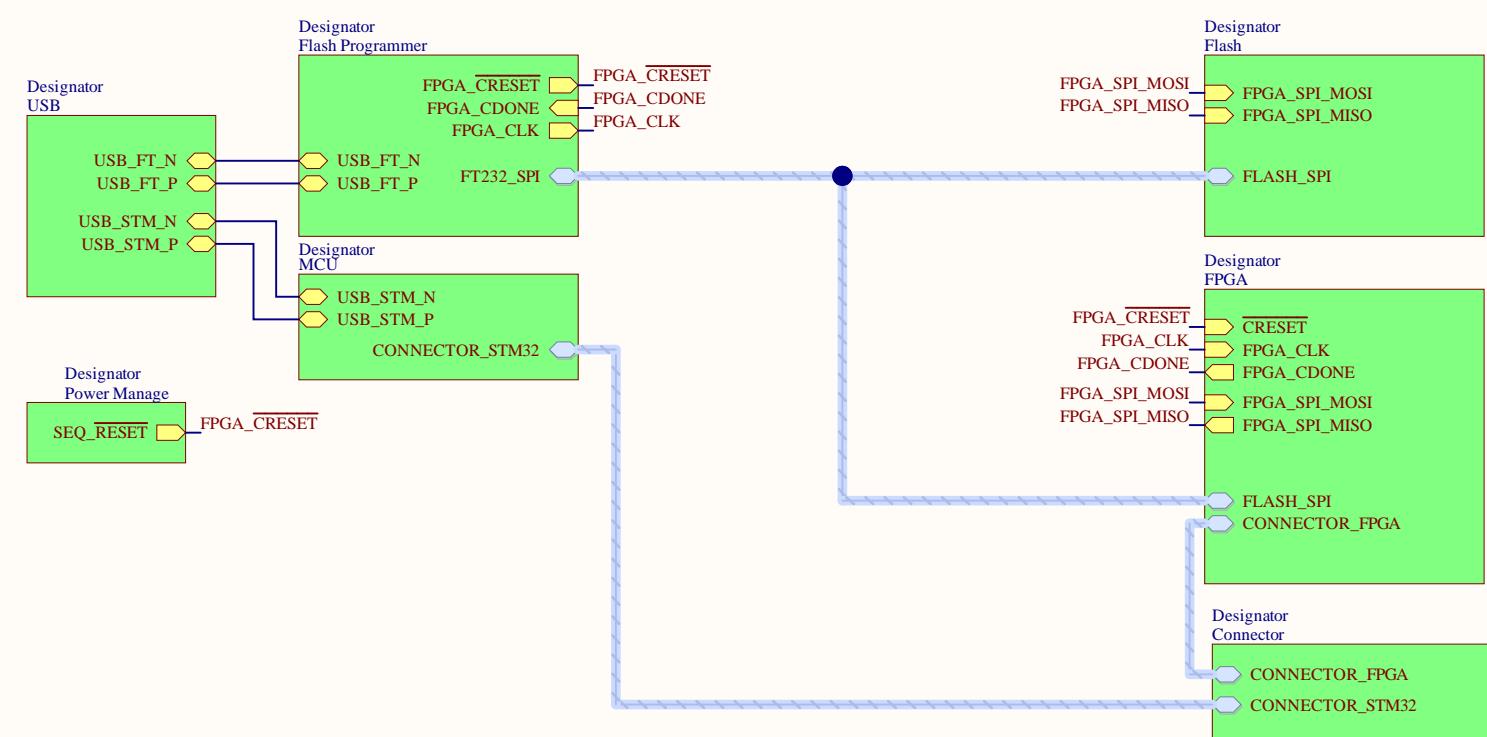


A

A



B

B

C

C

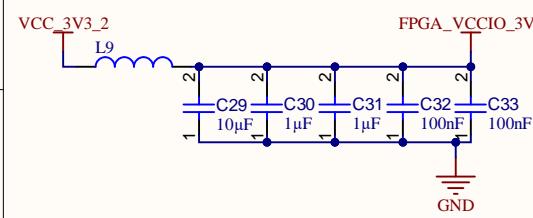
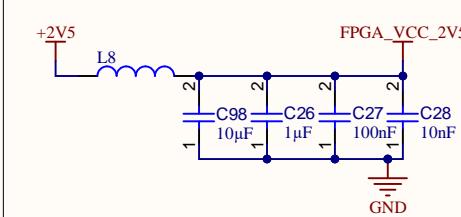
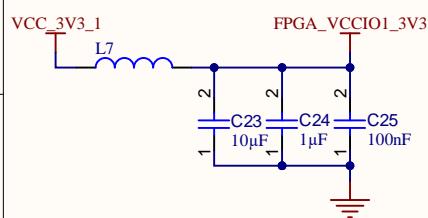
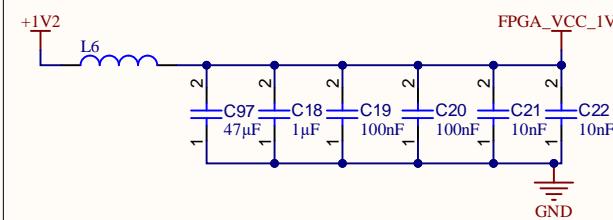
D

D

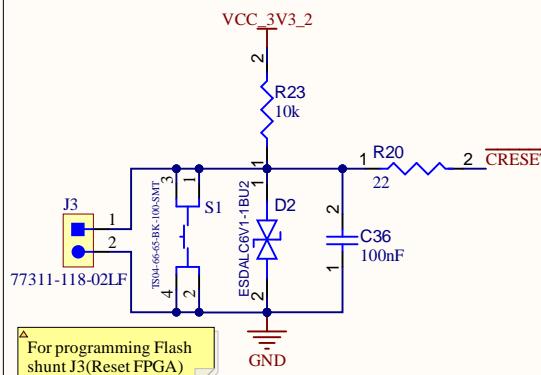


Warsaw University of Technology			
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Variant: [No Variations]			
Checked by:			
Page Contents: Main.SchDoc			
Size: -	DWG NO: -	Revision: -	
Date: 06.09.2024	Design by: Michal Karas	Sheet 1 of 9	

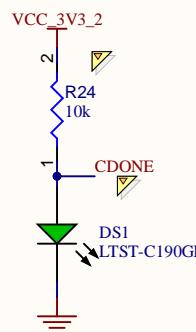
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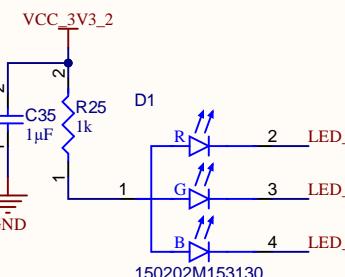
RESET



CDONE

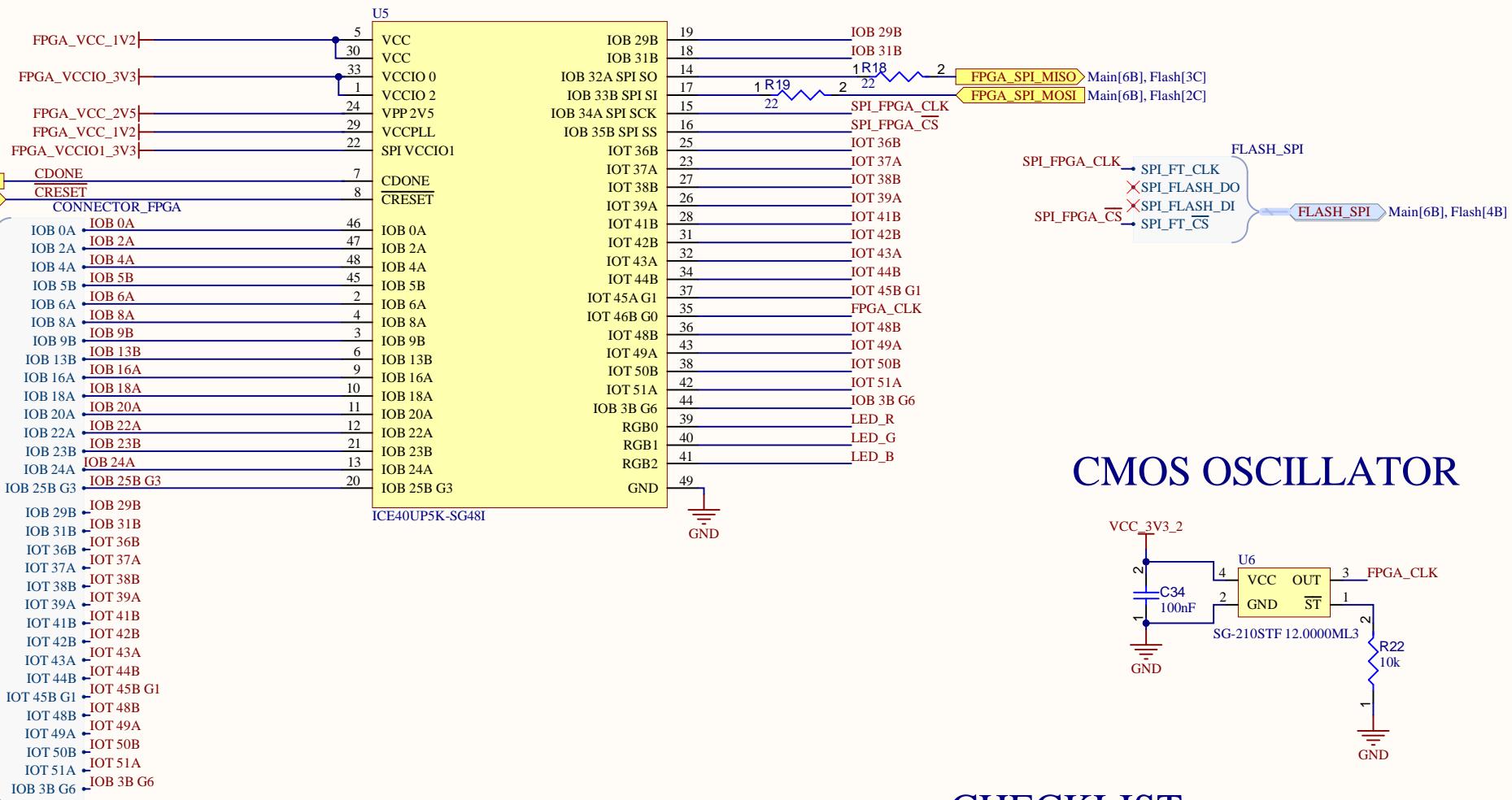


LED

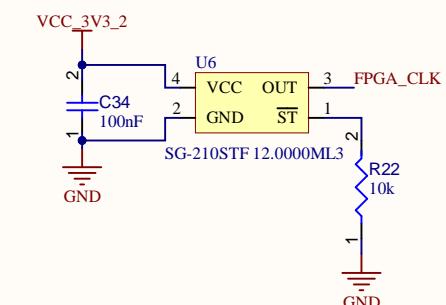


FPGA

ICE40



CMOS OSCILLATOR



CHECKLIST

Table 5.1. iCE40 Hardware Checklist

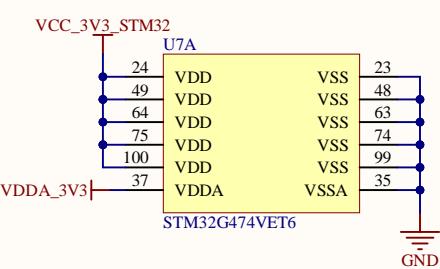
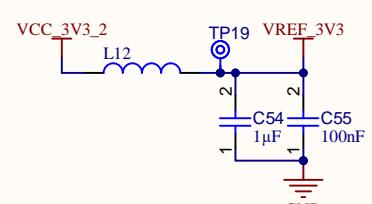
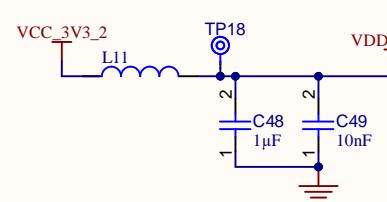
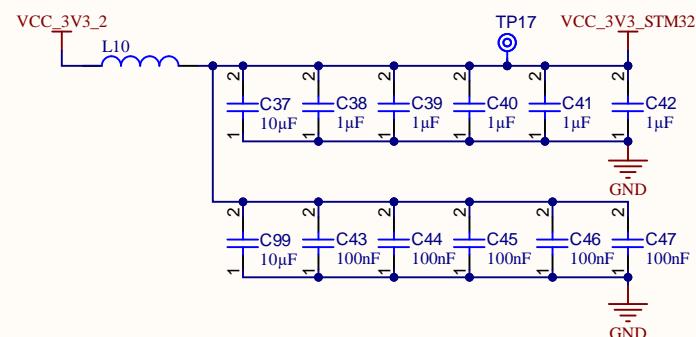
iCE40 Hardware Checklist Item	OK	N/A
1 Power Supply		
1.1 Core supply VCC at 1.2 V		
1.2 I/O power supply VCCIO 0-3 at 1.5 V to 3.3 V	X	
1.3 SPI_VCC at 1.8 V to 3.3 V	X	
1.4 VCCPLL pulled to VCC even if PLL not used	X	
1.5 Power supply filter for VCCPLL and GNDPLL		
1.6 GNDPLL must NOT be connected to the board*	X	
1.7 Power-up supply sequence and Ramp Rate requirements are met	X	
1.8 VPP_2V5 should not exceed 3.0V during NVCM programming	X	
2 Power-on-Reset (POR) inputs		
2.1 VCC	X	
2.2 SPI_VCC	X	
2.3 VCCIO_0-3	X	
2.4 VPP_2V5	X	
2.5 VPP_FAST		X
3 Configuration		
3.1 Configuration mode based on SPI_SS_B	X	
3.2 Pull-up on CRESET_B_CDONE pin	X	
3.3 TRST_B is kept low for normal operation	X	
4 I/O pin assignment		
4.1 LVDS pin assignment considerations		X



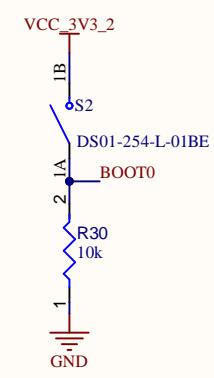
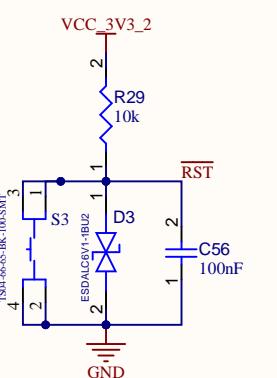
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Page Contents:	FPGA.SchDoc	
Size:	DWG NO:	
Revision:	-	
Date:	06.09.2024	
Design by:	*	
Sheet 2 of 9		

MCU

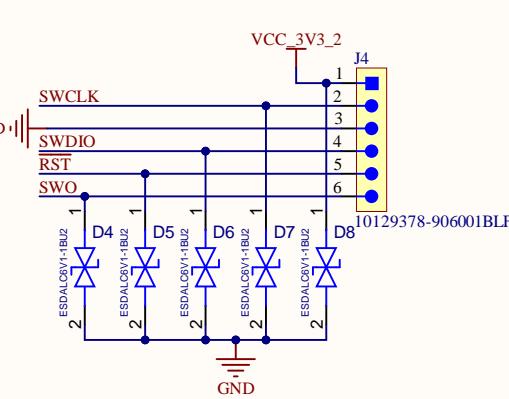
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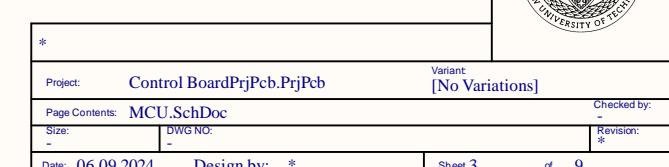
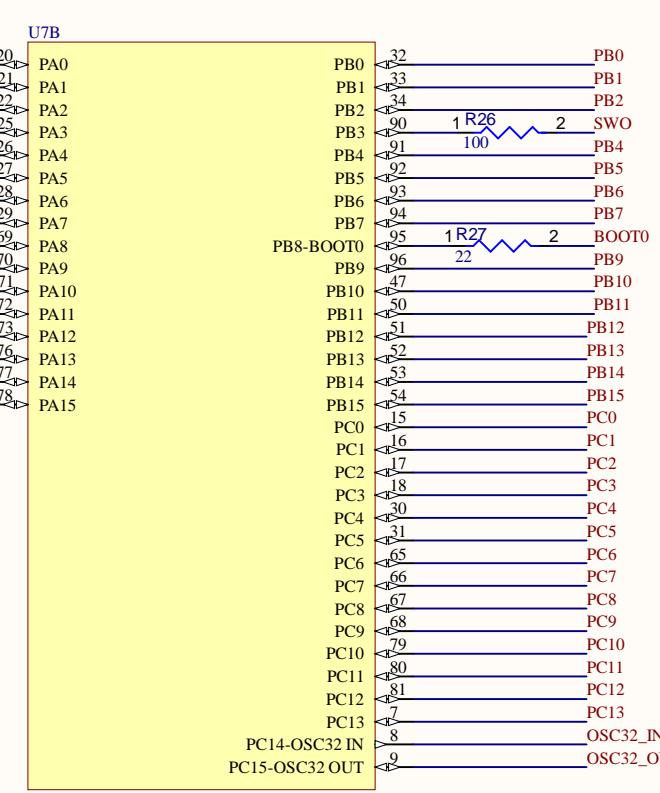
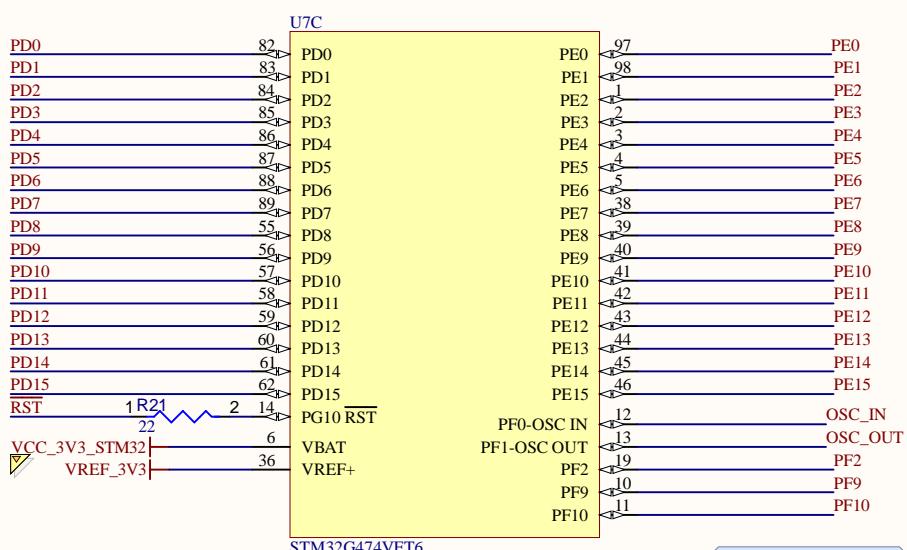
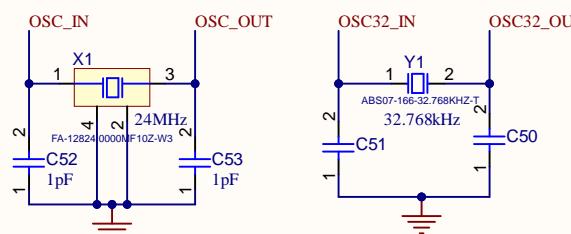
RESET



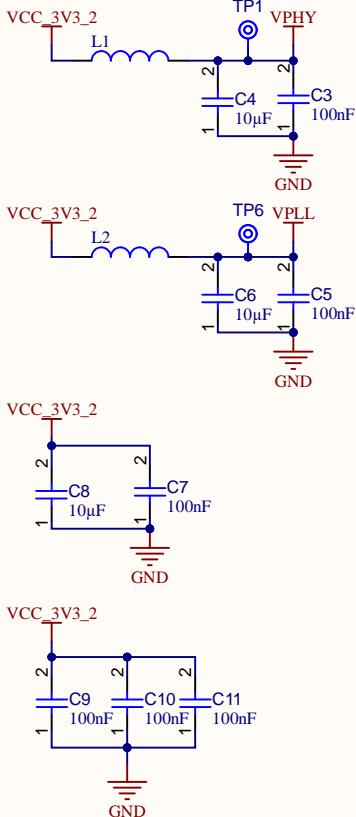
SWD&BOOT0



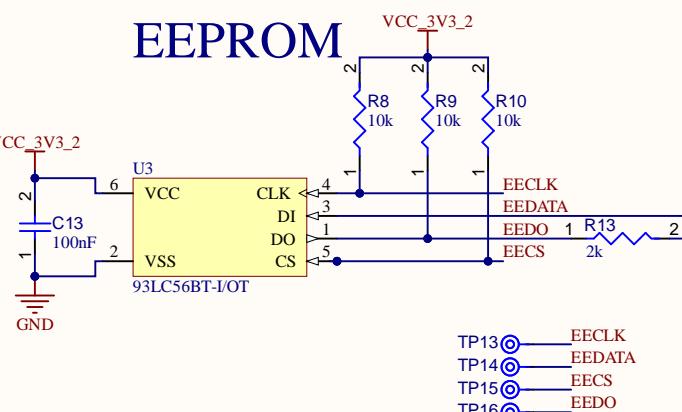
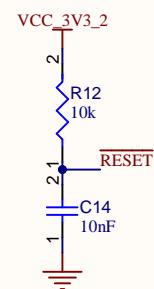
OSCILLATOR/CLOCK



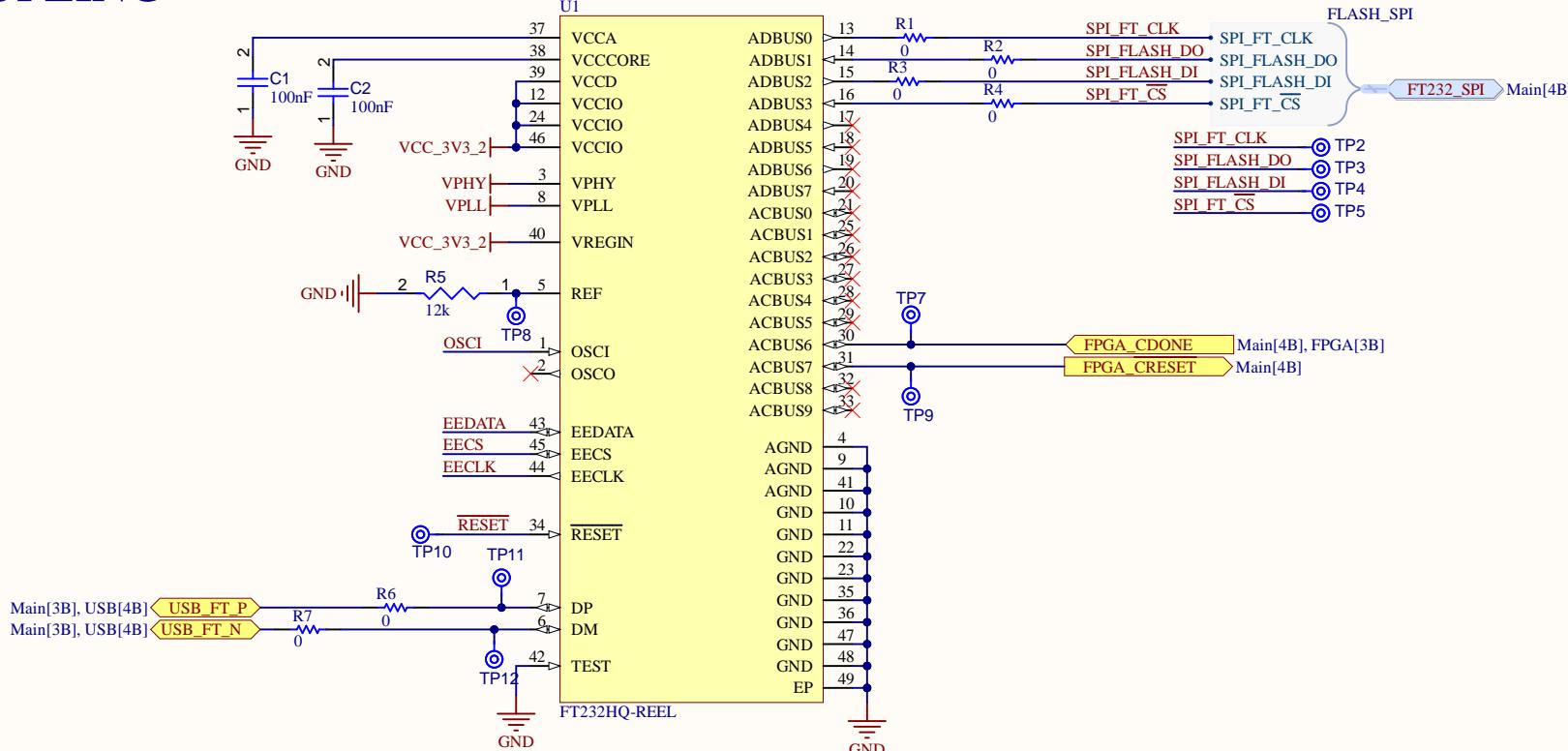
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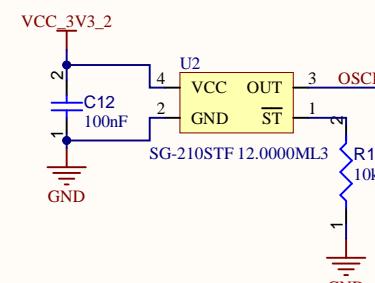
RESET



USB->SPI

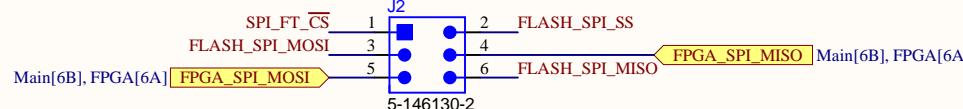
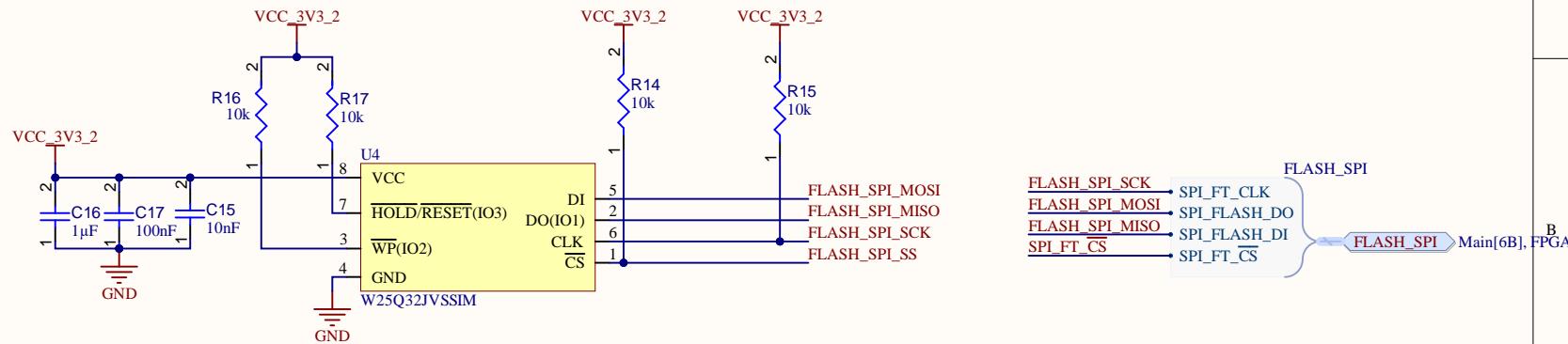


CMOS OSCILLATOR



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Page Contents: Flash Programmer.SchDoc		DWG NO:	Revision:	
Size: -		0	0	
Date: 06.09.2024		Design by: *	Sheet 4	d 9

FLASH



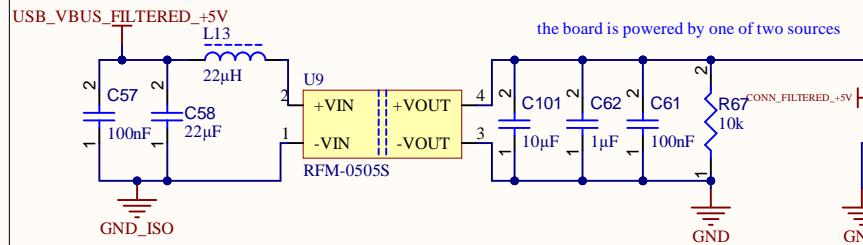
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Size:	-	-	Revision:
Date:	06.09.2024	Design by:	* Sheet 5 of 9

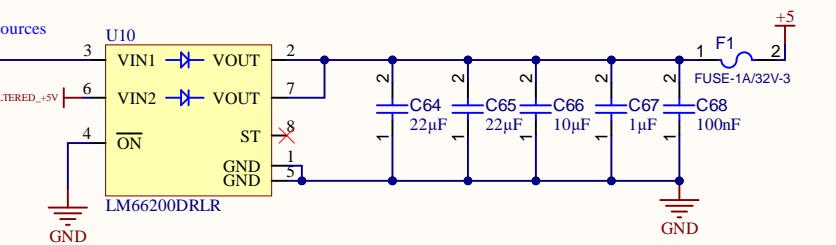


POWER MANAGE

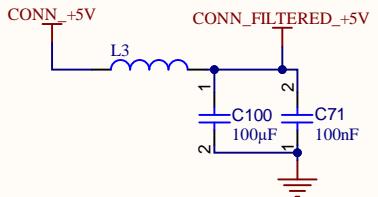
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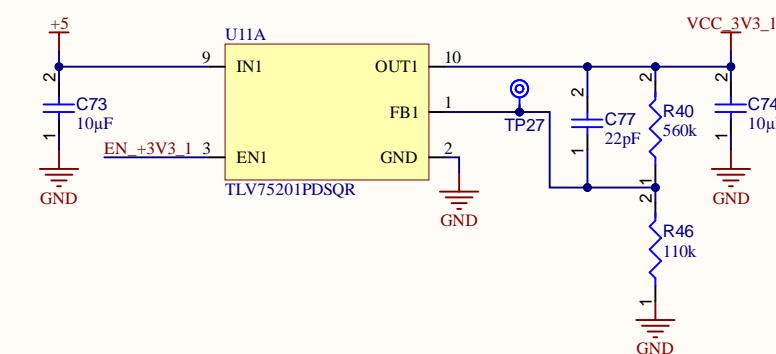
IDEAL DIODES



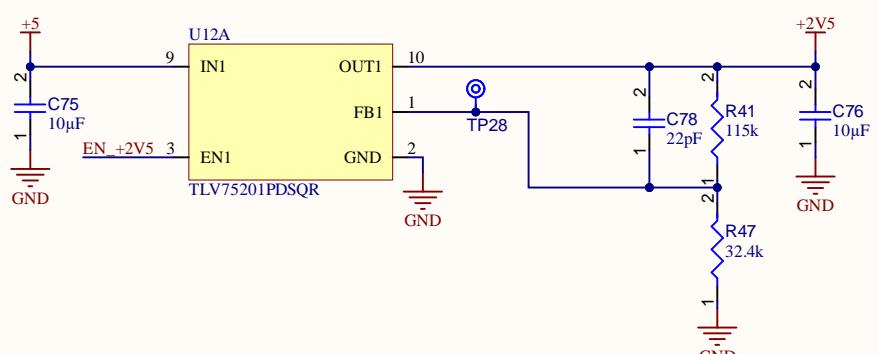
SUPPLU FROM CONNECTOR



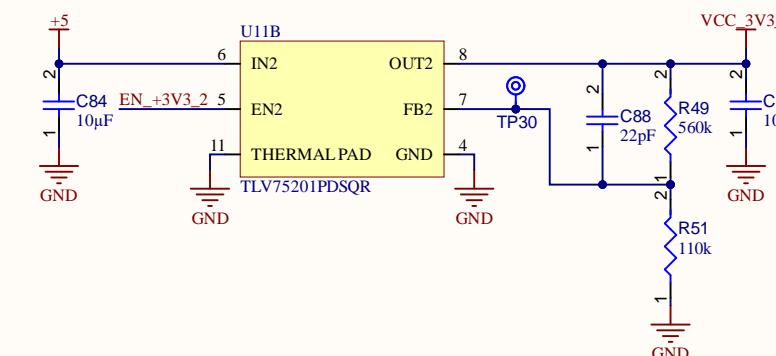
5V->3V3



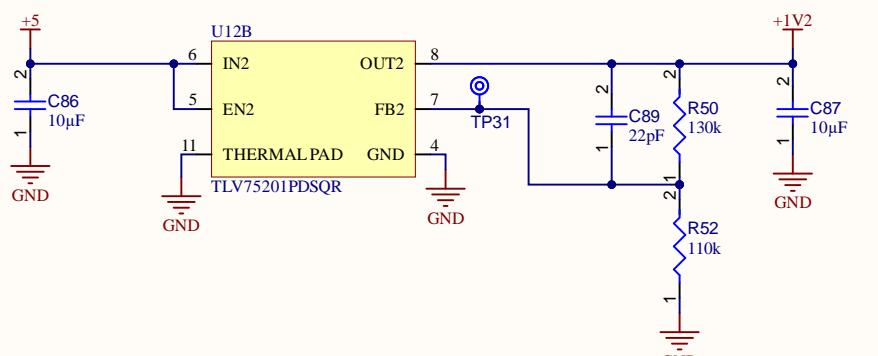
5V->2.5V



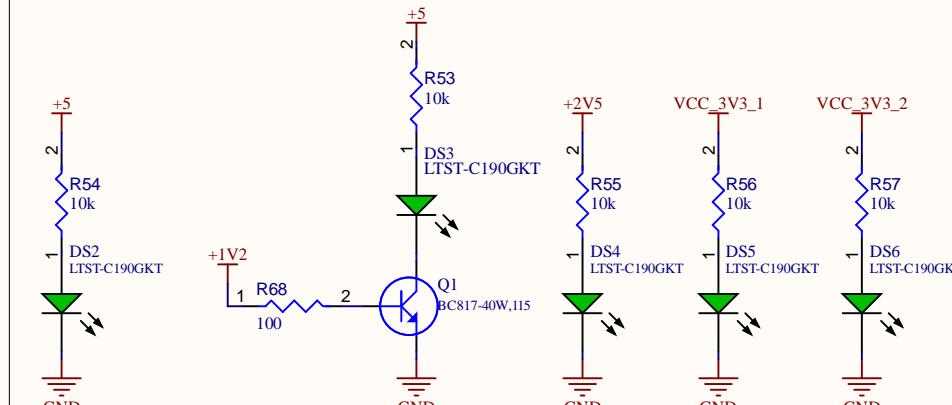
5V->3V3



5V->1.2V



CHECK DIODES



SEQUENCER

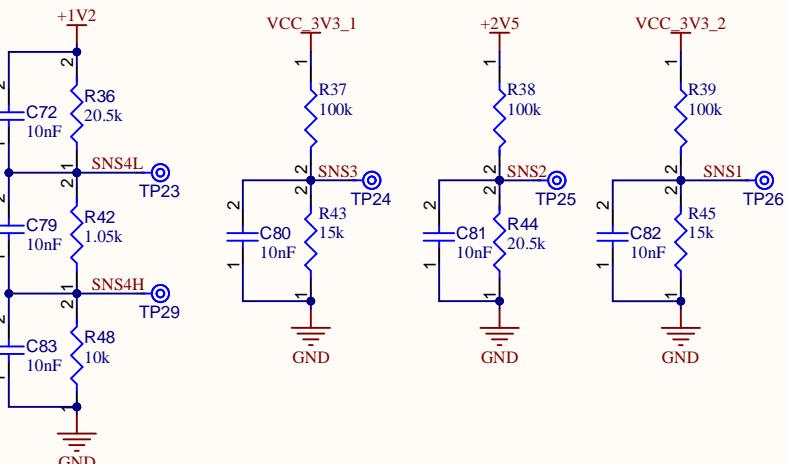
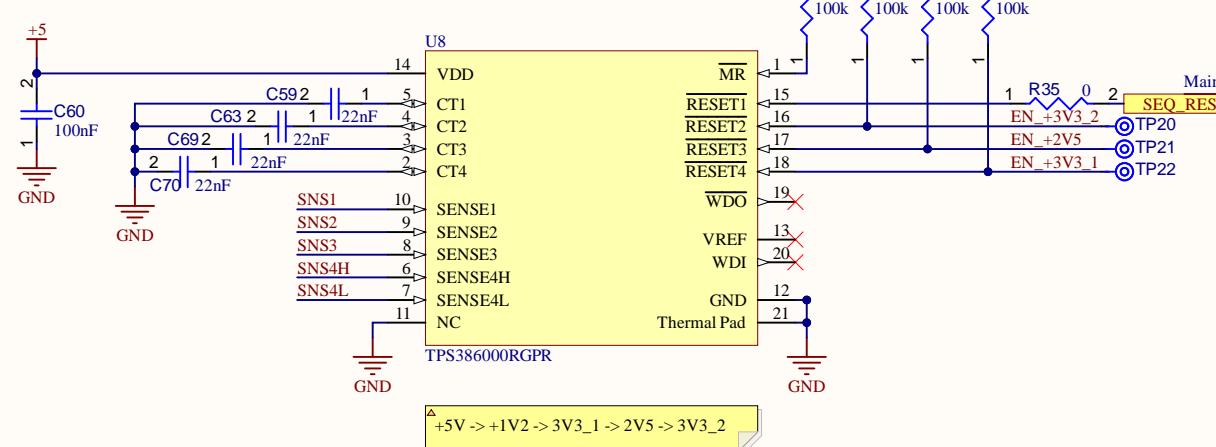


Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
V_{CC}	Core Supply Voltage	1.14	1.26	V	
V_{PP_2V5}	V _{PP_2V5} NVCM Programming and Operating Supply Voltage	1.71 ⁴	3.46	V	
	Slave SPI Configuration	1.71 ⁴	3.46	V	
	Master SPI Configuration	2.30	3.46	V	
	Configuration from NVCM	2.30	3.46	V	
	NVCM Programming	2.30	3.00	V	
V_{CCIO} ^{1,2,3}	I/O Driver Supply Voltage	V_{CCIO_0} , V_{CCIO_1} , V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V	
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C	
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C	
t_{PROG}	Junction Temperature NVCM Programming	10.00	30.00	°C	

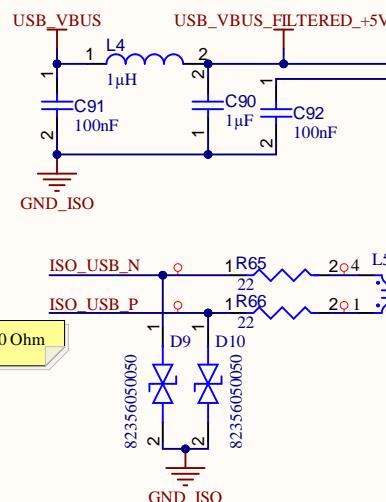
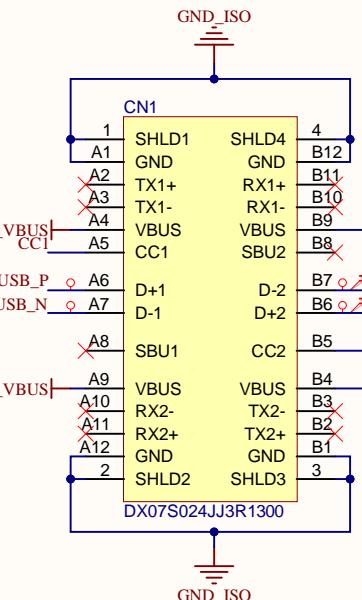
Notes:

- Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
- See recommended voltages by I/O standard in subsequent table.
- V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
- V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.



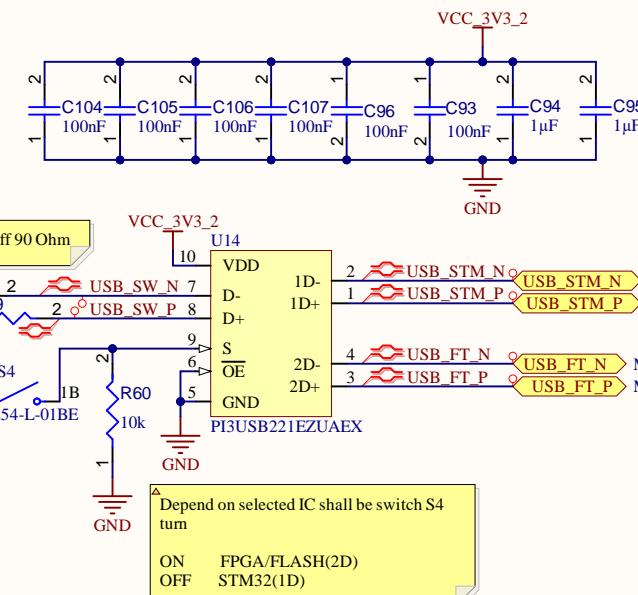
USB

USB-C CONNECTOR



$$P = V_{bus} \cdot I_{bus} = 3.3V \cdot 15.3mA = 50mW$$

ISOLATED USB REPEATER



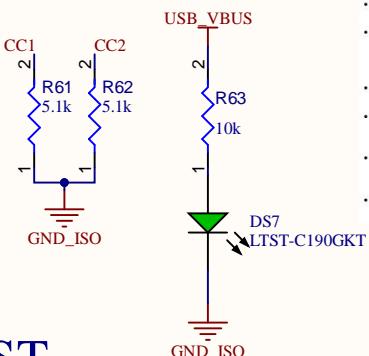
Depend on selected IC shall be switch S4 turn
ON FPGA/FLASH(2D)
OFF STM32(1D)

11 Layout

11.1 Layout Guidelines

Two layers are sufficient to accomplish a low EMI PCB design.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90Ω differential impedance and as close to 45Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2 .
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- ESD structures must be placed on the top layer, close to the connector, and right on the D+/D- traces without vias. Good routing for the ESD structures must be made in the top layer if possible, else must have a strong connection to the ground plane with multiple vias.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.



HOST

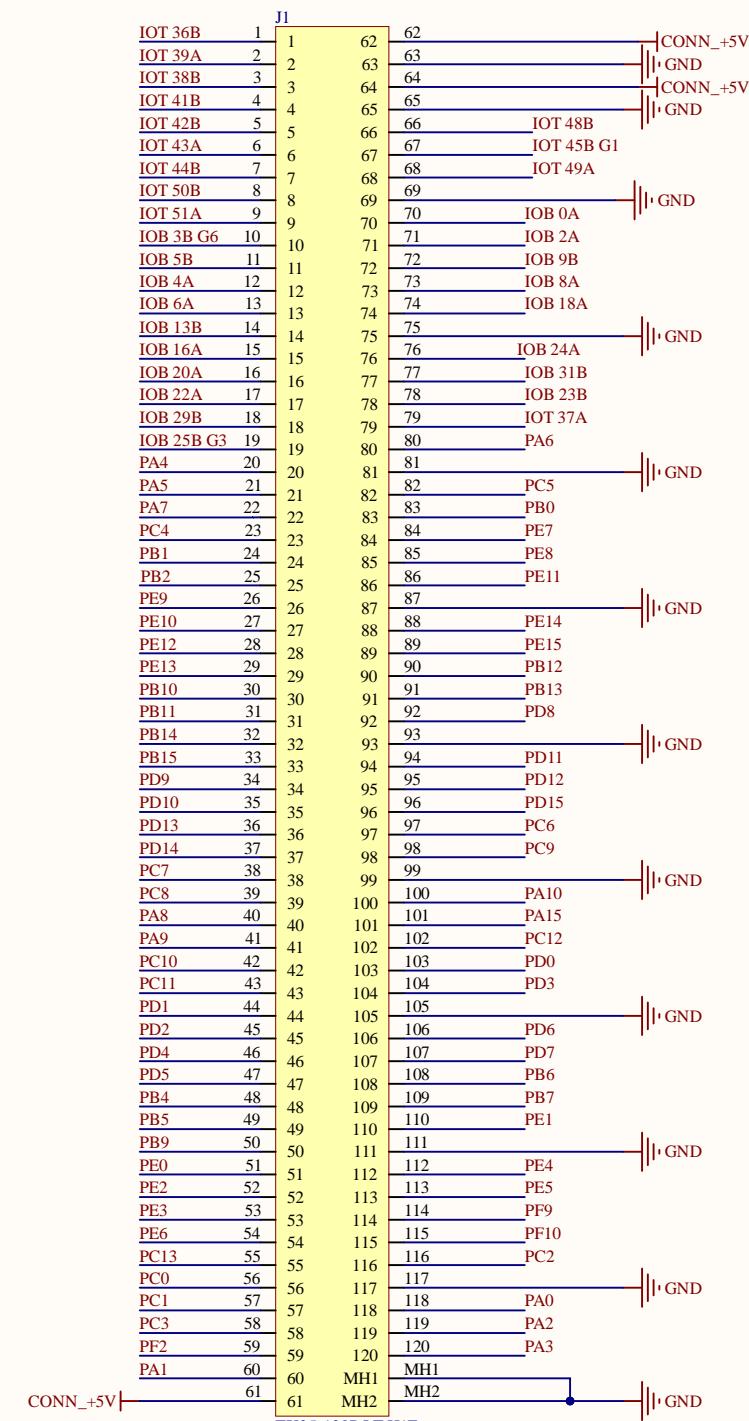
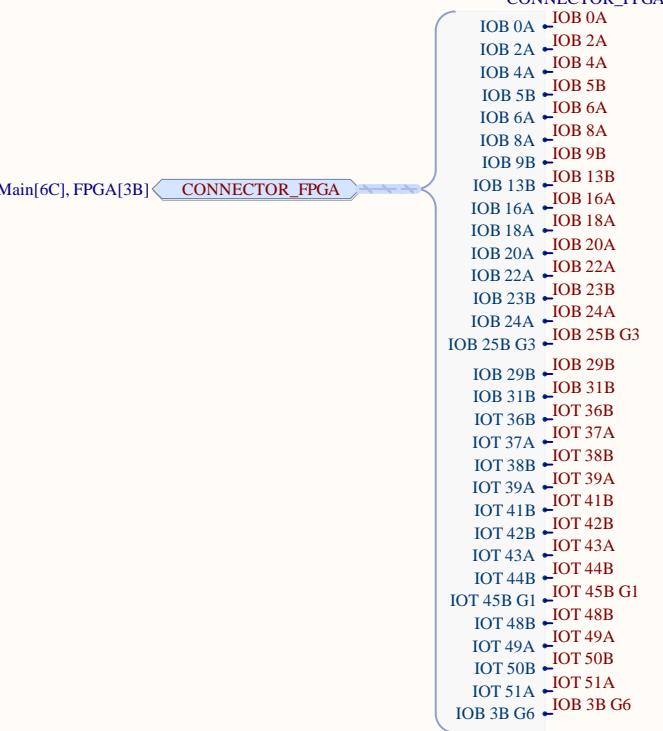
PARAMETER	TEST CONDITIONS	SPECIFICATIONS	DWG-16	DWG-16	UNIT
IEC 60664-1					
CLR External clearance ^[1]	Side 1 to side 2 distance through air	> 8 mm			mm
CPI External Creepage ^[1]	Side 1 to side 2 distance across package surface	> 8 mm			mm
DTI Dielectric strength of the insulation	Minimum insulation resistance (internal clearance)	> 21 < 21 μm			μm
CTI Comparative tracking index	IEC 60112, UL 746A	> 600 > 600 V			V
Material Group	According to IEC 60066-4	I	I	I	
Overvoltage category	Rated mains voltage < 600 V _{max}	I-IV	I-IV	I-IV	
	Rated mains voltage > 600 V _{max}	I-III	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-11) ^[2]					
V _{core}	Maximum repetitive peak test voltage	2121 2121 V _{rep}			
V _{core}	AC voltage (sine wave); time-dependent dielectric breakdown (TDB) test;	1500 1500 V _{rep}			
V _{core}	DC voltage (sine wave)	2121 2121 V _{dc}			
V _{core}	Maximum transient isolation voltage	$V_{core} = V_{core_t} + 0.5 \times (qualification); V_{core_t} = 1.2 \times V_{core}$, $t = 1 \times 100\mu\text{s}$	7071 7071 V _{rep}		
V _{imp}	Maximum impulse voltage ^[3]	Tested in air, 1.250-ns wavelength per IEC 62305	8000 8000 V _{rep}		
V _{imp}	Maximum surge isolation voltage ^[4]	Tested in air (qualification test), 1.250-μs waveform per IEC 62305	12800 12800 V _{rep}		
	Method 2: After 100% safety test subgroup 2, $V_{core} = V_{core_t} + 60\text{ }\mu\text{s}; V_{core_t} = 1.2 \times V_{core_t_0} + 10\text{ }\mu\text{s}$	≤ 5	≤ 5	≤ 5	
	Method 3: After 100% safety test subgroup 1, $V_{core} = V_{core_t} + 60\text{ }\mu\text{s}; V_{core_t} = 1.2 \times V_{core_t_0} + 10\text{ }\mu\text{s}$	≤ 5	≤ 5	≤ 5	
R _{d1}	Apparent charge ^[5]	Method 1: After 100% safety test subgroup 1, $V_{core} = V_{core_t} + 60\text{ }\mu\text{s}; V_{core_t} = 1.2 \times V_{core_t_0} + 10\text{ }\mu\text{s}$	≤ 5	≤ 5	pC
C _{di}	Barrier capacitance, input to output ^[6]	$V_{core} = 0.4 \times \sin(2\pi f t); f = 1 \text{ MHz}$	0.8 0.7 pF		
R _{d2}		$V_{core} = 500 \text{ V}, T_a = 25^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$	
	Insulation resistance, input to output ^[7]	$V_{core} = 500 \text{ V}, T_a = 100^\circ\text{C} \pm 10^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$	W
		$V_{core} = 500 \text{ V} \text{ at } T_a = 150^\circ\text{C}$	$> 10^9$	$> 10^9$	
	Pollution degree		2 2	2 2	
	Climatic category		40/125/21 40/125/21	40/125/21 40/125/21	
UL 1577	V _{test}	$V_{test} = V_{core} + 10\text{ }\mu\text{s} \text{ (qualification); } V_{test} = 1.2 \times V_{core}$, $t = 1 \times 100\mu\text{s}$	5000 5000 V _{rep}		
	V _{test}	$V_{test} = V_{core} + 10\text{ }\mu\text{s} \text{ (100\% production); } V_{test} = 1.2 \times V_{core}$, $t = 1 \times 100\mu\text{s}$	5000 5000 V _{rep}		

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Page Contents:	USB.SchDoc	Checked by:
Size:	-	DWG NO:
Date:	06.09.2024	Design by: *
		Sheet 7 of 9



CONNECTOR

A

**CONNECTOR_STM32**

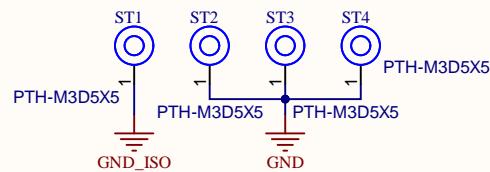
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|------|------|
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| PE1 | PE1 |
| PE2 | PE2 |
| PE3 | PE3 |
| PE4 | PE4 |
| PE5 | PE5 |
| PE6 | PE6 |
| PE7 | PE7 |
| PE8 | PE8 |
| PE9 | PE9 |
| PE10 | PE10 |
| PE11 | PE11 |
| PE12 | PE12 |
| PE13 | PE13 |
| PE14 | PE14 |
| PE15 | PE15 |
| PF2 | PF2 |
| PF9 | PF9 |
| PF10 | PF10 |
| PD0 | PD0 |
| PD1 | PD1 |
| PD2 | PD2 |
| PD3 | PD3 |
| PD4 | PD4 |
| PD5 | PD5 |
| PD6 | PD6 |
| PD7 | PD7 |
| PD8 | PD8 |
| PD9 | PD9 |
| PD10 | PD10 |
| PD11 | PD11 |
| PD12 | PD12 |
| PD13 | PD13 |
| PD14 | PD14 |
| PD15 | PD15 |
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| PB1 | PB1 |
| PB2 | PB2 |
| PB4 | PB4 |
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| PB13 | PB13 |
| PB14 | PB14 |
| PB15 | PB15 |
| PC0 | PC0 |
| PC1 | PC1 |
| PC2 | PC2 |
| PC3 | PC3 |
| PC4 | PC4 |
| PC5 | PC5 |
| PC6 | PC6 |
| PC7 | PC7 |
| PC8 | PC8 |
| PC9 | PC9 |
| PC10 | PC10 |
| PC11 | PC11 |
| PC12 | PC12 |
| PC13 | PC13 |
| PA0 | PA0 |
| PA1 | PA1 |
| PA2 | PA2 |
| PA3 | PA3 |
| PA4 | PA4 |
| PA5 | PA5 |
| PA6 | PA6 |
| PA7 | PA7 |
| PA8 | PA8 |
| PA9 | PA9 |
| PA10 | PA10 |
| PA15 | PA15 |

Main[6C], MCU[7B] CONNECTOR_STM32

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Page Contents:	Connector.SchDoc	
Size:	DWG NO: -	Revision: -
Date:	06.09.2024	Design by: *
		Sheet 8 of 9

Mechanicals

Mouting Holes

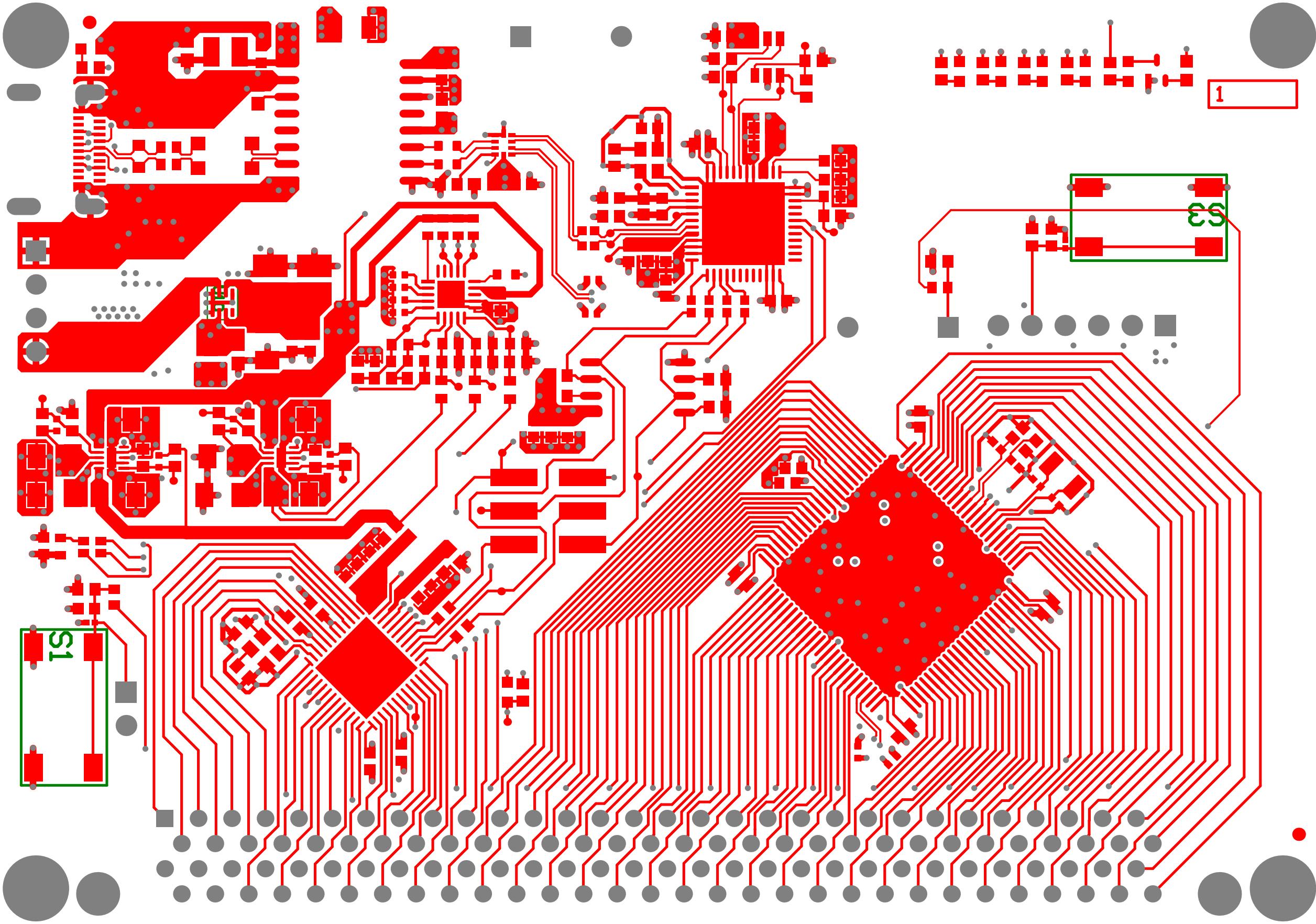


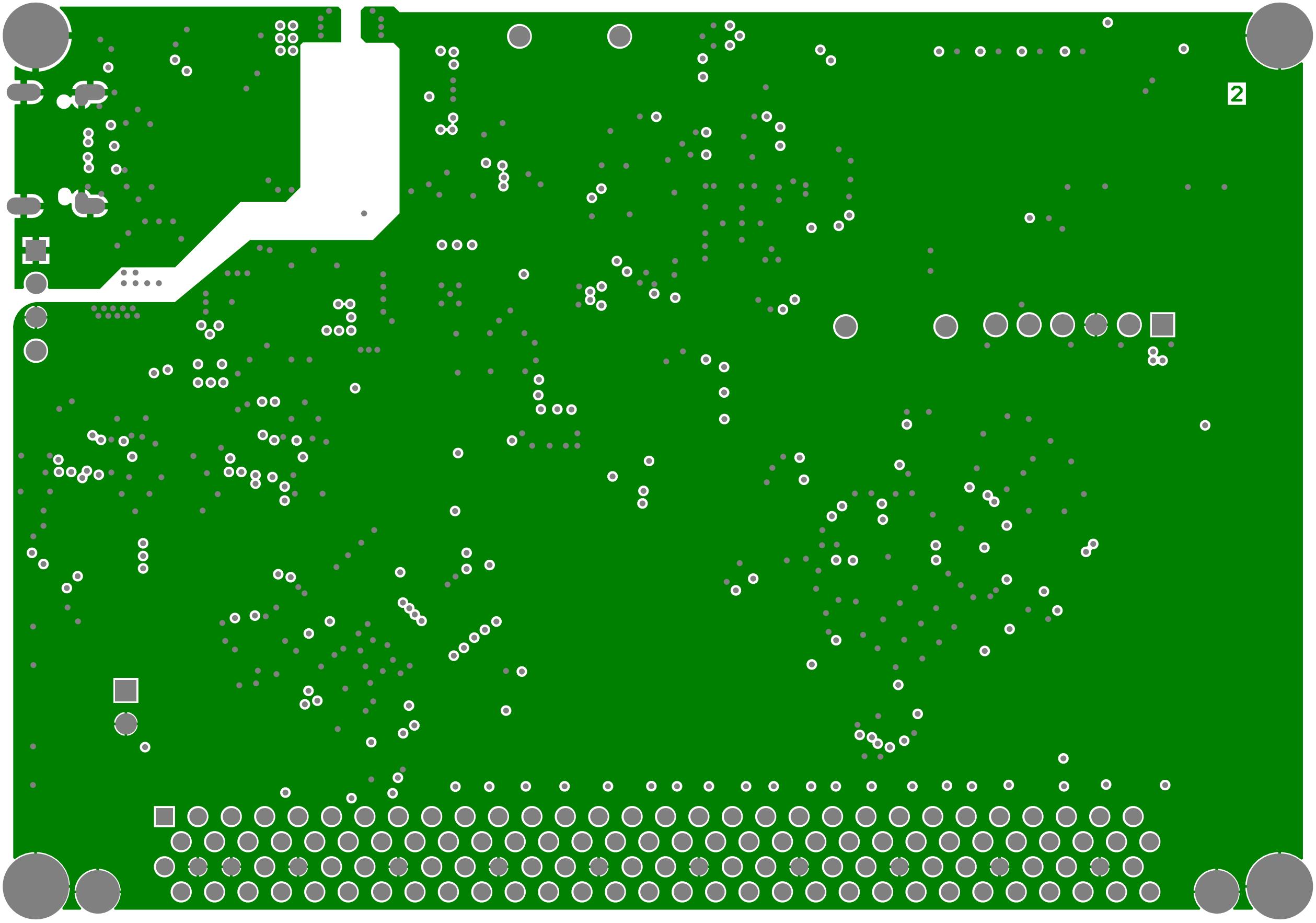
Fiducials



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Size:	DWG NO:	Revision:
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Date: 06.09.2024	Design by: *	Sheet 9 of 9

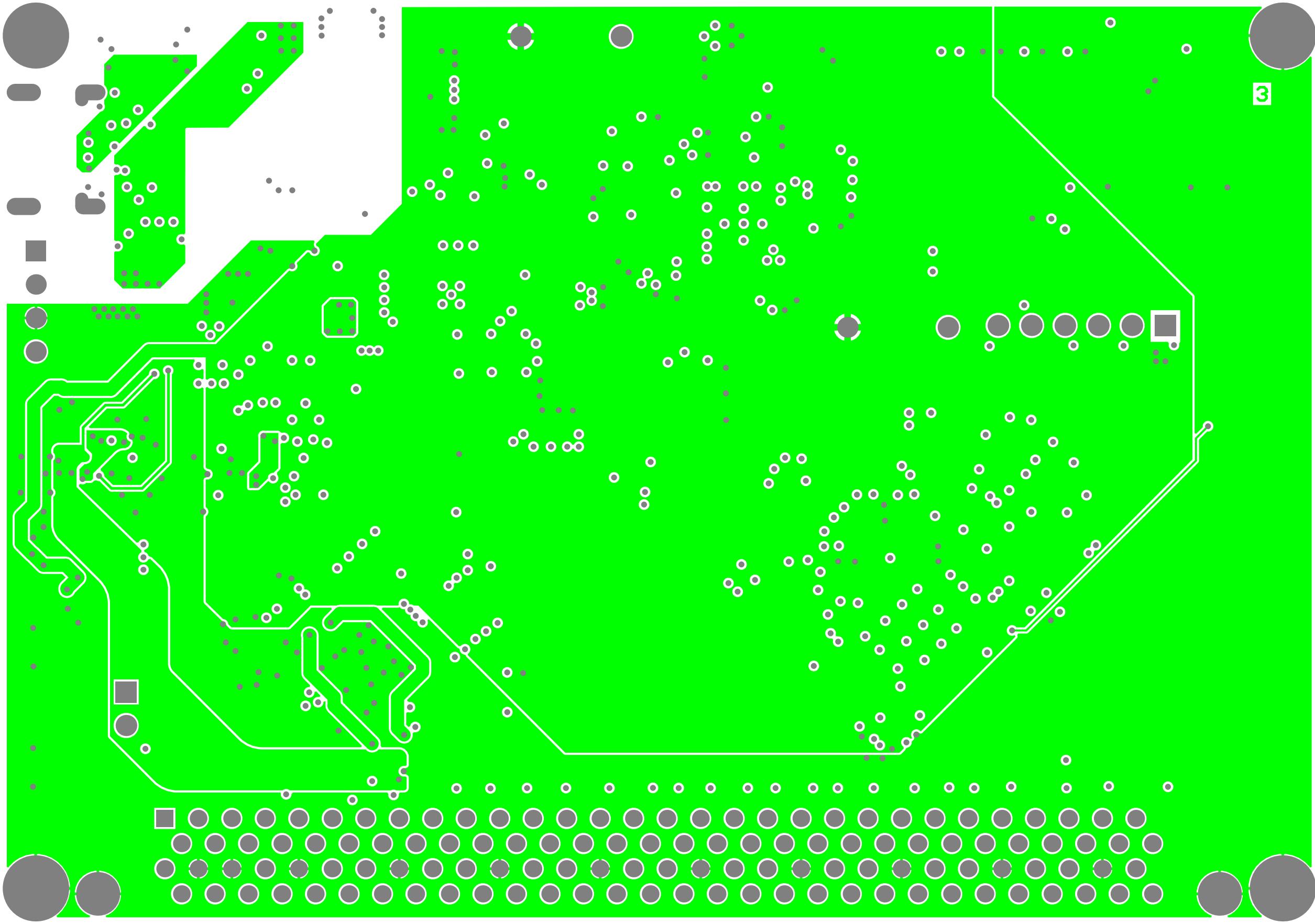




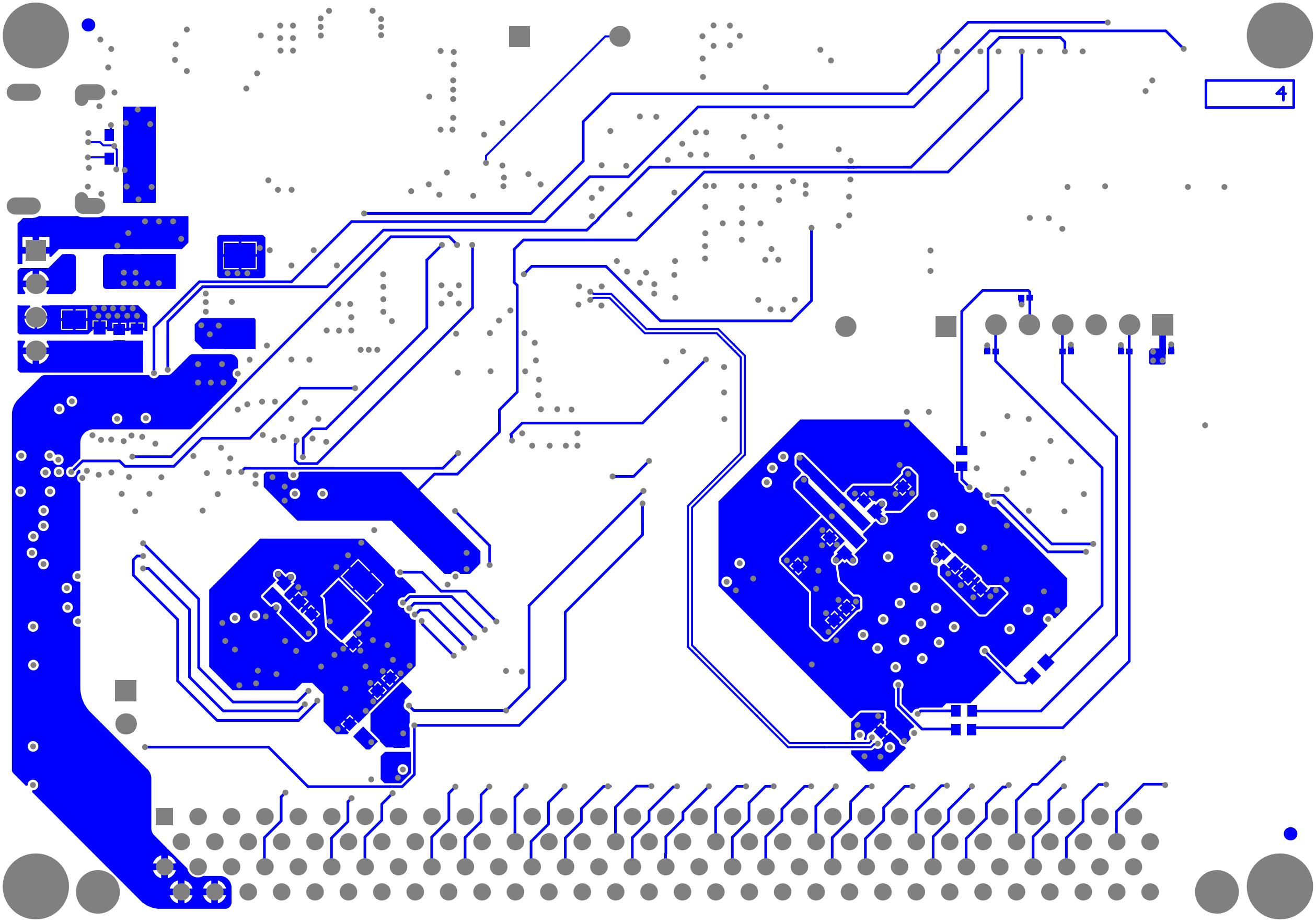


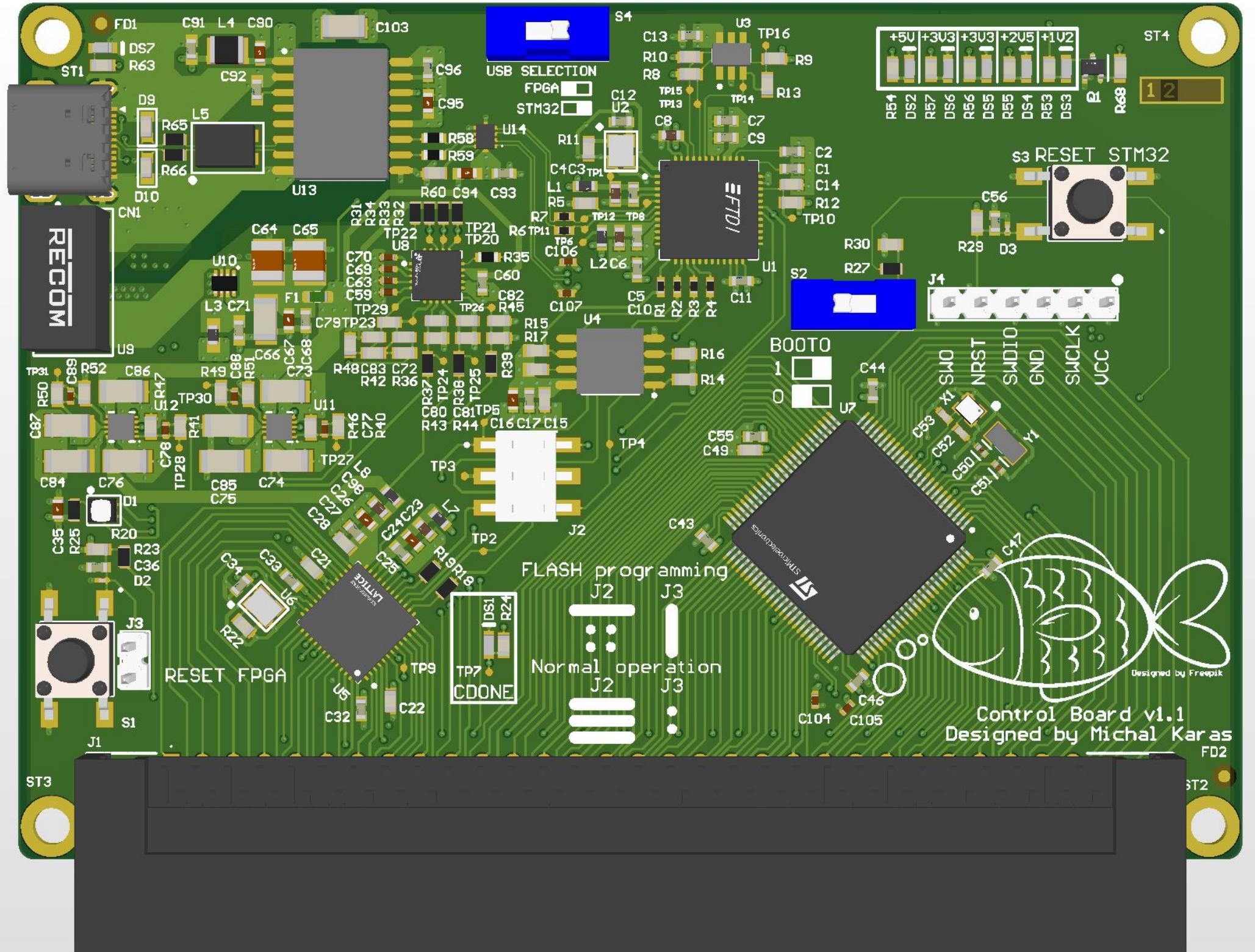
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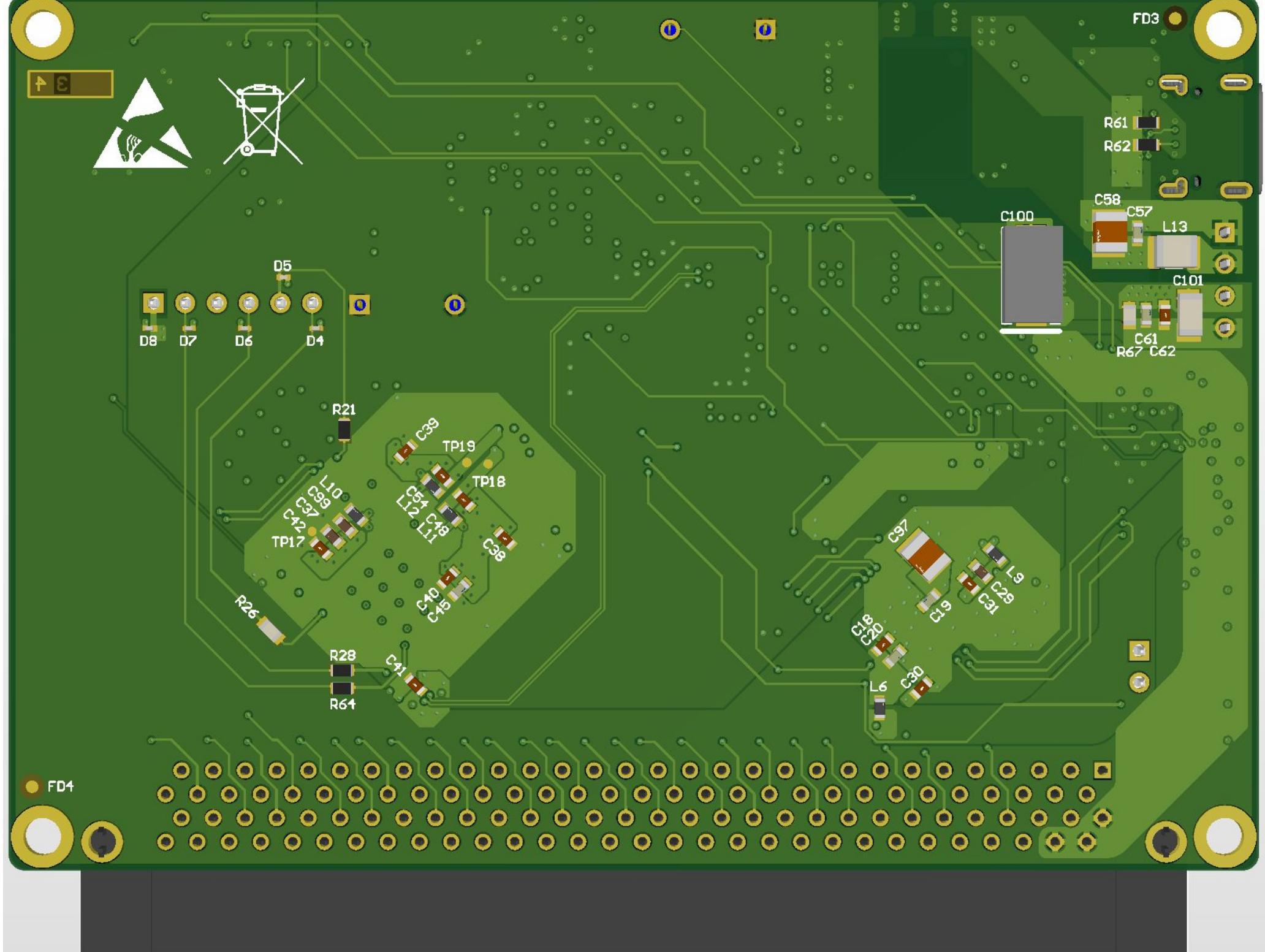
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4







Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0.013mm	3.8
4		Top Layer	Copper	0.035mm	
5		Dielectric 1	2313	0.210mm	4.4
6		Mid Layer 1	Copper	0.015mm	
7		Core	FR-4	1.065mm	4.6
8		Mid Layer 2	Copper	0.015mm	
9		Dielectric 2	2313	0.210mm	4.4
10		Bottom Layer	Copper	0.035mm	
11		Bottom Solder	Solder Resist	0.013mm	3.8
12		Bottom Overlay			
13		Bottom Paste			
Height : 1.612mm					