A Temperature-Insensitive Period-Modulation CDC with DLL-Based Comparator Delay Compensation Achieving 53.5ppm/°C without Calibration

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Abstract

This paper presents a temperature-insensitive period-modulation (PM) capacitance-to-digital converter (CDC) with a delay-locked-loop (DLL) based compensation alleviating temperature-dependent comparator delays. Moreover, a half-period alternate-sampling technique is proposed to track the comparator offset and mitigate its variation in a swing-boosted front-end. Our 180nm CMOS prototype achieves 53.5ppm/°C output variation over –40 to 85°C without any calibration or external clock. The conversion achieves the best FoM_w of 6.0pJ/conv.·step among temperature-insensitive PM CDCs.

Introduction

Capacitive sensors are widely used in the measurement of diverse physical quantities for low-cost IoT systems [1-5]. To support a broad range of applications, temperature-insensitive CDCs with a wide input range are in great demand. Among prior CDCs (Fig. 1 (top)), a time-locked delta-sigma (TL-ΔΣ) structure [2] provides excellent temperature robustness, but its input range is limited to a few-pF range only. Moreover, it requires a bulky crystal oscillator for its operation. Another CDC utilizing period modulation (PM) allows both standalone implementation and a wide input range thanks to on-chip time-domain operation. However, its temperature coefficient (TC) is typically poor due to the comparator's delay (τ_{comp}). Several techniques have been proposed to mitigate the temperature dependency of τ_{comp}. However, compensation techniques that control the biasing current [6] or the comparator threshold [7] require additional comparators, which inevitably decrease energy efficiency. The designs reported in [8,9] achieve low TC with only one comparator, but their relaxation oscillating scheme exhibits worse noise performance compared to swing-boosted (SB) oscillators.

To mitigate all these issues, we propose an SB-oscillator-based PM CDC, which utilizes a DLL structure to compensate for the comparator delay over temperature (Fig. 1 (bottom)). Moreover, the same SB oscillators with the DLL-based compensation are used in the sensor and reference oscillators to ensure that the ratio of their periods matches the ratio of the sensing capacitance C_S and reference capacitance C_R. The PLL is employed for the conversion process, as described in [5]. Thanks to all these, this work achieves a superior TC (53.5ppm/°C) and a wide input range (0.82nF) without an external clock, thus being suitable for cost-effective IoT systems.

Proposed PM CDC with DLL-Based Compensation

Fig. 2 (top) shows the conventional swing-boosted (SB) oscillator and its limitations. The oscillator's period is determined not only by the capacitance values but also by the delay of the comparator (τ_{comp}). Simulation results for τ_{comp} obtained under varying temperature and input capacitance are plotted in Fig. 2 (top-right). The results show that the delay drifts significantly over temperature. Moreover, τ_{comp} is also sensitive to the input capacitance, hindering effective τ_{comp} cancellation over temperature. Fig. 2. (bottom) shows the key concept of the proposed DLL-based τ_{comp}-compensation method. In the proposed structure, the resistor of the RC oscillator is split into large R_1 and much smaller R_2. From these, two oscillation signals V_{RRC} and V_{RC} are generated at the leading (Φ_{lead}) and lagging phases (Φ_{lag}), respectively. The feedback loop locks the sum of τ_{comp} and the delay of the voltage-controlled delay line (VCDL) to the time difference (τ_{ref}) between Φ_{lead} and Φ_{lag}, allowing for compensation of input-capacitance-dependent τ_{comp} without much design complexity and compromise in the input range.

Fig. 3 shows the detailed circuit implementation of the oscillator and timing diagram of major signals. Two p-poly resistors are used with a size ratio of 25:2. This configuration allows the V_{RRC} node to charge and discharge slightly earlier than the V_{RC} node (Fig. 3 (bottom)). The sampling phase detector (PD) alternately samples V_P and V_N from the V_{RC} node at each half cycle and compares them. The VCDL delay is adjusted according to this comparison result until V_P and V_N become the same. The crossing of V_{RRC} and V_{ref} generates the leading phase Φ_{comp}, delayed by τ_{comp}. After Φ_{comp} passes through VCDL, generating the phase Φ_{VCDL}, the sampling switch ($\Phi_{P,samp}$ and $\Phi_{N,samp}$ in the discharging and charging phases, respectively) opens, and the Φ_{int} pulse activates the charge pump. The simplified waveforms in Fig. 4. (left) depict this locking concept of the DLL. If the delay is too short, V_P exceeds V_N, increasing VCDL delay by charging C_{int}. If the delay is too long, the circuit operates oppositely.

The remainder of Fig. 4 presents schematics of the sampling PD, charge pump, and comparator. Chopping is performed in front of the input differential pair and at the current mirror stage in the sampling PD to remove the DC offset and flicker noise. The comparator offset is attenuated through SB oscillation [4]. The comparator is implemented as an inverter with no static power consumption. The V_{ref} in Figs. 2 and 3 correspond to the threshold voltage of this inverter-based comparator. The proposed half-period alternate-sampling PD tracks and cancels the comparator threshold variation. Thus, the compensation path inherits the advantages of the SB topology, providing an energy-efficient and temperature-variation-robust conversion mechanism.

Measurement Results

The prototype IC was fabricated in a 180nm CMOS. The IC occupies a core area of 459mm^2 (Fig. 8). Fig. 5. shows the measured D_{out} and absolute resolution of the CDC over the input capacitance. The verified input range is from 2.83pF to 820pF. Fig. 6 presents 5k-point conversion results, including the statistical distribution and transient behavior. At 4.7pF, the measured absolute resolution is 8.26fF_{rms}. Fig. 7 illustrates the temperature-insensitivity of measured D_{out}. The TC of output variation measured across 9 samples is 53.5ppm/°C over a temperature range from –40°C to 85°C, while the variations of the sensor and reference oscillator periods ($T_{S,DLL}$ and $T_{R,DLL}$) are 412.5ppm/°C and 390.4 ppm/°C, respectively. Note that the TC of D_{out} is effectively maintained small without any calibration. As shown in Fig. 8 (bottom), the total power consumption of CDC is 50.5μW, while the PLL and two oscillators consume 29.3μW and 13.0μW, respectively.

Table I compares the performance of the proposed PM CDC with state-of-the-art temperature-insensitive CDCs. The Walden FoM (FoM_w) is 6.0pJ/conv·step at Cs=4.7pF with 19μs conversion time. The best FoM_w is obtained in this work among temperature-insensitive PM CDCs [1,3,4]. Although the design in [2] achieves a better TC, it is not a standalone design, unlike the proposed PM CDC. In conclusion, the CDC presented in this paper utilizes the DLL-based comparator-delay compensation with half-period alternate-sampling. This approach eliminates the temperature-dependent comparator delay while maintaining a wide input range. This temperature-independent and highly linear conversion enables the proposed CDC to be an ideal solution for cost-effective IoT applications without requiring post-processing.

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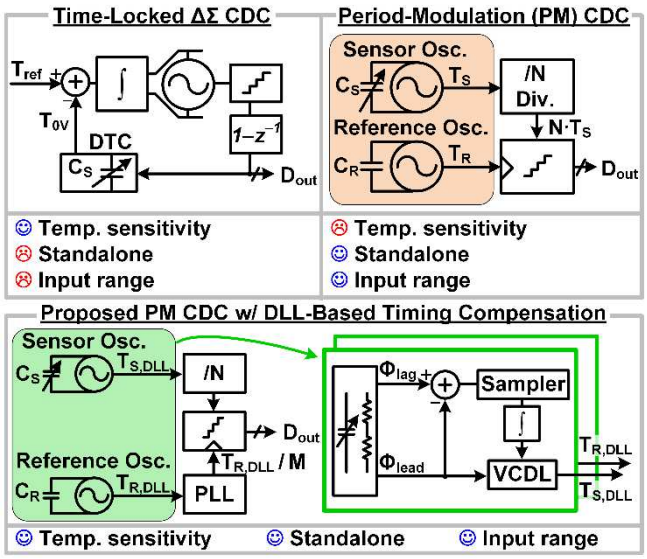

Fig. 1. Comparison between prior temperature-insensitive CDCs (top) and the proposed DLL-based PM CDC (bottom).

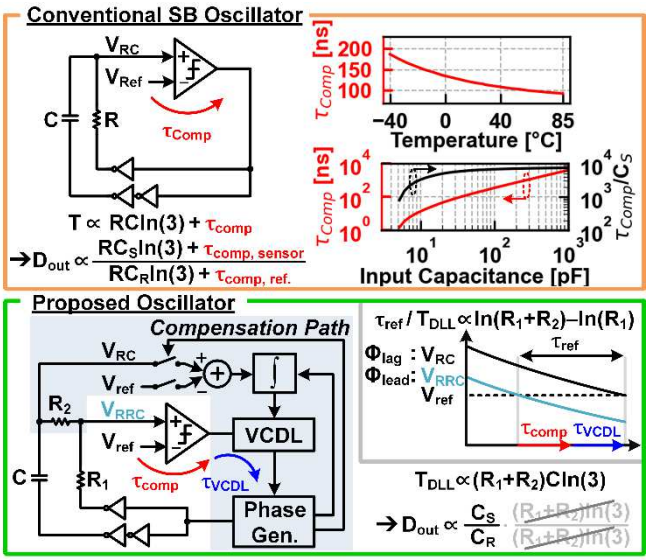

Fig. 2. Conventional SB oscillator and its comparator delay variation due to temperature and sensing capacitance (top); Proposed oscillator with key operation concept (bottom).

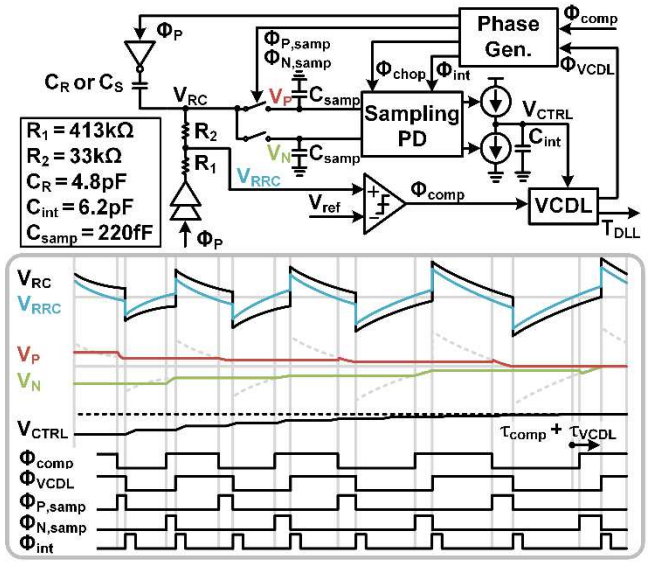

Fig. 3. Block and timing diagrams of the proposed oscillator.

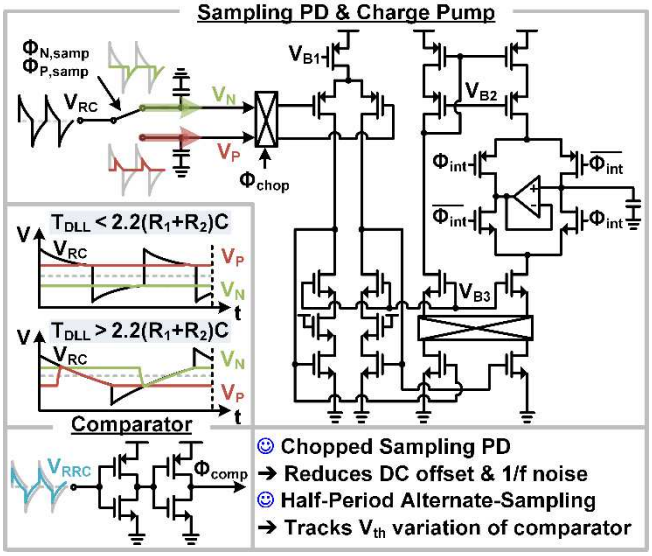

Fig. 4. Schematic of the sampling PD, charge pump, and comparator with simplified waveforms illustrating the DLL's locking operation.

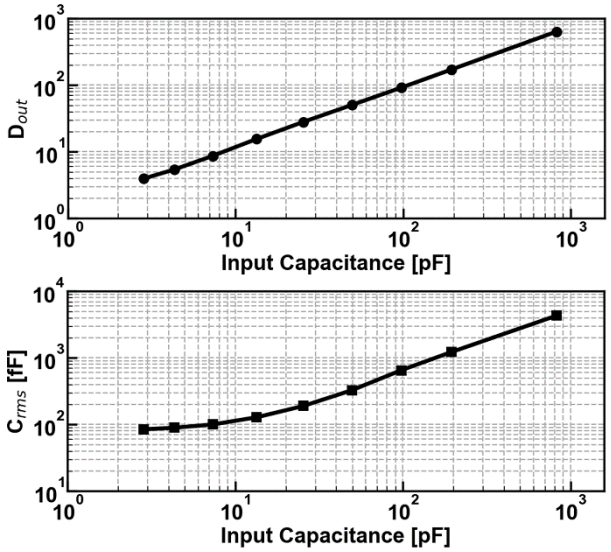

Fig. 5. Measured D_{out} and absolute resolution over input capacitance.

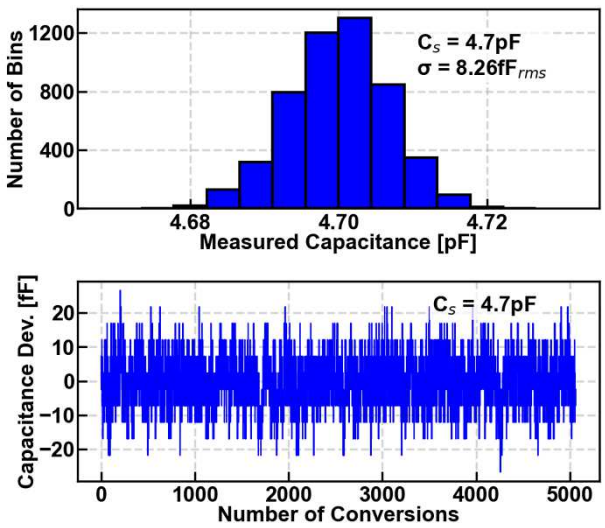

Fig. 6. Conversion results showing the statistical distribution of 5k points and corresponding transient plot.

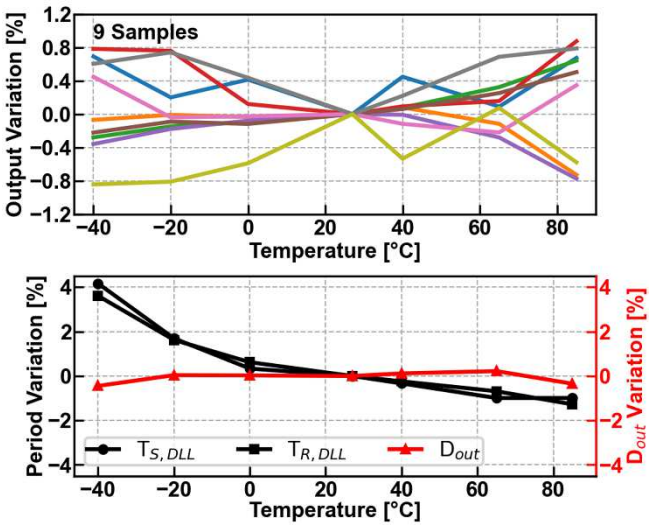

Fig. 7. Measured D_{out} variation over a temperature range of –40°C to 85°C across 9 samples.

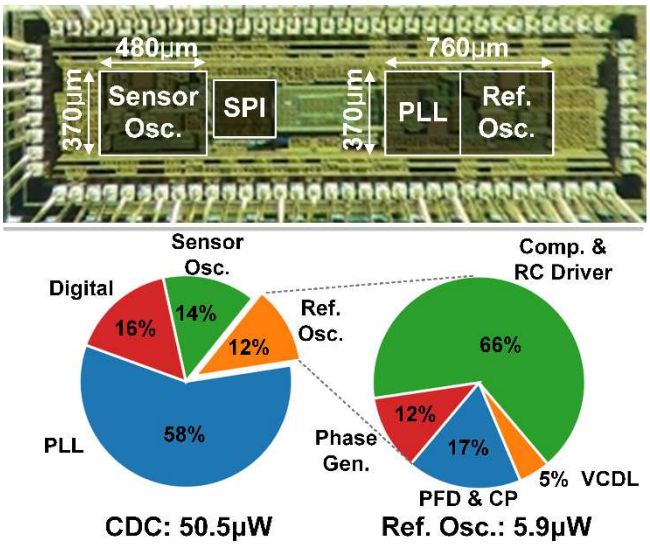

Fig. 8. Die micrograph of the proposed CDC (top); Power breakdown of the whole CDC and the reference oscillator (bottom).

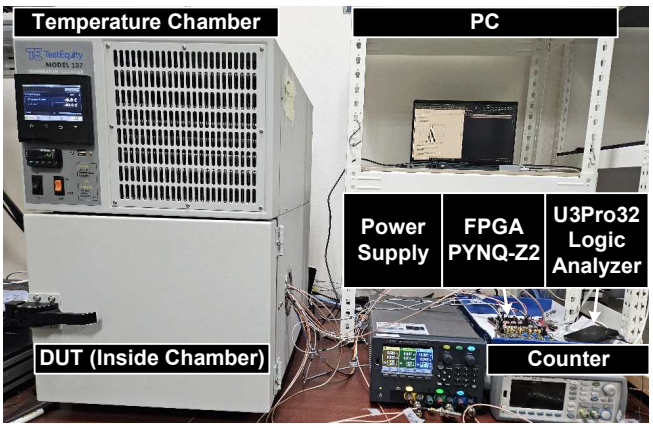

Fig. 9. Measurement setup. DUT is inside the temperature chamber.

TABLE I. Comparison with prior temperature-insensitive CDCs

	ISSCC'21 [1]	VLSI'22 [2]	SENSORS'16 [3]	TCAS-I'22 [4]	This Work
Process [nm]	180	180	180	180	180
Method	Self-cal. PM	TL-ΔΣ	PM	SB-PM	DLL SB-PM
Area [mm^2]	0.2	0.2	0.102	0.175	0.459
V_{DD} [V]	0.3–1.8	1.2–2.2	0.8–1.2	1	1
Power [µW]	0.00137	42.76	23	140	50.5
Measurement Time [ms]	1040	0.05	17.5	2.93	0.019
Resolution [fF$_{rms}$]	67	0.705	2.05	0.218	8.26
ENOB	7.0	14.8	9.4	15.7	7.4
Input Range [pF]	0–30	3.75–122	3.36	46,000	2.83–820*
FoM$_w$ [fJ/c·s]	11,100	74	474,051	7,735	5,998
Temp. Var. [ppm/°C]	250	49.1	153.4	64.2	53.5
TC Calibration	Yes	No	No	No	No
Standalone	Yes	No	Yes	Yes	Yes

* Extendable with larger VCDL delay cell

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