FPGA Implementation of VLC Communication Technology

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***Abstract*—Currently, Visible Light Communication (VLC) technology remains a lagging research in the field of Ultra-Wide Band (UWB), due to the inefficiency of data capture and synchronization period. Accordingly, this paper proposes a fundamental design and implementation of data communication of VLC on the MAC layer based on FPGA. This paper includes basic research context, design and implementation of UWB MAC layer, along with the simulation and verification results of this system.**

Keywords-Visible Light Communication (VLC); Ultra Wideband (UWB); Field-Programmable Gateway Array (FPGA); Verilog Hardware Design Language

I. INTRODUCTION

Visible Light Communication (VLC) technology uses visible light as a carrier to implement data transmission [2,5,6,7]. Compared to traditional wireless communication, VLC has much broader spectrum, which could provide higher transmission rate and less error rate, with less power emission by using LED as a producer. To implement the VLC technology, the entire design is based on the architecture of OSI (Open System Interconnection) model of VLC shown in Figure 1. Accordingly, it is applicable to use VLC technology to realize UWB service as high speed multimedia communication.

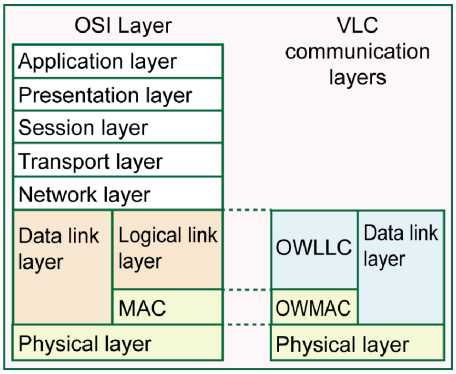

Figure 1. OSI Model of VLC technology

There is a variety of approaches to achieve UWB system in reality with different principles and structures. However, current and existing researches are suitable for traditional wireless communication networks, instead of meeting UWB network for efficiency of MAC mechanism with coordination of multiple users sharing a common channel.

This paper illustrates a VLC implementation of by using FPGA and UWB technology, especially the communication between MAC and PHY layer. Finite State Machine (FSM) of MAC layer and other hardware design based on FPGA is presented, along with system implementation and simulation results on DE1 development board. Section 2 presents the design of a UWB MAC layer controller with specific interfaces based on FPGA. Section 3 shows the simulation and verification results of this system. Conclusions are made in Section 4.

II. DESIGN OF UWB MAC CONTROLLER

This section will discuss about the design of UWB MAC Controller in details. Fundamentally, the system contains several integrated components in order to implement functionality of MAC controller. The architecture of the system based on FPGA chip is given in Figure 2.

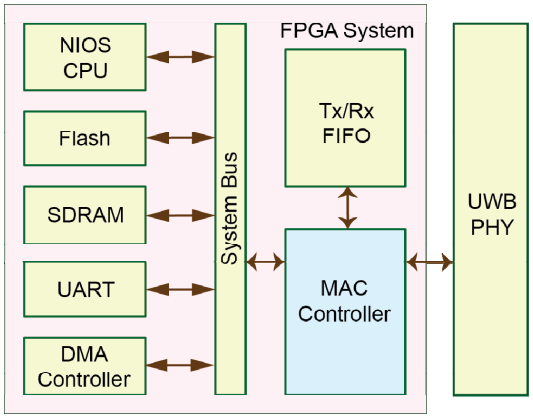

Figure 2. Architecture of a MAC Controller System

In this paper, we mainly focus on the design of MAC controller. The design of other parts of IP cores is available in [4]. Figure 3 illustrates the block diagram of MAC controller in highlight.

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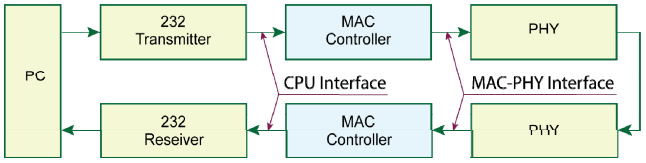

Figure 3. Framework of MAC Controller System

In this framework, in order to transmit data, PC issues instructions to send data packets from RS-232 transmitter to MAC controller and pass the data further to PHY layer through specific MAC-PHY interface; and receiving data is vice versa. To simplify the verification of system design, two MAC controllers are implemented for, transmitter and receiver respectively, which is easy to realize on an FPGA board. Below is the design details of each interface.

A. RS-232 Interface

RS-232 is a serial data transmission standard. It formally defines the signal connection between data terminal equipment such as a computer terminal or data circuit-terminating device like a modem. In this system, RS-232 is used for computer serial functions of MAC controller in order to realize communication between PC and demonstration board. The RS-232 interface is shown in Figure 4.

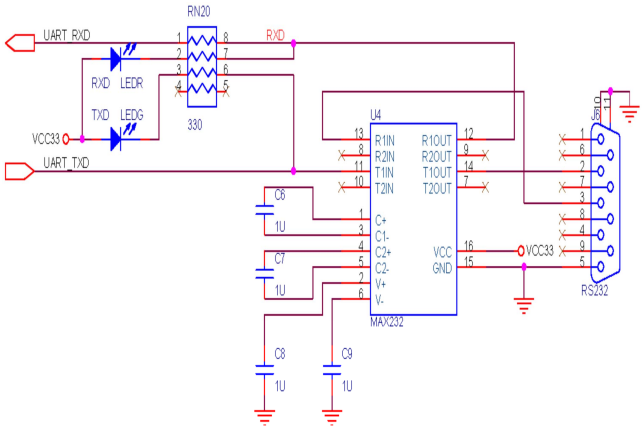

Figure 4. RS-232 Interface

Based on RS-232 interface, Universal Asynchronous Receiver/Transmitter (UART) mechanism is established in this prototype system as a data transmission protocol, which follows a frame format as illustrated in Table I.

TABLE I. UART FRAME FORMAT

Starting Bit	Data Bits	Even Parity Bit	Stop Bit
Logic "0"	8 bits	1 bits	Logic "1"

Furthermore, since there is no synchronous clock for UART to ensure correct data transmission, it is necessary to define a consistent clock, namely "baud rate", for both side of transmitter and receiver. Baud rate is defined according to the following considerations: the cable length and characteristics, and system environment among other factors. This system adopts the data package structure as shown in Figure 5.

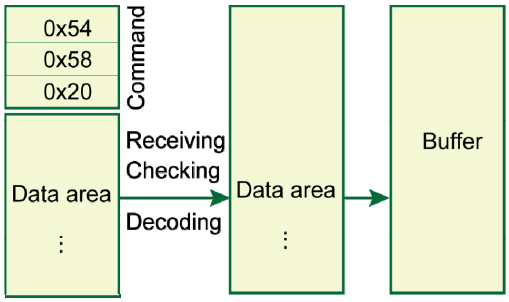

Figure 5. Data Packet Example

RS-232 transmitter receives the PC serial port data packets and completes transform from serial to parallel. If the instruction is decoded as a data transfer instruction, the data will be put into the MAC controller via the CPU interface. The whole process is summarized as a FSM in Figure 6.

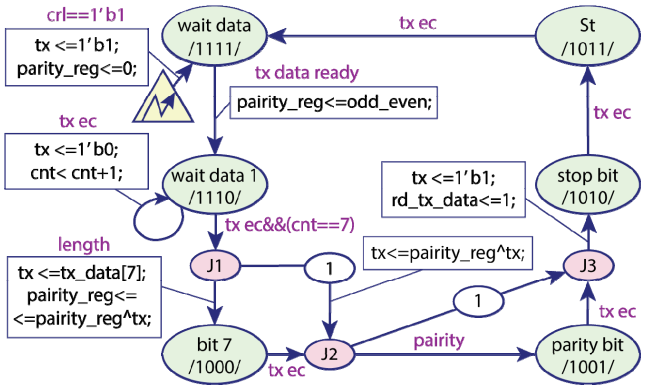

Figure 6. RS-232 Transmitter Described as FSM

Alternatively, RS-232 receiver receives data from MAC Controller through CPU interface and generates packages in the defined format. Then it conducts transforms form parallel to serial and display in the PC serial port interface. Figure 7 is the FSM for this RS-232 receiver.

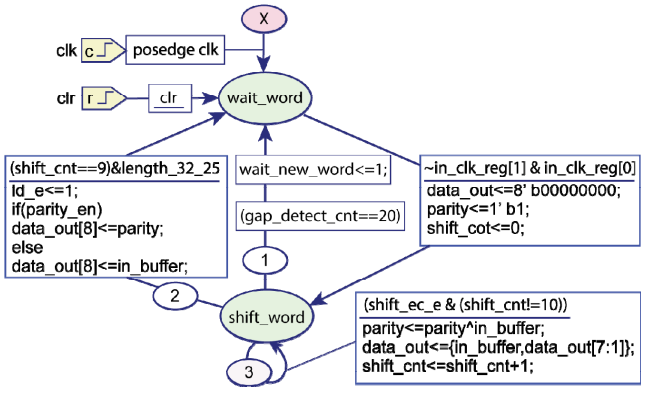

Figure 7. RS-232 Receiver Described as FSM

B. CPU Interface

As shown in Figure 8, the CPU interface is asynchronous and it implements the parallel signals inside the FPGA and RS-232 serial signal conversion, with 8 address lines, 16 data lines, and chip-select lines, as well as read and write control lines.

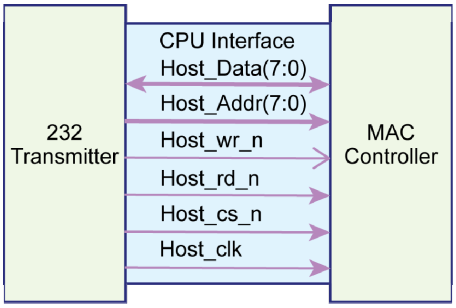

Figure 8. CPU Interface

Detailed parameters used in the CPU interface in Figure 8 are listed in Table II.

TABLE II. CPU INTERFACE PARAMETERS

Signal Namet	Description
Host_Data(7:0)	8-bit Data Bus
Host_Addr(7:0)	8-bit address Bus
Host_wr_n	Write Enable. Active-low
Host_rd_n	Read Enable. Active-low
Host_cs_n	Chip select，Active-low
Host_clk	Synchronous clock

C. MAC Controller

In system data workflow, MAC controller receives data form CPU and packs it to send via PHY interface with a specified frame format when sending data. In contrast, MAC controller decodes data packs from PHY interface and stores valid data into specified buffer for host to read when receiving external data. Figure 9 shows the UWB frame structure of MAC interface mentioned above.

SOF	Source Address	Destination Address	Payload	Frame Check

Figure 9. UWB frame structure

To be specific, Figure 10 shows MAC controller in a detailed function block diagram.

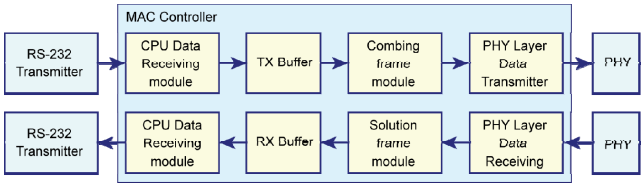

Figure 10. MAC controller framework

D. MAC-PHY Interface

We use common PHY interface for this system and the functionality of PHY interface is simulated in MAC-PHY interface

FIFO (First In, First Out) control module is introduced to handle with data cache between MAC and PHY layer. FIFO is operated through the controller to maintain internal read and write operation. In this system, the block diagram of FIFO design is shown in Figure 11.

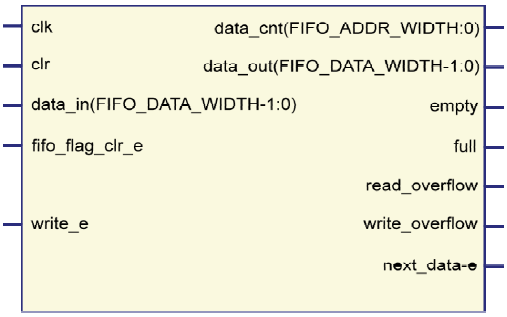

Figure 11. FIFO Block Diagram

In details, Table III below shows the pin parameters of the FIFO module.

TABLE III. FIFO PIN PARAMETERS

Signal names	Direction	Description
Data_in(7:0)	In	Write FIFO data
Write_e	In	Write FIFO signal, High Valid
Data_out(7:0)	Out	Read FIFO data
Data_cnt(7:0)	Out	The current number of data in FIFO
empty	Out	FIFO Empty, High Valid
full	Out	FIFO Full, High Valid
Read_overflow	Out	FIFO Read Overflow, High Valid
Write_overflow	Out	FIFO Write Overflow, High Valid
Next_data_e	In	Read FIFO signal, High Valid

III. SIMULATION AND VERIFICATION

This main purpose of this section is to present simulation and verification results of the system designed in prior sections. The whole system is implemented on the FPGA board. Simulation is carried out with SE ModelSim.

A. Simulation Setup

The entire design is implemented on Altera DE1 development board featuring Cyclone® II 2C20 FPGA in a 484-pin package as shown in Figure 12.

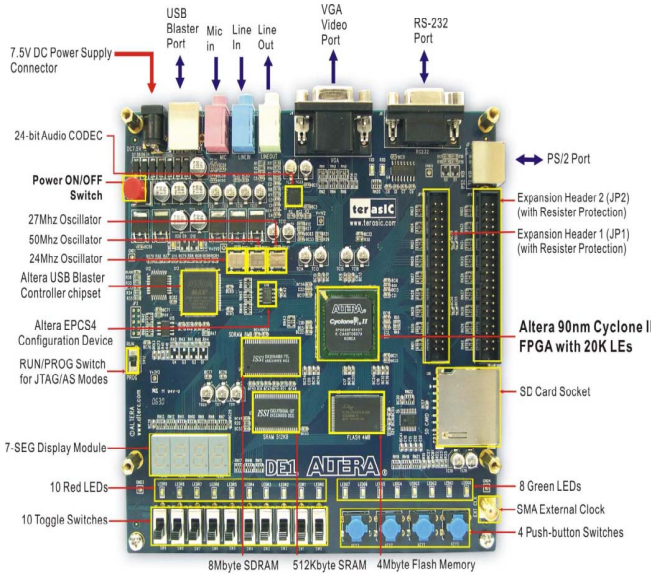

Figure 12. DE1 Development Board

B. *Simulation Test*

System test is carried out by using SE ModelSim, which is a multi-language HDL simulation environment by Mentor Graphics for independent simulation of hardware description languages with graphical user interface [1][2][3]. Figure 13 shows the test diagram of the system.

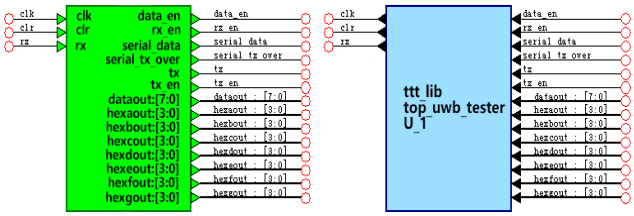

Figure 13. Simulation Test Diagram

C. *System Verification*

System implemented contains two MAC controllers aiming for transmitter and receiver. To evaluate the accuracy of system design in last section, verification is carried out and the outcomes are shown below.

1) Processor and Interface Waveform

Operation of processor interface is divided into read and write operations, with synchronous interface timing. Detailed read and write operating waveforms are shown in Figure 14 and Figure 15. FIFO waveform of MAC-PHY interface in single frame transmission is shown in Figure 16.

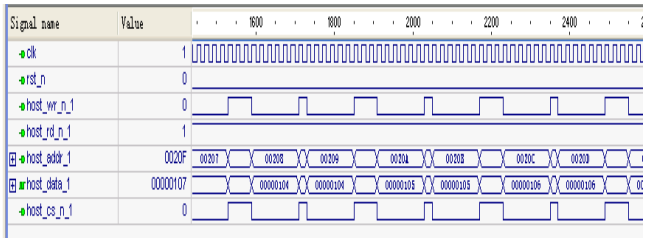

Figure 14. CPU Write Waveform

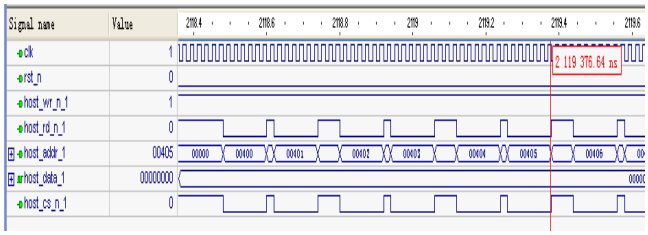

Figure 15. CPU Read Waveform

Figure 16. FIFO Waveform in Single Frame Transmission

2) Board Level Test

With serial debug assistant, test data are set to run 100 times. As a consequence, the system could keep to response for data transfer instructions, retrieve and handle both sending and receiving data, and allow the data being cleared by sending command “CL” to the system.

IV. CONCLUSIONS AND FUTURE WORK

This paper proposes a solution to implement UWB MAC controller based on FPGA and VLC technology. Finite state machine modelling technique has proved to be well suited to describe the behavior of the MAC layer system level. Meanwhile, based on the simulation of programmable logic design tools, signal timing of each module can be verified in advance. UWB is evaluated using different parameter settings on simulation platform. Using asynchronous serial port between PC and embedded platform, the system implements the core MAC controller module, which intercommunicates between CPU and PHY layer, so that users can send and receive commands and data between PC and embedded platform.

In the future, more advanced system implementation will be built to verify all kinds of MAC layer protocols in the field of UWB, so as to achieve a more efficient and reliable transmission.

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