

# GPIO Spec



# **Revision History**

Revision	Date	Author	Description
0.1	March 03, 2021	AWAXXXX	Initial version
0.2	March 12, 2021	AWAXXXX	Update the default value of PC_PULLO.





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# 1 Interfaces

#### 1.1 **GPIO**

#### 1.1.1 Overview

The general purpose input/output (GPIO) is one of the blocks controlling the chip multiplexing pins. The F133 supports 6 groups of GPIO pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

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The Port Controller has the following features:

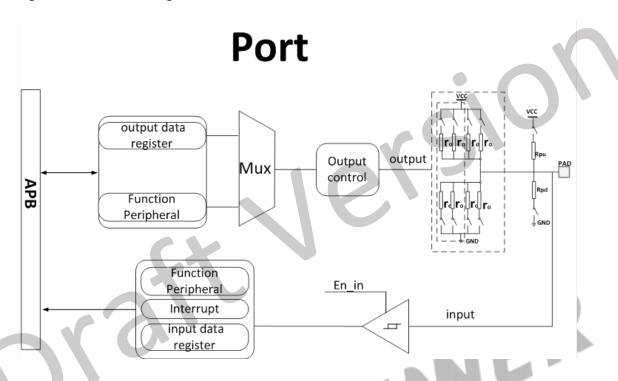
- 6 groups of ports (PB, PC, PD, PE, PF, PG)
- Software control for each signal pin
- Data input (capture)/output (drive)
- Each GPIO peripheral can produce an interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 72 interrupts
- Configurable interrupt edges

#### 1.1.2 Block Diagram

The following figure shows the block diagram of the GPIO.



Figure 1-1 GPIO Block Diagram



The GPIO consists of the digital part (GPIO, external interface) and IO analog part (output buffer, dual pull down, pad). The digital part can select the output interface by the MUX switch; the analog part can configure pull up/down and buffer strength.

When executing GPIO read state, the GPIO reads the current level of the pin into the internal register bus. When not executing GPIO read state, the external pin and the internal register bus are off-status, which is high-impedance.

#### 1.1.3 Functional Descriptions

#### 1.1.3.1 Multi-function Port

The F133 includes 72 multi-functional input/output port pins. There are 6 ports as listed below.

**Table 1-1 Multi-function Port** 

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
РВ	6	Schmitt	CMOS	LCD/I2S/TWI/PWM/IR/UART/PB-EINT	3.3 V
PC	6	Schmitt	CMOS	SPI/SMHC/UART/BOOT/TWI/TCON/ PC-EINT	3.3 V/ 1.8 V
PD	23	Schmitt	CMOS	LCD/LVDS/OWA/TWI/IR/DSI/SPI-DBI/ DMIC/UART/PWM/IR/PD-EINT	3.3 V/ 1.8 V



Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PE	14	Schmitt	CMOS	NCSI/TWI/UART/PWM/LCD/OWA/LEDC/IR /JTAG/EMAC/PE-EINT	3.3 V/ 2.8 V/ 1.8V
PF	7	Schmitt	CMOS	SMHC/JTAG/UART/OWA/TWI/IR/I2S/LEDC / PWM/PF-EINT	3.3 V/ 1.8 V
PG	16	Schmitt	CMOS	SMHC/UART/PWM/I2S/TWI/EMAC/OWA/IR/TCON/LEDC/SPI/PG-EINT	3.3 V/ 1.8 V





#### 1.1.3.2 GPIO Multiplex Function

Table 1-2 to Table 1-7 show the multiplex function pins of the F133.



For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

#### **Table 1-2 PB Multiplex Function**

<b>GPIO Port</b>	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PB2	LCD0-D0	I2S2-DOUT2	TWI0-SDA	I2S2-DIN2	LCD0-D18	UART4-TX		PB-EINT2
PB3	LCD0-D1	I2S2-DOUT1	TWI0-SCK	I2S2-DIN0	LCD0-D19	UART4-RX		PB-EINT3
PB4	LCD0-D8	I2S2-DOUT0	TWI1-SCK	I2S2-DIN1	LCD0-D20	UART5-TX		PB-EINT4
PB5	LCD0-D9	I2S2-BCLK	TWI1-SDA	PWM0	LCD0-D21	UART5-RX		PB-EINT5
PB6	LCD0-D16	I2S2-LRCK	TWI3-SCK	PWM1	LCD0-D22	UART3-TX	CPUBIST0	PB-EINT6
PB7	LCD0-D17	I2S2-MCLK	TWI3-SDA	IR-RX	LCD0-D23	UART3-RX	CPUBIST1	PB-EINT7

#### **Table 1-3 PC Multiplex Function**

<b>GPIO Port</b>	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PC2	SPIO-CLK	SDC2-CLK				)		PC-EINT2
PC3	SPIO-CSO	SDC2-CMD						PC-EINT3
PC4	SPI0-MOSI	SDC2-D2	BOOT-SEL0					PC-EINT4
PC5	SPI0-MISO	SDC2-D1	BOOT-SEL1					PC-EINT5
PC6	SPIO-WP	SDC2-D0	UART3-TX	TWI3-SCK	DBG-CLK			PC-EINT6
PC7	SPI0-HOLD	SDC2-D3	UART3-RX	TWI3-SDA	TCON-TRIG			PC-EINT7

# Table 1-4 PD Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PD0	LCD0-D2	LVDS0-V0P	DSI-D0P	TWI0-SCK				PD-EINTO
PD1	LCD0-D3	LVDS0-V0N	DSI-D0N	UART2-TX				PD-EINT1
PD2	LCD0-D4	LVDS0-V1P	DSI-D1P	UART2-RX				PD-EINT2
PD3	LCD0-D5	LVDS0-V1N	DSI-D1N	UART2-RTS				PD-EINT3
PD4	LCD0-D6	LVDS0-V2P	DSI-CKP	UART2-CTS				PD-EINT4
PD5	LCD0-D7	LVDS0-V2N	DSI-CKN	UART5-TX				PD-EINT5
PD6	LCD0-D10	LVDS0-CKP	DSI-D2P	UART5-RX				PD-EINT6
PD7	LCD0-D11	LVDS0-CKN	DSI-D2N	UART4-TX				PD-EINT7
PD8	LCD0-D12	LVDS0-V3P	DSI-D3P	UART4-RX				PD-EINT8
PD9	LCD0-D13	LVDS0-V3N	DSI-D3N	PWM6				PD-EINT9
PD10	LCD0-D14	LVDS1-V0P	SPI1-CS/DBI-CSX	UART3-TX				PD-EINT10
PD11	LCD0-D15	LVDS1-V0N	SPI1-CLK/ DBI-SCLK	UART3-RX				PD-EINT11
PD12	LCD0-D18	LVDS1-V1P	SPI1-MOSI/ DBI-SDO	TWI0-SDA				PD-EINT12



GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PD13	LCD0-D19	LVDS1-V1N	SPI1-MISO/	UART3-RTS				PD-EINT13
			DBI-SDI/DBI-TE/					
			DBI-DCX					
PD14	LCD0-D20	LVDS1-V2P	SPI1-HOLD/	UART3-CTS				PD-EINT14
		DBI-DCX/						
			DBI-WRX					
PD15	LCD0-D21	LVDS1-V2N	SPI1-WP/DBI-TE	IR-RX				PD-EINT15
PD16	LCD0-D22	LVDS1-CKP	DMIC-DATA3	PWM0				PD-EINT16
PD17	LCD0-D23	LVDS1-CKN	DMIC-DATA2	PWM1				PD-EINT17
PD18	LCD0-CLK	LVDS1-V3P	DMIC-DATA1	PWM2				PD-EINT18
PD19	LCD0-DE	LVDS1-V3N	DMIC-DATA0	PWM3				PD-EINT19
PD20	LCD0-HSYNC	TWI2-SCK	DMIC-CLK	PWM4				PD-EINT20
PD21	LCD0-VSYNC	TWI2-SDA	UART1-TX	PWM5				PD-EINT21
PD22	OWA-OUT	IR-RX	UART1-RX	PWM7	- /			PD-EINT22

### Table 1-5 PE Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PE0	NCSIO-HSYNC	UART2-RTS	TWI1-SCK	LCD0-HSYNC			RGMII-RXCTRL/	PE-EINTO
							RMII-CRS-DV	
PE1	NCSIO-VSYNC	UART2-CTS	TWI1-SDA	LCD0-VSYNC			RGMII-RXD0/	PE-EINT1
							RMII-RXD0	
PE2	NCSIO-PCLK	UART2-TX	TWI0-SCK	CLK-FANOUTO	UARTO-TX		RGMII-RXD1/	PE-EINT2
							RMII-RXD1	
PE3	NCSIO-MCLK	UART2-RX	TWI0-SDA	CLK-FANOUT1	UARTO-RX		RGMII-TXCK/	PE-EINT3
							RMII-TXCK	
PE4	NCSIO-DO	UART4-TX	TWI2-SCK	CLK-FANOUT2	D-JTAG-MS	R-JTAG-MS	RGMII-TXD0/	PE-EINT4
							RMII-TXD0	
PE5	NCSI0-D1	UART4-RX	TWI2-SDA	LEDC-DO	D-JTAG-DI	R-JTAG-DI	RGMII-TXD1/	PE-EINT5
				/			RMII-TXD1	
PE6	NCSI0-D2	UART5-TX	TWI3-SCK	OWA-IN	D-JTAG-DO	R-JTAG-DO	RGMII-TXCTRL/	PE-EINT6
							RMII-TXEN	
PE7	NCSI0-D3	UART5-RX	TWI3-SDA	OWA-OUT	D-JTAG-CK	R-JTAG-CK	RGMII-CLKIN/	PE-EINT7
							RMII-RXER	
PE8	NCSI0-D4	UART1-RTS	PWM2	UART3-TX	JTAG-MS		MDC	PE-EINT8
PE9	NCSIO-D5	UART1-CTS	PWM3	UART3-RX	JTAG-DI		MDIO	PE-EINT9
PE10	NCSI0-D6	UART1-TX	PWM4	IR-RX	JTAG-DO		EPHY-25M	PE-EINT10
PE11	NCSI0-D7	UART1-RX			JTAG-CK		RGMII-TXD2	PE-EINT11
PE12	TWI2-SCK	NCSIO-FIELD					RGMII-TXD3	PE-EINT12
PE13	TWI2-SDA	PWM5			DMIC-DATA3		RGMII-RXD2	PE-EINT13

# Table 1-6 PF Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PF0	SDC0-D1	JTAG-MS	R-JTAG-MS	I2S2-DOUT1	I2S2-DIN0			PF-EINTO
PF1	SDC0-D0	JTAG-DI	R-JTAG-DI	I2S2-DOUT0	I2S2-DIN1			PF-EINT1
PF2	SDC0-CLK	UARTO-TX	TWI0-SCK	LEDC-DO	OWA-IN			PF-EINT2
PF3	SDC0-CMD	JTAG-DO	R-JTAG-DO	I2S2-BCLK				PF-EINT3
PF4	SDC0-D3	UARTO-RX	TWI0-SDA	PWM6	IR-TX			PF-EINT4



GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PF5	SDC0-D2	JTAG-CK	R-JTAG-CK	I2S2-LRCK				PF-EINT5
PF6		OWA-OUT	IR-RX	I2S2-MCLK	PWM5			PF-EINT6

#### **Table 1-7 PG Multiplex Function**

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PG0	SDC1-CLK	UART3-TX	RGMII-RXCTRL/ RMII-CRS-DV	PWM7				PG-EINTO
PG1	SDC1-CMD	UART3-RX	RGMII-RXD0/ RMII-RXD0	PWM6				PG-EINT1
PG2	SDC1-D0	UART3-RTS	RGMII-RXD1/ RMII-RXD1	UART4-TX				PG-EINT2
PG3	SDC1-D1	UART3-CTS	RGMII-TXCK/ RMII-TXCK	UART4-RX	a C			PG-EINT3
PG4	SDC1-D2	UART5-TX	RGMII-TXD0/ RMII-TXD0	PWM5				PG-EINT4
PG5	SDC1-D3	UART5-RX	RGMII-TXD1/ RMII-TXD1	PWM4				PG-EINT5
PG6	UART1-TX	TWI2-SCK	RGMII-TXD2	PWM1				PG-EINT6
PG7	UART1-RX	TWI2-SDA	RGMII-TXD3	OWA-IN				PG-EINT7
PG8	UART1-RTS	TWI1-SCK	RGMII-RXD2	UART3-TX				PG-EINT8
PG9	UART1-CTS	TWI1-SDA	RGMII-RXD3	UART3-RX				PG-EINT9
PG10	PWM3	TWI3-SCK	RGMII-RXCK	CLK-FANOUT0	IR-RX			PG-EINT10
PG11	I2S1-MCLK	TWI3-SDA	EPHY-25M	CLK-FANOUT1	TCON-TRIG			PG-EINT11
PG12	I2S1-LRCK	TWIO-SCK	RGMII-TXCTRL/ RMII-TXEN	CLK-FANOUT2	PWM0	UART1-TX		PG-EINT12
PG13	I2S1-BCLK	TWI0-SDA	RGMII-CLKIN/ RMII-RXER	PWM2	LEDC-DO	UART1-RX		PG-EINT13
PG14	I2S1-DIN0	TWI2-SCK	MDC	I2S1-DOUT1	SPIO-WP	UART1-RTS		PG-EINT14
PG15	I2S1-DOUT0	TWI2-SDA	MDIO	I2S1-DIN1	SPIO-HOLD	UART1-CTS		PG-EINT15



#### 1.1.3.3 Port Function

The Port Controller supports 6 GPIOs, every GPIO can configure as Input, Output, Function Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

**Table 1-8 Port Function** 

	Function	<b>Buffer Strength</b>	Pull Up	Pull Down
Input	GPIO/Multiplexing Input		X	x
Output	GPIO/Multiplexing Output	Υ	x	x
	Pull Up	/	Υ	N
Disable	Pull Down	/	N	Υ
Interrupt	Trigger	/	x	X

/: non-configure, configuration is invalid

Y: configure

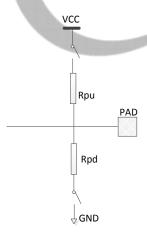
X: Select configuration according to the actual situation

N: Forbid to configure

#### 1.1.3.4 Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

Figure 1-2 Pull up/down Logic





**High-impedance**, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, the software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

**Pull-up**, an uncertain signal is pulled high by resistance, the resistance has a current-limiting function. When pulling up, the switch on Rpu is conducted by software configuration, the IO is pulled up to VCC by Rpu.

**Pull-down**, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is conducted by software configuration, the IO is pulled down to GND by Rpd.

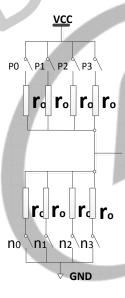
The pull-up/down of each IO is weak pull-up/down.

The setting of pull-down, pull-up, high-impedance is decided by the external circuit.

#### 1.1.3.5 Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

Figure 1-3 IO Buffer Strength Diagram



When output high level, the n0, n1, n2, n3 of NMOS is off, the p0, p1, p2, p3 of PMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the p0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the p0, p1, and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, the p0, p1, p2, and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0, p1, p2, p3 of PMOS is off, the n0, n1, n2, n3 of NMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the n0 is on, the output impedance is maximum, the



impedance value is r0. When the buffer strength is set to 1, only the n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the n0, n1, and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When the buffer strength is 3, the n0, n1, n2, and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between the output driver circuit and the port is unconnected, the driver configuration is invalid.

# NOTE

The typical value of r0 is  $180\Omega$ .

#### 1.1.3.6 Interrupt

Each group IO has an independent interrupt number. The IO within-group uses one interrupt number when one IO generates interrupt, the GPIO pins sent interrupt request to interrupt module. External Interrupt Status Register is used to query which IO generates interrupt.

The interrupt trigger of GPIO supports the following trigger types.

- Positive Edge: When a low level changes to a high level, the interrupt will generate. No matter how long a high level keeps, the interrupt generates only once.
- Negative Edge: When a high level changes to a low level, the interrupt will generate. No matter how long
  a low level keeps, the interrupt generates only once.
- High Level: Just keep a high level and the interrupt will always generate.
- Low Level: Just keep a low level and the interrupt will always generate.
- Double Edge: Positive and negative edge.

External Interrupt Configure Register is used to configure the trigger type.

The GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using a lower sample clock, to reach the debounce effect because the dither frequency of the signal is higher than the sample frequency.

Set the sample clock source by PIO\_INT\_CLK\_SELECT and the prescale factor by DEB\_CLK\_PRE\_SCALE.



#### 1.1.4 Register List

Module Name	Base Address	
GPIO	0x02000000	

Register Name	Offset	Description
PB_CFG0	0x0030	PB Configure Register 0
PB_CFG1	0x0034	PB Configure Register 1
PB_DAT	0x0040	PB Data Register
PB DRV0	0x0044	PB Multi_Driving Register 0
PB_DRV1	0x0048	PB Multi_Driving Register 1
PB_PULLO	0x0054	PB Pull Register 0
PC_CFG0	0x0060	PC Configure Register 0
PC_DAT	0x0070	PC Data Register
PC_DRV0	0x0074	PC Multi_Driving Register 0
PC_PULLO	0x0084	PC Pull Register 0
PD_CFG0	0x0090	PD Configure Register 0
PD_CFG1	0x0094	PD Configure Register 1
PD_CFG2	0x0098	PD Configure Register 2
PD_DAT	0x00A0	PD Data Register
PD_DRV0	0x00A4	PD Multi_Driving Register 0
PD_DRV1	0x00A4	PD Multi_Driving Register 1
PD_DRV2	0x00AC	PD Multi_Driving Register 2
PD_PULLO	0x00B4	PD Pull Register 0
PD_PULL1	0x00B8	PD Pull Register 1
PE CFG0	0x00C0	PE Configure Register 0
PE CFG1	0x00C4	PE Configure Register 1
PE_DAT	0x00D0	PE Data Register
PE_DRV0	0x00D4	PE Multi_Driving Register 0
PE_DRV1	0x00D8	PE Multi_Driving Register 1
PE_PULLO	0x00E4	PE Pull Register 0
PF_CFG0	0x00F0	PF Configure Register 0
PF_DAT	0x0100	PF Data Register
PF_DRV0	0x0104	PF Multi_Driving Register 0
PF_PULLO	0x0114	PF Pull Register 0
PG_CFG0	0x0120	PG Configure Register 0
PG_CFG1	0x0124	PG Configure Register 1
PG_DAT	0x0130	PG Data Register



Register Name	Offset	Description
PG_DRV0	0x0134	PG Multi_Driving Register 0
PG_DRV1	0x0138	PG Multi_Driving Register 1
PG_DRV3	0x0140	PG Multi_Driving Register 3
PG_PULL0	0x0144	PG Pull Register 0
PB_EINT_CFG0	0x0220	PB External Interrupt Configure Register 0
PB_EINT_CTL	0x0230	PB External Interrupt Control Register
PB_EINT_STATUS	0x0234	PB External Interrupt Status Register
PB_EINT_DEB	0x0238	PB External Interrupt Debounce Register
PC_EINT_CFG0	0x0240	PC External Interrupt Configure Register 0
PC_EINT_CTL	0x0250	PC External Interrupt Control Register
PC_EINT_STATUS	0x0254	PC External Interrupt Status Register
PC_EINT_DEB	0x0258	PC External Interrupt Debounce Register
PD_EINT_CFG0	0x0260	PD External Interrupt Configure Register 0
PD_EINT_CFG1	0x0264	PD External Interrupt Configure Register 1
PD_EINT_CFG2	0x0268	PD External Interrupt Configure Register 2
PD_EINT_CTL	0x0270	PD External Interrupt Control Register
PD_EINT_STATUS	0x0274	PD External Interrupt Status Register
PD_EINT_DEB	0x0278	PD External Interrupt Debounce Register
PE_EINT_CFG0	0x0280	PE External Interrupt Configure Register 0
PE_EINT_CFG1	0x0284	PE External Interrupt Configure Register 1
PE_EINT_CTL	0x0290	PE External Interrupt Control Register
PE_EINT_STATUS	0x0294	PE External Interrupt Status Register
PE_EINT_DEB	0x0298	PE External Interrupt Debounce Register
PF_EINT_CFG0	0x02A0	PF External Interrupt Configure Register 0
PF_EINT_CTL	0x02B0	PF External Interrupt Control Register
PF_EINT_STATUS	0x02B4	PF External Interrupt Status Register
PF_EINT_DEB	0x02B8	PF External Interrupt Debounce Register
PG_EINT_CFG0	0x02C0	PG External Interrupt Configure Register 0
PG_EINT_CFG1	0x02C4	PG External Interrupt Configure Register 1
PG_EINT_CTL	0x02D0	PG External Interrupt Control Register
PG_EINT_STATUS	0x02D4	PG External Interrupt Status Register
PG_EINT_DEB	0x02D8	PG External Interrupt Debounce Register
		PIO Group Withstand Voltage Mode Select
PIO_POW_MOD_SEL	0x0340	Register
		PIO Group Withstand Voltage Mode Select Control
PIO_POW_MS_CTL	0x0344	Register



#### 1.1.5 Register Description

#### 1.1.5.1 0x0030 PB Configure Register 0 (Default Value: 0xFFFF\_FFFF)

Offset: 0	x0030		Register Name: PB_CFG0	• 01
Bit	Read/Write	Default/Hex	Description	
			PB7_SELECT	
			PB7 Select	
			0000:Input	0001:Output
31:28	R/W	0xF	0010:LCD0-D17	0011:I2S2-MCLK
31.20	K) VV	UXF	0100:TWI3-SDA	0101:IR-RX
			0110:LCD0-D23	0111:UART3-RX
			1000:CPUBIST1	1001:Reserved
			1110:PB-EINT7	1111:IO Disable
			PB6_SELECT	
			PB6 Select	101
			0000:Input	0001:Output
27:24	R/W	0xF	0010:LCD0-D16	0011:I2S2-LRCK
27.24	K) VV	UXF	0100:TWI3-SCK	0101:PWM1
			0110:LCD0-D22	0111:UART3-TX
			1000:CPUBISTO	1001:Reserved
			1110:PB-EINT6	1111:IO Disable
			PB5_SELECT	
			PB5 Select	
			0000:Input	0001:Output
23:20	R/W	0xF	0010:LCD0-D9	0011:I2S2-BCLK
23.20	Tty VV	UXI	0100:TWI1-SDA	0101:PWM0
			0110:LCD0-D21	0111:UART5-RX
			1000:Reserved	1001:Reserved
			1110:PB-EINT5	1111:IO Disable
			PB4_SELECT	
			PB4 Select	
19:16	R/W		0000:Input	0001:Output
		0xF	0010:LCD0-D8	0011:I2S2-DOUT0
			0100:TWI1-SCK	0101:I2S2-DIN1
			0110:LCD0-D20	0111:UART5-TX
			1000:Reserved	1001:Reserved
			1110:PB-EINT4	1111:IO Disable



Offset: 0	x0030		Register Name: PB_CFG0	
Bit	Read/Write	Default/Hex	Description	
			PB3_SELECT	
			PB3 Select	
			0000:Input	0001:Output
15:12	R/W	0xF	0010:LCD0-D1	0011:I2S2-DOUT1
15:12	K/ W	UXF	0100:TWI0-SCK	0101:I2S2-DIN0
			0110:LCD0-D19	0111:UART4-RX
			1000:Reserved	1001:Reserved
			1110:PB-EINT3	1111:IO Disable
			PB2_SELECT	
	R/W	0xF	PB2 Select	
			0000:Input	0001:Output
11:8			0010:LCD0-D0	0011:I2S2-DOUT2
11.0	Ny VV		0100:TWI0-SDA	0101:I2S2-DIN2
			0110:LCD0-D18	0111:UART4-TX
			1000:Reserved	1001:Reserved
			1110:PB-EINT2	1111:IO Disable
7:4	R/W	0xF	Reserved	
3:0	R/W	0xF	Reserved	

# 1.1.5.2 0x0034 PB Configure Register 1 (Default Value: 0x000F\_FFFF)

Offset: 0x0034			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
31:20	1	1	/
19:16	R/W	0xF	Reserved
15:12	R/W	0xF	Reserved
11:8	R/W	0xF	Reserved
7:4	R/W	0xF	Reserved
3:0	R/W	0xF	Reserved



#### 1.1.5.3 0x0040 PB Data Register (Default Value: 0x0000\_0000)

Offset: 0x0040			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	1
7:0	R/W	0x0	PB_DAT  If the port is configured as the input function, the corresponding bit is the pin state. If the port is configured as the output function, the pin state is the same as the corresponding bit. The read bit value is the value set up by software. If the port is configured as a functional pin, the undefined value will be read.

#### 1.1.5.4 0x0044 PB Multi\_Driving Register 0 (Default Value: 0x1111\_1111)

Offset: 0	x0044		Register Name: PB_DRV0		
Bit	Read/Write	Default/Hex	Description		
31:30	1	1	1		
			PB7_DRV		
29:28	R/W	0x1	PB7 Multi_Driving Select		
29.20	K/ VV	UXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
27:26	/	1	1		
			PB6_DRV		
25:24	R/W	0x1	PB6 Multi_Driving Select		
25.24	N/ VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
23:22	1	1	1		
			PB5_DRV		
21:20	R/W	0x1	PB5 Multi_Driving Select		
21.20	TV VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
19:18	/	1	1		
			PB4_DRV		
17:16	17:16 R/W	0x1	PB4 Multi_Driving Select		
17.10			00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
15:14	/	1	1		



Offset: 0	x0044		Register Name: PB_DRV0		
Bit	Read/Write	Default/Hex	Description		
			PB3_DRV		
13:12	R/W	0x1	PB3 Multi_Driving Select		
13.12	IV VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
11:10	/	/	1		
			PB2_DRV		
9:8	R/W	0x1	PB2 Multi_Driving Select		
9.6	N/ VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
7:6	1	1	1		
5:4	R/W	0x1	Reserved		
3:2	1	1	/		
1:0	R/W	0x1	Reserved		

# 1.1.5.5 0x0048 PB Multi\_Driving Register 1 (Default Value: 0x0001\_1111)

Offset: 0	Offset: 0x0048		Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
31:18	1	1	1
17:16	R/W	0x1	Reserved
15:14	1	/	/
13:12	R/W	0x1	Reserved
11:10	/	1	/
9:8	R/W	0x1	Reserved
7:6	1	/	/
5:4	R/W	0x1	Reserved
3:2	/	/	/
1:0	R/W	0x1	Reserved



#### 1.1.5.6 0x0054 PB Pull Register 0 (Default Value: 0x0000\_0000)

Offset: 0	Offset: 0x0054		Register Name: PB_PULL0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	1
15:14	R/W	0x0	PB7_PULL PB7 Pull_up or down Select O0: Pull_up/down disable
13:12	R/W	0x0	PB6_PULL PB6 Pull_up or down Select 00: Pull_up/down disable
11:10	R/W	0x0	PB5_PULL  PB5 Pull_up or down Select  O0: Pull_up/down disable
9:8	R/W	0x0	PB4_PULL  PB4 Pull_up or down Select  00: Pull_up/down disable
7:6	R/W	0x0	PB3_PULL  PB3 Pull_up or down Select  O0: Pull_up/down disable
5:4	R/W	0x0	PB2_PULL PB2 Pull_up or down Select  00: Pull_up/down disable
3:2	R/W	0x0	Reserved
1:0	R/W	0x0	Reserved



# 1.1.5.7 0x0060 PC Configure Register 0 (Default Value: 0xFFFF\_FFFF)

Offset: 0	)x0060		Register Name: PC_CFG0	-
Bit	Read/Write	Default/Hex	Description	
			PC7_SELECT	
			PC7 Select	
			0000:Input	0001:Output
31:28	D /\A/	0xF	0010:SPI0-HOLD	0011:SDC2-D3
31:28	R/W	UXF	0100:UART3-RX	0101:TWI3-SDA
			0110:TCON-TRIG	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PC-EINT7	1111:IO Disable
			PC6_SELECT	
			PC6 Select	40
			0000:Input	0001:Output
27:24	R/W	OvE	0010:SPI0-WP	0011:SDC2-D0
27:24	K/VV	0xF	0100:UART3-TX	0101:TWI3-SCK
			0110:DBG-CLK	0111:Reserved
			1000:Reserved	1001:Reserved
		1	1110:PC-EINT6	1111:IO Disable
		Ma. 1	PC5_SELECT	
			PC5 Select	
			0000:Input	0001:Output
23:20	R/W	0xF	0010:SPI0-MISO	0011:SDC2-D1
23.20	IV, VV	UXI	0100:BOOT-SEL1	0101:Reserved
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PC-EINT5	1111:IO Disable
			PC4_SELECT	
	10:1C P/W		PC4 Select.	
			0000:Input	0001:Output
10:16			0010:SPI0-MOSI	0011:SDC2-D2
19:16	R/W	0xF	0100:BOOT-SEL0	0101:Reserved
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PC-EINT4	1111:IO Disable



Offset: 0	Offset: 0x0060		Register Name: PC_CFG0	
Bit	Read/Write	Default/Hex	Description	
			PC3_SELECT	
			PC3 Select	
			0000:Input	0001:Output
15:12	R/W	0xF	0010:SPI0-CS0	0011:SDC2-CMD
15.12	K/VV	UXF	0100:Reserved	0101:Reserved
		•	0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PC-EINT3	1111:IO Disable
		P 10	PC2_SELECT	
		0xF	PC2 Select	
			0000:Input	0001:Output
11:8	R/W		0010:SPI0-CLK	0011:SDC2-CLK
11.0	IN, VV		0100:Reserved	0101:Reserved
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PC-EINT2	1111:IO Disable
7:4	R/W	0xF	Reserved	
3:0	R/W	0xF	Reserved	

# 1.1.5.8 0x0070 PC Data Register (Default Value: 0x0000\_0000)

Offset: 0x0070			Register Name: PC_DAT	
Bit	Read/Write	Default/Hex	Description	
31:8	/	1	/	
			PC_DAT	
7:0	R/W	0x0	If the port is configured as the input function, the corresponding bit is the pin state. If the port is configured as the output function, the pin state is the same as the corresponding bit. The read bit value is the value set up by software. If the port is configured as a functional pin, the undefined value will be read.	



#### 1.1.5.9 0x0074 PC Multi\_Driving Register 0 (Default Value: 0x1111\_1111)

Offset: 0	)x0074		Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	1
			PC7_DRV
29:28	D /\A/	0.4	PC7 Multi_Driving Select
29:28	R/W	0x1	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
27:26	/	1	
			PC6_DRV
25:24	R/W	0x1	PC6 Multi_Driving Select
25.24	K/VV	UX1	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
23:22	1	/	
			PC5_DRV
21:20	R/W	0x1	PC5 Multi_Driving Select
21.20	IV, VV		00: Level 0 01: Level 1
			10: Level 2 11: Level 3
19:18	1	1	/
		0x1	PC4_DRV
17:16	R/W		PC4 Multi_Driving Select
17.10	IV, VV	OXI	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
15:14	/	/	
			PC3_DRV
13:12	R/W	0x1	PC3 Multi_Driving Select
13.12	Tty VV	OXI	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
11:10	/	/	/
			PC2_DRV
9:8	R/W	0x1	PC2 Multi_Driving Select
J.0	11,7 4		00: Level 0 01: Level 1
			10: Level 2 11: Level 3
7:6	/	1	/
5:4	R/W	0x1	Reserved
3:2	1	1	/
1:0	R/W	0x1	Reserved



#### 1.1.5.10 0x0084 PC Pull Register 0 (Default Value: 0x0000\_0540)

Offset: 0	Offset: 0x0084		Register Name: PC_PULL0	. 01,
Bit	Read/Write	Default/Hex	Description	
31:16	/	/	1	
15:14	R/W	0x0	PC7_PULL PC7 Pull_up/down Select	
	.,		00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
13:12	R/W	0x0	PC6_PULL PC6 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
11:10	R/W	0x1	PC5_PULL PC5 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
3:2	R/W	0x0	Reserved	
1:0	R/W	0x0	Reserved	



#### 1.1.5.11 0x0090 PD Configure Register 0 (Default Value: 0xFFFF\_FFFF)

Offset: 0	Offset: 0x0090		Register Name: PD_CFG0	-0
Bit	Read/Write	Default/Hex	Description	
			PD7_SELECT	
			PD7 Select	
			0000:Input	0001:Output
24.20	D/M	05	0010:LCD0-D11	0011:LVDS0-CKN
31:28	R/W	0xF	0100:DSI-D2N	0101:UART4-TX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT7	1111:IO Disable
			PD6_SELECT	
			PD6 Select	
			0000:Input	0001:Output
27.24	7/11	0.5	0010:LCD0-D10	0011:LVDS0-CKP
27:24	R/W	OxF	0100:DSI-D2P	0101:UART5-RX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT6	1111:IO Disable
			PD5_SELECT	
			PD5 Select	
			0000:Input	0001:Output
23:20	D /\A/	R/W 0xF	0010:LCD0-D7	0011:LVDS0-V2N
23.20	N/ VV		0100:DSI-CKN	0101:UART5-TX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT5	1111:IO Disable
			PD4_SELECT	
			PD4 Select	
			0000:Input	0001:Output
10.16	R/W		0010:LCD0-D6	0011:LVDS0-V2P
19:16		0xF	0100:DSI-CKP	0101:UART2-CTS
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT4	1111:IO Disable



Offset: 0	Offset: 0x0090		Register Name: PD_CFG0	
Bit	Read/Write	Default/Hex	Description	
			PD3_SELECT PD3 Select	
			0000:Input	0001:Output
	- 6		0010:LCD0-D5	0011:LVDS0-V1N
15:12	R/W	0xF	0100:DSI-D1N	0101:UART2-RTS
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
		•	1110:PD-EINT3	1111:IO Disable
			PD2_SELECT	
			PD2 Select	
			0000:Input	0001:Output
11.0	R/W	0xF	0010:LCD0-D4	0011:LVDS0-V1P
11:8	R/W	UXF	0100:DSI-D1P	0101:UART2-RX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT2	1111:IO Disable
			PD1_SELECT	
			PD1 Select	
			0000:Input	0001:Output
7:4	R/W	0xF	0010:LCD0-D3	0011:LVDS0-V0N
7.4	IN, VV	UXI	0100:DSI-D0N	0101:UART2-TX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT1	1111:IO Disable
			PD0_SELECT	
			PD0 Select	
			0000:Input	0001:Output
3:0	R/W	0xF	0010:LCD0-D2	0011:LVDS0-V0P
3.0	Tty VV	OXI	0100:DSI-D0P	0101:TWI0-SCK
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINTO	1111:IO Disable



#### 1.1.5.12 0x0094 PD Configure Register 1 (Default Value: 0xFFFF\_FFFF)

Offset: 0	x0094		Register Name: PD_CFG1	
Bit	Read/Write	Default/Hex	Description	
			PD15_SELECT	
			PD15 Select	
			0000:Input	0001:Output
31:28	D /\A/	٥٧٢	0010:LCD0-D21	0011:LVDS1-V2N
31:28	R/W	0xF	0100:SPI1-WP/DBI-TE	0101:IR-RX
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT15	1111:IO Disable
			PD14_SELECT	
			PD14 Select	
			0000:Input	0001:Output
27:24	D/M	OvE	0010:LCD0-D20	0011:LVDS1-V2P
27:24	R/W	0xF	0100:SPI1-HOLD/DBI-DCX/DBI-WR	X 0101:UART3-CTS
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
		1	1110:PD-EINT14	1111:IO Disable
			PD13_SELECT	
			PD13 Select	
			0000:Input	0001:Output
23:20	R/W	0xF	0010:LCD0-D19	0011:LVDS1-V1N
23.20	Ny VV	UXF	0100:SPI1-MISO/DBI-SDI/DBI-TE/D	BI-DCX 0101:UART3-RTS
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT13	1111:IO Disable
			PD12_SELECT	
			PD12 Select	
			0000:Input 00	01:Output
19:16	R/W	0xF	0010:LCD0-D18 001	l1:LVDS1-V1P
19.10		UXI	0100:SPI1-MOSI/DBI-SDO 010	01:TWI0-SDA
			0110:Reserved 01	11:Reserved
			1000:Reserved 10	01:Reserved
			1110:PD-EINT12 11	11:IO Disable



Offset: 0	Offset: 0x0094		Register Name: PD_CFG1	
Bit	Read/Write	Default/Hex	Description	
15:12	R/W	0xF	PD11_SELECT PD11 Select 0000:Input 0010:LCD0-D15 0100:SPI1-CLK/DBI-SCLK	0001:Output 0011:LVDS1-V0N 0101:UART3-RX
		•	0110:Reserved 1000:Reserved 1110:PD-EINT11	0111:Reserved 1001:Reserved 1111:IO Disable
11:8	R/W	0xF	PD10_SELECT PD10 Select 0000:Input 0010:LCD0-D14	0001:Output 0011:LVDS1-V0P
11.6	Nyw	UXF	0100:SPI1-CS/DBI-CSX 0110:Reserved 1000:Reserved 1110:PD-EINT10	0101:UART3-TX 0111:Reserved 1001:Reserved 1111:IO Disable
7:4	R/W	OxF	PD9_SELECT PD9 Select 0000:Input 0010:LCD0-D13 0100:DSI-D3N 0110:Reserved 1000:Reserved 1110:PD-EINT9	0001:Output 0011:LVDS0-V3N 0101:PWM6 0111:Reserved 1001:Reserved 1111:IO Disable
3:0	R/W	OxF	PD8_SELECT PD8 Select 0000:Input 0010:LCD0-D12 0100:DSI-D3P 0110:Reserved 1000:Reserved	0001:Output 0011:LVDS0-V3P 0101:UART4-RX 0111:Reserved 1001:Reserved



#### 1.1.5.13 0x0098 PD Configure Register 2 (Default Value: 0x0FFF\_FFFF)

Offset: 0	x0098		Register Name: PD_CI	FG2
Bit	Read/Write	Default/Hex	Description	
31:28	/	/	/	
			PD22_SELECT	
			PD22 Select	.66
			0000:Input	0001:Output
27.24	5 /14/	0.5	0010:OWA-OUT	0011:IR-RX
27:24	R/W	0xF	0100:UART1-RX	0101:PWM7
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT22	1111:IO Disable
			PD21_SELECT	
			PD21 Select	
			0000:Input	0001:Output
22.20	D /A/	0xF	0010:LCD0-VSYNC	0011:TWI2-SDA
23:20	R/W		0100:UART1-TX	0101:PWM5
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT21	1111:IO Disable
			PD20_SELECT	
			PD20 Select	
			0000:Input	0001:Output
19:16	R/W	0xF	0010:LCD0-HSYNC	0011:TWI2-SCK
19.10	IV VV	OXI	0100:DMIC-CLK	0101:PWM4
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT20	1111:IO Disable
			PD19_SELECT	
			PD19 Select	
			0000:Input	0001:Output
15:12	R/W	05	0010:LCD0-DE	0011:LVDS1-V3N
13.12		0xF	0100:DMIC-DATA0	0101:PWM3
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT19	1111:IO Disable



Offset: 0x0098			Register Name: PD_CFG2	
Bit	Read/Write	Default/Hex	Description	
			PD18_SELECT	
			PD18 Select	
			0000:Input	0001:Output
11.0	D /\A/	05	0010:LCD0-CLK	0011:LVDS1-V3P
11:8	R/W	0xF	0100:DMIC-DATA1	0101:PWM2
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT18	1111:IO Disable
			PD17_SELECT	
	R/W	OxF	PD17 Select.	
			0000:Input	0001:Output
7:4			0010:LCD0-D23	0011:LVDS1-CKN
7.4	K/ VV		0100:DMIC-DATA2	0101:PWM1
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT17	1111:IO Disable
		V 0xF	PD16_SELECT	
			PD16 Select	
			0000:Input	0001:Output
3:0	D /\A/		0010:LCD0-D22	0011:LVDS1-CKP
3.0	R/W		0100:DMIC-DATA3	0101:PWM0
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PD-EINT16	1111:IO Disable

# 1.1.5.14 0x00A0 PD Data Register (Default Value: 0x0000\_0000)

Offset: 0x00A0			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/



Offset: 0x00A0			Register Name: PD_DAT	
Bit Read/Write Default/Hex		Default/Hex	Description	
	R/W	0x0	PD_DAT	
			PD Data	
			If the port is configured as the input function, the corresponding	
22:0			bit is the pin state. If the port is configured as the output function,	
			the pin state is the same as the corresponding bit. The read bit	
			value is the value set up by software. If the port is configured as	
			a functional pin, the undefined value will be read.	

# 1.1.5.15 0x00A4 PD Multi\_Driving Register 0 (Default Value: 0x1111\_1111)

Offset: 0x00A4			Register Name: PD_DRV0	
Bit	Read/Write	Default/Hex	Description	
31:30	/	/	/	
			PD7_DRV	
29:28	R/W	0x1	PD7 Multi_Driving Select.	
29.20	N/ VV	UXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
27:26	1	/	1	
			PD6_DRV	
25:24	R/W	0x1	PD6 Multi_Driving Select.	
25.24	IV, VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	/	1	1	
			PD5_DRV	
21:20	R/W	0x1	PD5 Multi_Driving Select.	
21.20	Tty VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
19:18	/	/	1	
			PD4_DRV	
17:16	R/W	0x1	PD4 Multi_Driving Select.	
17.10			00: Level 0	01: Level 1
			10: Level 2	11: Level 3
15:14	/	1	/	



Offset: 0x00A4			Register Name: PD_DRV0	
Bit	Read/Write	Default/Hex	Description	
			PD3_DRV	
13:12	R/W	0x1	PD3 Multi_Driving Select.	
13.12	I I V V V	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
11:10	/	/	1	
			PD2_DRV	
9:8	R/W	0x1	PD2 Multi_Driving Select.	
9.0	R/W	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
7:6	/	1	1	
			PD1_DRV	
5:4	R/W	0x1	PD1 Multi_Driving Select.	40
3.4	IV, VV	OX1	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
3:2	1	1	1	
			PD0_DRV	
1:0	R/W	0x1	PD0 Multi_Driving Select.	
	R/W		00: Level 0	01: Level 1
			10: Level 2	11: Level 3

# 1.1.5.16 0x00A8 PD Multi\_Driving Register 1 (Default Value: 0x1111\_1111)

Offset: 0	x00A8		Register Name: PD_DRV1	
Bit	Read/Write	Default/Hex	Description	
31:30	1	1	/	
			PD15_DRV	
29:28	D/M	0x1	PD15 Multi_Driving Select.	
29.28	R/W		00: Level 0	01: Level 1
			10: Level 2	11: Level 3
27:26	/	/	1	
	R/W	0x1	PD14_DRV	
25:24			PD14 Multi_Driving Select.	
25.24			00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	/	/	1	



Offset: 0	x00A8		Register Name: PD_DRV1		
Bit	Read/Write	Default/Hex	Description		
21:20	R/W	0x1	PD13_DRV PD13 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	O
19:18	/	/	1	5	
17:16	R/W	0x1	PD12_DRV PD12 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	
15:14	/	1	/		
13:12	R/W	0x1	PD11_DRV PD11 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	ER
11:10	1	1	/		
9:8	R/W	0x1	PD10_DRV PD10 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	
7:6	1	1	1		
5:4	R/W	0x1	PD9_DRV PD9 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	
3:2	/	1	/		
1:0	R/W	0x1	PD8_DRV PD8 Multi_Driving Select. 00: Level 0 10: Level 2	01: Level 1 11: Level 3	

#### 1.1.5.17 0x00AC PD Multi\_Driving Register 2 (Default Value: 0x0111\_1111)

Offset: 0x00AC			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
31:26	1	/	/



Offset: 0	x00AC		Register Name: PD_DRV2	
Bit	Read/Write	Default/Hex	Description	
			PD22_DRV	
25:24	R/W	0x1	PD22 Multi_Driving Select.	
23.24	IV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	/	/	1	
			PD21_DRV	
21:20	R/W	0x1	PD21 Multi_Driving Select.	
21.20	r/ vv	UXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
19:18	/	1	1	
			PD20_DRV	
17:16	R/W	01	PD20 Multi_Driving Select.	
17:16	K/W	0x1	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
15:14	1	1	/	
			PD19_DRV	
13:12	R/W	0x1	PD19 Multi_Driving Select.	
13:12	K/VV		00: Level 0	01: Level 1
			10: Level 2	11: Level 3
11:10	/	1	1	
			PD18_DRV	
9:8	R/W	0x1	PD18 Multi_Driving Select.	
9.8	Ity VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
7:6	/	1	1	
-			PD17_DRV	
5.4	R/W	0x1	PD17 Multi_Driving Select.	
5:4	IV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
3:2	1	/	1	
			PD16_DRV	
1:0	R/W	0x1	PD16 Multi_Driving Select.	
1:0			00: Level 0	01: Level 1
			10: Level 2	11: Level 3



#### 1.1.5.18 0x00B4 PD Pull Register 0 (Default Value: 0x0000\_0000)

Offset: 0x00B4		Register Name: PD_PULL0		
Bit	Read/Write	Default/Hex	Description	
			PD15_PULL	
24.20	D /\A/	0.0	PD15 Pull_up or down Select	t.
31:30	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD14_PULL	
20.20	D /\A/	00	PD14 Pull_up or down Select	t.
29:28	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD13_PULL	
27.26	D/M	0.0	PD13 Pull_up or down Select	L
27:26	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD12_PULL	
25.24	R/W	0x0	PD12 Pull_up or down Select.	
25:24			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD11_PULL	
22.22	D /\A/	00	PD11 Pull_up or down Select	t.
23:22	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD10_PULL	
21:20	D /\A/	040	PD10 Pull_up or down Select	t.
21:20	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD9_PULL	
10.10	D /\A/	00	PD9 Pull_up or down Select.	
19:18	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD8_PULL	
17.16	R/W	0x0	PD8 Pull_up or down Select.	
17:16			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved



Offset: 0	Offset: 0x00B4		Register Name: PD_PULL0
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0x0	PD7_PULL PD7 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull_up or down Select.  00: Pull_up/down disable
9:8	R/W	0x0	PD4_PULL PD4 Pull_up or down Select.  00: Pull_up/down disable 01: Pull_up  10: Pull_down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull_up or down Select.  00: Pull_up/down disable
5:4	R/W	0x0	PD2_PULL PD2 Pull_up or down Select.  00: Pull_up/down disable
3:2	R/W	0x0	PD1_PULL PD1 Pull_up or down Select.  00: Pull_up/down disable
1:0	R/W	0x0	PD0_PULL PD0 Pull_up or down Select.  00: Pull_up/down disable



## 1.1.5.19 0x00B8 PD Pull Register 1 (Default Value: 0x0000\_0000)

Offset: 0	Offset: 0x00B8		Register Name: PD_PULL1	
Bit	Read/Write	Default/Hex	Description	
31:14	/	/	/	
			PD22_PULL	
13:12	R/W	0x0	PD22 Pull_up or down Select	5
15.12	IV VV	0.00	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD21_PULL	
11:10	R/W	0x0	PD21 Pull_up or down Select	
11.10	1,7 00	OXO .	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD20_PULL	40
9:8	R/W	0x0	PD20 Pull_up or down Select	
			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD19_PULL	
7:6	R/W	0x0	PD19 Pull_up or down Select	
	.0		00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD18_PULL	
5:4	R/W	0x0	PD18 Pull_up or down Select	
			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD17_PULL	
3:2	R/W	0x0	PD17 Pull_up or down Select	
			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PD16_PULL PD16 Pull_up or down Select	
1:0	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			TO. Pull_uowii	11. VG26I AGN



#### 1.1.5.20 0x00C0 PE Configure Register 0 (Default Value: 0xFFFF\_FFFF)

Offset: 0	Offset: 0x00C0		Register Name: PE_CFG0		
Bit	Read/Write	Default/Hex	Description		
			PE7_SELECT		
			PE7 Select		
			0000:Input	0001:Output	
21.20	R/W	OvE	0010:NCSI0-D3	0011:UART5-RX	
31:28	K/ W	0xF	0100:TWI3-SDA	0101:OWA-OUT	
			0110:D-JTAG-CK	0111:R-JTAG-CK	
			1000:RGMII-CLKIN/RMII-RXER	1001:Reserved	
			1110:PE-EINT7	1111:IO Disable	
			PE6_SELECT		
			PE6 Select	40	
			0000:Input	0001:Output	
27:24	R/W	0xF	0010:NCSI0-D2	0011:UART5-TX	
27.24	K/VV	UXF	0100:TWI3-SCK	0101:OWA-IN	
			0110:D-JTAG-DO	0111:R-JTAG-DO	
			1000:RMII-TXCTRL/RMII-TXEN	1001:Reserved	
		1	1110:PE-EINT6	1111:IO Disable	
		TO. 1	PE5_SELECT		
			PE5 Select		
			0000:Input	0001:Output	
23:20	R/W	0xF	0010:NCSI0-D1	0011:UART4-RX	
25.20	Ity VV	OXI	0100:TWI2-SDA	0101:LEDC-DO	
			0110:D-JTAG-DI	0111:R-JTAG-DI	
			1000:RGMII-TXD1/RMII-TXD1	1001:Reserved	
			1110:PE-EINT5	1111:IO Disable	
			PE4_SELECT		
			PE4 Select		
			0000:Input	0001:Output	
19:16	R/W	0xF	0010:NCSI0-D0	0011:UART4-TX	
19.10	IV VV	UXI	0100:TWI2-SCK	0101:CLK-FANOUT2	
			0110:D-JTAG-MS	0111:R-JTAG-MS	
			1000:RGMII-TXD0/RMII-TXD0	1001:Reserved	
			1110:PE-EINT4	1111:IO Disable	



Offset: 0	Offset: 0x00C0		Register Name: PE_CFG0	
Bit	Read/Write	Default/Hex	Description	
			PE3_SELECT PE3 Select	
				0001:Output
			0010:NCSI0-MCLK	0011:UART2-RX
15:12	R/W	0xF	0100:TWI0-SDA	0101:CLK-FANOUT1
				0111:Reserved
				1001:Reserved
				.111:IO Disable
			PE2_SELECT	
			PE2 Select	
			0000:Input	0001:Output
			0010:NCSIO-PCLK	0011:UART2-TX
11:8	R/W	0xF	0100:TWI0-SCK	0101:CLK-FANOUT0
			0110:UART0-TX	0111:Reserved
			1000:RGMII-RXD1/RMII-RXD1	1001:Reserved
			1110:PE-EINT2	1111:IO Disable
			PE1_SELECT	
			PE1 Select	
		TO. 1	0000:Input	0001:Output
7:4	R/W	0xF	0010:NCSIO-VSYNC	0011:UART2-CTS
7.4	K/ W	UXF	0100:TWI1-SDA	0101:LCD0-VSYNC
			0110:Reserved	0111:Reserved
			1000:RGMII-RXD0/RMII-RXD0	1001:Reserved
			1110:PE-EINT1	1111:IO Disable
			PEO_SELECT	
			PEO Select	
			0000:Input	0001:Output
3:0	R/W	0xF	0010:NCSI0-HSYNC	0011:UART2-RTS
3.0	Tty VV	OXI	0100:TWI1-SCK	0101:LCD0-HSYNC
			0110:Reserved	0111:Reserved
			1000:RGMII-RXCTRL/RMII-CRS-I	DV 1001:Reserved
			1110:PE-EINTO	1111:IO Disable



#### 1.1.5.21 0x00C4 PE Configure Register 1 (Default Value: 0xFFFF\_FFFF)

Offset: 0x00C4		Register Name: PE_CFG1		
Bit	Read/Write	Default/Hex	Description	
31:28	R/W	0xF	Reserved	
27:24	R/W	0xF	Reserved	
			PE13_SELECT	6
			PE13 Select	
			0000:Input	0001:Output
22.20	D /\A/	0xF	0010:TWI2-SDA	0011:PWM5
23:20	R/W	UXF	0100:Reserved	0101:Reserved
			0110:DMIC-DATA3	0111:Reserved
			1000:RGMII-RXD2	1001:Reserved
			1110:PE-EINT13	1111:IO Disable
			PE12_SELECT	
			PE12 Select	
			0000:Input	0001:Output
19:16	R/W	OvE	0010:TWI2-SCK	0011:NCSIO-FIELD
19:16	R/ W	OxF	0100:Reserved	0101:Reserved
			0110:Reserved	0111:Reserved
			1000:RGMII-TXD3	1001:Reserved
			1110:PE-EINT12	1111:IO Disable
			PE11_SELECT	
			PE11 Select	
		,	0000:Input	0001:Output
15:12	R/W	/	0010:NCSI0-D7	0011:UART1-RX
15.12	r/ vv	0xF	0100:Reserved	0101:Reserved
			0110:JTAG-CK	0111:Reserved
			1000:RGMII-TXD2	1001:Reserved
			1110:PE-EINT11	1111:IO Disable
			PE10_SELECT	
			PE10 Select	
			0000:Input	0001:Output
11·9 D/\A/	05	0010:NCSI0-D6	0011:UART1-TX	
11.0	11:8 R/W	0xF	0100:PWM4	0101:IR-RX
			0110:JTAG-DO	0111:Reserved
			1000:EPHY-25M	1001:Reserved
			1110:PE-EINT10	1111:IO Disable



Offset: 0	Offset: 0x00C4		Register Name: PE_CFG1		
Bit	Read/Write	Default/Hex	Description		
			PE9_SELECT		
			PE9 Select		
			0000:Input	0001:Output	
7:4	R/W	0xF	0010:NCSI0-D5	0011:UART1-CTS	
7.4	K/ VV	UXF	0100:PWM3	0101:UART3-RX	
			0110:JTAG-DI	0111:Reserved	
			1000:MDIO	1001:Reserved	
			1110:PE-EINT9	1111:IO Disable	
		CX	PE8_SELECT		
			PE8 Select		
			0000:Input	0001:Output	
3:0	R/W	0xF	0010:NCSI0-D4	0011:UART1-RTS	
3.0	K/VV		0100:PWM_2	0101:UART3-TX	
			0110:JTAG-MS	0111:Reserved	
			1000:MDC	1001:Reserved	
			1110:PE_EINT8	1111:IO Disable	

# 1.1.5.22 0x00D0 PE Data Register (Default Value: 0x0000\_0000)

Offset: 0x00D0			Register Name: PE_DAT	
Bit	Read/Write	Default/Hex	Description	
31:14	1	1	//	
			PE_DAT	
			PE Data	
			If the port is configured as input, the corresponding bit is the pin	
13:0	R/W	0x0	state. If the port is configured as output, the pin state is the same	
			as the corresponding bit. The read bit value is the value setup by	
			software. If the port is configured as functional pin, the	
			undefined value will be read.	



#### 1.1.5.23 0x00D4 PE Multi\_Driving Register 0 (Default Value: 0x1111\_1111)

Offset: 0	Offset: 0x00D4		Register Name: PE_DRV0	
Bit	Read/Write	Default/Hex	Description	
31:30	/	/	/	
			PE7_DRV	
20.20	D /\A/	0v1	PE7 Multi_Driving Select	51
29:28	R/W	0x1	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
27:26	/	1		
			PE6_DRV	
25:24	R/W	0x1	PE6 Multi_Driving Select	
25.24	N/ VV	UXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22		1	/	
			PE5_DRV	
21:20	R/W	0x1	PE5 Multi_Driving Select	
21.20	N, W	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
19:18	1	1	1	
			PE4_DRV	
17:16	R/W	0x1	PE4 Multi_Driving Select	
17.10	11, 11	OAI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
15:14	1	1	/	
			PE3_DRV	
13:12	R/W	0x1	PE3 Multi_Driving Select	
13.12	11,7 17	OAI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
11:10	/	1	1	
			PE2_DRV	
9:8	R/W	0x1	PE2 Multi_Driving Select	
	· · · · ·		00: Level 0	01: Level 1
			10: Level 2	11: Level 3
7:6	/	/	1	



Offset: 0x00D4		Register Name: PE_DRV0			
Bit	Read/Write	Default/Hex	Description		
			PE1_DRV		
5:4	R/W	0x1	PE1 Multi_Driving Select		
5.4	K/ VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
3:2	/	/	1		
			PEO_DRV		
1:0 R/W	D /\A/	0.4	PE0 Multi_Driving Select		
	N/ VV	0x1	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	

# 1.1.5.24 0x00D8 PE Multi\_Driving Register 1 (Default Value: 0x1111\_1111)

Offset: 0	Offset: 0x00D8		Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	1	1	/
29:28	R/W	0x1	Reserved
27:26	1	1	/
25:24	R/W	0x1	Reserved
23:22	/	1	1
			PE13_DRV
21:20	R/W	0x1	PE13 Multi_Driving Select
21.20	21:20   R/W	OXI	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
19:18	/	1	/
			PE12_DRV
17:16	R/W	0x1	PE12 Multi_Driving Select
17.10	11, 10	OXI	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
15:14	/	/	/
			PE11_DRV
13:12 R/W	R/W	0x1	PE11 Multi_Driving Select
13.12	11/ VV	OVI	00: Level 0 01: Level 1
			10: Level 2 11: Level 3
11:10	/	/	/



Offset: 0	Offset: 0x00D8		Register Name: PE_DRV1		
Bit	Read/Write	Default/Hex	Description		
			PE10_DRV		
9:8	R/W	0x1	PE10 Multi_Driving Select		
9.8	IV VV	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
7:6	1	/	1	5	
			PE9_DRV		
5:4	R/W	0x1	PE9 Multi_Driving Select		
3.4	N/ VV	OXI	00: Level 0	01: Level 1	
		2 10	10: Level 2	11: Level 3	
3:2	1	1	1		
			PE8_DRV		
1.0	R/W	0x1	PE8 Multi_Driving Select		40
1.0	1:0 R/W	OXI	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	

# 1.1.5.25 0x00E4 PE Pull Register 0 (Default Value: 0x0000\_0000)

Offset: 0	Offset: 0x00E4		Register Name: PE_PULL0	
Bit	Read/Write	Default/Hex	Description	
31:30	R/W	0x0	Reserved	
29:28	R/W	0x0	Reserved	
			PE13_PULL	
27:26	D/M	0x0	PE13 Pull_up or down Select	t
27:26	R/W	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PE12_PULL	
25:24	D //A/	0.0	PE12 Pull_up or down Select	t
25.24	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PE11_PULL	
23:22 R/W	0x0	PE11 Pull_up or down Select		
		00: Pull_up/down disable	01: Pull_up	
			10: Pull_down	11: Reserved



Offset: 0	x00E4		Register Name: PE_PULL0	
Bit	Read/Write	Default/Hex	Description	
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select 00: Pull_up/down disable	01: Pull_up 11: Reserved
19:18	R/W	0x0	10: Pull_down  PE9_PULL  PE9 Pull_up or down Select  00: Pull_up/down disable  10: Pull_down	01: Pull_up 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved



Offset: 0x00E4		Register Name: PE_PULL0		
Bit	Read/Write	Default/Hex	Description	
			PE1_PULL	
2.2	0.0	PE1 Pull_up or down Select		
3:2	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PEO_PULL	51
1:0	R/W	0x0	PEO Pull_up or down Select	
1.0			00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved

# 1.1.5.26 0x00F0 PF Configure Register 0 (Default Value: 0x0FFF\_FFFF)

Offset: 0	0x00F0		Register Name: PF_CFG0	
Bit	Read/Write	Default/Hex	Description	
31:28	1	1	/	
			PF6_SELECT	
		4	PF6 Select	
		4	0000:Input	0001:Output
27.24	D /\A/	OvE	0010:Reserved	0011:OWA-OUT
27:24	R/W	0xF	0100:IR-RX	0101:I2S2-MCLK
			0110:PWM5	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PF-EINT6	1111:IO Disable
			PF5_SELECT	
		0xF	PF5 Select	
			0000:Input	0001:Output
22.20	23:20 R/W		0010:SDC0-D2	0011:JTAG-CK
23:20			0100:R-JTAG-CK	0101:I2S2-LRCK
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PF-EINT5	1111:IO Disable



Offset: 0	Offset: 0x00F0		Register Name: PF_CFG0	
Bit	Read/Write	Default/Hex	Description	
19:16	R/W	0xF	PF4_SELECT PF4 Select 0000:Input 0010:SDC0-D3 0100:TWI0-SDA 0110:IR-TX 1000:Reserved	0001:Output 0011:UARTO-RX 0101:PWM6 0111:Reserved 1001:Reserved
15:12	R/W	0xF	PF3_SELECT PF3 Select 0000:Input 0010:SDC0-CMD 0100:R-JTAG-DO 0110:Reserved 1000:Reserved 1110:PF-EINT3	1111:IO Disable  0001:Output 0011:JTAG-DO 0101:I2S2-BCLK 0111:Reserved 1001:Reserved 1111:IO Disable
11:8	R/W	OxF	PF2_SELECT PF2 Select 0000:Input 0010:SDC0-CLK 0100:TWI0-SCK 0110:OWA-IN 1000:Reserved 1110:PF-EINT2	0001:Output 0011:UART0-TX 0101:LEDC-DO 0111:Reserved 1001:Reserved 1111:IO Disable
7:4	R/W	0xF	PF1_SELECT PF1 Select 0000:Input 0010:SDC0-D0 0100:R-JTAG-DI 0110:I2S2-DIN1 1000:Reserved 1110:PF-EINT1	0001:Output 0011:JTAG-DI 0101:I2S2-DOUT0 0111:Reserved 1001:Reserved 1111:IO Disable



Offset: 0x00F0		Register Name: PF_CFG0		
Bit	Read/Write	Default/Hex	Description	
			PF0_SELECT	
			PF0 Select	
	D/M	OxF	0000:Input	0001:Output
2.0			0010:SDC0-D1	0011:JTAG-MS
3:0	R/W		0100:R-JTAG-MS	0101:I2S2-DOUT1
			0110:I2S2-DIN0	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PF-EINT0	1111:IO Disable

#### 1.1.5.27 0x0100 PF Data Register (Default Value: 0x0000\_0000)

Offset: 0x0100			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	1	/	1
			PF_DAT
			PF Data
		1	If the port is configured as input, the corresponding bit is the pin
6:0	R/W	0	state. If the port is configured as output, the pin state is the same
			as the corresponding bit. The read bit value is the value setup by
			software. If the port is configured as functional pin, the
			undefined value will be read.

#### 1.1.5.28 0x0104 PF Multi\_Driving Register 0 (Default Value: 0x0111\_1111)

Offset: 0x0104		Register Name: PF_DRV0		
Bit	Read/Write	Default/Hex	Description	
31:26	/	/	/	
			PF6_DRV	
25:24	R/W	0.4	PF6 Multi_Driving Select	
25.24	K/VV	0x1	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	/	/	/	



Offset: 0x0104			Register Name: PF_DRV0	
Bit	Read/Write	Default/Hex	Description	
21:20	R/W	0x1	PF5_DRV PF5 Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3
19:18	/	/	1	5
17:16	R/W	0x1	PF4_DRV PF4 Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3
15:14	/	1	1	
13:12	R/W	0x1	PF3_DRV PF3 Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3
11:10	1	1	/	
9:8	R/W	0x1	PF2_DRV PF2 Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3
7:6	1	1	1	
5:4	R/W	0x1	PF1_DRV PF1 Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3
3:2	/	1	1	
1:0	R/W	0x1	PFO_DRV PFO Multi_Driving Select 00: Level 0 10: Level 2	01: Level 1 11: Level 3

#### 1.1.5.29 0x0114 PF Pull Register 0 (Default Value: 0x0000\_0000)

Offset: 0	Offset: 0x0114		Register Name: PF_PULL0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/



Offset: 0	x0114		Register Name: PF_PULL0	
Bit	Read/Write	Default/Hex	Description	
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select 00: Pull_up/down disable 10: Pull_down	01: Pull_up 11: Reserved



#### 1.1.5.30 0x0120 PG Configure Register 0 (Default Value: 0xFFFF\_FFFF)

Offset: 0	x0120		Register Name: PG_CFG0	
Bit	Read/Write	Default/Hex	Description	
			PG7_SELECT	
			PG7 Select	
			0000:Input	0001:Output
21.20	R/W	OvE	0010:UART1-RX	0011:TWI2-SDA
31:28	K/W	0xF	0100:RGMII-TXD3	0101:OWA-IN
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PG-EINT7	1111:IO Disable
			PG6_SELECT	
			PG6 Select	40
			0000:Input	0001:Output
27:24	DAM	OvE	0010:UART1-TX	0011:TWI2-SCK
27:24	R/W	0xF	0100:RGMII-TXD2	0101:PWM1
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PG-EINT6	1111:IO Disable
			PG5_SELECT	
			PG5 Select	
			0000:Input	0001:Output
23:20	R/W	Ove	0010:SDC1-D3	0011:UART5-RX
23.20	Tty VV	0xF	0100:RGMII-TXD1/RMII-TXD1	0101:PWM4
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PG-EINT5	1111:IO Disable
			PG4_SELECT	
			PG4 Select	
19:16 R/\			0000:Input	0001:Output
	D /\A/	0xF	0010:SDC1-D2	0011:UART5-TX
	R/W	UXI	0100:RGMII-TXD0/RMII-TXD0	0101:PWM5
			0110:Reserved	0111:Reserved
			1000:Reserved	1001:Reserved
			1110:PG-EINT4	1111:IO Disable



Offset: 0	x0120		Register Name: PG_CFG0		
Bit	Read/Write	Default/Hex	Description		
15:12	R/W	OxF	0010:SDC1-D1	0001:Output 0011:UART3-CTS 0101:UART4-RX 0111:Reserved 1001:Reserved	
11:8	R/W	OxF	PG2_SELECT PG2 Select 0000:Input 0010:SDC1-D0 0100:RGMII-RXD1/RMII-RXD1 0110:Reserved 1000:Reserved 1110:PG-EINT2 PG1_SELECT PG1 Select	1111:IO Disable  0001:Output 0011:UART3-RTS 0101:UART4-TX 0111:Reserved 1001:Reserved 1111:IO Disable	
7:4	R/W	OxF	0000:Input 0010:SDC1-CMD 0100:RGMII-RXD0/RMII-RXD0 0110:Reserved 1000:Reserved 1110:PG-EINT1	0001:Output 0011:UART3-RX 0101:PWM6 0111:Reserved 1001:Reserved 1111:IO Disable	
3:0	R/W	OxF	PG0_SELECT PG0 Select 0000:Input 0010:SDC1-CLK 0100:RGMII-RXCTRL/RMII-CRS-DN 0110:Reserved 1000:Reserved 1110:PG-EINT0	0001:Output 0011:UART3-TX / 0101:PWM7 0111:Reserved 1001:Reserved 1111:IO Disable	



#### 1.1.5.31 0x0124 PG Configure Register 1 (Default Value: 0xFFFF\_FFFF)

Offset: 0	Offset: 0x0124		Register Name: PG_CFG1	
Bit	Read/Write	Default/Hex	Description	
			PG15_SELECT	
			PG15 Select	
			0000:Input	0001:Output
31:28	R/W	0xF	0010:I2S1-DOUT0	0011:TWI2-SDA
31.20	r/vv	UXF	0100:MDIO	0101:I2S1-DIN1
			0110:SPI0-HOLD	0111:UART1-CTS
			1000:Reserved	1001:Reserved
			1110:PG-EINT15	1111:IO Disable
			PG14_SELECT	
			PG14 Select	40
			0000:Input	0001:Output
27:24	D/M	OvE	0010:I2S1-DIN0	0011:TWI2-SCK
27:24	R/W	0xF	0100:MDC	0101:I2S1-DOUT1
			0110:SPI0-WP	0111:UART1-RTS
			1000:Reserved	1001:Reserved
			1110:PG-EINT14	1111:IO Disable
		0xF	PG13_SELECT	
			PG13 Select.	
			0000:Input	0001:Output
23:20	R/W		0010:I2S1-BCLK	0011:TWI0-SDA
23.20	N/ VV	UXF	0100:RGMII-CLKIN/RMII-RXER	0101:PWM2
			0110:LEDC-DO	0111:UART1_RX
			1000:Reserved	1001:Reserved
			1110:PG-EINT13	1111:IO Disable
			PG12_SELECT	
			PG12 Select	
19:16 R/W			0000:Input	0001:Output
	D /\A/	OvE	0010:I2S1-LRCK	0011:TWI0-SCK
	r/ vv	W 0xF	0100:RGMII-TXCTRL/RMII-TXEN	N 0101:CLK-FANOUT2
			0110:PWM0	0111:UART1-TX
			1000:Reserved	1001:Reserved
			1110:PG-EINT12	1111:IO Disable



Offset: 0	Offset: 0x0124		Register Name: PG_CFG1	
Bit	Read/Write	Default/Hex	Description	
15:12	R/W	OxF	PG11_SELECT PG11 Select 0000:Input 0010:I2S1-MCLK	0001:Output 0011:TWI3-SDA
		•	0100:EPHY-25M 0110:TCON-TRIG 1000:Reserved 1110:PG-EINT11	0101:CLK-FANOUT1 0111:Reserved 1001:Reserved 1111:IO Disable
11:8	R/W	OxF	PG10_SELECT PG10 Select 0000:Input 0010:PWM3 0100:RGMII-RXCK 0110:IR-RX 1000:Reserved 1110:PG-EINT10	0001:Output 0011:TWI3-SCK 0101:CLK-FANOUT0 0111:Reserved 1001:Reserved 1111:IO Disable
7:4	R/W	OxF	PG9_SELECT PG9 Select. 0000:Input 0010:UART1-CTS 0100:RGMII-RXD3 0110:Reserved 1000:Reserved 1110:PG-EINT9	0001:Output 0011:TWI1-SDA 0101:UART3-RX 0111:Reserved 1001:Reserved 1111:IO Disable
3:0	R/W	OxF	PG8_SELECT PG8 Select 0000:Input 0010:UART1-RTS 0100:RGMII-RXD2 0110:Reserved 1000:Reserved 1110:PG-EINT8	0001:Output 0011:TWI1-SCK 0101:UART3-TX 0111:Reserved 1001:Reserved 1111:IO Disable



#### 1.1.5.32 0x0130 PG Data Register (Default Value: 0x0000\_0000)

Offset: 0	Offset: 0x0130		Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	1
15:0	R/W	0x0	PG_DAT  If the port is configured as the input function, the corresponding bit is the pin state. If the port is configured as the output function, the pin state is the same as the corresponding bit. The read bit value is the value set up by software. If the port is configured as a functional pin, the undefined value will be read.

#### 1.1.5.33 0x0134 PG Multi\_Driving Register 0 (Default Value: 0x1111\_1111)

Offset: 0	(0134		Register Name: PG_DRV0	
Bit	Read/Write	Default/Hex	Description	
31:30	1	1	/	
			PG7_DRV	
29:28	R/W	0x1	PG7 Multi_Driving Select	
29.20	K/VV	UXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
27:26	/	1	1	
			PG6_DRV	
25:24	R/W	0x1	PG6 Multi_Driving Select	
23.24	IV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	1	1	1	
			PG5_DRV	
21:20	R/W	0x1	PG5 Multi_Driving Select	
21.20	IV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
19:18	/	1	1	
			PG4_DRV	
17:16	17:16 R/W	0x1	PG4 Multi_Driving Select	
17.10	IV VV	OVI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
15:14	/	/	1	



Offset: 0	Offset: 0x0134		Register Name: PG_DRV0	
Bit	Read/Write	Default/Hex	Description	
			PG3_DRV	
13:12	R/W	0x1	PG3 Multi_Driving Select	
15.12	11,7 4	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
11:10	/	/	1	51
			PG2_DRV	
9:8	R/W	0x1	PG2 Multi_Driving Select	
9.8	IV VV	UXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
7:6	1	1	1	
			PG1_DRV	
5:4	R/W	0x1	PG1 Multi_Driving Select	
3.4	II, W	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
3:2	1	1	1	
			PG0_DRV	
1:0	R/W	0v1	PG0 Multi_Driving Select	
1.0	17, 00	0x1	00: Level 0	01: Level 1
			10: Level 2	11: Level 3

# 1.1.5.34 0x0138 PG Multi\_Driving Register 1 (Default Value: 0x1111\_1111)

Offset: 0	Offset: 0x0138		Register Name: PG_DRV1	
Bit	Read/Write	Default/Hex	Description	
31:30	1	1	1	
			PG15_DRV	
29:28	R/W	0x1	PG15 Multi_Driving Select	
29.20	29:28 K/W	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
27:26	/	/	1	
		0x1	PG14_DRV	
25:24	R/W		PG14 Multi_Driving Select	
23.24 N/W	IV VV		00: Level 0	01: Level 1
			10: Level 2	11: Level 3
23:22	/	/	1	



Offset: 0x	<b>(0138</b>		Register Name: PG_DRV1	
Bit	Read/Write	Default/Hex	Description	
			PG13_DRV	
21:20	R/W	0x1	PG13 Multi_Driving Select	
21.20	IV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
19:18	/	/	1	51
			PG12_DRV	
17:16	R/W	0x1	PG12 Multi_Driving Select	
17.10	TV VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
15:14	/	1	1	
			PG11_DRV	
13:12	R/W	0x1	PG11 Multi_Driving Select	
13.12	IN, VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
11:10	1	1	1	
			PG10_DRV	
9:8	R/W	0x1	PG10 Multi_Driving Select	
5.6	11,11	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
7:6	/	1	1	
			PG9_DRV	
5:4	R/W	0x1	PG9 Multi_Driving Select	
3.4	.4 N/ VV	OXI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3
3:2	/	1	1	
			PG8_DRV	
1:0	R/W	0x1	PG8 Multi_Driving Select	
1.0	11/ VV	OVI	00: Level 0	01: Level 1
			10: Level 2	11: Level 3



#### 1.1.5.35 0x0144 PG Pull Register 0 (Default Value: 0x0000\_0000)

Offset: 0x	Offset: 0x0144		Register Name: PG_PULL0	
Bit	Read/Write	Default/Hex	Description	
			PG15_PULL	
31:30	R/W	0x0	PG15 Pull_up or down Select	t.
31.30	I N/ VV	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG14_PULL	
29:28	R/W	0x0	PG14 Pull_up or down Select	t.
29.20	IN/ VV	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG13_PULL	
27:26	R/W	0x0	PG13 Pull_up or down Select	
27.20	K/ VV	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
		W 0x0	PG12_PULL	
25:24	25:24 R/W		PG12 Pull_up or down Select	
25.24	IV, VV		00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
		W. I	PG11_PULL	
23:22	R/W	0x0	PG11 Pull_up or down Select	t.
23.22	1,7 00	0.00	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG10_PULL	
21:20	R/W	0x0	PG10 Pull_up or down Select	t.
21.20	1,7 00	ONG	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG9_PULL	
19:18 R/W	R/W	0x0	PG9 Pull_up or down Select.	
13.10	1,7 00	ONO	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG8_PULL	
17:16	R/W	0x0	PG8 Pull_up or down Select.	
17.10	K/VV	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved



Offset: 0x	<b>k</b> 0144		Register Name: PG_PULL0	
Bit	Read/Write	Default/Hex	Description	
			PG7_PULL	
15.14	D /\A/	00	PG7 Pull_up or down Select.	
15:14	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG6_PULL	91
12.12	D /\A/	00	PG6 Pull_up or down Select.	
13:12	R/W	0x0	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG5_PULL	
11.10	D //A/	0x0	PG5 Pull_up or down Select.	
11:10	R/W	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG4_PULL	
9:8	R/W	0x0	PG4 Pull_up or down Select.	
9.8	K) VV		00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
		0x0	PG3_PULL	
7:6	R/W		PG3 Pull_up or down Select.	
7.0	IV, VV		00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG2_PULL	
5:4	R/W	0x0	PG2 Pull_up or down Select.	
3.4	Tty VV	0.00	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
	3:2 R/W		PG1_PULL	
3:2		0x0	PG1 Pull_up or down Select.	
3.2	Tty VV	UXU	00: Pull_up/down disable	01: Pull_up
			10: Pull_down	11: Reserved
			PG0_PULL	
1:0	R/W	0x0	PG0 Pull_up or down Select.	
1.0	11/ VV	UXU	00: Pull_up/down disable	01: Pull_up
		10: Pull_down	11: Reserved	



#### 1.1.5.36 0x0220 PB External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x02	20		Register Name:PB_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT7_CFG
			External INT7 Mode
			0x0: Positive Edge
31:28	R/W	0x0	0x1: Negative Edge
31.20	IN VV	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT6_CFG
			External INT6 Mode
			0x0: Positive Edge
27:24	R/W	0x0	0x1: Negative Edge
27.24	R/W	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
		4	Others: Reserved
			EINT5_CFG
			External INT5 Mode
			0x0: Positive Edge
23:20	R/W	0x0	0x1: Negative Edge
25.20	11,7 17	OAG /	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT4_CFG
			External INT4 Mode
19:16			0x0: Positive Edge
	R/W	0x0	0x1: Negative Edge
13.10	1,7 00	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x02	Offset: 0x0220		Register Name:PB_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT3_CFG
			External INT3 Mode
			0x0: Positive Edge
15:12	R/W	0x0	0x1: Negative Edge
13.12	I I V V V	0.00	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT2_CFG
			External INT2 Mode
	_7		0x0: Positive Edge
11:8	R/W	0x0	0x1: Negative Edge
11.0	II, VV	0.00	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	Reserved

#### 1.1.5.37 0x0230 PB External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x	Offset: 0x0230		Register Name: PB_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	1	/
			EINT7_CTL
7	R/W	0x0	External INT7 Enable
'	/ K/VV		0: Disable
			1: Enable
	6 R/W 0x0	0.0	EINT6_CTL
6			External INT6 Enable
6 K/VV	0x0	0: Disable	
			1: Enable



Offset: 0x	0230		Register Name: PB_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT5_CTL
5	R/W	0x0	External INT5 Enable
3	IV VV	OXO	0: Disable
			1: Enable
			EINT4_CTL
4	R/W	0x0	External INT4 Enable
4	r/vv	UXU	0: Disable
			1: Enable
			EINT3_CTL
3	R/W	0x0	External INT3 Enable
3	K/VV	OXU	0: Disable
			1: Enable
			EINT2_CTL
2	R/W	0x0	External INT2 Enable
2	K/VV	UXU	0: Disable
			1: Enable
1	R/W	0x0	Reserved
0	R/W	0x0	Reserved

#### 1.1.5.38 0x0234 PB External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0x0234			Register Name: PB_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
31:8	/	1	/
			EINT7_STATUS
			External INT7 Pending Bit
7	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT6_STATUS
			External INT6 Pending Bit
6	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	0234		Register Name: PB_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT5_STATUS
			External INT5 Pending Bit
5	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT4_STATUS
			External INT4 Pending Bit
4	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT3_STATUS
			External INT3 Pending Bit
3	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT2_STATUS
		4	External INT2 Pending Bit
2	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
1	R/W	0x0	Reserved
0	R/W	0x0	Reserved

## 1.1.5.39 0x0238 PB External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x0238			Register Name: PB_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
			DEB_CLK_PRE_SCALE
6:4	R/W	0x0	Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	/	/	/



Offset: 0x0238			Register Name: PB_EINT_DEB
Bit	Read/Write	Default/Hex	Description
	R/W	0x0	PIO_INT_CLK_SELECT
			PIO Interrupt Clock Select
			0: LOSC 32KHz
			1: HOSC 24MHz

## 1.1.5.40 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x02	40	1	Register Name:PC_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT7_CFG
			External INT7 Mode
V			0x0: Positive Edge
31:28	D /\A/	0.0	0x1: Negative Edge
31:28	R/W	0x0	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
		- 1	Others: Reserved
			EINT6_CFG
			External INT6 Mode
		0x0	0x0: Positive Edge
27:24	D /\A/		0x1: Negative Edge
27.24	R/W		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT5_CFG
			External INT5 Mode
			0x0: Positive Edge
23:20	D /\A/	0x0	0x1: Negative Edge
23.20	R/W	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x02	40		Register Name:PC_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG  External INT4 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	Reserved

## 1.1.5.41 0x0250 PC External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x0250			Register Name: PC_EINT_CTL
Bit	Bit Read/Write Default/Hex		Description
31:8	/	/	/



Offset: 0x	0250		Register Name: PC_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT7_CTL
7	D /\A/	00	External INT7 Enable
7	R/W	0x0	0: Disable
			1: Enable
			EINT6_CTL
C	R/W	0.40	External INT6 Enable
6	K/VV	0x0	0: Disable
			1: Enable
			EINT5_CTL
5	R/W	0x0	External INT5 Enable
5	N/ VV	UXU	0: Disable
			1: Enable
			EINT4_CTL
4	R/W	0x0	External INT4 Enable
7	Ty VV	OAO	0: Disable
			1: Enable
			EINT3_CTL
3	R/W	0x0	External INT3 Enable
	11,700	OAO	0: Disable
			1: Enable
			EINT2_CTL
2	R/W	0x0	External INT2 Enable
	.,, ••		0: Disable
			1: Enable
1	R/W	0x0	Reserved
0	R/W	0x0	Reserved

## 1.1.5.42 0x0254 PC External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0x0254			Register Name: PC_EINT_STATUS
Bit Read/Write Default/Hex		Default/Hex	Description
31:8	/	/	/



Offset: 0x	0254		Register Name: PC_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT7_STATUS
			External INT7 Pending Bit
7	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT6_STATUS
			External INT6 Pending Bit
6	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT5_STATUS
			External INT5 Pending Bit
5	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT4_STATUS
			External INT4 Pending Bit
4	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT3_STATUS
			External INT3 Pending Bit
3	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT2_STATUS
			External INT2 Pending Bit
2	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
1	R/W	0x0	Reserved
0	R/W	0x0	Reserved



#### 1.1.5.43 0x0258 PC External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x0258			Register Name: PC_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	1	1
		0x0	DEB_CLK_PRE_SCALE
6:4	R/W		Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	/	1	1
	R/W	0x0	PIO_INT_CLK_SELECT
0			PIO Interrupt Clock Select
U			0: LOSC 32KHz
			1: HOSC 24MHz

## 1.1.5.44 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x0260			Register Name:PD_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
	R/W	0x0	EINT7_CFG
			External INT7 Mode
			0x0: Positive Edge
21.20			0x1: Negative Edge
31:28			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT6_CFG
	R/W	0x0	External INT6 Mode
			0x0: Positive Edge
27:24			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x0260			Register Name:PD_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT5_CFG External INT5 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved  EINT3_CFG External INT3 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
11:8	R/W	0x0	EINT2_CFG  External INT2 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved



Offset: 0x0260			Register Name:PD_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
	R/W	0x0	EINT1_CFG
			External INT1 Mode
			0x0: Positive Edge
7:4			0x1: Negative Edge
7.4			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
	R/W		EINTO_CFG
3:0			External INTO Mode
		0x0	0x0: Positive Edge
			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

# 1.1.5.45 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000\_0000)

Offset: 0x0264			Register Name:PD_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG
			External INT15 Mode
			0x0: Positive Edge
			0x1: Negative Edge
		UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x0264			Register Name:PD_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
			EINT14_CFG
			External INT14 Mode
		0x0	0x0: Positive Edge
27:24	R/W		0x1: Negative Edge
27.24			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT13_CFG
			External INT13 Mode
			0x0: Positive Edge
23:20	R/W	0х0	0x1: Negative Edge
23.20	I, W		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
		4	EINT12_CFG
	R/W	0x0	External INT12 Mode
			0x0: Positive Edge
19:16			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT11_CFG
15:12	R/W	0x0	External INT11 Mode
			0x0: Positive Edge
			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0	x0264		Register Name:PD_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
			EINT10_CFG
			External INT10 Mode
			0x0: Positive Edge
11:8	R/W	0x0	0x1: Negative Edge
11.0	K) VV	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
		- 10	EINT9_CFG
	R/W	0x0	External INT9 Mode
			0x0: Positive Edge
7:4			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
		4	EINT8_CFG
		4	External INT8 Mode
			0x0: Positive Edge
3:0	R/W	0x0	0x1: Negative Edge
3.0	.,	O.KO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

## 1.1.5.46 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000\_0000)

Offset: 0x0268			Register Name:PD_EINT_CFG2
Bit	Read/Write Default/Hex		Description
31:28	/	/	/



Offset: 0	x0268		Register Name:PD_EINT_CFG2
Bit	Read/Write	Default/Hex	Description
			EINT22_CFG
			External INT22 Mode
			0x0: Positive Edge
27:24	D /\A/	0.40	0x1: Negative Edge
27:24	R/W	0x0	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT21_CFG
			External INT21 Mode
			0x0: Positive Edge
23:20	R/W	0x0	0x1: Negative Edge
23.20	IN, W	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
		4	EINT20_CFG
		1	External INT20 Mode
			0x0: Positive Edge
19:16	R/W	0x0	0x1: Negative Edge
13.120	.,,	ONO .	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT19_CFG
			External INT19 Mode
			0x0: Positive Edge
15:12	R/W	0x0	0x1: Negative Edge
	,		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0	x0268		Register Name:PD_EINT_CFG2
Bit	Read/Write	Default/Hex	Description
			EINT18_CFG
			External INT18 Mode
			0x0: Positive Edge
11:8	R/W	0x0	0x1: Negative Edge
11:8	K/ W	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT17_CFG
	R/W	0x0	External INT17 Mode
			0x0: Positive Edge
7:4			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
		4	EINT16_CFG
		4	External INT16 Mode
		0x0	0x0: Positive Edge
3:0	R/W		0x1: Negative Edge
3.0	.,	O.KO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

## 1.1.5.47 0x0270 PD External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x0270			Register Name: PD_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
	R/W	0x0	EINT22_CTL
22			External INT22 Enable
22			0: Disable
			1: Enable



Offset: 0x	0270		Register Name: PD_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT21_CTL
21	R/W	0x0	External INT21 Enable
21	K/VV	UXU	0: Disable
			1: Enable
			EINT20_CTL
20	R/W	0x0	External INT20 Enable
20	1,700	OXO	0: Disable
			1: Enable
			EINT19_CTL
19	R/W	0x0	External INT19 Enable
	.,		0: Disable
			1: Enable
- V			EINT18_CTL
18	R/W	0x0	External INT18 Enable
			0: Disable
			1: Enable
			EINT17_CTL
17	R/W	0x0	External INT17 Enable
			0: Disable
			1: Enable
			EINT16_CTL
16	R/W	0x0	External INT16 Enable
			0: Disable
			1: Enable
			EINT15_CTL
15	R/W	0x0	External INT15 Enable
			0: Disable
			1: Enable
			EINT14_CTL
14	R/W	0x0	External INT14 Enable
			0: Disable
			1: Enable
	R/W		EINT13_CTL  External INT13 Enable
13		0x0	External INT13 Enable
			0: Disable
			1: Enable



Offset: 0x	:0270		Register Name: PD_EINT_CTL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL  External INT10 Enable  0: Disable  1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable



Offset: 0x	0270		Register Name: PD_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT3_CTL
3	R/W	0x0	External INT3 Enable
3	IV VV	OXO	0: Disable
			1: Enable
			EINT2_CTL
2	R/W	0x0	External INT2 Enable
2			0: Disable
			1: Enable
			EINT1_CTL
1	R/W	0x0	External INT1 Enable
1			0: Disable
			1: Enable
N			EINTO_CTL
0	R/W	0x0	External INTO Enable
	ry vv	UXU	0: Disable
			1: Enable

### 1.1.5.48 0x0274 PD External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0x0274			Register Name: PD_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
			EINT22_STATUS
			External INT22 Pending Bit
22	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT21_STATUS
			External INT21 Pending Bit
21	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	0274		Register Name: PD_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT20_STATUS
			External INT20 Pending Bit
20	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT19_STATUS
			External INT19 Pending Bit
19	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT18_STATUS
			External INT18 Pending Bit
18	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT17_STATUS
			External INT17 Pending Bit
17	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT16_STATUS
			External INT16 Pending Bit
16	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT15_STATUS
			External INT15 Pending Bit
15	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT14_STATUS
			External INT14 Pending Bit
14	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	0274		Register Name: PD_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT13_STATUS
			External INT13 Pending Bit
13	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT12_STATUS
			External INT12 Pending Bit
12	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT11_STATUS
			External INT11 Pending Bit
11	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT10_STATUS
			External INT10 Pending Bit
10	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT9_STATUS
			External INT9 Pending Bit
9	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT8_STATUS
			External INT8 Pending Bit
8	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT7_STATUS
			External INT7 Pending Bit
7	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	0274		Register Name: PD_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT6_STATUS
			External INT6 Pending Bit
6	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT5_STATUS
			External INT5 Pending Bit
5	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT4_STATUS
			External INT4 Pending Bit
4	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT3_STATUS
			External INT3 Pending Bit
3	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT2_STATUS
			External INT2 Pending Bit
2	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT1_STATUS
			External INT1 Pending Bit
1	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINTO_STATUS
			External INTO Pending Bit
0	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



#### 1.1.5.49 0x0278 PD External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x0278			Register Name: PD_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	1
			DEB_CLK_PRE_SCALE
6:4	R/W	0x0	Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	/	1	1
	R/W	0x0	PIO_INT_CLK_SELECT
0			PIO Interrupt Clock Select
			0: LOSC 32KHz
			1: HOSC 24MHz

### 1.1.5.50 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x0280			Register Name:PE_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT7_CFG
			External INT7 Mode
			0x0: Positive Edge
31:28	R/W	0x0	0x1: Negative Edge
31.28	IV, VV	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT6_CFG
	R/W	0x0	External INT6 Mode
			0x0: Positive Edge
27:24			0x1: Negative Edge
27.24			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x02	80		Register Name:PE_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT5_CFG
			External INT5 Mode
			0x0: Positive Edge
23:20	R/W	0x0	0x1: Negative Edge
23.20	K/ VV	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT4_CFG
			External INT4 Mode
	-7		0x0: Positive Edge
19:16	R/W	0x0	0x1: Negative Edge
19.10	R/W		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT3_CFG
		4	External INT3 Mode
	R/W	0x0	0x0: Positive Edge
15:12			0x1: Negative Edge
13.12			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT2_CFG
			External INT2 Mode
			0x0: Positive Edge
11:8	R/W	0x0	0x1: Negative Edge
	I I V V V	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x0280			Register Name:PE_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT1_CFG
			External INT1 Mode
			0x0: Positive Edge
7:4	R/W	0x0	0x1: Negative Edge
7.4	I IV VV	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINTO_CFG
	R/W		External INTO Mode
			0x0: Positive Edge
3:0		0x0	0x1: Negative Edge
3.0			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

## 1.1.5.51 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000\_0000)

Offset: 0x0284			Register Name: PE_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	Reserved
27:24	R/W	0x0	Reserved
			EINT13_CFG
	R/W	0x0	External INT13 Mode
			0x0: Positive Edge
23:20			0x1: Negative Edge
23.20			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x02	84		Register Name: PE_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
			EINT12_CFG
			External INT12 Mode
			0x0: Positive Edge
19:16	R/W	0x0	0x1: Negative Edge
19:16	K/VV	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT11_CFG
			External INT11 Mode
	-7		0x0: Positive Edge
15:12	R/W	0x0	0x1: Negative Edge
13.12	R/W		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT10_CFG
	R/W	0x0	External INT10 Mode
			0x0: Positive Edge
11:8			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT9_CFG
			External INT9 Mode
	R/W	0x0	0x0: Positive Edge
7:4			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x0284			Register Name: PE_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
			EINT8_CFG
			External INT8 Mode
			0x0: Positive Edge
3:0	R/W	0x0	0x1: Negative Edge
	R/ VV		0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

#### 1.1.5.52 0x0290 PE External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x0290			Register Name: PE_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:14	1	1	/
			EINT13_CTL
13	R/W	0x0	External INT13 Enable
	.,,		0: Disable
			1: Enable
			EINT12_CTL
12	R/W	0x0	External INT12 Enable
	1,717	ONO	0: Disable
			1: Enable
		0x0	EINT11_CTL
11	R/W		External INT11 Enable
11	11,7 17		0: Disable
			1: Enable
			EINT10_CTL
10	R/W	0x0	External INT10 Enable
10	IV VV	UXU	0: Disable
			1: Enable
			EINT9_CTL
9	R/W	00	External INT9 Enable
9		0x0	0: Disable
			1: Enable



Offset: 0x	0290		Register Name: PE_EINT_CTL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL  External INT6 Enable  0: Disable  1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL  External INT1 Enable  0: Disable  1: Enable
0	R/W	0x0	EINTO_CTL External INTO Enable 0: Disable 1: Enable



#### 1.1.5.53 0x0294 PE External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0	k0294		Register Name: PE_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
31:14	/	/	1
			EINT13_STATUS
			External INT13 Pending Bit
13	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT12_STATUS
			External INT12 Pending Bit
12	R/W1C	0x0	0: No IRQ pending
		,	1: IRQ pending
			Write '1' to clear
			EINT11_STATUS
			External INT11 Pending Bit
11	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT10_STATUS
			External INT10 Pending Bit
10	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT9_STATUS
			External INT9 Pending Bit
9	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT8_STATUS
			External INT8 Pending Bit
8	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	0294		Register Name: PE_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT7_STATUS
			External INT7 Pending Bit
7	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT6_STATUS
			External INT6 Pending Bit
6	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT5_STATUS
			External INT5 Pending Bit
5	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT4_STATUS
		4	External INT4 Pending Bit
4	R/W1C	0x0	0: No IRQ pending
		W. I	1: IRQ pending
			Write '1' to clear
			EINT3_STATUS
			External INT3 Pending Bit
3	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT2_STATUS
			External INT2 Pending Bit
2	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT1_STATUS
			External INT1 Pending Bit
1	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x0294			Register Name: PE_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINTO_STATUS
			External INTO Pending Bit
0	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear

### 1.1.5.54 0x0298 PE External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x	0298	39	Register Name: PE_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	1	1	1
	5		DEB_CLK_PRE_SCALE
6:4	R/W	0x0	Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	1	1	/
			PIO_INT_CLK_SELECT
0	R/W	0x0	PIO Interrupt Clock Select
0			0: LOSC 32KHz
			1: HOSC 24MHz

#### 1.1.5.55 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
			EINT6_CFG
	R/W	0x0	External INT6 Mode
			0x0: Positive Edge
27:24			0x1: Negative Edge
27.24			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x	02A0		Register Name: PF_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT5_CFG  External INT5 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
19:16	R/W	0x0 0x0	EINT4_CFG External INT4 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved  EINT3_CFG External INT3 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved



Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT1_CFG
			External INT1 Mode
			0x0: Positive Edge
7:4	R/W	0x0	0x1: Negative Edge
7.4	N/ VV	OXO	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINTO_CFG
	R/W	0x0	External INTO Mode
			0x0: Positive Edge
2.0			0x1: Negative Edge
3:0			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

# 1.1.5.56 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:7	1	1	/
			EINT6_CTL
6	R/W	0.0	External INT6 Enable
0	N/ VV	0x0	0: Disable
			1: Enable
			EINT5_CTL
5	R/W	0x0	External INT5 Enable
3	R/W	OXO	0: Disable
			1: Enable
	R/W	0x0	EINT4_CTL
4			External INT4 Enable
			0: Disable
			1: Enable



Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT3_CTL
3	R/W	0x0	External INT3 Enable
3	IN/ VV	OXO	0: Disable
			1: Enable
			EINT2_CTL
2	R/W	0x0	External INT2 Enable
2	K/VV	UXU	0: Disable
			1: Enable
			EINT1_CTL
1	R/W	0x0	External INT1 Enable
1	N/ VV	OXU	0: Disable
			1: Enable
			EINTO_CTL
	R/W	0x0	External INTO Enable
0	Try VV	UXU	0: Disable
			1: Enable

### 1.1.5.57 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
31:7	1	/	/
			EINT6_STATUS
			External INT6 Pending Bit
6	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT5_STATUS
			External INT5 Pending Bit
5	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	02B4		Register Name: PF_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT4_STATUS
	5 /114 6		External INT4 Pending Bit
4	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT3_STATUS
			External INT3 Pending Bit
3	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT2_STATUS
			External INT2 Pending Bit
2	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT1_STATUS
			External INT1 Pending Bit
1	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINTO_STATUS
			External INTO Pending Bit
0	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear

### 1.1.5.58 0x02B8 PF External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
			DEB_CLK_PRE_SCALE
6:4	R/W	0x0	Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	/	/	/



Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	Read/Write	Default/Hex	Description
	R/W	0x0	PIO_INT_CLK_SELECT
			PIO Interrupt Clock Select
			0: LOSC 32KHz
			1: HOSC 24MHz

## 1.1.5.59 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000\_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINT7_CFG
			External INT7 Mode
N			0x0: Positive Edge
31:28	R/W	0x0	0x1: Negative Edge
31.28	N/ VV	UXU	0x2: High Level
			0x3: Low Level
		4	0x4: Double Edge (Positive/Negative)
		1	Others: Reserved
			EINT6_CFG
		0x0	External INT6 Mode
			0x0: Positive Edge
27:24	D // /		0x1: Negative Edge
27.24	R/W		0x2: High Level
W.			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT5_CFG
			External INT5 Mode
			0x0: Positive Edge
23:20	R/W	0x0	0x1: Negative Edge
23.20	K/W	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved



Offset: 0x	02C0		Register Name:PG_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG  External INT4 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)
15:12	R/W	0x0	Others: Reserved  EINT3_CFG  External INT3 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
7:4	R/W	0x0	EINT1_CFG  External INT1 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved



Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
			EINTO_CFG
3:0	R/W	0x0	External INTO Mode
			0x0: Positive Edge
			0x1: Negative Edge
			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

## 1.1.5.60 0x02C4 PG External Interrupt Configure Register 1 (Default Value: 0x0000\_0000)

Offset: 0x	02C4		Register Name: PG_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG  External INT15 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
27:24	R/W	0x0	EINT14_CFG  External INT14 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved



Offset: 0x	Offset: 0x02C4		Register Name: PG_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT13_CFG  External INT13 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved
11:8	R/W	0x0	EINT10_CFG  External INT10 Mode  0x0: Positive Edge  0x1: Negative Edge  0x2: High Level  0x3: Low Level  0x4: Double Edge (Positive/Negative)  Others: Reserved



Offset: 0x	02C4		Register Name: PG_EINT_CFG1
Bit	Read/Write	Default/Hex	Description
			EINT9_CFG
			External INT9 Mode
			0x0: Positive Edge
7:4	R/W	0x0	0x1: Negative Edge
7.4	n/ vv	UXU	0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved
			EINT8_CFG
	R/W	0x0	External INT8 Mode
			0x0: Positive Edge
2.0			0x1: Negative Edge
3:0			0x2: High Level
			0x3: Low Level
			0x4: Double Edge (Positive/Negative)
			Others: Reserved

# 1.1.5.61 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000\_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:16	1	/	/
			EINT15_CTL
15	R/W	0x0	External INT15 Enable
13	N/ VV	UXU	0: Disable
			1: Enable
		0x0	EINT14_CTL
14	R/W		External INT14 Enable
14	N/ VV		0: Disable
			1: Enable
	R/W	0x0	EINT13_CTL
13			External INT13 Enable
13			0: Disable
			1: Enable



Offset: 0x	Offset: 0x02D0		Register Name: PG_EINT_CTL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable



Offset: 0x	02D0		Register Name: PG_EINT_CTL
Bit	Read/Write	Default/Hex	Description
			EINT3_CTL
3	R/W	0x0	External INT3 Enable
3	IX/ VV	OXO	0: Disable
			1: Enable
			EINT2_CTL
2	R/W	0x0	External INT2 Enable
2			0: Disable
			1: Enable
		0x0	EINT1_CTL
1	D/M		External INT1 Enable
1	R/W		0: Disable
			1: Enable
N			EINTO_CTL
0	R/W	0x0	External INTO Enable
			0: Disable
			1: Enable

## 1.1.5.62 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000\_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
31:16	1	/	/
			EINT15_STATUS
			External INT15 Pending Bit
15	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT14_STATUS
			External INT14 Pending Bit
14	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	02D4		Register Name: PG_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
			EINT13_STATUS
			External INT13 Pending Bit
13	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT12_STATUS
			External INT12 Pending Bit
12	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT11_STATUS
			External INT11 Pending Bit
11	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT10_STATUS
		4	External INT10 Pending Bit
10	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT9_STATUS
			External INT9 Pending Bit
9	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT8_STATUS
			External INT8 Pending Bit
8	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear
			EINT7_STATUS
			External INT7 Pending Bit
7	R/W1C	0x0	0: No IRQ pending
			1: IRQ pending
			Write '1' to clear



Offset: 0x	02D4		Register Name: PG_EINT_STATUS
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending
5	R/W1C	0x0	Write '1' to clear  EINT5_STATUS  External INT5 Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS  External INT2 Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS  External INT1 Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear
0	R/W1C	0x0	EINTO_STATUS  External INTO Pending Bit  0: No IRQ pending  1: IRQ pending  Write '1' to clear



#### 1.1.5.63 0x02D8 PG External Interrupt Debounce Register (Default Value: 0x0000\_0000)

Offset: 0x02D8			Register Name: PG_EINT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	1	1
			DEB_CLK_PRE_SCALE
6:4	R/W	0x0	Debounce Clock Pre_scale n
			The selected clock source is prescaled by 2 <sup>n</sup> .
3:1	/	1	1
	R/W	0x0	PIO_INT_CLK_SELECT
			PIO Interrupt Clock Select
0			0: LOSC 32KHz
			1: HOSC 24MHz

#### 1.1.5.64 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000\_0000)

When the power domain of GPIO is larger than 1.8 V, the withstand voltage is set to 3.3 V mode, the corresponding value in the 0x0340 register is set to 0.

When the power domain of GPIO is 1.8 V, the withstand voltage is set to 1.8 V mode, the corresponding value in the 0x0340 register is set to 1.

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:13	1	1	/
			VCC_IO POWER MODE Select
12	R/W	0x0	0: 3.3 V
			1: 1.8 V
11:7	1	/	/
			PG_POWER MODE Select
6	R/W	0x0	0: 3.3 V
О			1: 1.8 V
			If PG_Port Power Source selects VCC_IO, this bit is invalid.
			PF_POWER MODE Select
_	5/14/	0.0	0: 3.3 V
5	R/W	0x0	1: 1.8 V
			If PF_Port Power Source selects VCC_IO, this bit is invalid.



Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
			PE_PWR_MOD_SEL
			PE_POWER MODE Select
4	R/W	0x0	0: 3.3 V
			1: 1.8 V
			If PE_Port Power Source selects VCC_IO, this bit is invalid.
			PD_PWR_MOD_SEL
			PD_POWER MODE Select
3	R/W	0x0	0: 3.3 V
			1: 1.8 V
			If PD_Port Power Source selects VCC_IO, this bit is invalid.
			PC_PWR_MOD_SEL
			PC_POWER MODE Select
2	R/W	0x0	0: 3.3 V
			1: 1.8 V
			If PC_Port Power Source selects VCC_IO, this bit is invalid.
1:0	1	1	

#### 1.1.5.65 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000\_0000)

For 1.8 V and 3.3 V power, the withstand function is enabled by default, the corresponding bit in the 0x0344 register is set to 0.

For 2.5 V power, the withstand function is disabled, the corresponding bit in the 0x0344 register is set to 1, and the corresponding withstand voltage in the 0x0340 register needs to be set to 3.3 V.

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
31:13	1	/	/
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL
			VCC_IO Withstand Voltage Mode Select Control
			0: Enable
			1: Disable
11:7	/	1	/
6	R/W	0x0	VCC_PG_WS_VOL_MOD_SEL
			VCC_PG Withstand Voltage Mode Select Control
			0: Enable
			1: Disable



Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
-	R/W	0x0	VCC_PF_WS_VOL_MOD_SEL
			VCC_PF Withstand Voltage Mode Select Control
5			0: Enable
			1: Disable
	R/W	0x0	VCC_PE_WS_VOL_MOD_SEL
4			VCC_PE Withstand Voltage Mode Select Control
4			0: Enable
			1: Disable
	R/W	0x0	VCC_PD_WS_VOL_MOD_SEL
3			VCC_PD Withstand Voltage Mode Select Control
			0: Enable
			1: Disable
	R/W	0x0	VCC_PC_WS_VOL_MOD_SEL
2			VCC_PC Withstand Voltage Mode Select Control
			0: Enable
			1: Disable
1:0	1	/	

#### 1.1.5.66 0x0348 PIO Group Power Value Register (Default Value: 0x0000\_0000)

When the reading value of the 0x0348 register is 0, it indicates that the IO power voltage is greater than 2.5 V. When the reading value of the 0x0348 register is 1, it indicates that the IO power voltage is less than 2.0 V.

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:13	1	1	/
42	12 R	0x0	VCCIO_PWR_VAL
12			VCC_IO Power Value
11:7	/	/	/
	R	0x0	PG_PWR_VAL
6			PG_Port Power Value
			If PG_Port power source selects VCC_IO, this bit is invalid.
5	R	0x0	PF_PWR_VAL
			PF_Port Power Value
			If PF_Port power source selects VCC_IO, this bit is invalid.



Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
			PE_PWR_VAL
4	R	0x0	PE_Port Power Value
			If PE_Port power source selects VCC_IO, this bit is invalid.
			PD_PWR_VAL
3	R	0x0	PD_Port Power Value
			If PD_Port power source selects VCC_IO, this bit is invalid.
			PC_PWR_VAL
2	R	0x0	PC_Port Power Value
			If PC_Port power source selects VCC_IO, this bit is invalid.
1:0	/	1	/

## 1.1.5.67 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000\_0001)

Offset: 0x0350			Register Name: PIO_POW_VOL_SEL_CTL
Bit	Read/Write	Default/Hex	Description
31:1	1	1	
			VCC-PF Power Voltage Select Control
0	R/W	0x1	0: 1.8 V
			1: 3.3 V



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