

Dongyun Kam, Ph.D.

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RESEARCH INTEREST

Designing hardware-friendly algorithms and efficient hardware architectures for a variety of applications

- **Applications:** Large-scale DNN inference, wireless communication systems, signal processing units
- **Keywords:** VLSI architectures, digital circuits, algorithm-hardware co-optimizations, ASIC

EDUCATION

Ph.D. in Electrical Engineering

Sep. 2020 - Aug. 2024

- Pohang University of Science and Technology (POSTECH), Republic of Korea
- Advisor: Prof. Youngjoo Lee

M.S. in Electrical Engineering

Sep. 2018 - Aug. 2020

- Pohang University of Science and Technology (POSTECH), Republic of Korea
- Advisor: Prof. Youngjoo Lee

B.S. in Electrical Engineering

Mar. 2014 - Aug. 2018

- Pohang University of Science and Technology (POSTECH), Republic of Korea

WORK EXPERIENCE

Assistant Professor

Nov. 2025 - Present

UNIST, Republic of Korea

- Digital Processor & System-on-Chip (DiPS) Lab

Postdoctoral Researcher

Mar. 2025 - Oct. 2025

KAIST, Republic of Korea

- Optimizing speculative decoding for a fast LLM inference
- PI: Prof. Youngjoo Lee

Postdoctoral Researcher

Aug. 2024 - Aug. 2025

POSTECH Institute of Artificial Intelligence, Republic of Korea

- Accelerating state space machine (SSM)-based LLM models with bit-serial computations
- PI: Prof. Youngjoo Lee

Visiting Researcher

Mar. 2023 - Sep. 2023

University of Michigan, USA

- Designing energy-efficient inference accelerator design for large-scale DNN models
- Research collaboration with Prof. Zhengya Zhang

Research Assistant

Mar. 2018 - Aug. 2024

POSTECH, Republic of Korea

- Forward Error Correction (FEC) decoder design for 5G/6G communication systems
- Hardware verification and ASIC implementation with EDA tools.

Internship Program

Jan. 2017 - June 2017

Alticast, Republic of Korea

- Speech recognition-based Educational software for a set-top Box

SKILLS

- General coding: C/C++/Python/Matlab/Verilog/CUDA
- DNN frameworks: Pytorch, Huggingface, LM-Eval, TensorRT-LLM
- EDA tools: Synopsys DC, ICC, ICC2, STA, VCS, Cadence Virtuoso
- FPGA tools: Quartus (Intel FPGA), Vivado (Xilinx FPGA)

HONORS AND AWARDS

Best Paper Award, Samsung-POSTECH Research center

Aug. 2024

- Paper: "A 21.9 ns, 15.7 Gbps/mm² (128, 15) BOSS FEC decoder for 5G/6G URLLC applications"

Postdoctoral Fellowship, granted by POSTECH

Aug. 2024

POSTECHIAN Fellowship, granted by POSTECH EE	May 2024
Encouragement Award, POSTECH BK21 Four	Jan. 2024
• POSTECH EE Achievement Competition	
International Research Scholarship, granted by SNU, Korea Institute for Advancement of Technology (KIAT)	Dec. 2022
• Human Resource Development Program for Industrial Innovation	
• Supporting the collaboration with Prof. Zhengya Zhang at the University of Michigan	
IEEE SSCS Seoul Chapter Award (Best Design Award), International SoC Design Conference (ISOCC)	Oct. 2020
• Design: "Low-Latency SCL polar decoder using overlapped pruning operations"	
Special Award, 21st Korea Semiconductor Design Contest	Oct. 2020
• Design: "Noise resilient CNN accelerator with network stacking"	
Best Paper Award, Summer Annual Conference of IEIE	Aug. 2020
• Domestic Conference Paper: "Complexity Analysis of OSD Algorithm for Short Error Correction Codes"	
Student Travel Grant Award, IEEE International Symposium on Circuits and Systems (ISCAS)	May. 2019
Samsung Humantech Encouragement Paper Award, Samsung Electronics.	Feb. 2019
• Paper: "Massive MIMO systems with low-resolution ADCs: Baseband energy consumption vs. Symbol detection performance"	
Cum Laude, POSTECH EE	Aug. 2018

PUBLICATION

Journal Papers

- [1] S. Yoo, S. Hong, **Dongyun Kam**, and Y. Lee, "A Lightweight ML-Based ECG Classification System using Self-Personalized Anomaly Detector," *IEEE Journal of Biomedical and Health Informatics (JBHI)*, July 2025.
- [2] J. Kim, C. Kim, S. Yun, **Dongyun Kam**, S. Kwon, Y. Kim, and Y. Lee, "Hybrid ordered statistics decoding of short-length BCH codes for URLLC systems: Theoretical analysis and decoder implementation," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Dec. 2024. (**invited**)
- [3] J. Kim+, S. Han+, **Dongyun Kam**, B. Y. Kong, and Y. Lee, "A Design Framework for Cost-Efficient Sorters With Arbitrary Input/Output Constraints," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Dec. 2024. (**invited**)
- [4] D. Park, **Dongyun Kam**, S. Yun, J. Choe, and Y. Lee, "Hard-decision SCL polar decoder with weighted pruning operation for storage application," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, Sep. 2024.
- [5] **Dongyun Kam**, B. Y. Kong and Y. Lee, "Ultra-Low-Latency SCL Polar Decoder Architecture Using Overlapped Pruning Operations," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Mar. 2023.
- [6] C. Kim, **Dongyun Kam**, S. Kim, G. Park, and Y. Lee, "Simplified ordered statistic decoding for short-length linear block codes," *IEEE Communications Letters (CL)*, Aug. 2022.
- [7] S. Hong, **Dongyun Kam**, S. Yun, J. Choe, N. Lee, and Y. Lee, "Low-complexity and low-latency SVC decoding architecture using modified MAP-SP algorithm," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, Apr. 2022.
- [8] **Dongyun Kam**, H. Yoo, Y. Lee, "Ultra-low-latency successive cancellation polar decoding architecture using tree-level parallelism," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, June 2021.
- [9] S. Hwang, S. Moon, **Dongyun Kam**, I. Oh, Y. Lee, "High-throughput and low-latency digital baseband architecture for energy-efficient wireless VR systems," *MDPI Electronics*, July 2019.
- [10] S. Moon, I. Kim, **Dongyun Kam**, D. Jee, J. Choi, Y. Lee, "Massive MIMO systems with low-resolution ADCs: Baseband energy consumption vs. Symbol detection performance," *IEEE Access*, Jan. 2019. (**Samsung HumanTech Paper Award**)

Conference Papers

- [1] S. Yoo+, **Dongyun Kam+**, G. Park, S. Kwon, D. Lee, and Y. Lee, "LUT-SSM: A 99.3TFLOPs/W LUT-based state-space model accelerator using energy-efficient element-wise layer fusion and LUT-friendly weight-only quantization," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2026.
- [2] S. Hong, J. G. Min, J. Hyun, J. Kim, **Dongyun Kam**, E. Yoo, P. Kim, J. Yoo, H. Lee, and Y. Lee, "FPGA-based real-time ISP accelerator using low-cost line buffers and non-linear functions," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2025.
- [3] J. Oh, S. Kwon, **Dongyun Kam**, and Y. Lee, "On the hardware efficiency of short-length polarization-adjusted convolutional polar decoders," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2025.
- [4] J. Kim, C. Kim, S. Yun, **Dongyun Kam**, S. Kwon, Y. Kim, and Y. Lee, "Hybrid ordered statistics decoding of short-length BCH codes for URLLC systems: Theoretical analysis and decoder implementation," *IEEE International Symposium on Integrated Circuits and Systems (ISICAS, TCAS-I Special Issue)*, Oct. 2025.

- [5] **Dongyun Kam**, M. Yun, S. Yoo, S. Hong, Z. Zhang, and Y. Lee, "Panacea: Novel DNN accelerator using accuracy-preserving asymmetric quantization and energy-saving bit-slice sparsity," *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Mar. 2025. (**Samsung HumanTech Paper Award**)
- [6] S. Han, J. Kim, **Dongyun Kam**, B. Y. Kong, M. Kim, Y. Kim, Y. Lee, "Constrained sorter design using zero-one principle," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2024.
- [7] **Dongyun Kam**, S. Yun, J. Choe, Z. Zhang, N. Lee, Y. Lee, "A 21.9 ns, 15.7 Gbps/mm² (128, 15) BOSS FEC decoder for 5G/6G URLLC applications," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2024.
- [8] J. G. Min, **Dongyun Kam**, Y. Byun, G. Park, Y. Lee, "Energy-efficient RISC-V-based vector processor for cache-aware structurally-pruned transformers," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2023.
- [9] M. Kang, R. Hwang, J. Lee, **Dongyun Kam**, Y. Lee, M. Rhu, "GROW: A Row-Stationary Sparse-Dense GEMM Accelerator for Memory-Efficient Graph Convolutional Neural Network," *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Mar. 2023.
- [10] **Dongyun Kam**, B. Y. Kong, and Y. Lee, "A 1.1 μ s 1.56Gb/s/mm² Cost Efficient Large-List SCL Polar Decoder Using Fully-Reusable LLR Buffers in 28nm CMOS Technology," *IEEE Symposium on VLSI Technology and Circuits (VLSI)*, June 2022.
- [11] **Dongyun Kam+**, J. G. Min+, J. Yoon, S. Kim, S. Kang, and Y. Lee, "Design and evaluation frameworks for advanced RISC-based ternary processor," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Mar. 2022. (+ denotes equal contribution)
- [12] C. Kim, D. Rim, J. Choe, **Dongyun Kam**, G. Park, S. Kim, and Y. Lee, "FPGA-based ordered statistic decoding architecture for B5G/6G URLLC IIOT networks," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, Nov. 2021.
- [13] **Dongyun Kam**, B. Kong, Y. Lee, "Low-latency polar decoder using overlapped SCL processing," *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, June 2021.
- [14] S. Yun, **Dongyun Kam**, J. Choi, B. Kong, Y. Lee, "Ultra-low-latency LDPC decoding architecture using reweighted offset min-sum algorithm," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Oct. 2020.
- [15] **Dongyun Kam**, Y. Lee, "Ultra-low-latency parallel SC polar decoding architecture for 5G wireless communications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019. (**IEEE CASS Student Travel Grant Award**)

International Patents

- [1] Jemin Lee, Youngjoo Lee, and **Dongyun Kam**, "Multi-bit partial sum network device for parallel SC decoder," PCT/KR2019/017108.
- [2] Jemin Lee, Youngjoo Lee, and **Dongyun Kam**, "Polar codes decoding device and method thereof," PCT/KR2019/015834.

PROJECTS

NRC: Advanced Channel Coding and Channel Estimation for Wireless Communication Evolution Institute for Information & Communication Technology Planning & evaluation (IITP)	Apr. 2024 - Aug. 2024
• Developing α -TECC: All-in-one Paradigm Changing Technologies in Error Control Coding	
AI-ISP SW/HW Co-Optimization Samsung Advanced Institute of Technology (SAIT), Samsung Electronics	Nov. 2022 - Aug. 2024
• Developing baseline ISP hardware modules and AI-ISP inference simulators	
InSeCT: Intelligent Secure Underwater Communication Technology Korea Research Institute for defense Technology planning and advancement (KRIT)	Dec. 2022 - Aug. 2024
• Developing efficient FEC decoder architectures for BOSS codes	
Algorithm-Hardware Co-Optimization Methods for Energy-Efficient 6G Baseband Systems National Research Foundation of Korea (NRF)	Sep. 2022 - Aug. 2024
• Developing short-length FEC decoders for 5G/6G URLLC scenarios	
Low-cost & Low-latency polar decoder designs for B5G URLLC scenarios National Research Foundation of Korea (NRF)	June 2019 - Feb 2022
• Optimizing node-pruning methods of SCL decoding and implementing polar decoders at the ASIC level	
Low-cost & Low-power ECC/signal processing HW IP development Samsung Electronics	July 2018 - Sep. 2023
• Developing ECC decoder architectures for emerging memory devices	

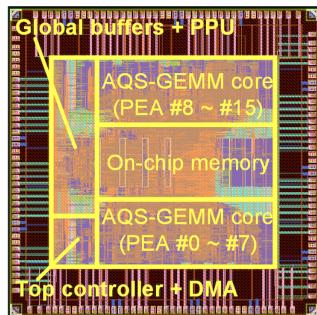
TEACHING SERVICE

EECE276, Electronics & Electrical Eng. Lab I Teaching Assistant for the lecture on micro-controller applications	Fall 2022
EECE199, Freshmen Research Participation Teaching Assistant	Fall 2022

CHIP GALLERY

Samsung 28nm CMOS Technology (2024)

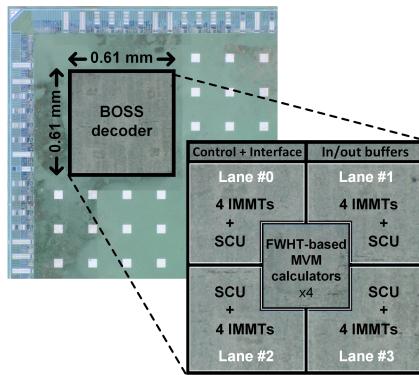
Panacea: DNN accelerator using accuracy-preserving asymmetric quantization and energy-saving bit-slice sparsity (HPCA '25)



Technology	28 nm
# of 4bx4b multipliers	3072
Overall area	2.11 mm ²
Core gate area	1.31 mm ²
Supply voltage	1.0 V
Operating Frequency	250 MHz
Throughput	1.268 TOPS
Energy efficiency	12.5 TOPS/W

Samsung 28nm CMOS Technology (2023)

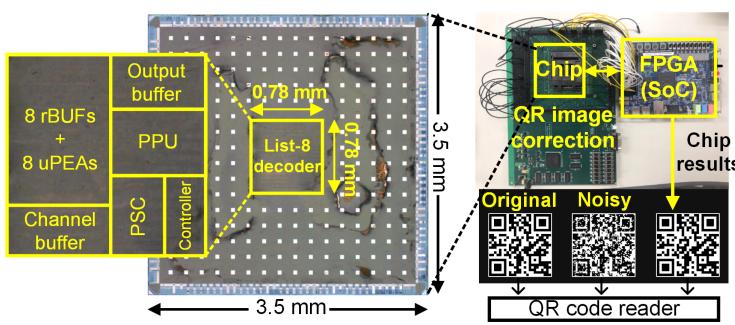
Cost-efficient BOSS FEC decoder for URLLC scenarios (ISSCC '24)



Technology	28 nm
Target code	(128, 15) BOSS code
Decoding algorithm	Two-stage MAP
Core area	0.37 mm ²
Supply voltage	1.05 V
Operating Frequency	590 MHz
Power	33.3 mW
Coded Throughput	5.84 Gb/s
Area efficiency	15.78 Gb/s/mm ²
Energy efficiency	5.7 pJ/bit

Samsung 28nm CMOS Technology (2021)

Cost efficient large-list SCL polar decoder using fully-reusable LLR buffers (VLSI '22)



Technology	28 nm
Target code	N=1024 polar codes
Decoding algorithm	List-8 SCL
Core area	0.595 mm ²
Supply voltage	1.05 V
Operating Frequency	413 MHz
Power	101.4 mW
Throughput	925 Mb/s
Area efficiency	1.56 Gb/s/mm ²
Energy efficiency	109.5 pJ/bit