Cairo University

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Home Automation System

Done by

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Supervised by:

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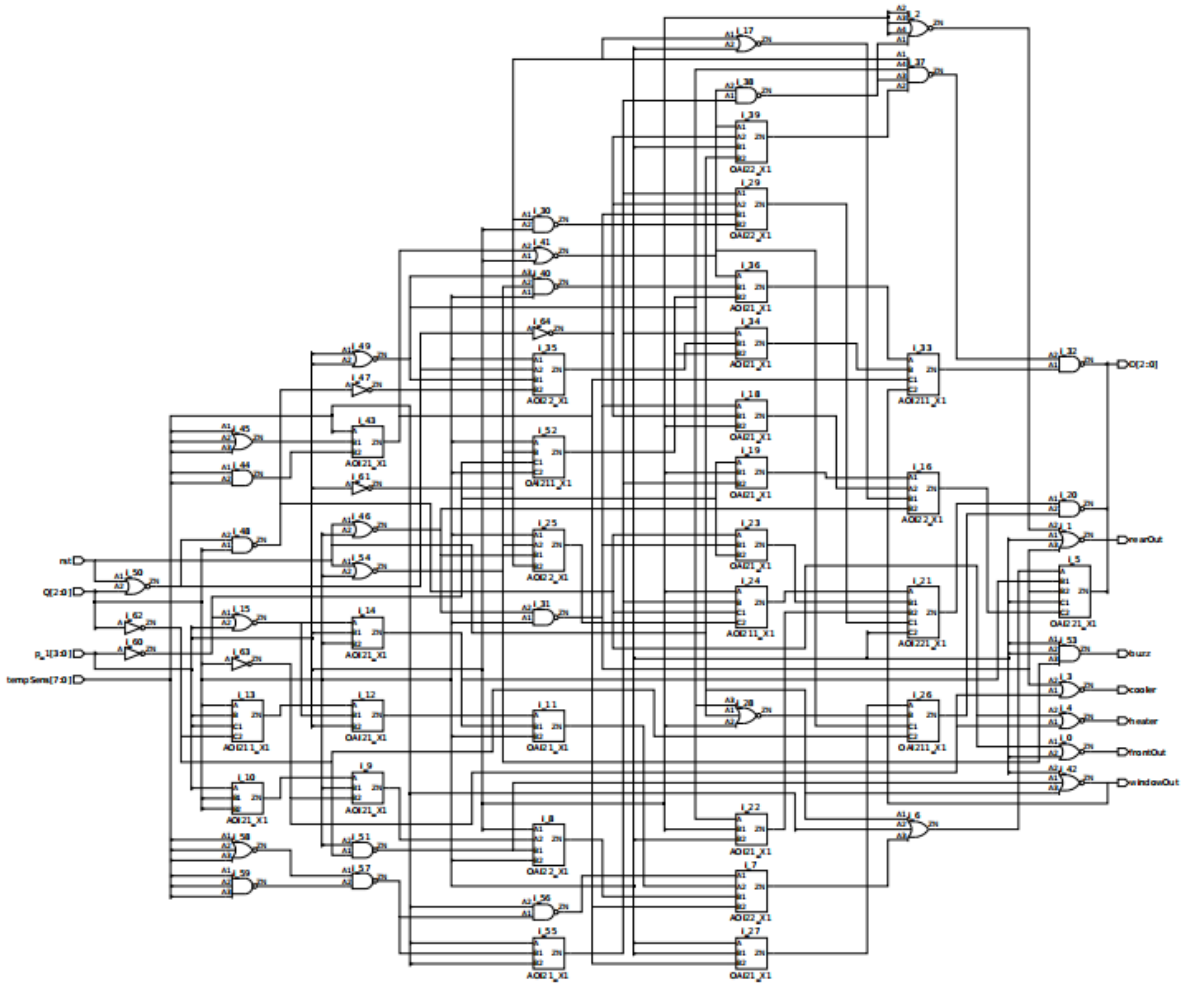
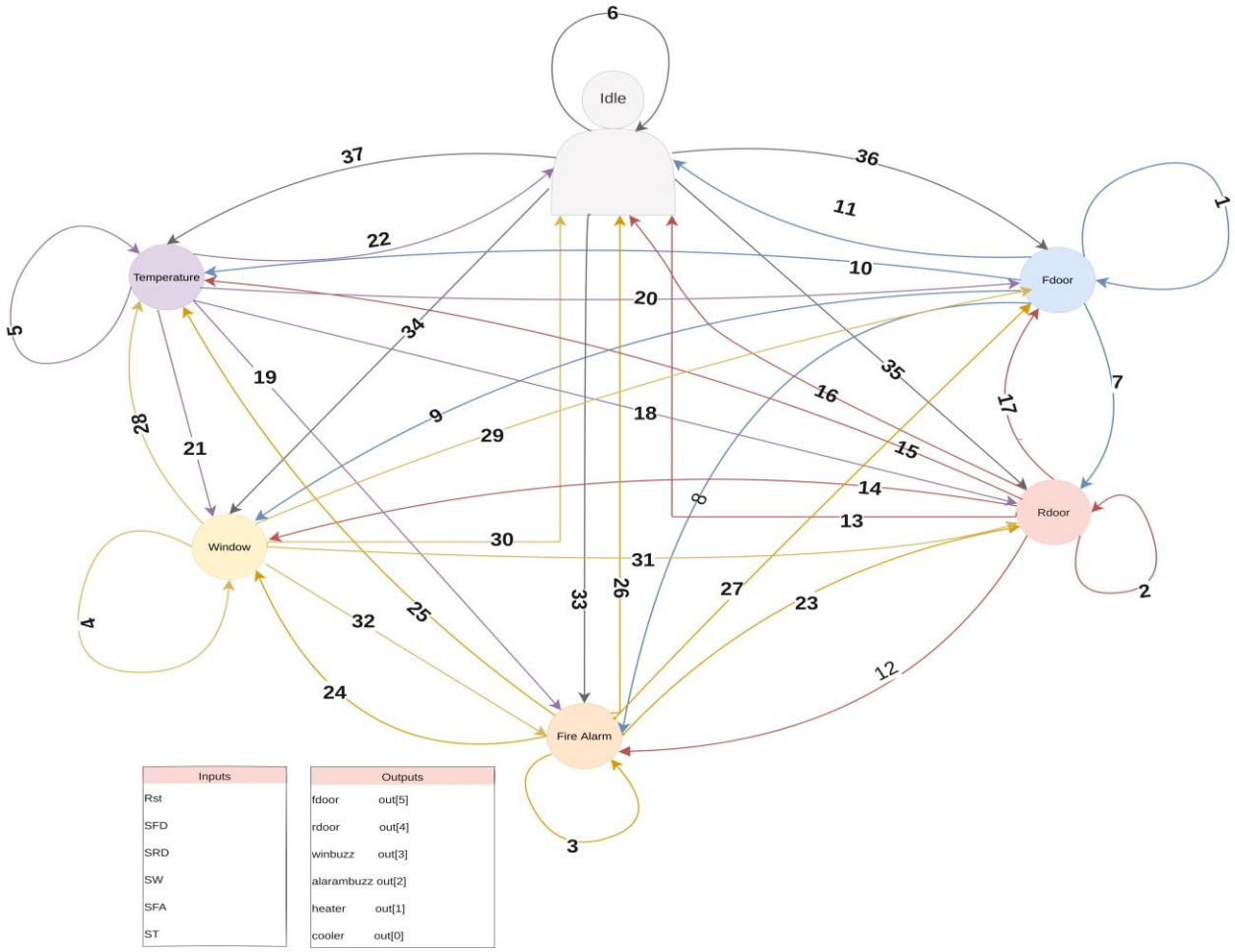
Design Schematic

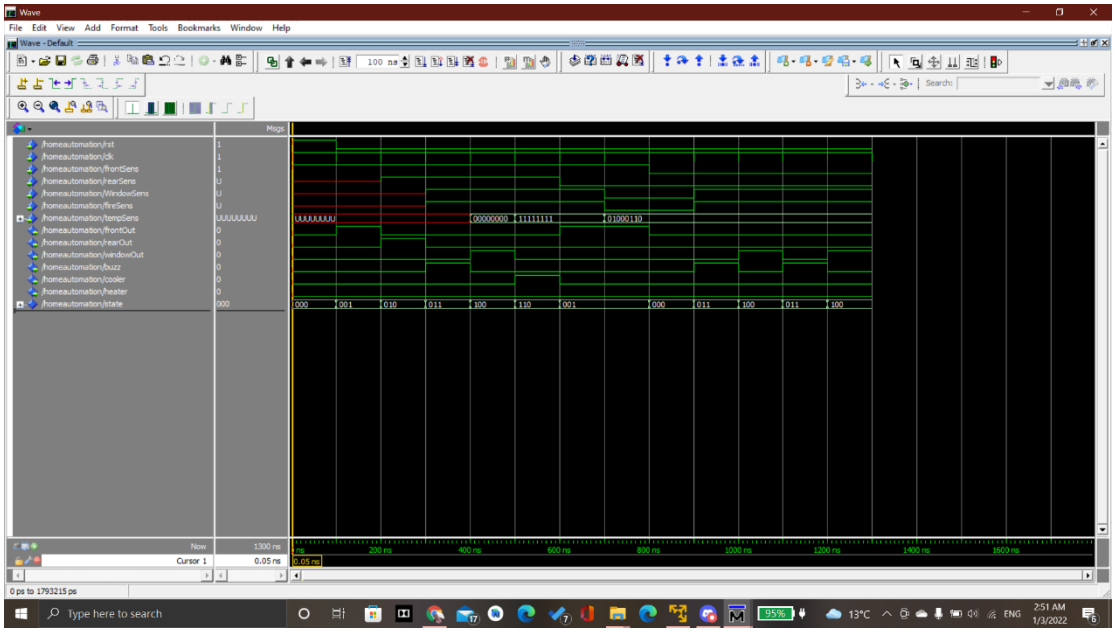


FSM

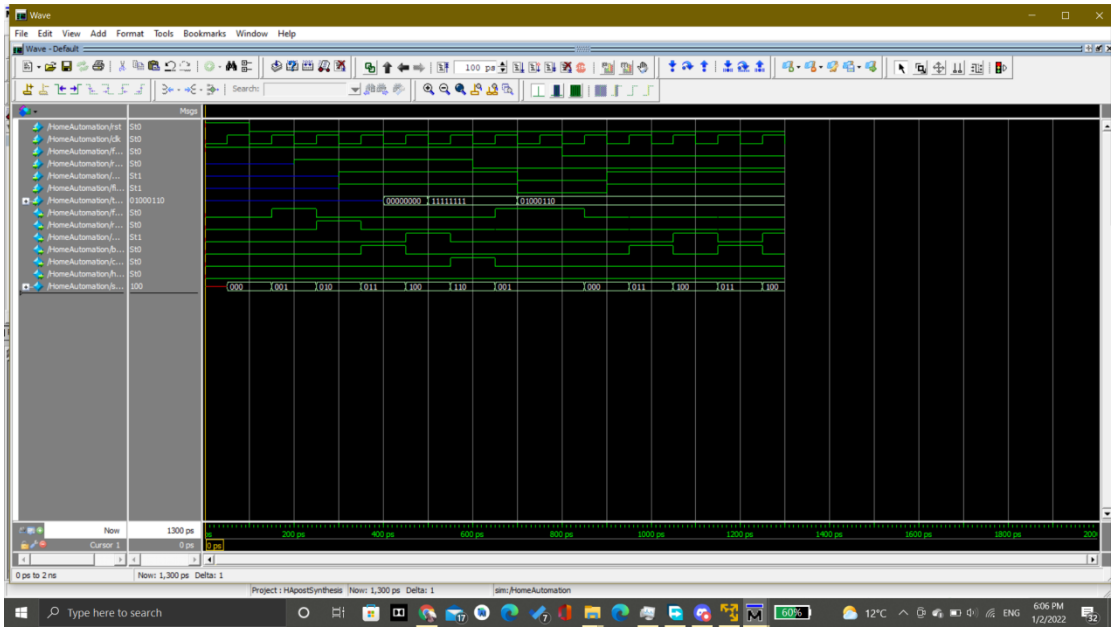

Idle
Temperature
Fdoor
Window
Rdoor
Fire Alarm
Inputs
Rst
SFD
SRD
SW
SFA
ST
Outputs
fdoor out[5]
rdoor out[4]
winbuzz out[3]
alarambuzz out[2]
heater out[1]
cooler out[0]

1	SRD=0 & SFA=0 & SW=0 & (st>=50 && st<=70) & SFD =1 / out = 100000
2	SFA=0 & SW=0 & (st>=50 && st<=70) & SRD =1 / out = 010000
3	SW=0 & & (st<=50 || st<=70) & SFA= 1 / out= 000100
4	(st>=50 && st<=70) & SW=1 / out = 001000
5	(st <50 || st >70) / if(st<=50) out= 000010 else out = 000001
6	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
7	SRD=1 & others = x(don't care) / out= 010000
8	SRD=0 & SFA= 1 & others = x(don't care) / out= 000100
9	SRD=0 & SFA=0 S SW=1 & others = x(don't care) / out= 001000
10	SRD=0 & SFA=0 & SW=0 & (st< 50 || st > 70) / if(st<=50) out= 000010 else out = 000001
11	SRD=0 & SFA=0 & SW=0 & (st>=50 && st<=70) & SFD =0 / out = 000000
12	SFA=1 & others = x(don't care) / out= 000100
13	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
14	**SFA=0 & SW=1 & others = x(don't care)** **/ out= 001000**
15	**SFA=0 & SW=0** & (st< 50 || st > 70) **& others = x(don't care)** / if(st<=50) out= 000010 else out = 000001
16	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
17	SFA=0 & SW=0 & (st>=50 && st<=70) & SFD =1 / out = 100000
18	SFD=0 & (st>=50 && st<=70) & SRD =1 / out = 010000
19	SW=0 & & (st<=50 || st<=70) & SFA= 1 / out= 000100
20	SRD=0 & SFA=0 & SW=0 & (st>=50 && st<=70) & SFD =1 / out = 100000
21	(st>=50 && st<=70) & SW=1 / out = 001000
22	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
23	**SFA=0 & SW=0 & (st>=50 && st<=70) & SRD =1** **/ out = 010000**
24	SW=1 & others = x(don't care) / out= 001000
25	SW=0 & (st <50 || st > 70) / if(st<=50) out= 000010 else out = 000001
26	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
27	**SFA=0& SFD=1 & others = x** **/ out= 100000**
28	(st <50 || st >70) / if(st<=50) out= 000010 else out = 000001
29	(st>=50 && st<=70) & SW=0 & SFD=1 / out = 100000
30	(sfd=0 & srd=0 & sw=0 & sfa=0 & (st>=50 && st<=70)) / out= 000000
31	(st>=50 && st<=70) & SW=0 & SRD=1 / out = 010000
32	(st>=50 && st<=70) & SW=0 & SFA=1 / out = 000100
33	SFD=0& SRD=0 & SFA=1 & others = x / out= 000100
34	SFD=0& SRD=0 & SFA=0 & SW=1 & others = x / out= 001000
35	**SFD=0& SRD=1 & others = x** **/ out= 010000**
36	SFD=1 & others = x(don't care) / out= 100000
37	SFD=0& SRD=0 & SFA=0 & SW=0 & (st< 50 || st > 70) / if(st<=50) out= 000010 else out = 000001

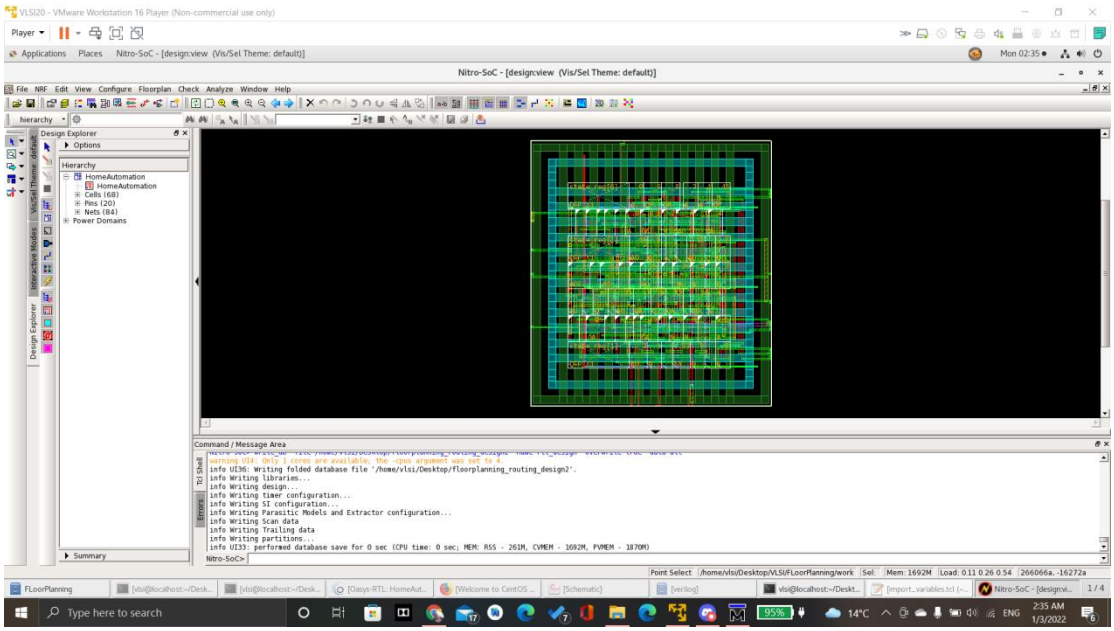
Pre-synthesis simulation results



Post-synthesis simulation results



Chip Schematic after floorplanning, placement, and routing



Synthesis Reports

1. Design rpt

```
Report Physical info:
------------------------+--------------+-----------+------------
                        |              |Area (squm)|Leakage (uW)
------------------------+--------------+-----------+------------
Design Name             |HomeAutomation|           |
  Total Instances       |            68|         80|       1.801
    Macros              |             0|          0|       0.000
    Pads                |             0|          0|       0.000
    Phys                |             0|          0|       0.000
    Blackboxes          |             0|          0|       0.000
    Cells               |            68|         80|       1.801
      Buffers           |             0|          0|       0.000
      Inverters         |             6|          3|       0.086
      Clock-Gates       |             0|          0|       0.000
      Combinational     |            59|         63|       1.478
      Latches           |             0|          0|       0.000
      FlipFlops         |             3|         14|       0.237
       Single-Bit FF    |             3|         14|       0.237
       Multi-Bit FF     |             0|          0|       0.000
       Clock-Gated      |             0|           |
       Bits             |             3|         14|       0.237
         Load-Enabled   |             0|           |
         Clock-Gated    |             0|           |
  Tristate Pin Count    |             0|           |
Physical Info           |Placed        |           |
  Chip Size (mm x mm)   |0.073 x 0.073 |       5307|
  Fixed Cell Area       |              |          0|
    Phys Only           |             0|          0|
  Placeable Area        |              |        160|
  Movable Cell Area     |              |         80|
  Utilization (%)       |            49|           |
  Chip Utilization (%)  |            49|           |
  Total Wire Length (mm)|         0.728|           |
  Longest Wire (mm)     |         0.037|           |
  Average Wire (mm)     |         0.036|           |
------------------------+--------------+-----------+------------
```

2. Path rpt

```
Report Path Groups:
-----+-------+------+---------+---------
     | Path  |Weight|Critical |Worst
     | Group |      |Range(ps)|Slack(ps)
-----+-------+------+---------+---------
1    |default| 1.000|      0.0|   2575.1
2    |I2R    | 1.000|      0.0|   1993.2
3    |I2O    | 1.000|      0.0|    432.9
4    |R2O    | 1.000|      0.0|    121.0
-----+-------+------+---------+---------
```

3. Power rpt

```
warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found in the
database for power domain '/PD_TOP'  [NL-174]
Report Power (instances with prefix '*' are included in total) :
-----+------------+------------------+--------------------+------------------+----------------
     | Instance   | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
-----+------------+------------------+--------------------+------------------+----------------
1    |*state_reg[2]|          1.171167|            6.165482|          0.079112|         7.415761
2    |*state_reg[1]|          1.290418|            6.542564|          0.079112|         7.912094
3    |*state_reg[0]|          0.963690|            2.780069|          0.079112|         3.822872
4    |*i_0_0_0    |          0.312302|            0.482551|          0.021200|         0.816052
5    |*i_0_0_1    |          0.244516|            0.340809|          0.026832|         0.612156
6    |*i_0_0_2    |          0.057080|            0.059550|          0.032601|         0.149232
7    |*i_0_0_3    |          0.079158|            0.145222|          0.021200|         0.245580
8    |*i_0_0_4    |          0.063426|            0.118570|          0.021200|         0.203196
9    |*i_0_0_5    |          0.311005|            0.146008|          0.033938|         0.490951
10   |*i_0_0_6    |          0.145307|            0.102531|          0.024415|         0.272252
11   |*i_0_0_7    |          0.319008|            0.260275|          0.032612|         0.611894
12   |*i_0_0_8    |          0.347167|            0.446854|          0.034026|         0.828047
13   |*i_0_0_9    |          0.295857|            0.482193|          0.027858|         0.805908
14   |*i_0_0_10   |          0.348019|            0.462577|          0.027858|         0.838454
15   |*i_0_0_11   |          0.276505|            0.472098|          0.022619|         0.771223
16   |*i_0_0_12   |          0.179995|            0.239241|          0.022619|         0.441855
17   |*i_0_0_13   |          0.287753|            0.345827|          0.034566|         0.668145
18   |*i_0_0_14   |          0.317862|            0.757659|          0.027858|         1.103380
19   |*i_0_0_15   |          0.612209|            2.102632|          0.021200|         2.736040
20   |*i_0_0_16   |          0.295609|            0.260251|          0.032612|         0.588472
21   |*i_0_0_17   |          0.197516|            0.405238|          0.021200|         0.623954
22   |*i_0_0_18   |          0.240991|            0.365188|          0.022619|         0.628799
23   |*i_0_0_19   |          0.917396|            1.273385|          0.022619|         2.213400
24   |*i_0_0_20   |          0.231232|            0.164908|          0.017393|         0.413534
25   |*i_0_0_21   |          0.328418|            0.349200|          0.041741|         0.719359
26   |*i_0_0_22   |          0.330595|            0.297841|          0.027858|         0.656294
27   |*i_0_0_23   |          0.123857|            0.128426|          0.022619|         0.274903
28   |*i_0_0_24   |          0.124185|            0.117684|          0.034566|         0.276435
29   |*i_0_0_25   |          0.249769|            0.220024|          0.032612|         0.502405
30   |*i_0_0_26   |          0.152678|            0.195117|          0.022039|         0.369834
31   |*i_0_0_27   |          0.174129|            0.276967|          0.022619|         0.473716
32   |*i_0_0_28   |          0.584361|            0.902139|          0.026832|         1.513331
33   |*i_0_0_29   |          0.248761|            0.249002|          0.034026|         0.531789
```

34	*i_0_0_30	0.668399	1.084271	0.017393	1.770063
35	*i_0_0_31	0.284477	0.858290	0.017393	1.160161
36	*i_0_0_32	0.176910	0.131809	0.017393	0.326113
37	*i_0_0_33	0.216571	0.278465	0.034566	0.529601
38	*i_0_0_34	0.121167	0.143506	0.027858	0.292531
39	*i_0_0_35	0.133255	0.209050	0.032612	0.374917
40	*i_0_0_36	0.057288	0.059385	0.027858	0.144531
41	*i_0_0_37	0.082477	0.101083	0.018127	0.201687
42	*i_0_0_38	0.226489	0.886286	0.017393	1.130168
43	*i_0_0_39	0.440835	0.457681	0.034026	0.932543
44	*i_0_0_40	0.023378	0.036055	0.018105	0.077538
45	*i_0_0_41	0.689617	4.793136	0.021200	5.503953
46	*i_0_0_42	0.367103	0.500691	0.026832	0.894625
47	*i_0_0_43	1.032434	5.105583	0.027858	6.165875
48	*i_0_0_44	1.187018	1.103167	0.025066	2.315252
49	*i_0_0_45	0.704582	0.628889	0.024415	1.357886
50	*i_0_0_46	0.829863	1.353266	0.021200	2.204328
51	*i_0_0_47	0.041337	0.127510	0.014353	0.183200
52	*i_0_0_48	0.236589	1.148788	0.017393	1.402771
53	*i_0_0_49	0.645910	5.358412	0.021200	6.025522
54	*i_0_0_50	0.797967	3.157250	0.021200	3.976417
55	*i_0_0_51	0.527322	0.599211	0.017393	1.143927
56	*i_0_0_52	0.068866	0.199826	0.022039	0.290732
57	*i_0_0_53	0.133020	0.109030	0.026481	0.268531
58	*i_0_0_54	0.813706	1.653362	0.021200	2.488267
59	*i_0_0_55	0.881930	5.342503	0.027858	6.252291
60	*i_0_0_56	1.007925	1.429725	0.017393	2.455043
61	*i_0_0_57	0.272537	1.071601	0.017393	1.361531
62	*i_0_0_58	0.503714	0.588410	0.026832	1.118956
63	*i_0_0_59	0.551846	0.608840	0.018105	1.178791
64	*i_0_0_60	0.790664	5.719367	0.014353	6.524384
65	*i_0_0_61	0.795029	5.601731	0.014353	6.411113
66	*i_0_0_62	0.143526	1.139875	0.014353	1.297755
67	*i_0_0_63	0.130238	1.206300	0.014353	1.350891
68	*i_0_0_64	0.139387	1.274756	0.014353	1.428496
69					
70	*TOTAL	27.545321	81.725182	1.801196	111.071701

Score

$0.5\times80+.3\times(3000-121)+0.2\times111.071701 = 925.914$