ASIC and FPGA Design NANENG-422

Final Project- Design of a 64×12 bits 6T SRAM

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Abstract

This study highlights the successful integration of a 64x12 6T SRAM using TSMC 65nm technology in Cadence Virtuoso. To assure the SRAM's compatibility, transistor-level design, layout construction, simulations, and operation were all part of the design process.

Introduction

6T SRAM is a type of memory cell that is frequently seen in microprocessors and integrated circuits. It is a crucial part of modern electronic devices like smartphones, computers, and other digital systems. The number of transistors required to construct a single memory cell is 6 transistors. Each memory cell is composed of six transistors arranged in a cross-coupled flip-flop design. Together, these transistors offer dependable data storage for a single bit of information, such as a 0 or a 1. One of the primary characteristics of 6T SRAM is its ability to retain stored data if power is delivered to the circuit. It is ideal for cache memory storage because of this feature, which demands trustworthy and fast data access. From the drawbacks of 6TSRAM is that it requires more storage than DRAM for example and consumes more power than other memories but due to its quick access times, non-volatility, and durability, 6T SRAM continues to be widely employed in a variety of applications.

Circuit analysis

The schematic of a single cell in the 6TSRAM is represented in figure1. Regarding sizing, the used length is the minimum which is 65 nm, and the width is applied to ensure the best functionality as follows: the pull-up PMOS and two NMOS access transistors have 120 nm width and pulldown NMOS transistors of 200 nm width as larger width for pulldown transistors make them can pass more current, providing stronger drive to overcome leakage currents and maintain the integrity of stored data.

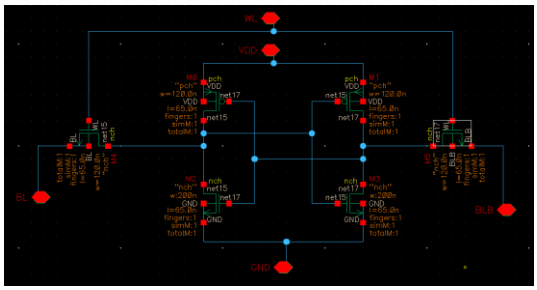

Figure 1 6TSRAM 1 cell schematic.

Layout

The Layout of a bit-cell (shown in figure2) is created then multiplied to 12 cells to make row, then this row is multiplied 64 times to create the whole 6TSRAM.

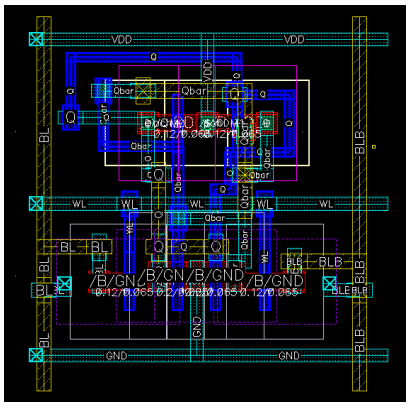

Figure 2 1-bit cell layout.

Figure3 shows the 12 cells row.

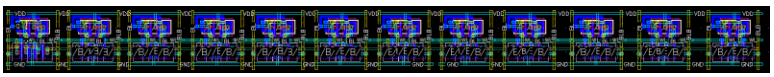

Figure 3. 12cells in a row

When multiplying this row 64 times this is the whole layout shown in figure4.

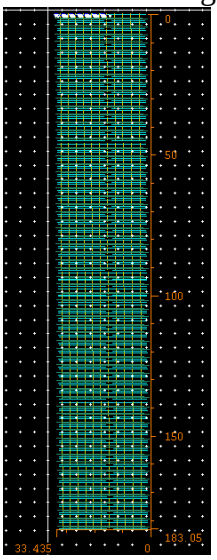

Figure 4 whole layout

DRC test

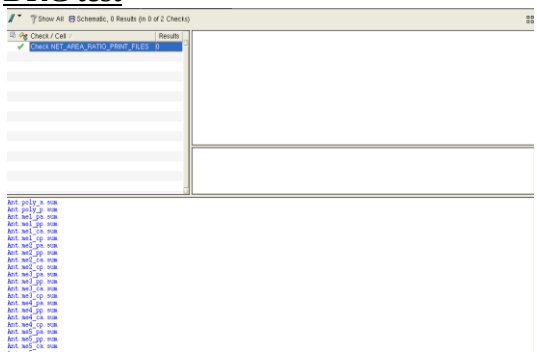
Figure 5 DRC test

LVS test

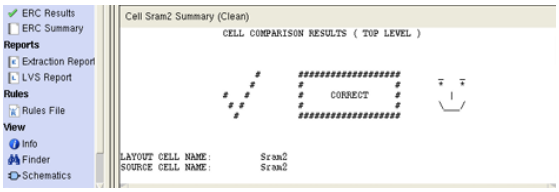

Figure 6 LVS test

The area of the whole layout is about 6112um^2.

Results

I. Static noise margin (SNM)

The SNM is an important metric to evaluate the stability and reliability of the stored data and the ability of the memory cell to retain the information accurately.

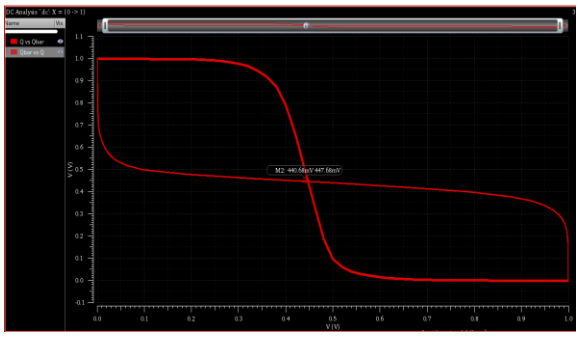
Figure 7 SNM curve.

A higher SNM indicates a stronger signal relative to the noise, resulting in better data integrity and lower susceptibility to errors.

Since the minimum SNM is 0.1Vdd, then it's observed from figure 7 that the margin is higher than this value showing the butterfly curve, so this design has more immunity to noise.

II. Power consumption

Figure 8 shows the total power consumption of the 1-bit cell of nearly maximum of 38 mW.

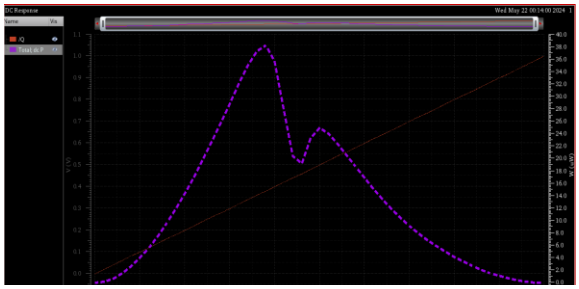
Figure 8 Power consumption.

III. Read Function

To read values on the 1-bit cell these are introduced parameters to the V-pulse:

WL: 11

BL :1010

BLB 0101

‘0’ read case:

Figure 9 represents the read of 0, the power consumption and the delay of the cell to read’0’.

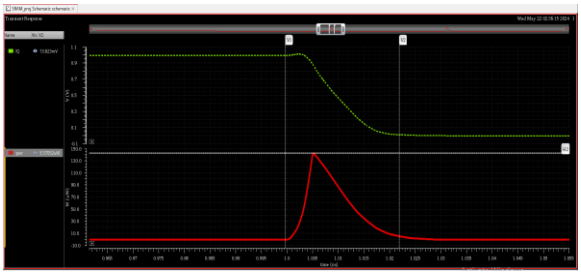

Figure 9 ‘0’ read delay time and power consumption.

As observed from the graph the delay of the cell to read’0’ is about 0.0229 ns and max power consumption is 5.57 uW.

‘1’ read case:

Figure 10 represents the read of 1, the power consumption and the delay of the cell to read’1’.

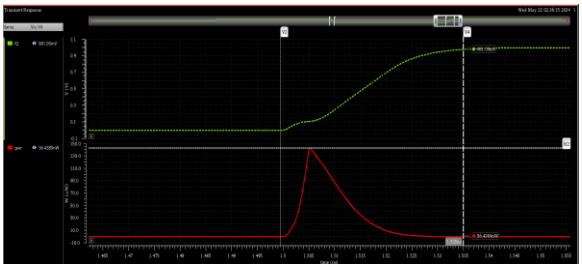

Figure 10 ‘1’ read delay time and power consumption.

As observed from the graph the delay of the cell to read’1’ is about 0.0355 ns and max power consumption is 56.45 nW.

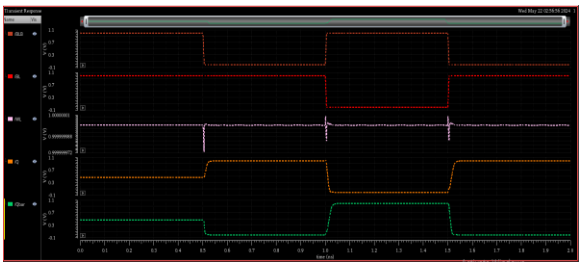

Figure 11 READ parameters transient response.

IV. Write function.

To read values on the 1-bit cell these are introduced parameters to the V-pulse:

WL: 11

BL: 0101

BLB: 1010

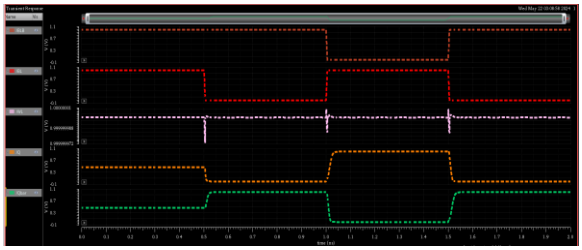

Figure 12 WRITE parameters transient response.

‘1’ write case:

Figure 13 represents the write of 1, the power consumption and the delay of the cell to write’1’.

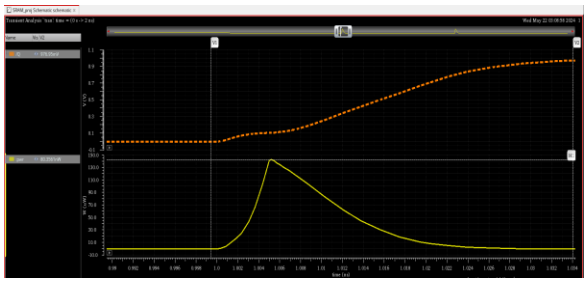

Figure 13 ‘’1’write delay time and power consumption.

As observed from the graph the delay of the cell to write’1’ is about 0.044 ns and max power consumption is 80.3nW.

‘0’ write case:

Figure 14 represents the write of 0, the power consumption and the delay of the cell to write’0’.

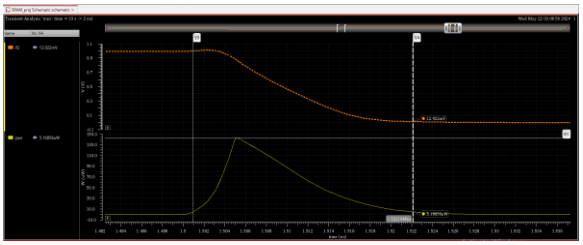

Figure 14 ‘0’write delay time and power consumption.

As observed from the graph the delay of the cell to write’1’ is about 0.022 ns and max power consumption is 5.168 uW.

Conclusion and discussion

In this project, we embarked on the design and analysis of a 6T Static Random-Access Memory (SRAM) array, focusing on evaluating critical performance metrics including Static Noise Margin (SNM), read and write delays, and power consumption. Through comprehensive simulations and characterization, we gained valuable insights into the behavior and optimization opportunities of our SRAM design.

The specs of the design could be good enough and ready for synthesizing. The figure of merit can be calculated as follows:

$$FM = POWER \times AREA \times DELAY^2$$

References

J. M. Rabaey, Digital Integrated Circuits. 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2002.

SUBBARAYAPPA, M , The implementation of a hierarchical predecoder/decoder structure in OpenRAM, an open-source memory compiler, 2011.

https://www.researchgate.net/figure/Conventional-6T-SRAM-cell-design-in-cadence_fig6_266462789