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# 350 nm node technology CMOS fabrication technique phase 2.

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## **Introduction:**

CMOS (Complementary Metal-Oxide-Semiconductor) fabrication process is now one of the important technologies for creating integrated circuits on a silicon wafer. There are many techniques and technology nodes used to fabricate a CMOS but, in our project, we work on 350 nm technology node and use N-well Technology as in N-well technology an n-type well is diffused on a p-type substrate and we will use silicide layer at the end of the design for providing ohmic contacts, interconnects, and as Schottky barriers for integrated circuits in microelectronics due to their low electrical resistivity and good compatibility with silicon substrate.

In the next sections we will discuss the process of CMOS fabrication in details for each process.

## **CMOS main process:**

1. Cleaning and preparation of silicon wafer using RCA solutions.
2. Oxidation process of applying layer of oxide (silicon dioxide) on the wafer surface.
3. Photoresist application that is a light sensitive material used for selective etching.
4. Applying masking process as a mask is used above the photoresist and exposed to UV light for pattern transfer.
5. Chemical Etching that removes oxide layer from the exposed areas to transfer the pattern from photomask to oxide layer.
6. Oxide etching to remove the oxide layer from the areas not covered by the photoresist.
7. Photoresist removal leaving the oxide layer with the circuit pattern on it.
8. Formation of N-well by diffusing n-type impurities into the p-type substrate through the exposed region.
9. STI formation as some shallow trenches are etched into the wafer of silicon to isolate certain regions from the circuit.
10. Removing the whole oxide ( $\text{SiO}_2$ ) layer by acid like HF which is called chemical mechanical polishing process (CMP) leaving smooth and flat surface.
11. Deposition of thin gate oxide layer that prevent further doping under the gate region.
12. Deposition of polysilicon that is the gate electrode formation process.
13. Silicide formation process as a thin layer of metal such as nickel or cobalt is deposited on the surface of the polysilicon that reacts with the silicon to form a silicide layer.
14. Source and drain formation through ion implantation process that implement dopant atoms.
15. An extra oxidation layer is added to protect structure during further diffusion and metallization processes.
16. Masking and diffusion process as small gaps are made to diffuse n-type impurities then remove the oxide layer.
17. P-type diffusion.

18. Applying thick field oxide before forming the metallic terminals to form protective layer for regions of the wafer where no terminals are required.
19. Metallization process to provide interconnections.
20. Removing excess metals.
21. Formation of terminals (NMOS and PMOS transistors).

Now we going to go through the main steps from the distribution above:

### **Choose substrate:**

First the substrate is p-doped that has impurities such as boron for a concentration up to  $10^{16} /cm^3$  and the material of the wafer itself is silicon and the thickness of the substrate can be about 5000nm (5um).

### **Oxide layer:**

For the techniques we use here we can work with wet or dry oxidation, we chose to work with dry oxidation that is slower than the wet oxidation reaction but produces higher quality and denser oxide. Oxidation rate depends on some factors as silicon orientation (100 or 111), temperature (800:1000 °C) for massoud model and dopant concentration. For field oxide formation process we wish to create insulating layer.

For clean dry oxidation process, the typical cycle is nearly 45 minutes at 1000°C.

#### Parameters used for dry oxidation:

Temperature: 1000 °C.

Silicon orientation: 100, due to its superior electrical properties and its high trap density compared to 111.

Pressure: 1atm (100% oxygen ambient).

Time for oxidation process = 15.789 min

Here we work with massoud model rather than deal-grove model as massoud is more accurate at dry oxidation for thin oxide layer that is less than 500 Å for temperature range (800:1000°C) as by increasing the temperature, the implemented oxide layer can be thicker.

#### Results fig (1):

final thickness of oxide layer= 200 Å =20 nm.

Silicon thickness consumed =88 Å =8.8 nm.

Since in dry thermal oxidation silicon is replaced by roughly twice its volume of silicon dioxide then silicon consumed is calculated from densities and molar masses of silicon and silicon dioxide:

$$\rho_{\text{Si}} = 2.329 \text{ g/cm}^3.$$

$$\rho_{\text{SiO}_2} = 2.196 \text{ g/cm}^3.$$

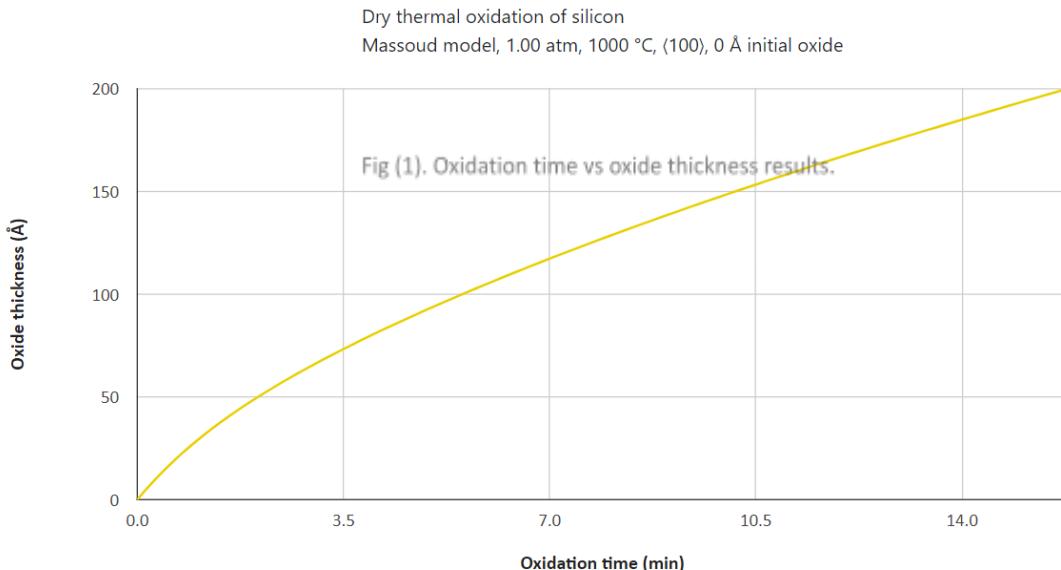
$$M_{\text{Si}} = 28.0855 \text{ g/mol.}$$

$$M_{\text{O}} = 15.9994 \text{ g/mol.}$$

$$\text{Then } M_{\text{SiO}_2} = 28.0855 + (2 * 15.9994) = 60.0843 \text{ g/mol.}$$

And %Si consumed =  $N_{\text{Si}} / N_{\text{SiO}_2}$ , for N is number of moles.

$$\text{Then \% Si consumed} = 0.4407 D_{\text{oxide}} = 0.4407 * 200 \text{ \AA} = 88 \text{ \AA}.$$

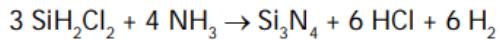


## LPCVD Silicon Nitride:

Silicon nitride deposition on the substrate works on protecting the underlying layers during the etching and patterning process or as a passivation layer, it also used as a mask for ion implantation as it is a hard and durable material that can withstand the harsh chemical and physical conditions involved in these processes. Also due to its chemical, electrical and optical properties it's used as an etch stop material in wet and plasma etching for example.

Silicon nitride is deposited after silicon dioxide because SiO<sub>2</sub> protect the substrate from the effect of the normal tensile stress come from silicon nitride deposition process and also because SiO<sub>2</sub> acts as a good diffusion barrier for impurities.

Silicon nitride is deposited by low pressure chemical vapor pressure via this reaction:



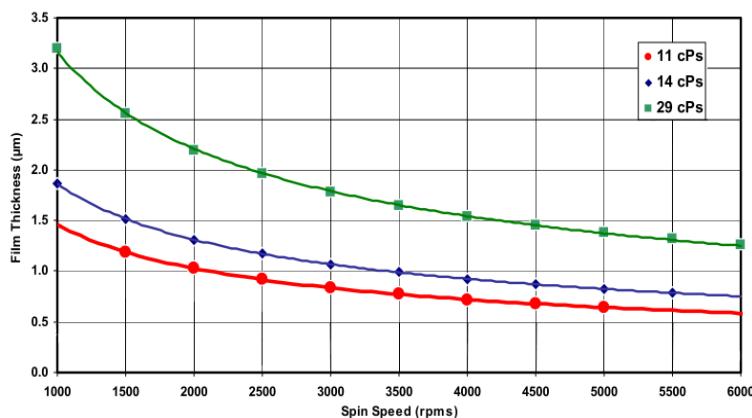
As LPCVD is done under temperature range (700: 850°C) so we will work on 800 °C in the CVD furnace and at 1 torr. Also, the thickness of this layer is 50nm.

### Photoresist application:

Photoresist application can be done by two types which are positive photoresist or negative photoresist. We will use positive photoresist as the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. Photoresist is a liquid applied on the surface of the oxide layer with spin coating process at specific speed to achieve specific thickness. The thickness of the photoresist layer is usually 10 to 12 times the thickness of the oxide layer and the substrate (wafer) is about 500 times the thickness of the photoresist layer.

The chosen photoresist to work with is **AZ MIR 701** (14cps) which is positive tone photoresist as Low exposure dose requirements provide excellent throughput; it has a reliable performance in both dry and wet etch process environments and works well with MIF developers (AZ 300MIF or AZ 726MIF).

**AZ MiR 701 Photoresist  
Spin Speed Curve**



so, to reach a thickness of 1um for the photoresist layer for AZMIR701 (14cps), the required spin speed is 3500 rpms.

The parameters of the whole process are:

Soft Bake: 90°C for 60 seconds.

Expose: i-line/broadband (180mJ/cm<sup>2</sup>)

Post Expose Bake: 110°C

Develop: spray or puddle

Developer: Fig (3). Lines in AZMIR 701 AZ 300MIF

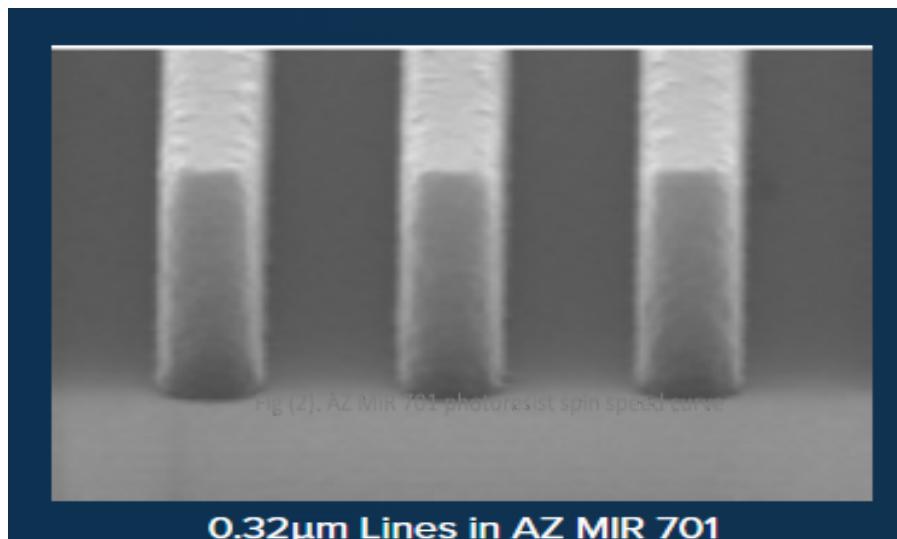
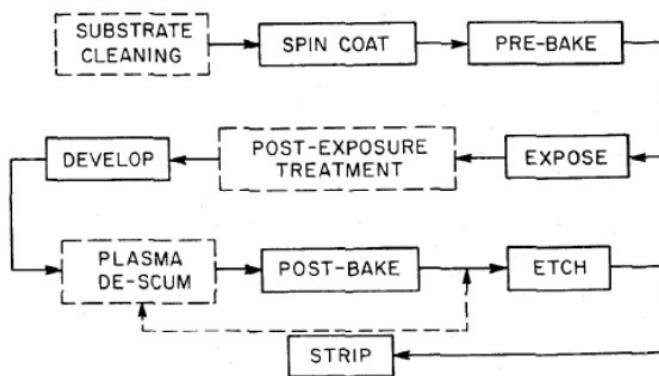


Fig (2). AZ MIR 701 photoresist spin speed curve

0.32µm Lines in AZ MIR 701

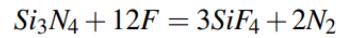
Photolithography process can be represented by these steps as a flow chart (fig4):



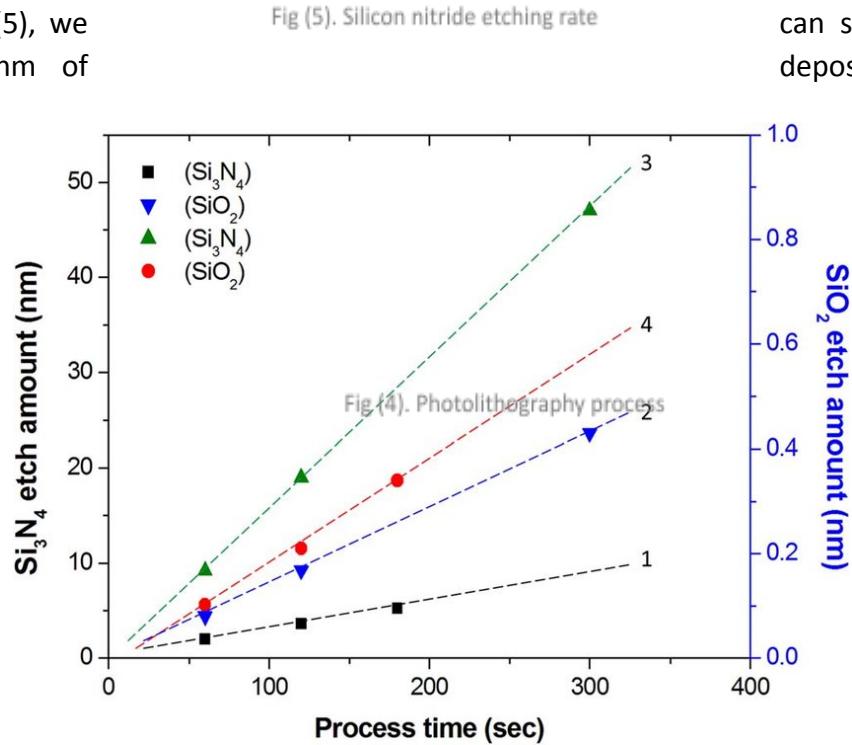
## Silicon nitride layer etching:

$\text{Si}_3\text{N}_4$  is etched in a dry environment with a resist as a mask in a fluorine plasma dry etching. This etching process happens in two parallel plates to confine gas reactants involved in the process. This happens with RF voltage applied between electrodes equals nearly 13.5 volts.

This process is usually completed with fluorine plasma and generation of Fluorine atoms using CF or NF<sub>3</sub> gas source and the reaction will occur as:



From fig (5), we total 50 nm of nitride, process 300 to 320



can see to remove the deposited silicon the required time is nearly seconds.

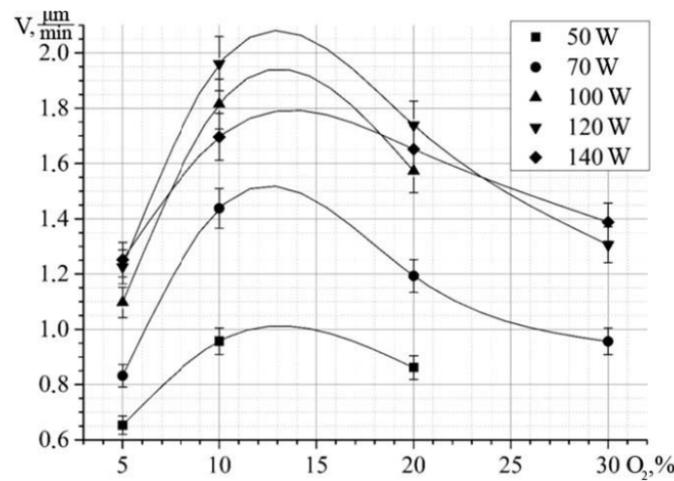
## Shallow trench isolation formation (STI):

This process is a method used to form an isolation region between active devices (PMOS and NMOS), this process is better than LOCOS isolation because it eliminates one drawback of this process which is the “bird’s beak” region. Here in STI the oxidation extends for a distance inside the silicon substrate after etching  $\text{SiO}_2$  (that can be etched by HF) and  $\text{Si}_3\text{N}_4$  (dry plasma etching) layers, as an additional etching is done to etch in the silicon substrate itself by using silicon nitride pattern as hard mask.

The trenched depth in the silicon can be 400 nm deep. This process of etching can be done by Reactive Ion Etching (RIE) technique which is a dry etching process that uses mixture of gases such as  $\text{SF}_6$  (sulfur hexafluoride) and  $\text{O}_2$  that increases etching rate. This process should be done under low pressure to assure a steep sidewall for the trench (high directionality).

The average etching rate of silicon in  $\text{SF}_6$  with an amount of oxygen gas is about 650 nm/min which means to etch about 400 nm deep we need about 37 seconds and to put in our consideration the over etching time to ensure that the process went to completion then time is 40 seconds.

We work with RF source power equals 50 watt with 6 % of oxygen in the gas mixture with rate of 650 nm/min as shown in fig (6).



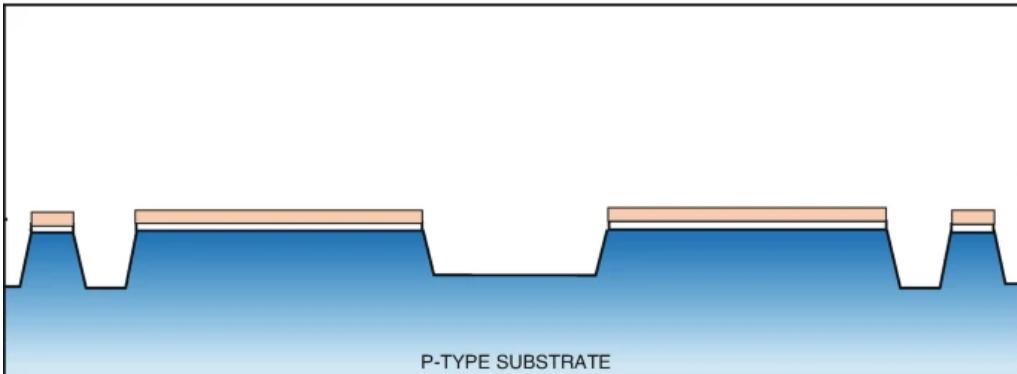


Fig (6). Silicon etch rate versus oxygen content in the gas mixture at various RF powers.

Now after we have made a trench in the silicon to isolate between device regions, a thin linear oxide layer of about (10 nm) at nearly 1100 °C will be thermally deposited on the trench surface with the same technique of the first deposited oxide layer.

The propose of this thin thermally deposited oxide layer is that it produces a better silicon/silicon dioxide interface and the high temperature process will round the corners of the trench and reduce the problems of sharp corners.

### **Thick oxide layer**

After the trench applying the thick oxide called field oxide, a thick applied by CVD (chemical vapor deposition) with amorphous structure of  $\text{SiO}_4$  tetrahedra with an empirical formula  $\text{SiO}_2$ . It is important in this process to make sure that no voids or gaps happened in the trench. That may happen if deposition happened in the top part before lower one.

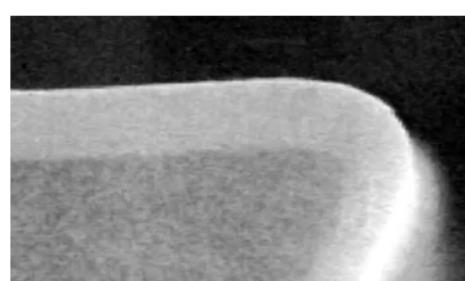
Fig (7). STI formed on the silicon substrate

### **deposition:**

production and layer which is oxide layer will be

The required oxide thickness is more than 400 nm to be able to fill all the trench region perfectly so we will deposit 500 nm thickness of silicon dioxide layer with plasma enhanced chemical vapur deposition (PECVD) to enture the increase diffusivity of deposited oxide at tempreture of 300 °C. this process provides good step coverage to avoid gabs that may be made during filling the trench as shown in fig (8).

Typical rate of PECVD oxide deposition is 50 nm/min which means to deposit 500 nm the time required is about 10 minutes.



## **Polishing The Excess of SiO<sub>2</sub>:**

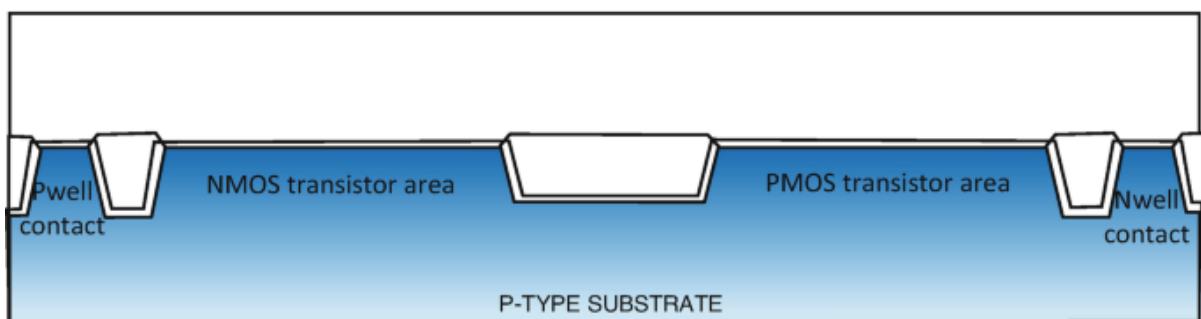
Some SiO<sub>2</sub> remained non uniform on the top, so this process is mandatory to leave a planar substrate. This (Chemical –Mechanical wafer is placed in a and the top part is PH =8 silica slurry.

Fig (8). Good step coverage using PECVD.

process uses CMP Polishing). The polishing machine polished by high

Following the CMP process for silicon dioxide, the remaining nitride is stripped off selectively using wet etching with hot phosphoric acid (H<sub>3</sub>PO<sub>4</sub>) at 140°C and the thin layer of the pad oxide removed using HF.

To get the final structure as shown in figure (9).



## **N well Formation:**

This process is done by applying a photoresist on the supposed area for PMOS and the exposed area will be doped to form N well region. N-doping is done by using phosphorous due to its high diffusivity in substrate and consumes low energy to be implemented.

Firstly, we use  
701 (14cps) of

Fig (9). STI after removing oxide and nitride layer

photoresist \_AZ® MIR  
about 1um thickness

and spin rate of 35000 rpm to expose the areas where N well will be formed by using ion implementation as the process involves accelerating a beam of ions towards the target material, where they collide with atoms and form a new, modified layer with altered electrical, optical, and structural properties.

Since sometimes damage of the substrate can happen due to bombardment of dopant into the silicon which dislocate some ions of silicon leading to damage of the substrate, but this damage can be solved by annealing process done at 800°C for about 30 minutes.

Since the node applied here is 350 thickness of the 2.8 um with dopant This process cycle be done at 1000°C and since the typical energy for implanting phosphorus is from 300 to 400 KeV, we are working on energy of 350KeV.

Fig (11), N-well implantation

technology that is nm, so we can let N-well equals about dose of  $10^{16} \text{ cm}^{-2}$ .

takes about 4 hours

By using these parameters, we can calculate ion concentration at junction depth of 2.8 um and to plot the impurity Concentration vs. Substrate Depth for above Parameters as shown in figure 10.

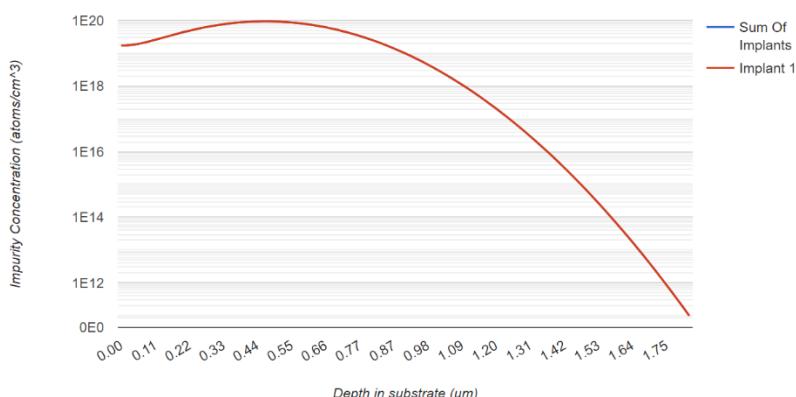
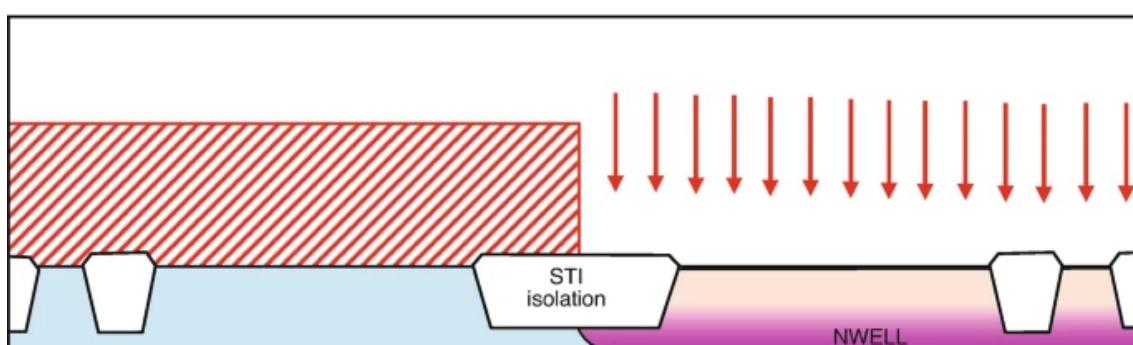


Fig (10), impurity Concentration vs. Substrate Depth

As peak concentration form figure 10 is nearly 1E20 atoms/cm<sup>3</sup> at 0.55um depth.

Also figure 11 shows the process of N-well formation and this process also is done mostly in inert ambient as no additional oxidation is needed.



## Threshold (turning on) voltage:

Isolation trench purpose is to isolate the two devices, and it can have the highest threshold voltage possible by increasing the doping and thickness of field oxide as much as we can to keep the cmos turned off.

After N-well implanting, the most important step comes which is determine threshold voltage as both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called sub-threshold current) through the device drops exponentially. The value of  $V_{th}$  is positive for NMOS and negative for PMOS as  $V_{th}$  equation is shown in equation (1).

$$v_{TH} = V_{FB} + 2\phi_f + \frac{\sqrt{2\epsilon_s q N_A (2\phi_f)}}{C_{OX}} + \frac{Q_t}{C_{OX}} \quad (1)$$

$V_{FB}$  is the gate voltage required to compensate the work function between gate and substrate,  $\epsilon_s$  is the relative permittivity of silicon and  $N_A$  is the dopant concentration in silicon and  $C_{OX}$  the oxide capacitance,  $Q_t$  is the implant dose

we can see from equation (1) that  $V_{th}$  is inversely proportional with  $C_{OX}$  and  $V_{FB}$  is the flat band voltage that can be calculated from following equation: [(Work function of gate material) - (work function of substrate) - (charge density)  $Q_{ss}$ / (capacitance of oxide layer)  $C_{OX}$ ].

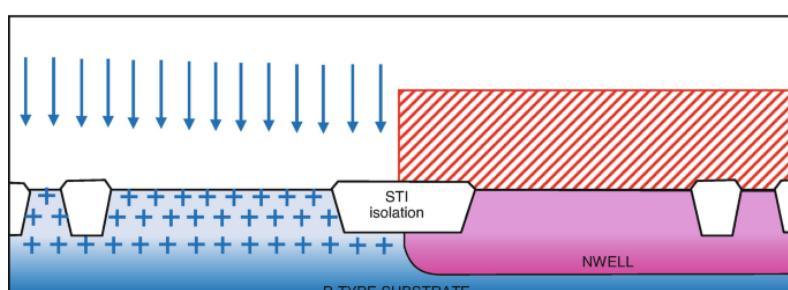
The  $C_{ox} = \frac{\epsilon}{t_{ox}}$  as  $t_{ox}$  is the gate oxide thickness that is 5.7 nm (0.057 um).

Work function if silicon is 4.85 eV and for silicon dioxide is nearly 5 eV.

$V_{th}$  is in the range of 0.5:0.8 V with the same value for NMOS and PMOS devices but it's negative for PMOS and positive for NMOS.

## NMOS transistor turn-on voltage:

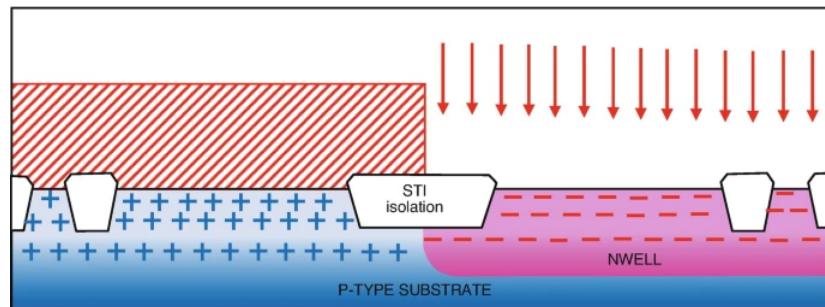
The process of turning-on voltage of threshold voltage is done by a process of implanting p-type dopant in the channel to increase p-type doping near surface. As more p-type dopant is implanted at slightly higher energy to increase p-type doping under the transistor channel between the source and drain diffusions. If the temperature used is very high this will increase dopant implantation under isolation region which causes increasing in turning-on voltage, so this leads to that the NMOS always remains off. A mask is utilized to expose the areas containing NMOS devices as shown in figure 12.



## PMOS transistor turn-on voltage:

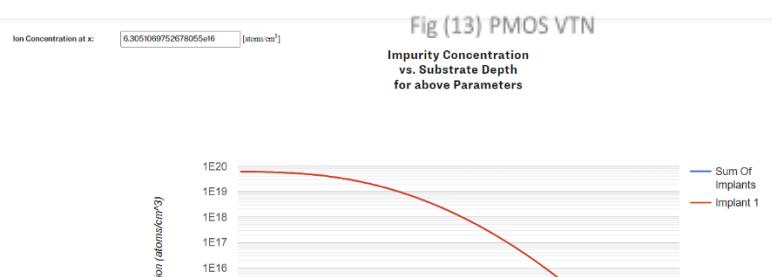
A photoresist pattern to adjust the turn ON voltage (VTP) of the core PMOS transistors is now printed on the wafer. The VTP implant pattern opens NWELL regions where core PMOS transistors are to be built and blocks PWELL regions where NMOS transistors are to be built.

An Fig (12) NMOS VTN n-type dopant is implanted to adjust the n-type doping near the surface of the NWELL so that the turn ON voltage (VTP) of the core PMOS transistor meets specification.



## n- doping in the PMOS part:

This is phosphorus implantation for about 200 nm with ion dose of  $10^{15}$  [ion/cm<sup>2</sup>] at 1100°C at 30 KeV for about 1 minute as shown in figure 14.



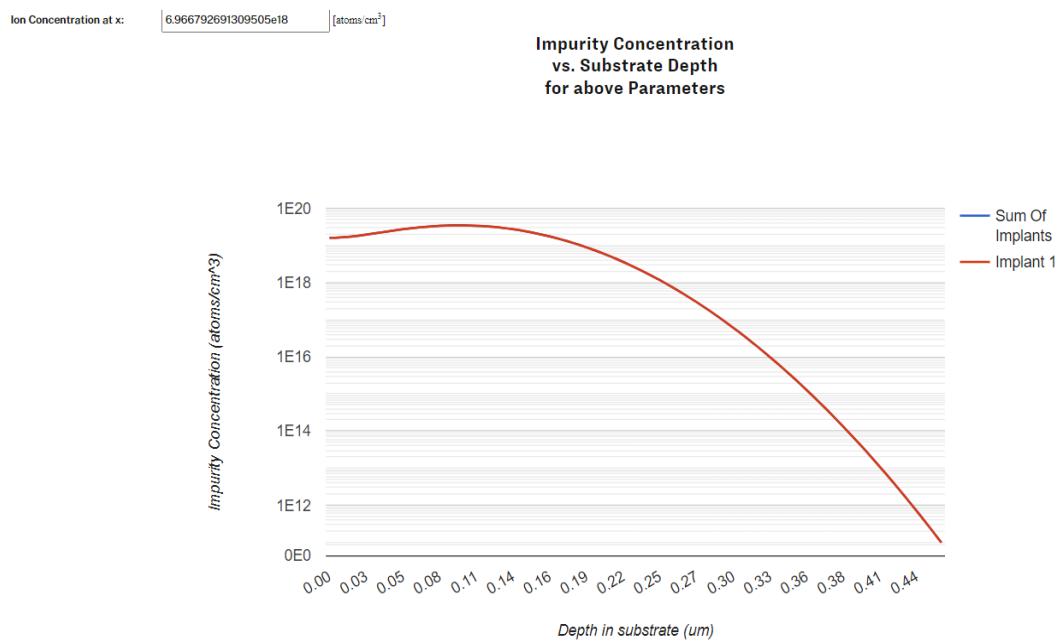
## p- doping in NMOS

Same process  
but here the dopant in  
figure 15.

Fig (15) phosphorus implantation

part:

done at PMOS part  
boron as shown in



## Gate oxide forming:

Oxide

Fig (14) boron implantation

removal:

First step here is to remove all the oxide layer as it's too thick and got exposed to many implanting processes with chemical etching using HF acid by rate of 1 angstrom/second. From the figure 16 we use 3% concentrated HF.

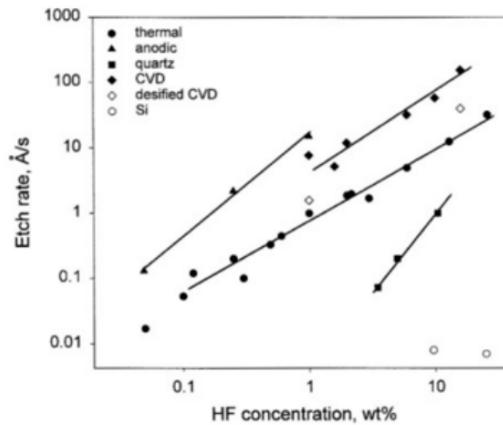


FIGURE 4.2. Etch rate of different silicon oxides as a function of HF concentration.

### Gate Oxide

Fig (16) etch rate with HF concentration

forming:

#### Gate

oxide used in the isolation trench but here it's so much thinner layer made of dielectric silicon dioxide, its purpose is to separate the gate terminal form of the MOSFET from the underlying source and drain terminals.

Gate oxide is about 5.7 nm with dry thermal oxidation at 800°C, this process will take about an hour as shown in figure 17.

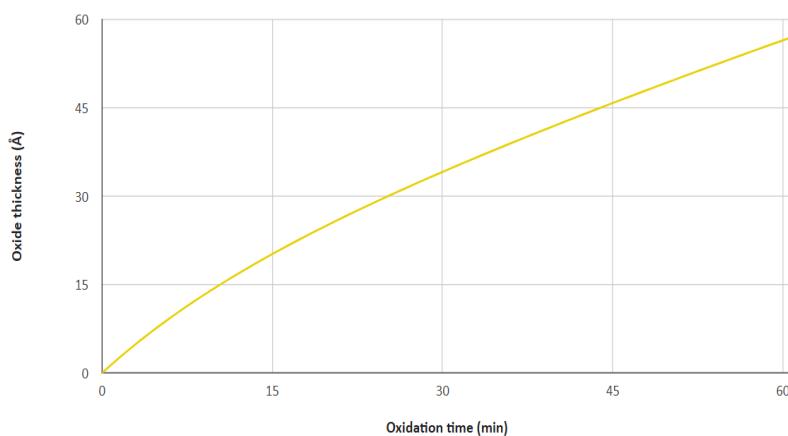


Fig (17) oxide thickness vs time

The process of adding the gate oxide is critical so it has to be with high quality oxide and surface with no defects.

### Polysilicon layer:

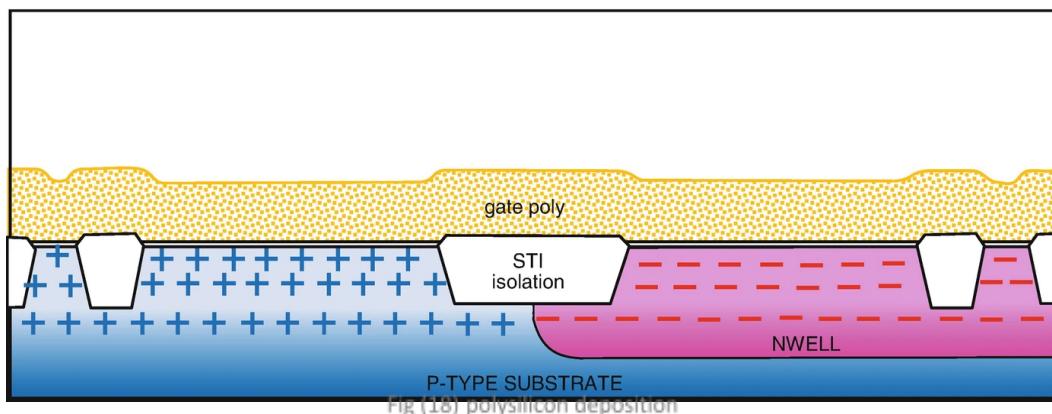
After applying layer of gate oxide, now a layer of polysilicon will be deposited using LPCVD (low pressure chemical vapor deposition) all over the wafer and at this process silane is added by thermal deposition with H<sub>2</sub> as a by product and produce the layer of SiH<sub>4</sub>. Figure 18 shows polysilicon deposition.

The applied polysilicon layer is about 350 nm at 600 °C and 50 torr. After that the polysilicon is N doped with phosphorus, but due to that phosphorus is highly soluble in silicon and polysilicon and distribute quickly so the doping energy is not critical here as the phosphorus won't penetrate to gate oxide of the substrate.

The applied N<sup>+</sup> dose also is not critical but has to be as high as possible to obtain low poly sheet resistance of about  $5 \times 10^{13} \text{ cm}^{-2}$  this done at nearly 1 hour.

Since poly sheet resistance is relatively high to metal layer, so long interconnects between devices is not made by polysilicon, it's only used in wiring between active devices.

Finally, the polysilicon is etched from the parts that don't need polysilicon by plasma etching with chlorine to achieve high resistivity.



### Gate patterning:

A photoresist gate pattern is formed on the polysilicon. The transistor gate pattern is the most critical pattern on an integrated circuit. The most advanced photoresist chemistry, the most advanced optical proximity correction, and the most advanced photolithography tools are used at this process. Figure 19 shows gate patterning using photoresist.

the selected photoresist for this process is AZ5214E positive photoresist over the polysilicon with 1.40 um thickness with 4000 rpm spin. For all the required data in this process look at table 1.

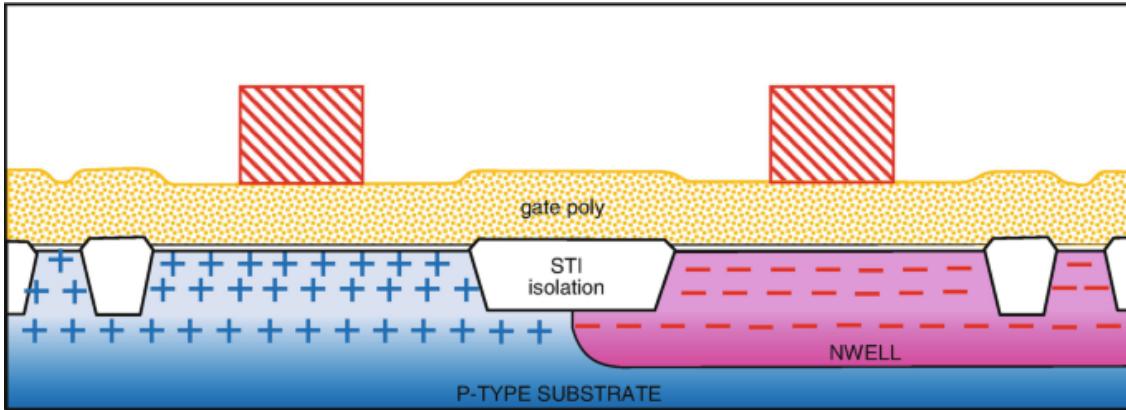
#### FILM THICKNESS [μm] as FUNCTION of SPIN SPEED (characteristically)

spin speed [rpm]	2000	3000	4000	5000	6000
AZ 5214E	1.98	1.62	1.40	1.25	1.14

#### PROCESSING GUIDELINES

Dilution and edge bead removal	AZ EBR Solvent
Prebake	110°C, 50", hotplate
Exposure	broadband and monochromatic h- and i-line
Reversal bake	120°C, 2 min., hotplate (most critical step)
Flood exposure	> 200 mJ/cm² (uncritical)
Development	AZ 351B, 1:4 (tank, spray) or AZ 726 (puddle)
Postbake	120°C, 50s hotplate (optional)
Removal	AZ 100 Remover, conc.

Table (1). AZ5214E positive photoresist



**LDD formation  
(drain) extensions:**

**(lightly doped**

The purpose of this step is to grade dope NMOS and PMOS parts with N and P type dopants as this allows to drop drain voltage over larger distance and reduce the peak value of electric field in the near drain regions, which then improve the efficiency of the device.

N type doping in N\_well region:

This done with phosphorus or arsenic is ion implanted in low energy with dose about  $1 \times 10^{15} \text{ cm}^{-2}$  and to thickness of 30 nm at  $1100^\circ\text{C}$  for 20 minutes and at 30KeV to get ion concentration of  $2.04 \times 10^{19} \text{ cm}^{-3}$ . Figure 20 shows this relation.

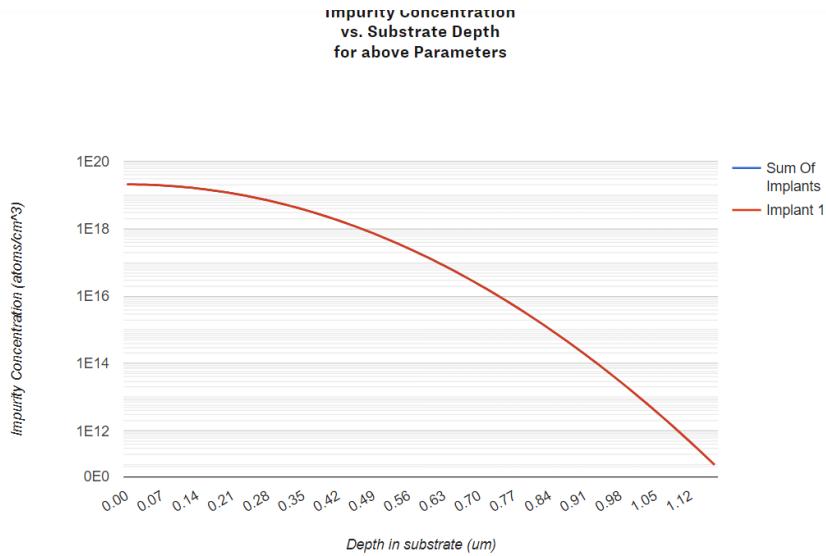


Fig (20) phosphorus LDD implantation

Same process goes in the PMOS part but with boron as a dopant. And figure 21 shows this to get ion concentration of  $1.77 \times 10^{19} \text{ cm}^{-3}$

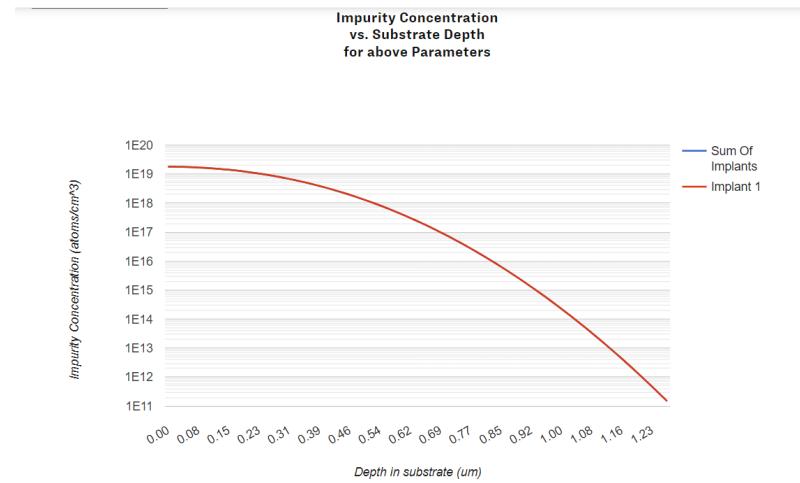


Fig (21) boron LDD implantation

**Side wall**

**Spacers:**

After the source/drain extensions are formed, dielectric sidewalls are formed on the vertical sides of the transistor gates to define the spacing between the deep source and drain diodes. The thickness of thin layer is tightly controlled with uniform thickness as a thin layer of silicon oxide that is exposed by LPCVD. This thickness is viewed figured 22.c that shows the relation between spaces width and polysilicon layer.

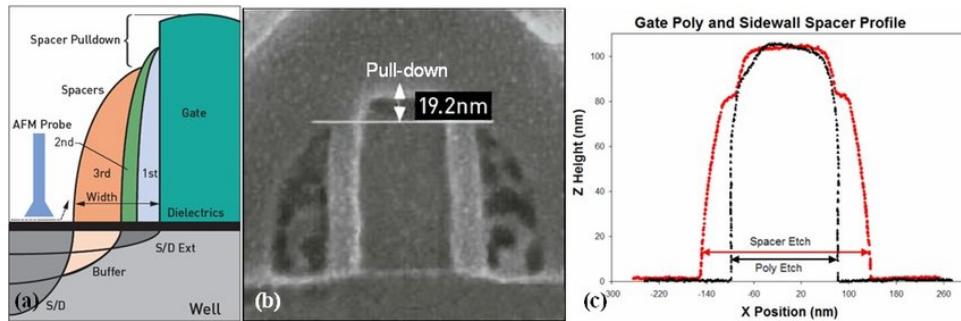
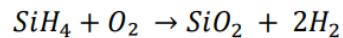


Fig (22) sidewall spacers

If  $\text{SiO}_2$  is used, it  
a  $\text{SiH}_4 + \text{O}_2$  reaction  
silicon oxide at the end through

could de- posited by  
at about  $400^\circ\text{C}$  to get  
the following reaction:



After the deposition of spacers on the whole surface it must be etched from all the surface except for the vertical sides of the blocks of polysilicon this can be done by fluorine-based plasma etcher that is can work completely with anisotropic etching (high directionality) to avoid removing any polysilicon or other layers.

### Source and drain formation:

Figure 23 shows the main steps that done tell now, and the source and drain regions.

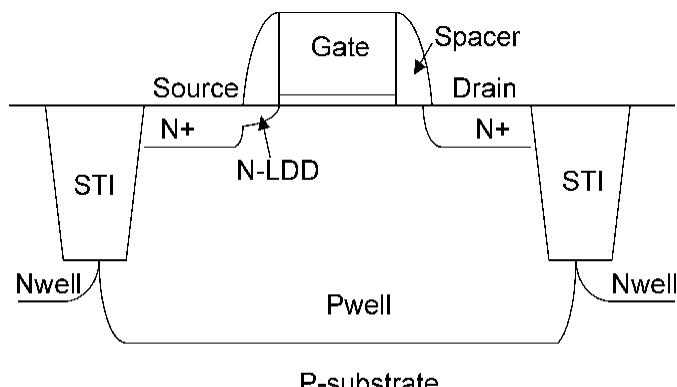


Fig (23) main structure

### Oxide layer forming:

An oxide of 10 nm is applied above the exposed surface, dry oxidation at 900°C.

### Apply photoresist:

AZ5214E positive photoresist is applied for 0.5um with the other parameters mentioned in previous steps.

### Arsenic doping with masking:

NMOS area will now be doped with arsenic of  $4 \times 10^{15} \text{ cm}^{-2}$  at 75 KeV. This energy will allow arsenic to penetrate screen oxide but still be easily masked by the photoresist.

### Boron doping with masking:

PMOS area will be doped with boron with dose of  $3 \times 10^{15} \text{ cm}^{-2}$  at 10 KeV. This energy is much less than the energy in arsenic doping because boron is much lighter.

### Furnace annealing:

This is the final step here that is a rapid thermal annealing (RTA) for about 1 minute at 1050 °C that drives junctions to their final depth and correct all the damages in the structure as it activates the dopants (replace silicon atoms in the single crystal silicon lattice with dopant atoms)

Figure 24 shows the structure after source and drain formation.

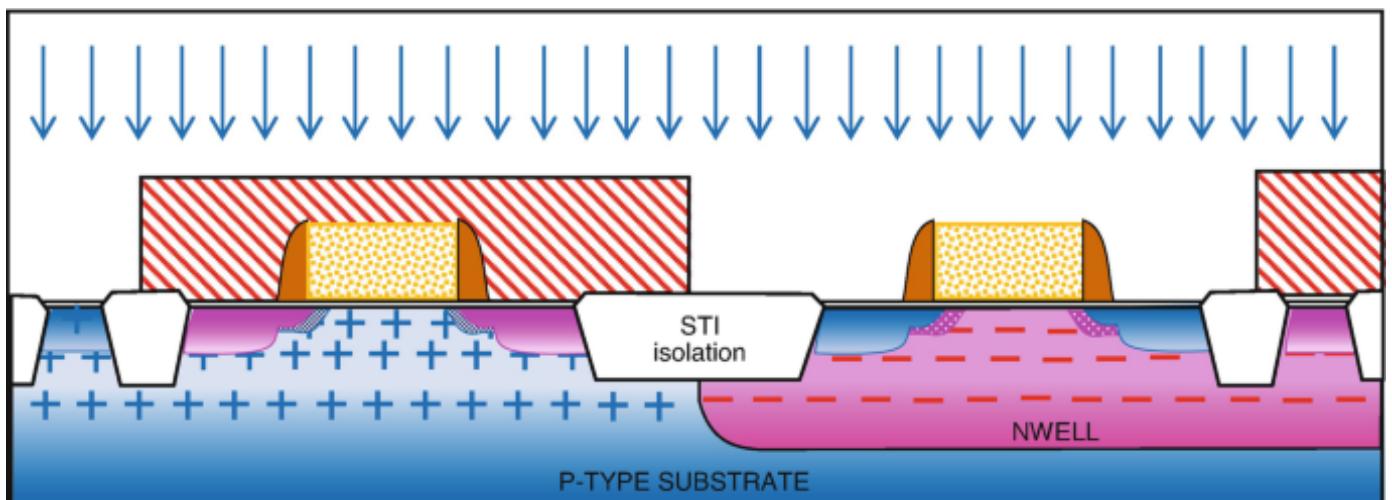


Fig (24) structure after source and drain

## Silicide layer:

It's a metallic nickel (sometimes with platinum and titanium nitride) is deposited onto the wafer and reacted for several seconds using rapid thermal anneal (RTA) at a temperature of about 300 °C for 30 seconds with thickness of 15nm layer. as in figure 25.

The nickel metal reacts with the exposed silicon to form a mixture of NiSi and Ni<sub>31</sub>Si<sub>12</sub> crystalline phases of nickel silicide. Over dielectric regions, where silicon is not exposed, the nickel does not react with SiO<sub>2</sub> and remains nickel metal.

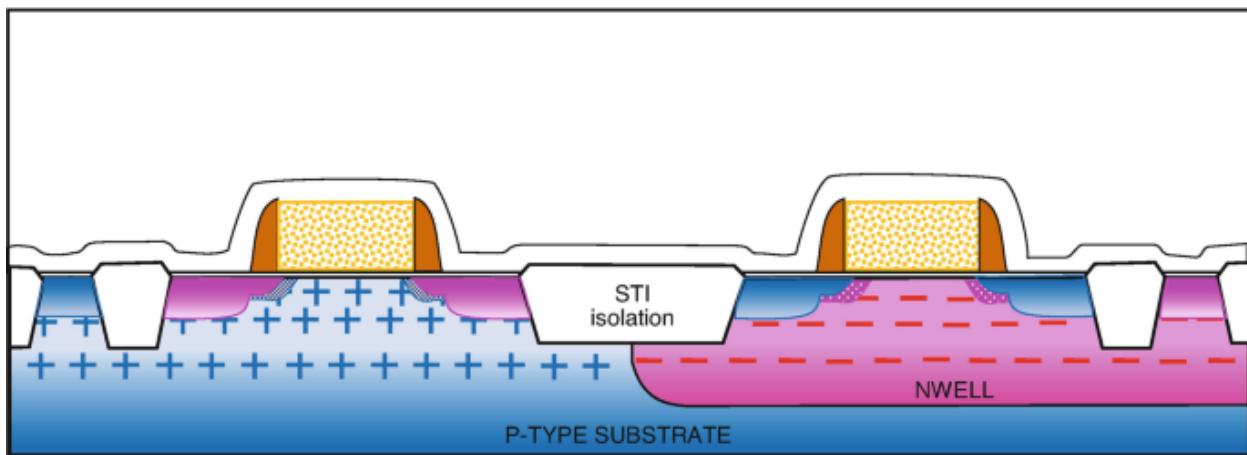


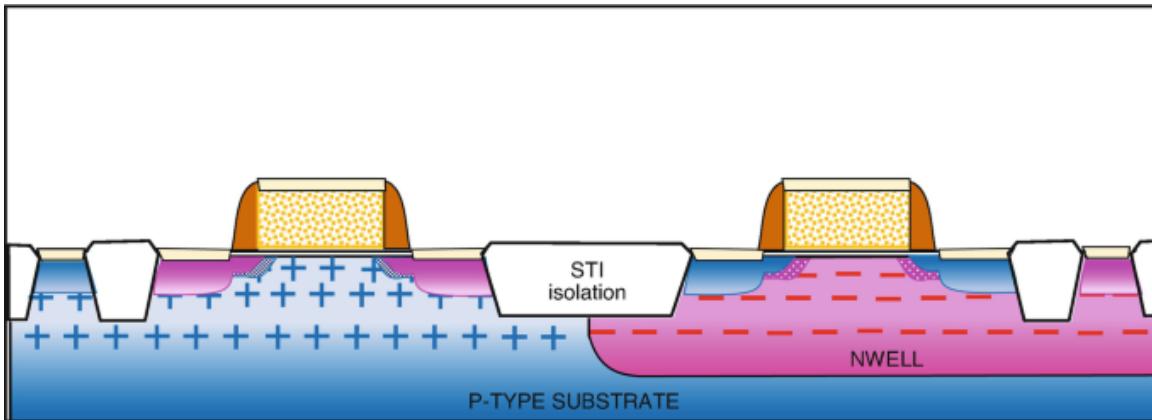
Fig (25) silicide deposition

after that the nickel metal is etched by dipping the whole wafer in liquid etching bath that etches metallic nickel without etching nickel silicide. The following table2 shows etching chemistry for nickel.

Phase	Etchant	Temp (°C)	Etch rate (nm/min)
Solution	30 HNO <sub>3</sub> :10 H <sub>2</sub> SO <sub>4</sub> :50 HAc:10 H <sub>2</sub> O	85	10 000
	80% H <sub>3</sub> PO <sub>4</sub> + 5% HNO <sub>3</sub> + 5% HAc + 10% H <sub>2</sub> O	50	29
	30% FeCl <sub>3</sub> + 4% HCl + 66% H <sub>2</sub> O	20	21
	3 HCl:1 HNO <sub>3</sub> :2 H <sub>2</sub> O	30	100
	50 H <sub>2</sub> SO <sub>4</sub> : 1 H <sub>2</sub> O <sub>2</sub>	120	380
Gas	Ar* 500 V ion milling	—	66
	50% CO + 50% NH <sub>3</sub> plasma	—	30–90
	20% Cl <sub>2</sub> + 80% Ar plasma	—	40

Table2.nickel etchers

to reach the following structure as shown in figure 26.



Now a second reduce resistivity of wafers are annealed microseconds using a thousandth of a second) anneal at a temperature of about 500 °C.

Fig (26) silicide after first annealing

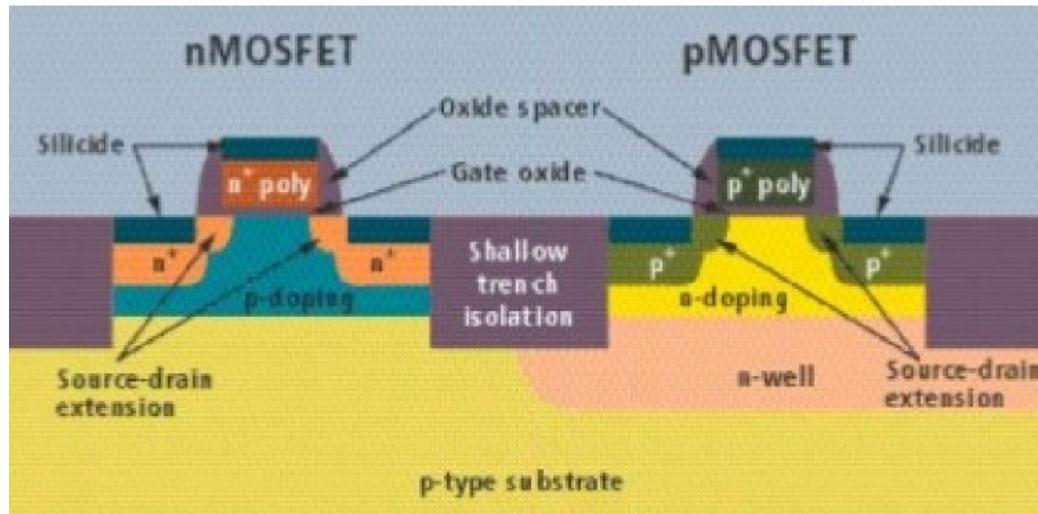
annealing happen to silicide layer. As the for a few spike (about a

### **metal layer:**

First metal level formation in CMOS (Complementary Metal-Oxide-Semiconductor) refers to the process of creating the initial layer of interconnects or metal wires in an integrated circuit (IC) that electrically connects the various active elements of the device, such as transistors, resistors, and capacitors. This process is crucial to the proper functioning of the IC as it establishes the foundation for signal transmission and power distribution throughout the chip. The metal interconnects are typically fabricated using materials like aluminum, copper, or their alloys, which offer low resistivity and high reliability.

The formation of the first metal level in CMOS technology involves several key steps. First, a layer of dielectric material is deposited on the substrate, over the active regions, to act as an insulating layer. Then, a patterned mask is created that defines the layout of the metal interconnects. Using this mask, a layer of metal is deposited selectively on the dielectric layer and etched away where it is not needed, forming the desired interconnect pattern. Finally, a passivation layer is applied to protect the metal interconnects from environmental factors and to prevent unwanted electrical interactions among the various components of the IC. This process may be repeated multiple times to create multiple layers of interconnects, as needed for complex circuits.

Here we reached the final structure that is shown in figure 27.



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Fig (27). Final structure.

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## Phase 3:

### Section I: Mesh:

#### # Meshing lines

```
line x loc=0 spac =0.5  
line x loc =2 spac =0.5  
line x loc =4 spac =0.5  
line x loc =6 spac =0.5  
line x loc =8 spac =0.5  
line x loc =10 spac =0.5
```

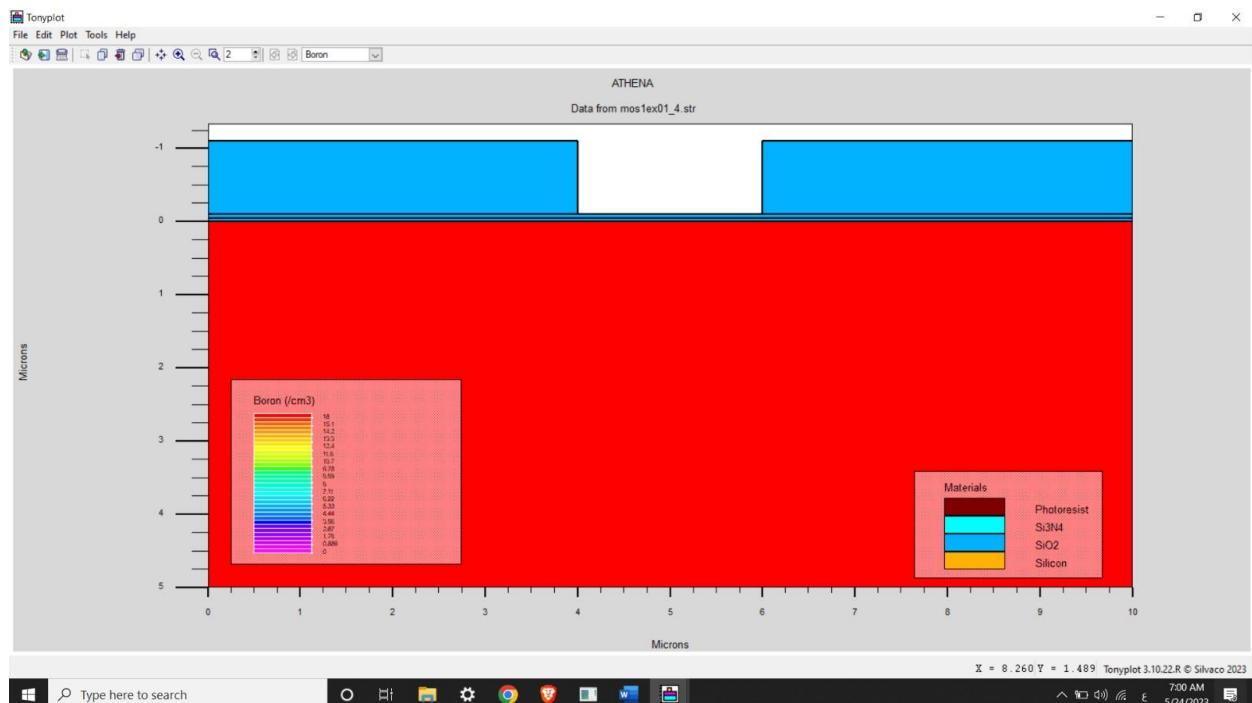
#### # Meshing lines

```
line y loc = 0 spac = 0.5  
line y loc = 2 spac = 0.5  
line y loc = 3 spac = 0.5  
line y loc = 4 spac = 0.5  
line y loc = 5 spac = 1
```

### Section II: Choose substrate:

#### # Initialization

```
init orientation=100 c.boron=10e15 space.mul=2  
structure outfile=mos1ex00_0.str
```

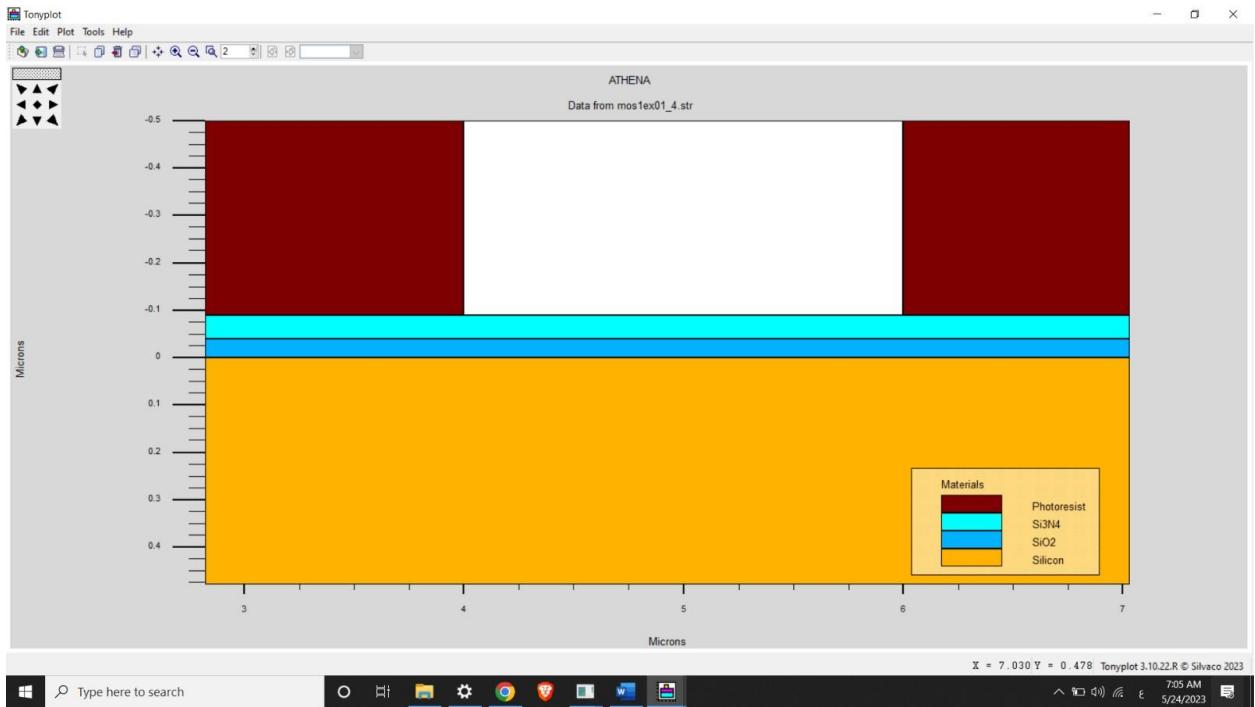


### Section III: Oxide layer:

#### # Oxide layer

deposit oxide thickness=0.04

```
structure outfile=mos1ex01_0.str
```



## Section IV: LPCVD Silicon Nitride :

#nitride layer

deposit nitride thickness =0.05

```
structure outfile=mos1ex02_0.str
```

#photoresist layer

deposit photoresist thickness=1

```
structure outfile=mos1ex01_3.str
```

#etch layer in photoresist

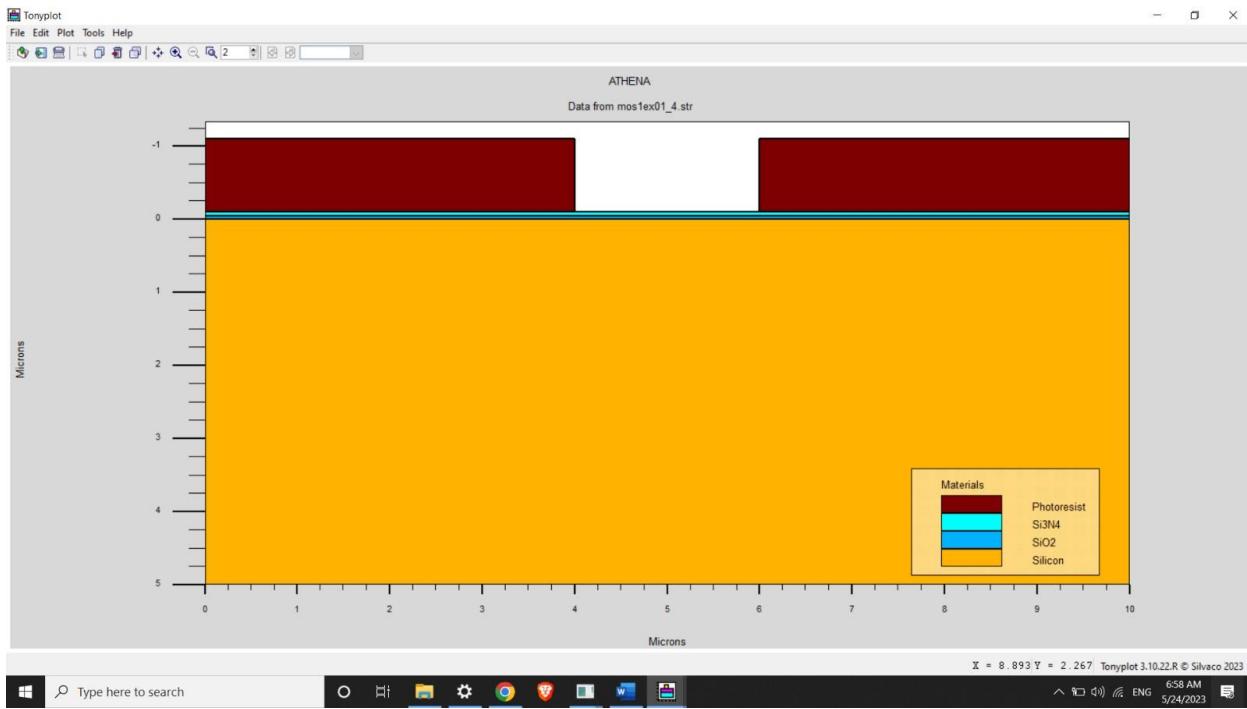
etch photoresist start x=4 y = 0.09

etch continue x=6 y = 0.09

etch continue x=6 y = -1.09

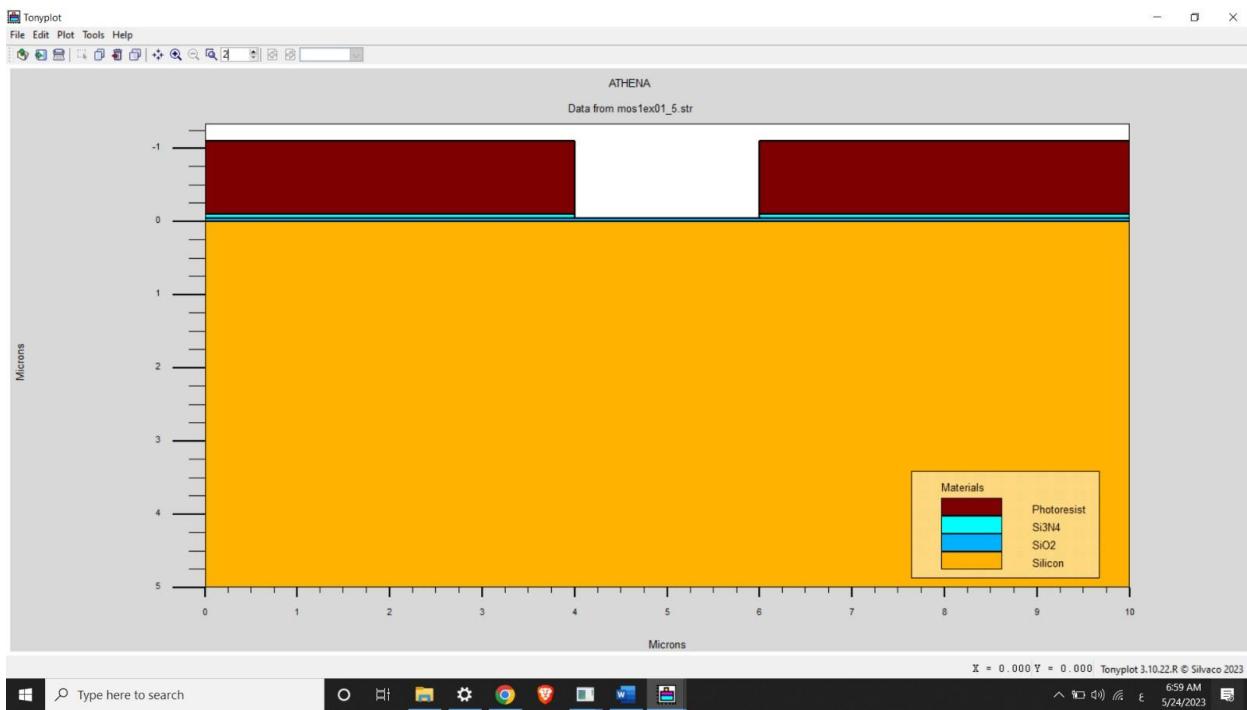
etch done x=4 y = -1.09

```
structure outfile=mos1ex01_4.str
```

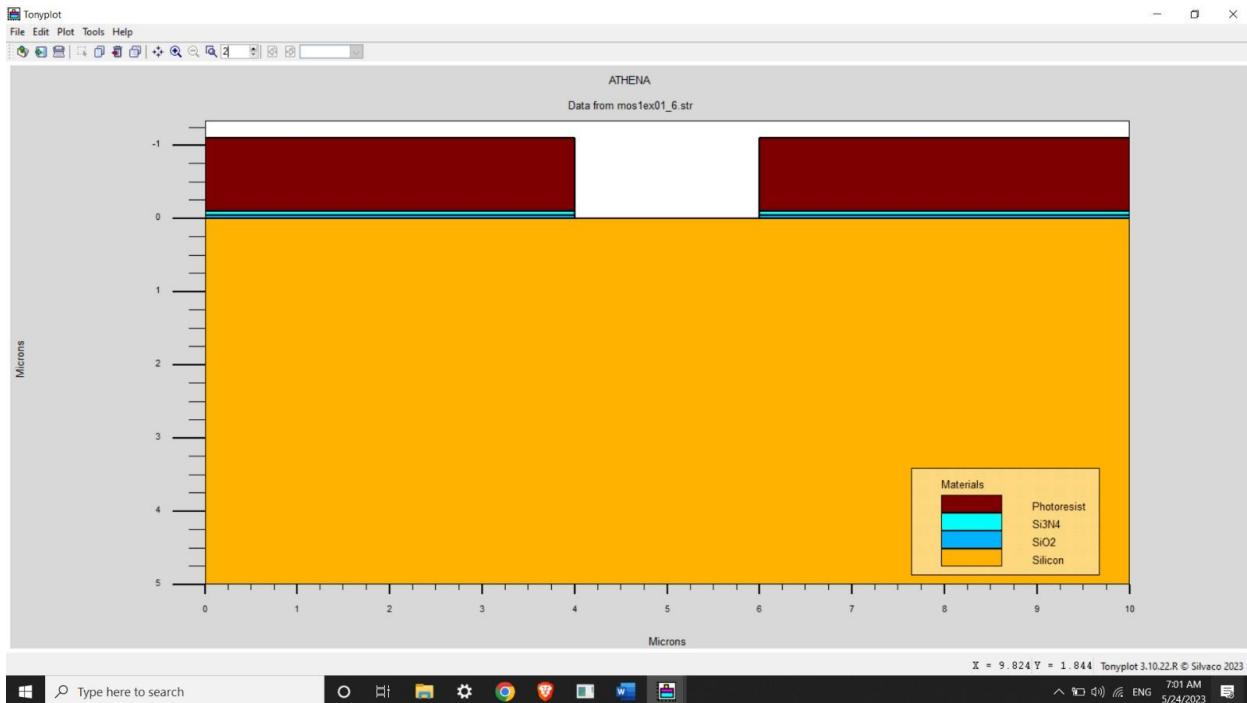


### # etch nitride

```
etch nitride start x=4 y=-0.04
etch continue x=6 y = -0.09
etch continue x=6 y = -0.04
etch done x=4 y = -0.09
structure outfile=mos1ex01_5.str
```



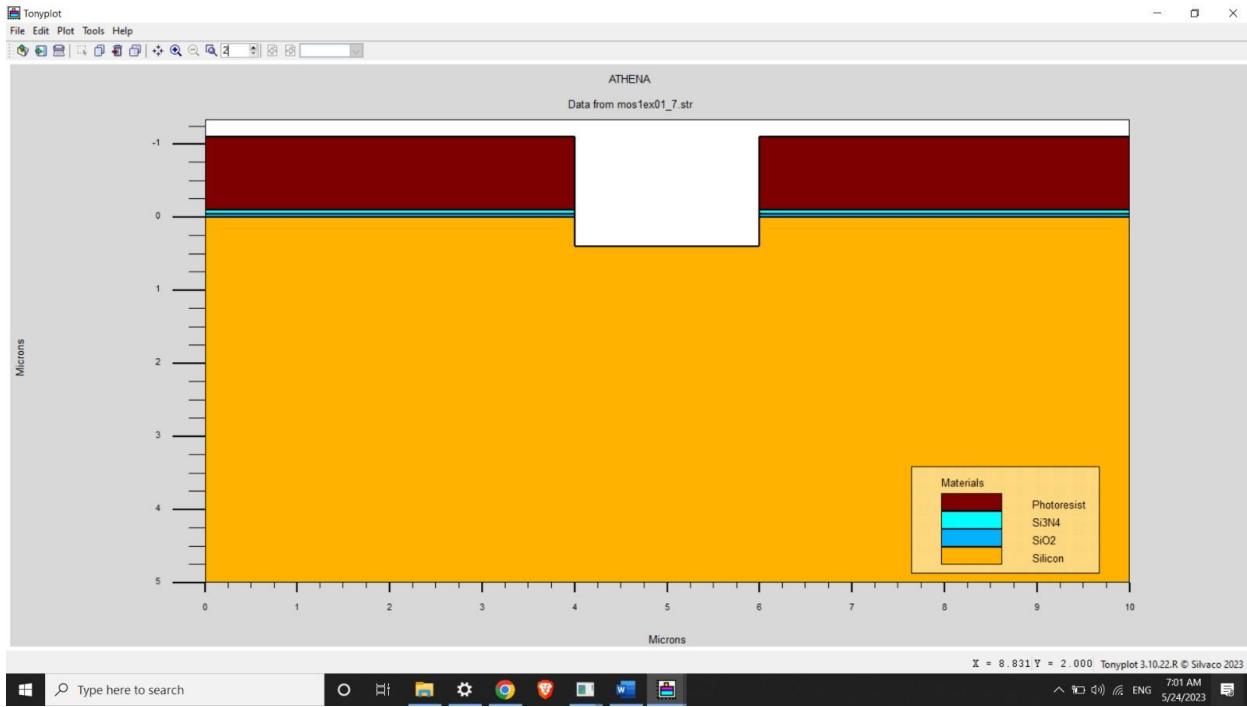
```
#etch oxide
etch oxide start x=4 y=0
etch continue x=6 y = 0
etch continue x=6 y = -0.04
etch done x=4 y = -0.04
structure outfile=mos1ex01_6.str
```



## Section V: Shallow trench isolation formation (STI):

#form trench

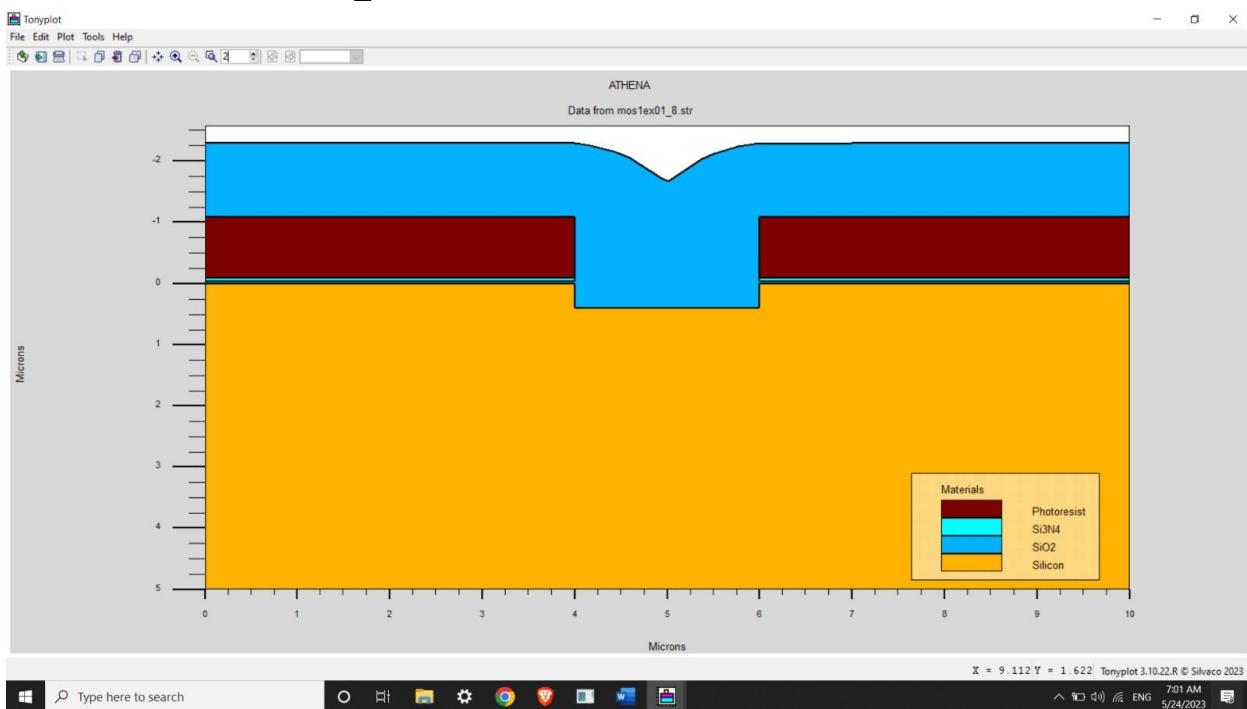
```
etch silicon start x=4 y = 0
etch continue x=6 y = 0
etch continue x=6 y = 0.4
etch done x=4 y = 0.4
structure outfile=mos1ex01_7.str
```



#oxide deposit

deposit oxide thickness=1.2

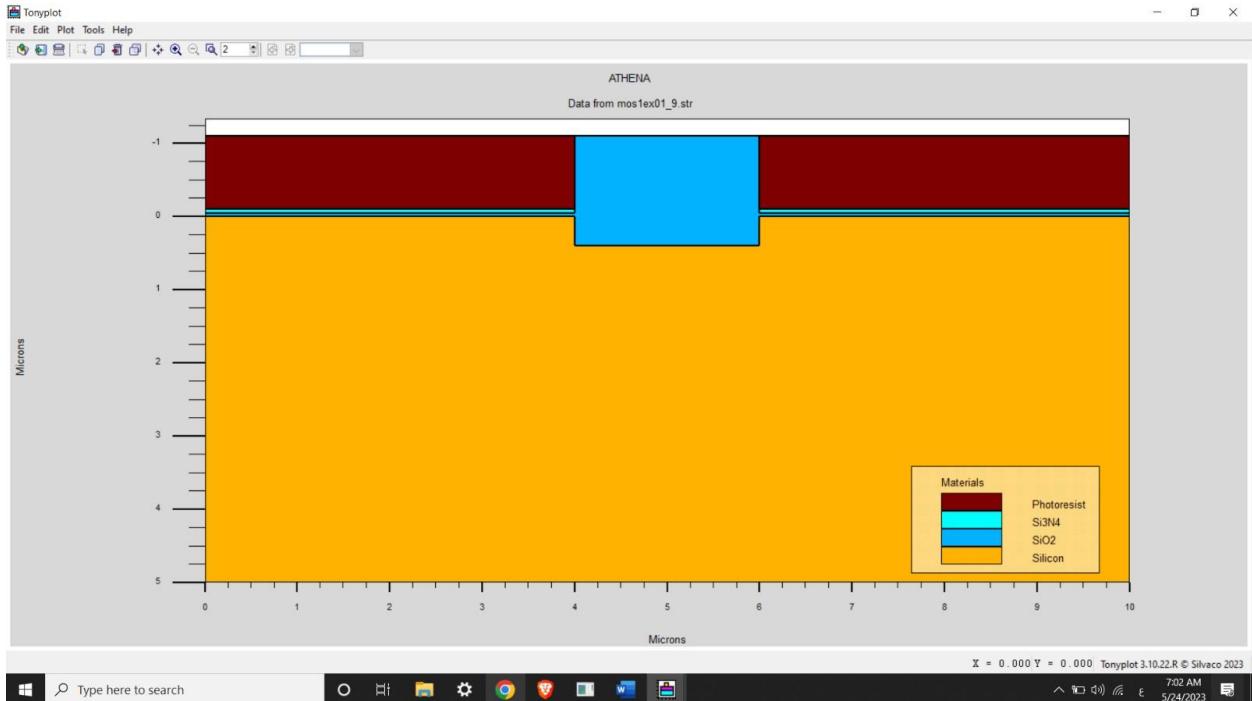
structure outfile=mos1ex01\_8.str



#oxide polishing

etch oxide start x=0 y=-1.09

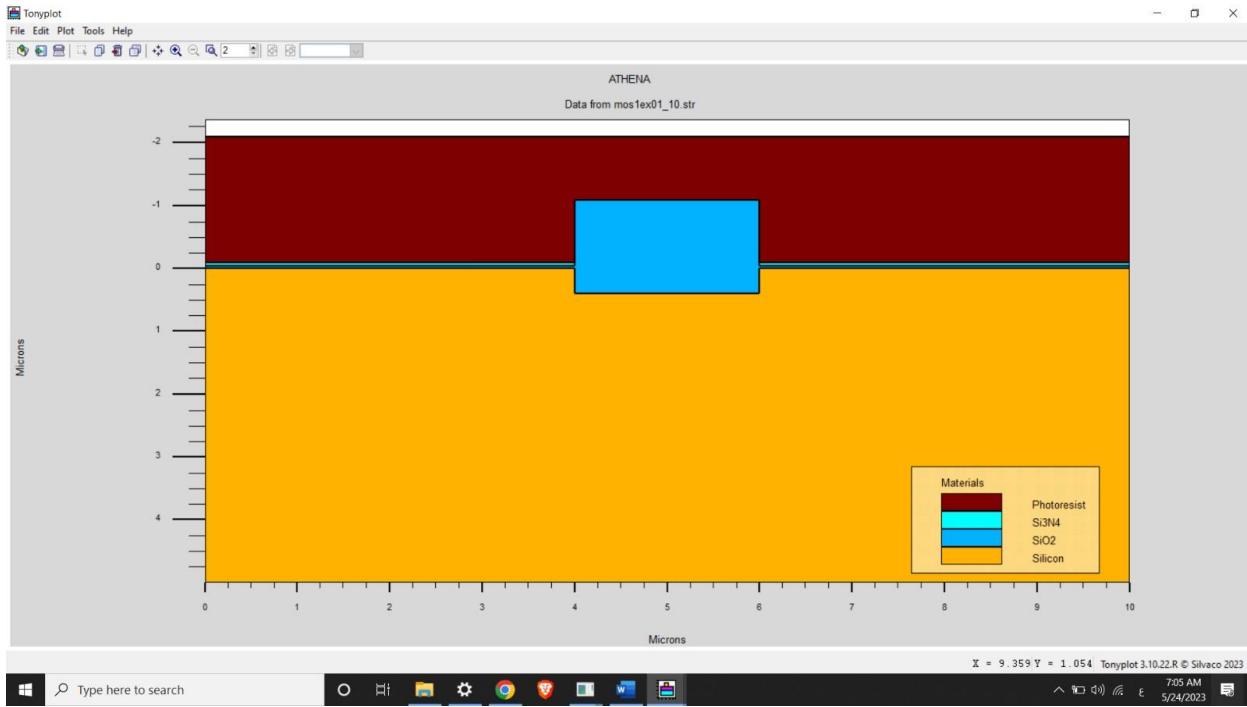
```
etch continue x=10 y =-1.09  
etch continue x=10 y = -2.6  
etch done x=4 y = -2.6  
structure outfile=mos1ex01_9.str
```



## Section VI: N well Formation:

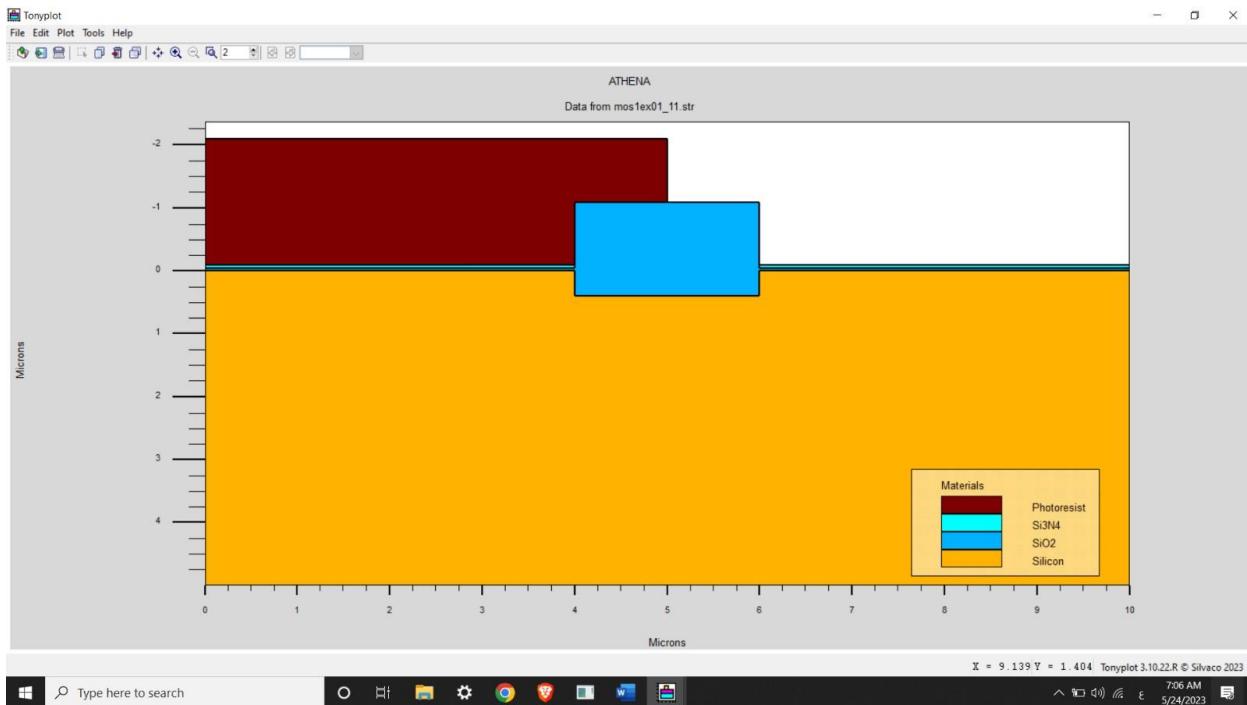
#apply photoresist for n-well formation

```
deposit photoresist thickness=1  
structure outfile=mos1ex01_10.str
```



#etch part

```
etch photoresist right p1.x=5
structure outfile=mos1ex01_11.str
```

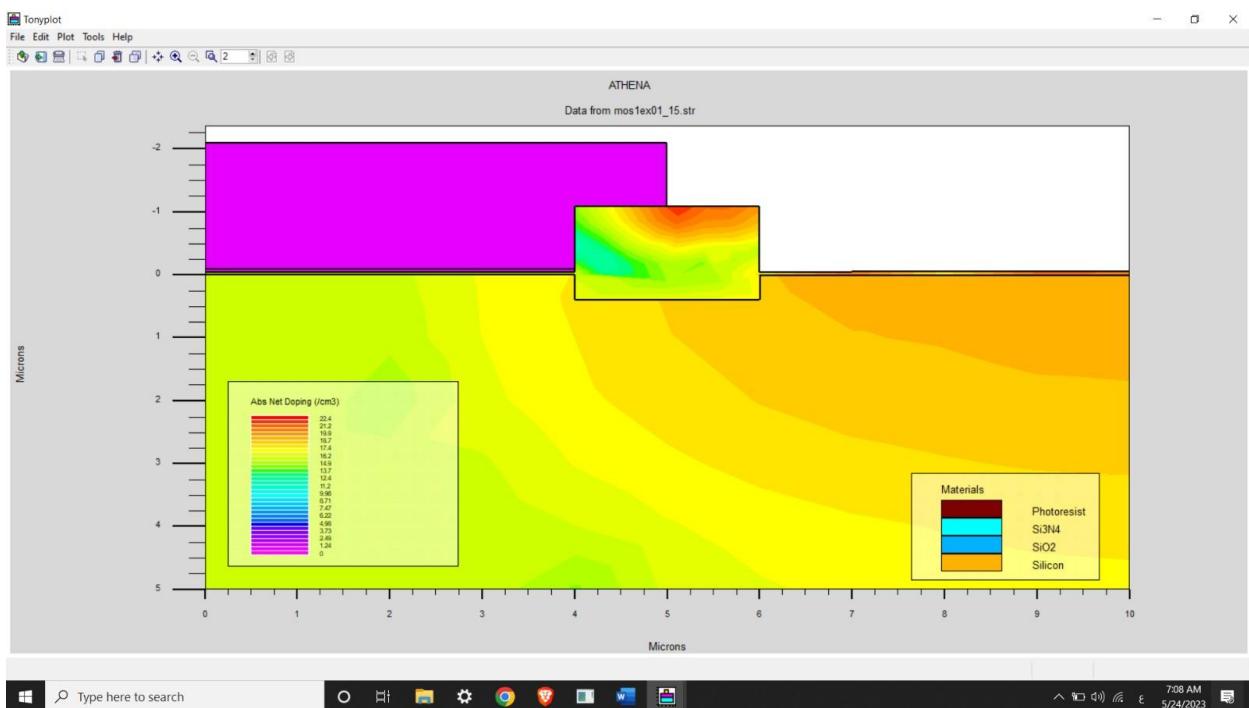


#etch nitride

```
etch nitride right p1.x=6
structure outfile=mos1ex01_12.str
```

```
#anneling  
anneal
```

```
#n-well formation  
IMPLANT phosph DOSE=1E16 ENERGY=350e3  
ADAPT.PAR DIFF.LEN=0.1 SILICON I.BORON  
DIFFUSE TEMP=1000 TIME=240 NITROGEN  
structure outfile=mos1ex01_13.str  
diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3  
diffus time=220 temp=1200 nitro press=1  
diffus time=90 temp=1200 t.rate=-4.444 nitro press=1  
structure outfile=mos1ex01_14.str
```

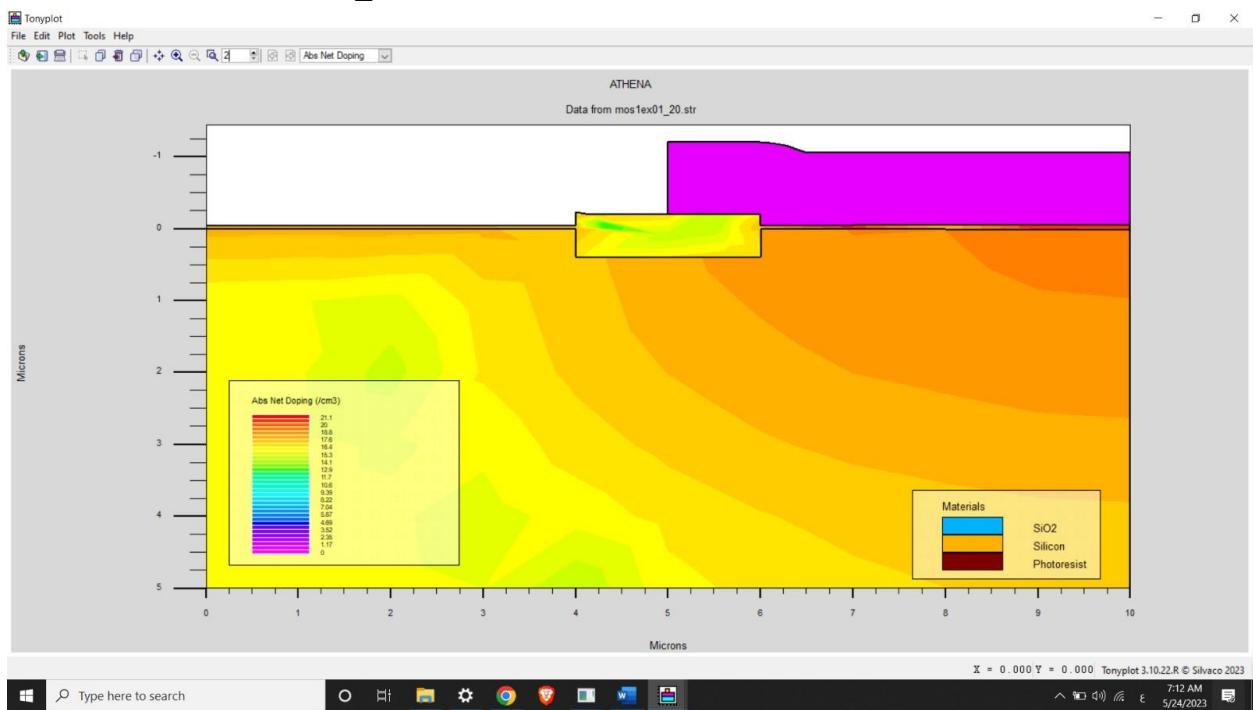


## Section VII: Threshold (turning on) voltage:

```
#vth adjustment nmos
```

```
implant boron energy =10 dose =5.0e12 persion
```

```
structure outfile=mos1ex01_20.str
```

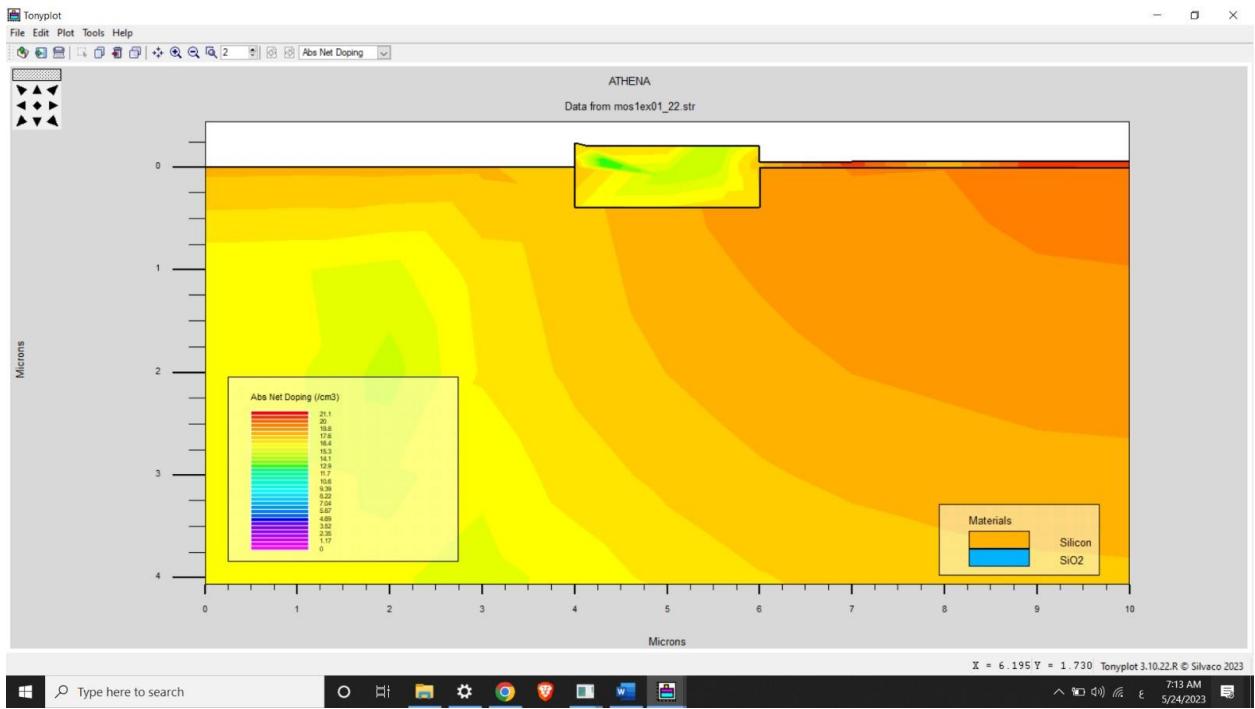


```
#etch
```

```
etch photoresist right p1.x=5
structure outfile=mos1ex01_21.str
#etch left oxide
etch oxide left p1.x=4
structure outfile=mos1ex01_22.str
```

```
#etch right oxide
```

```
etch oxide right p1.x=6
structure outfile=mos1ex01_23.str
```



## Section VII: Gate oxide forming:

# The growing of high-quality oxide in dry oxygen

deposit oxide thickness = $5.7 \times 10^{-3}$

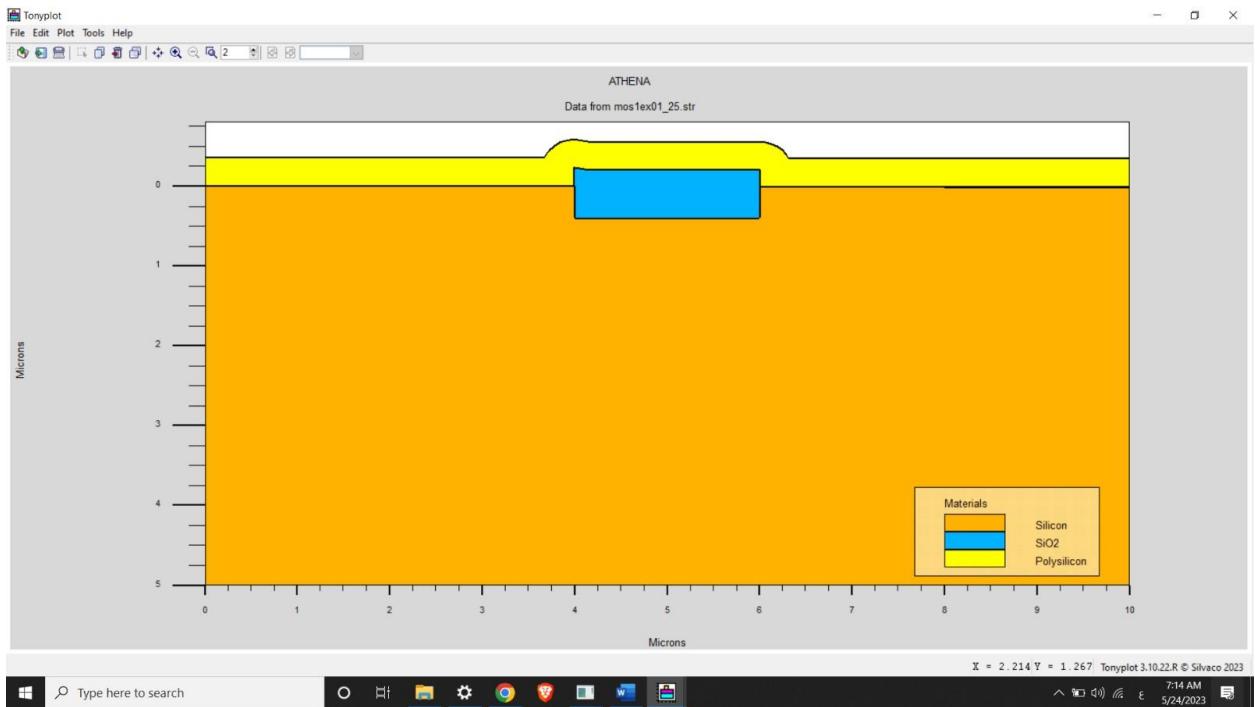
diffus time = 10 temp = 900 dryO2 press=1.00

structure outfile=mos1ex01\_24.str

# Poly deposition

depo poly thick= $350 \times 10^{-3}$  divi=10

```
structure outfile=mos1ex01_25.str
```



```
# Gate patterning
```

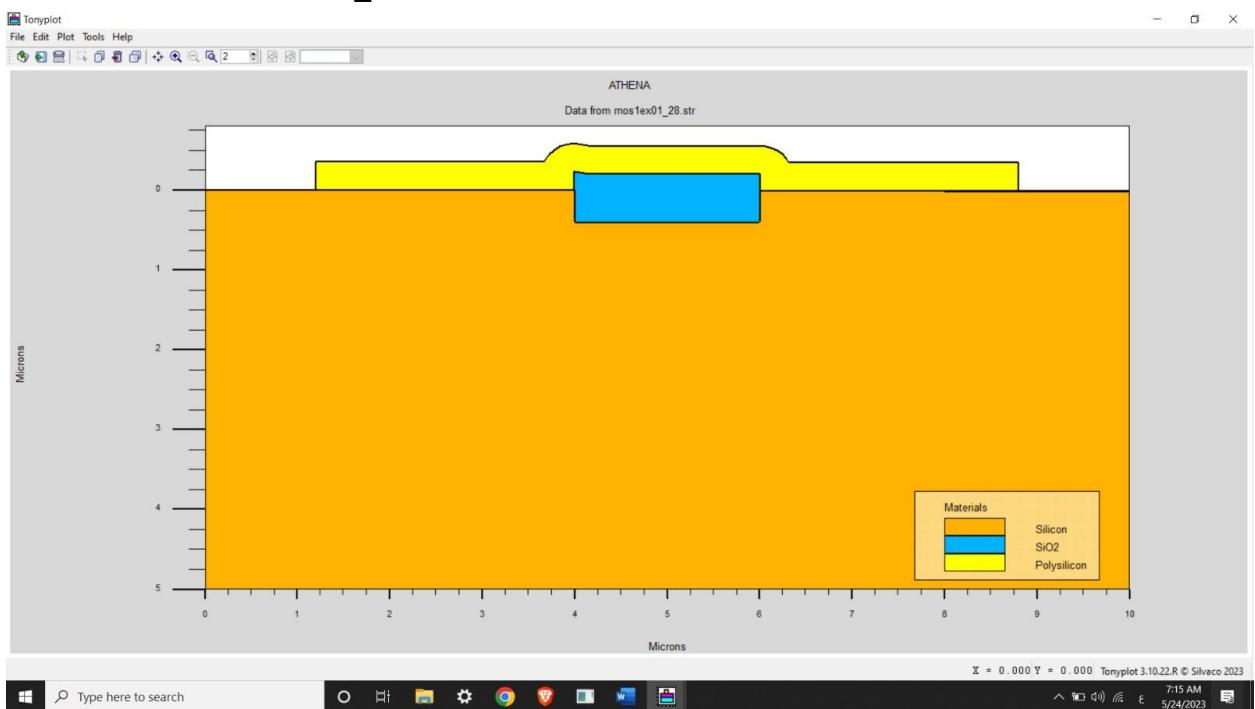
```
etch poly left p1.x=1.2
```

```
structure outfile=mos1ex01_27.str
```

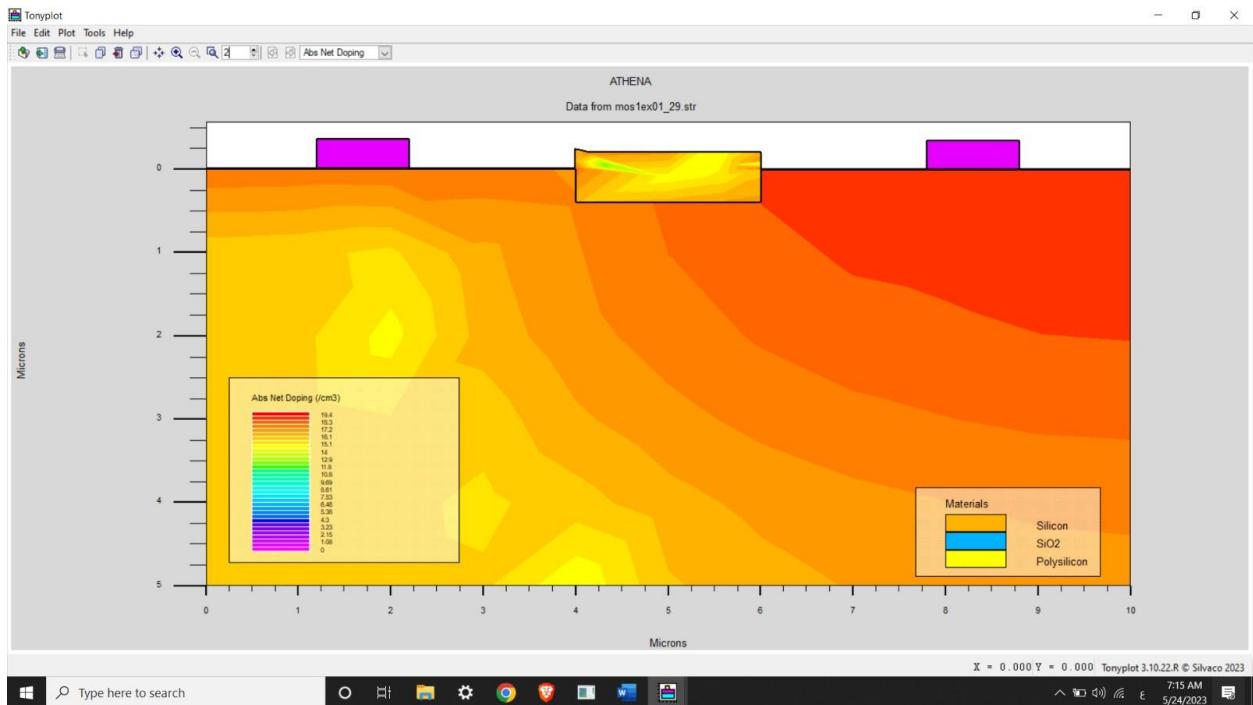
```
#etch2
```

```
etch poly right p1.x=8.8
```

```
structure outfile=mos1ex01_28.str
```



```
#etch 3
etch poly start x=2.2 y=0.2
etch continue x=7.8 y = 0.2
etch continue x=7.8 y = -2.4
etch done x=2.2 y = -2.4
structure outfile=mos1ex01_29.str
```



```
# Poly reoxidation
diffuse time=3 temp=900 weto2 press=1.0
```

structure outfile=mos1ex01\_30.str



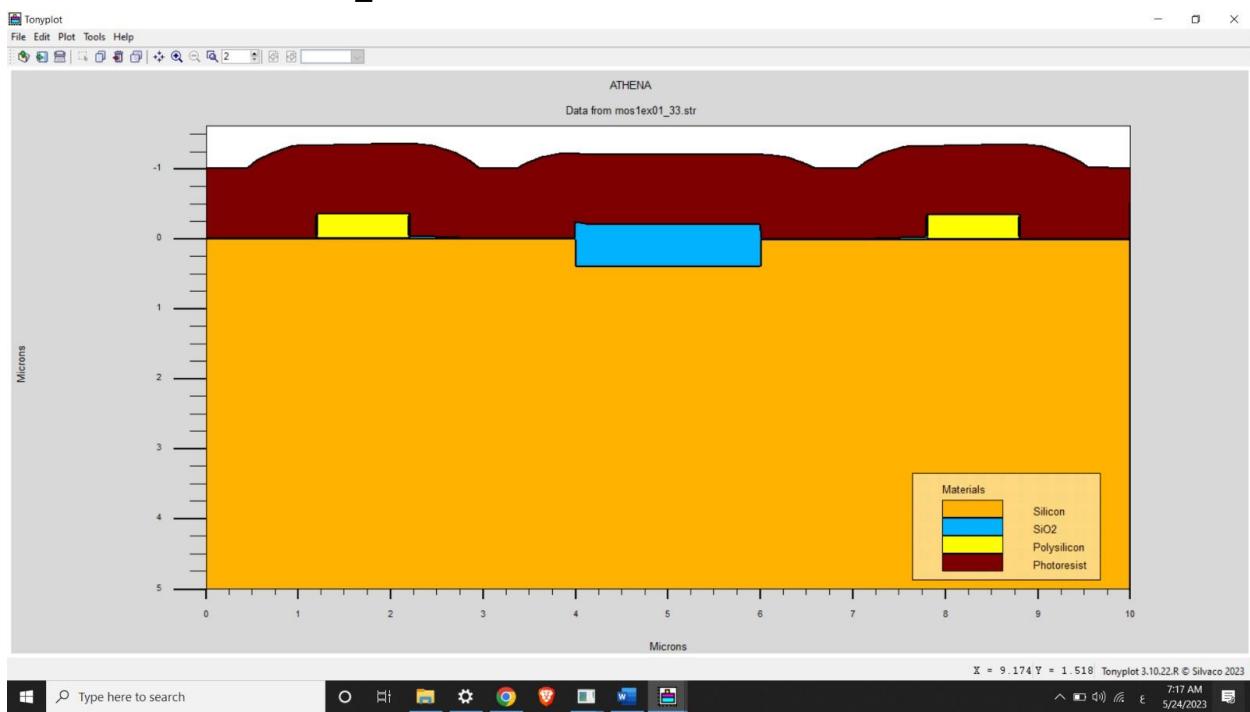
## Section VIII: LDD formation (lightly doped drain) extensions:

#LDD formation

#deposit photoresist

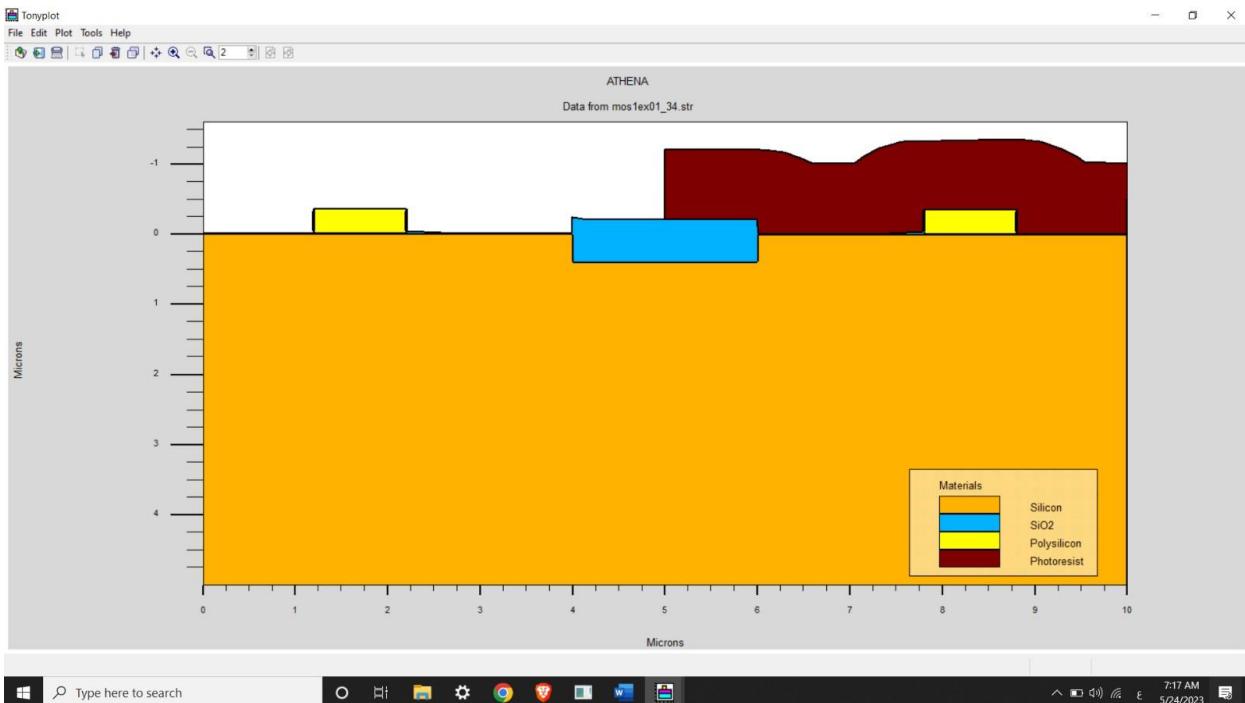
deposit photoresist thickness=1

structure outfile=mos1ex01\_33.str



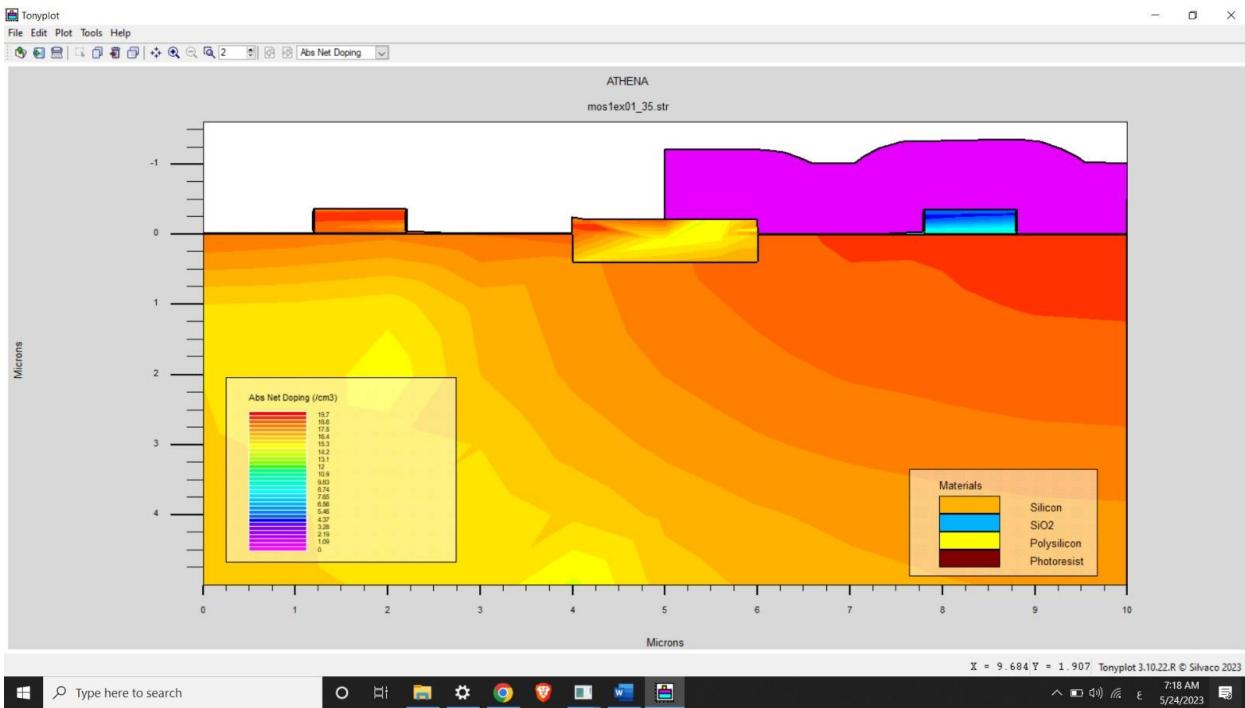
```
#etch
```

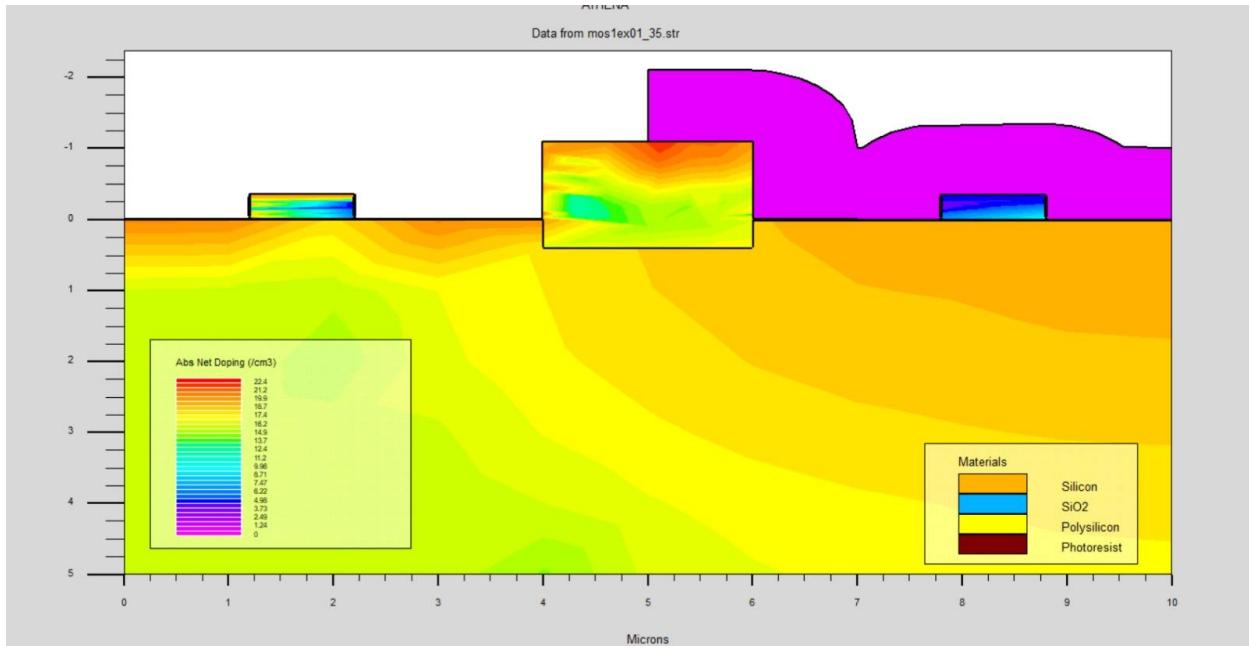
```
etch photoresist left p1.x=5  
structure outfile=mos1ex01_34.str
```



```
#implant phosphor
```

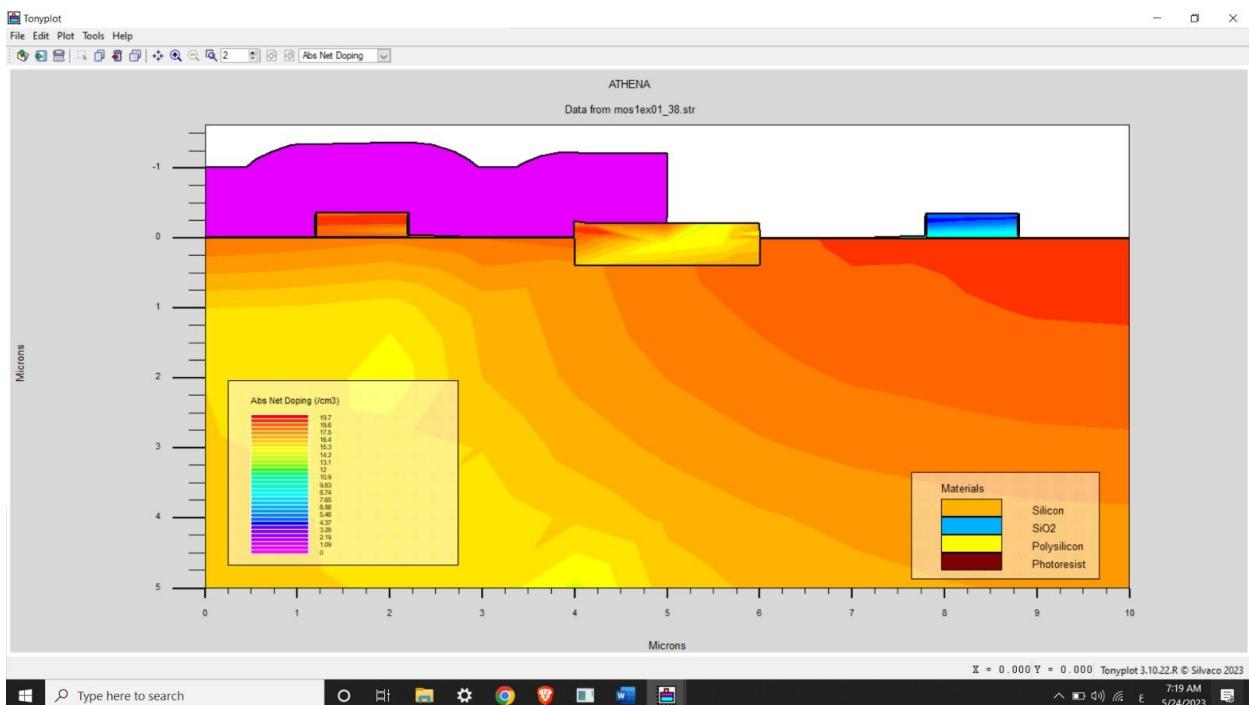
```
implant phospho energy =75 dose =5.0e14 persion  
structure outfile=mos1ex01_35.str
```





#etch

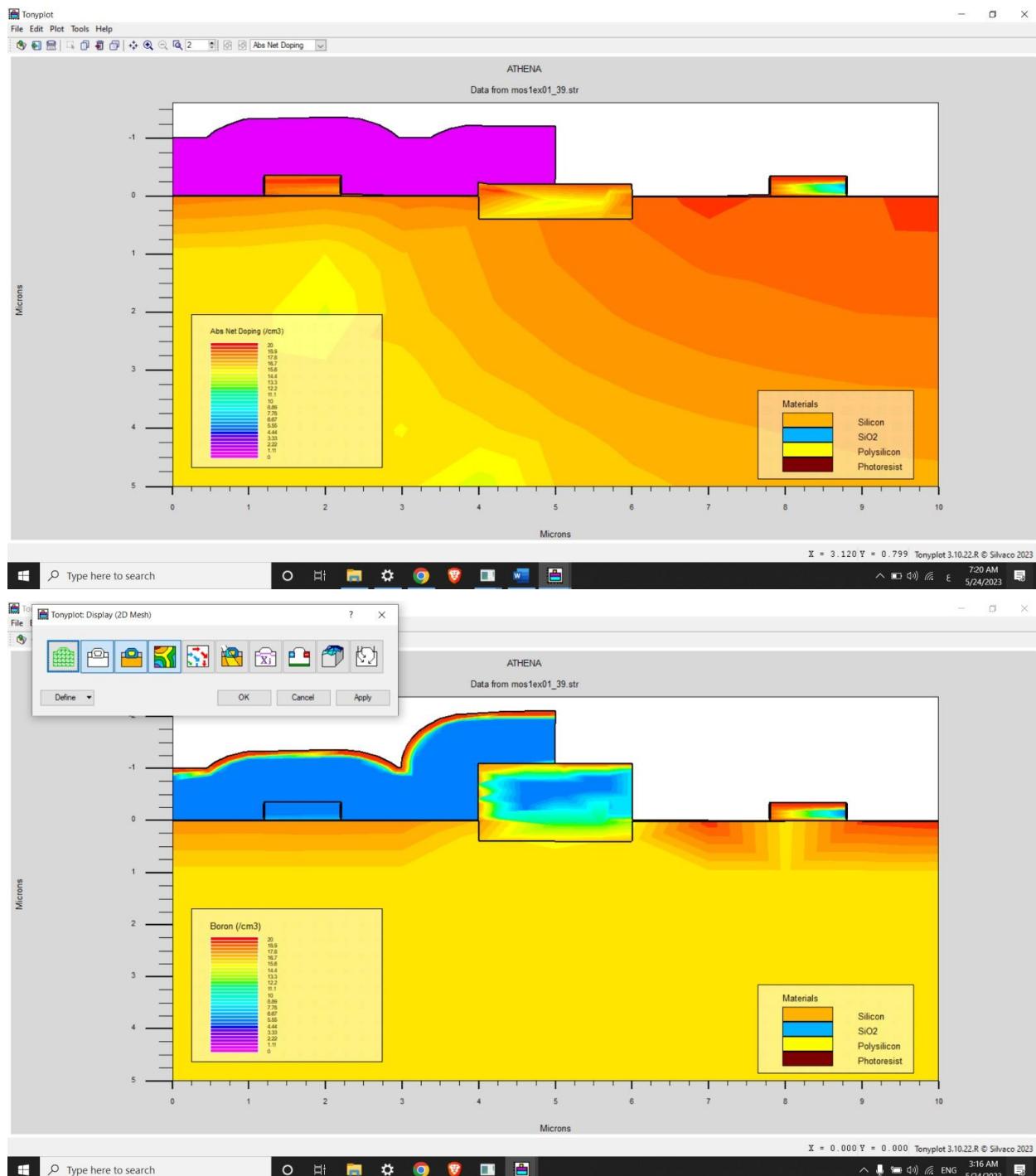
```
etch photoresist right p1.x=5
structure outfile=mos1ex01_36.str
#apply left resist
deposit photoresist thickness=1
structure outfile=mos1ex01_37.str
#etch
etch photoresist right p1.x=5
structure outfile=mos1ex01_38.str
```



```
#implant boron
```

```
implant boron energy =10 dose =5.0e14 persion
```

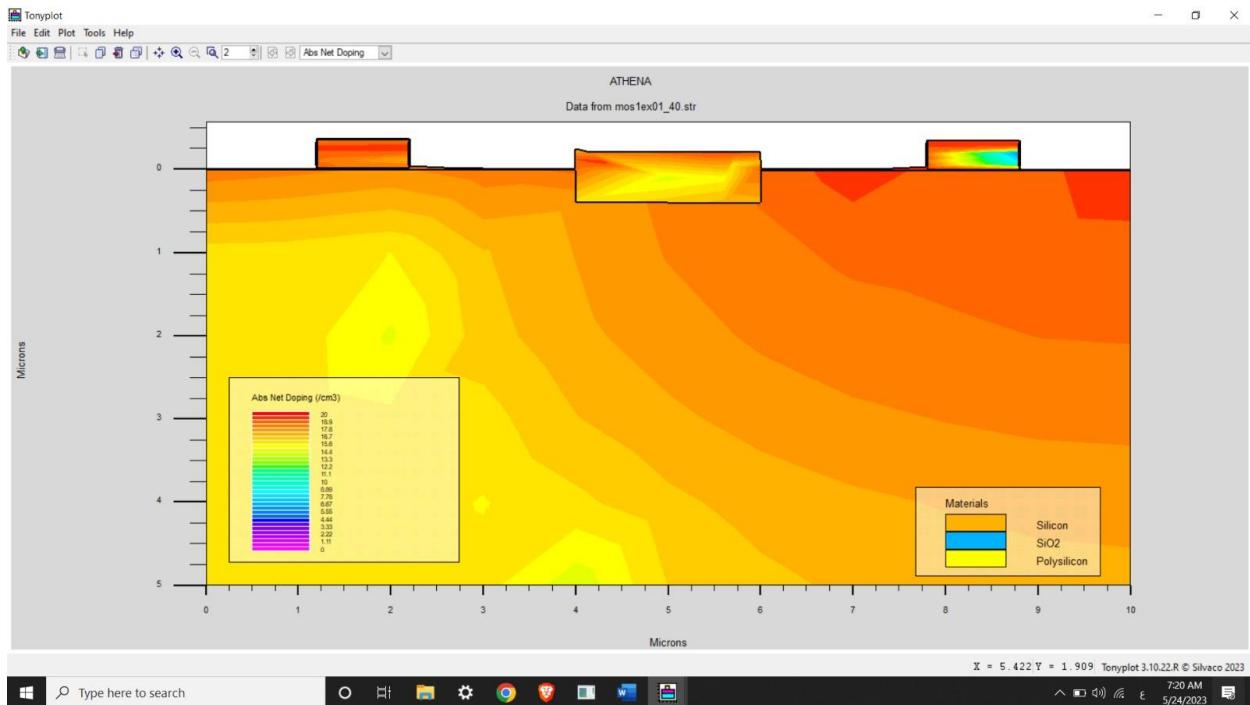
```
structure outfile=mos1ex01_39.str
```



```
#etch photoresist
```

```
etch photoresist left p1.x=5
```

structure outfile=mos1ex01\_40.str

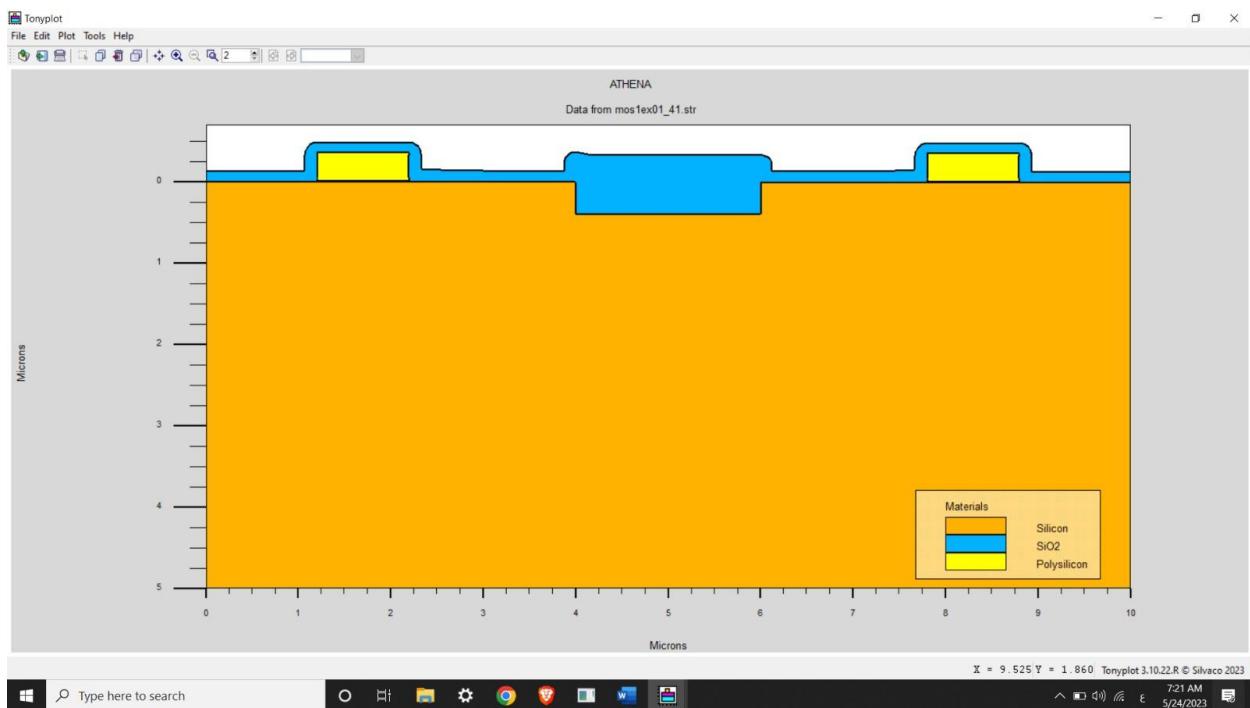


## Section IX: Side wall Spacers:

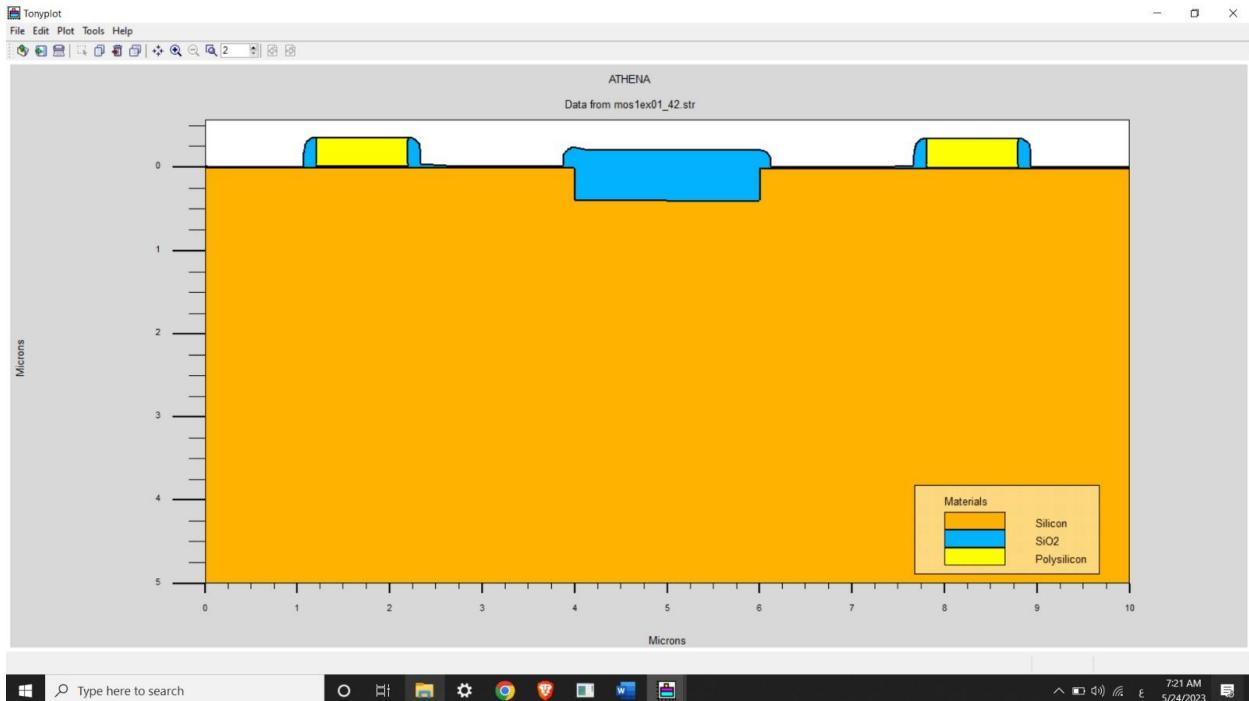
# Gate oxide spacer deposition

depo oxide thick=0.120 divisions=10

structure outfile=mos1ex01\_41.str

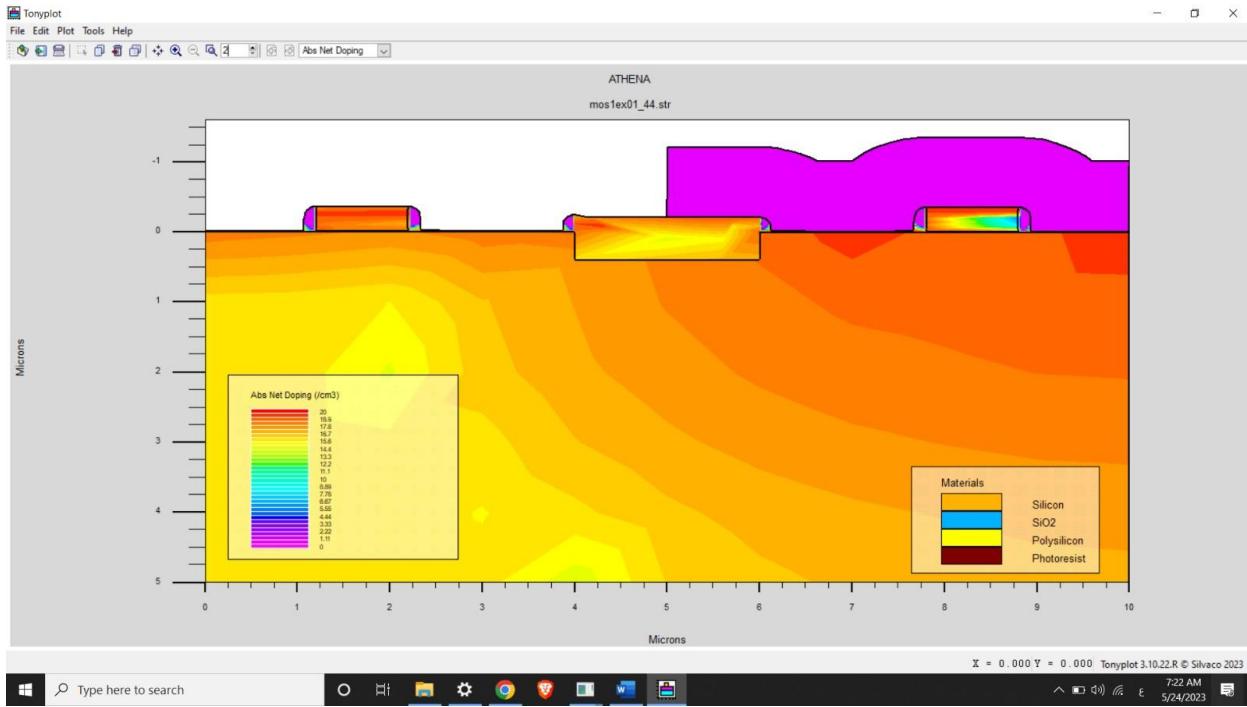


```
# Gate spacer formation  
etch oxide dry thick=0.120  
structure outfile=mos1ex01_42.str
```



## Section X: Source and drain formation:

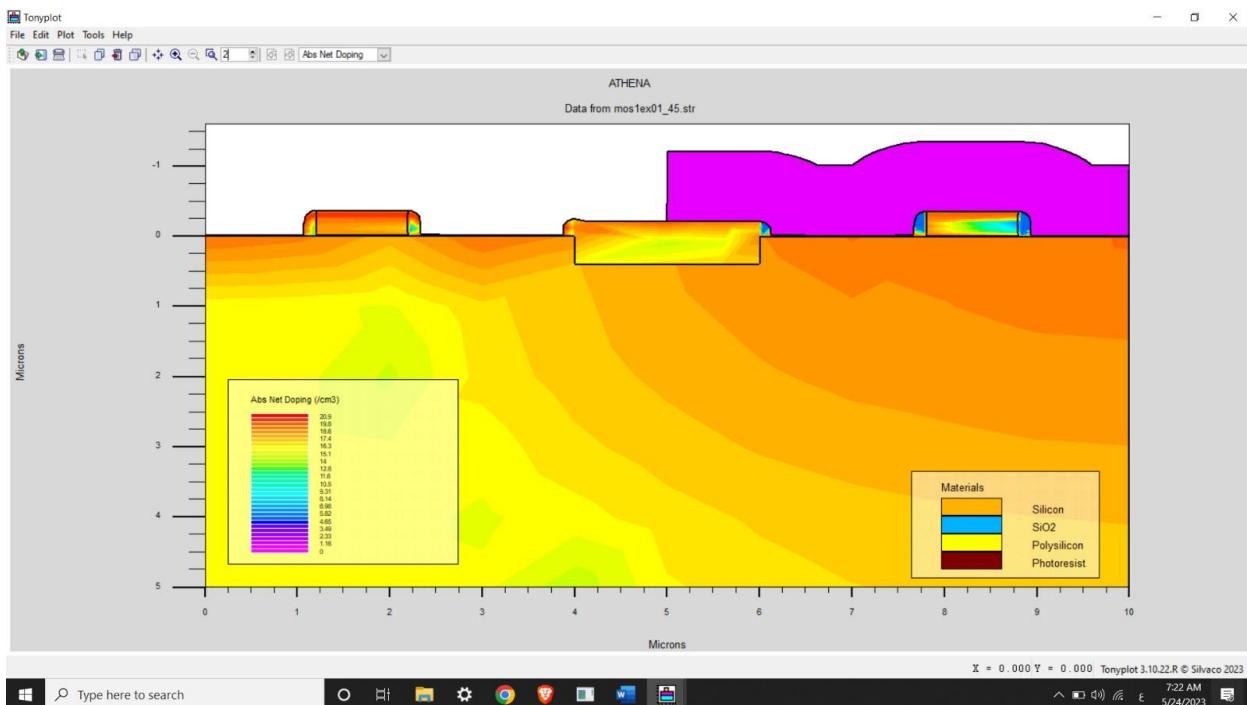
```
#source and drain  
#apply photoresist  
deposit photoresist thickness =1  
structure outfile=mos1ex01_43.str  
#etch  
etch photoresist left p1.x=5  
structure outfile=mos1ex01_44.str
```



#arsenic doping

implant arsenic energy = 75 dose = 4.0e15 pereon

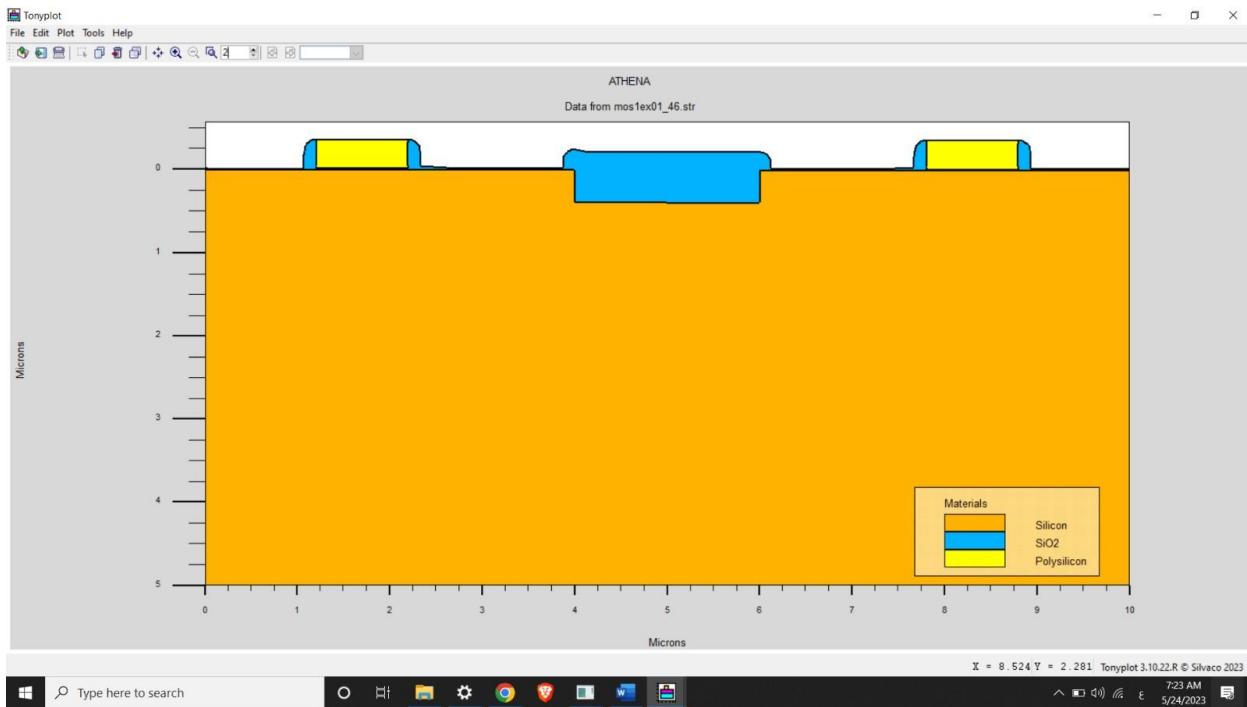
structure outfile=mos1ex01\_45.str



#etch photoresist

etch photoresist right p1.x=5

```
structure outfile=mos1ex01_46.str
```



```
#apply photoresist
```

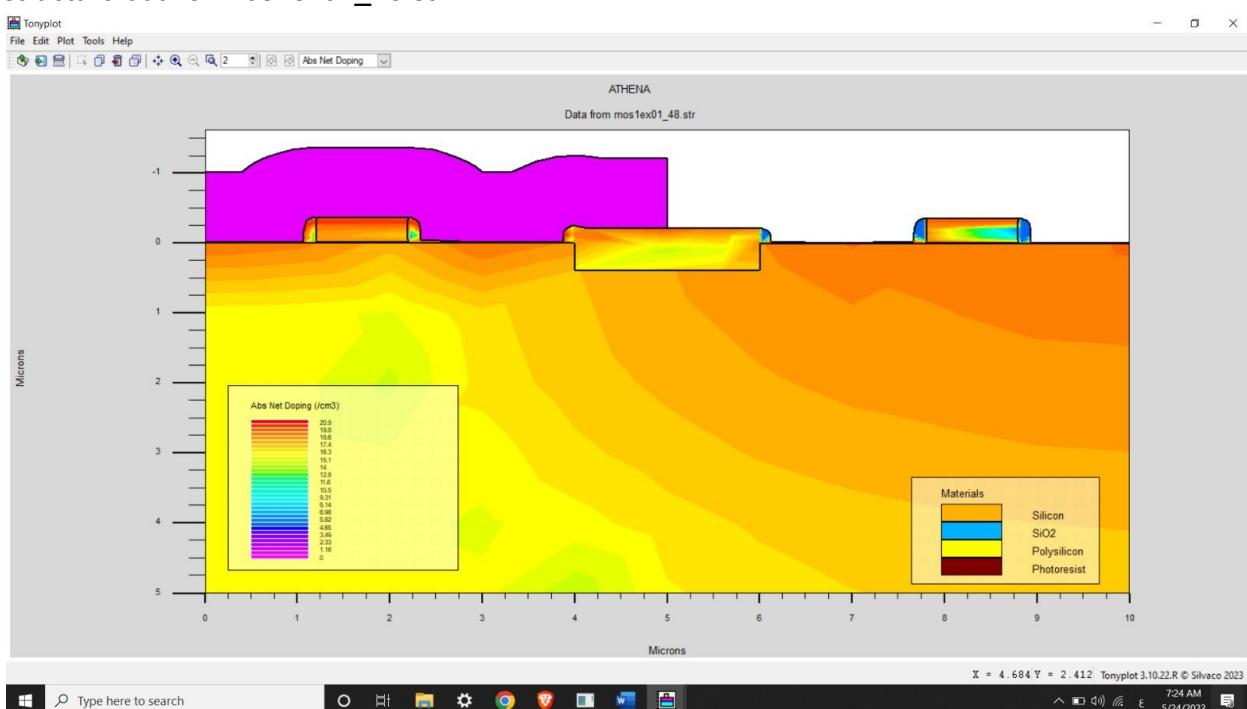
```
deposit photoresist thickness =1
```

```
structure outfile=mos1ex01_47.str
```

```
#etch photoresist
```

```
etch photoresist right p1.x=5
```

```
structure outfile=mos1ex01_48.str
```



```

#dope
implant boron energy =10 dose = 3.0e15 pearson
structure outfile=mos1ex01_49.str
#etch
etch photoresist left p1.x=5
structure outfile=mos1ex01_50.str

```

## Section XI: Silicide layer:

```

# pattern S/D ohmic contact
etch oxide left p1.x=0.2
deposit Ni thick=0.03 divi=10
structure outfile=mos1ex01_52.str

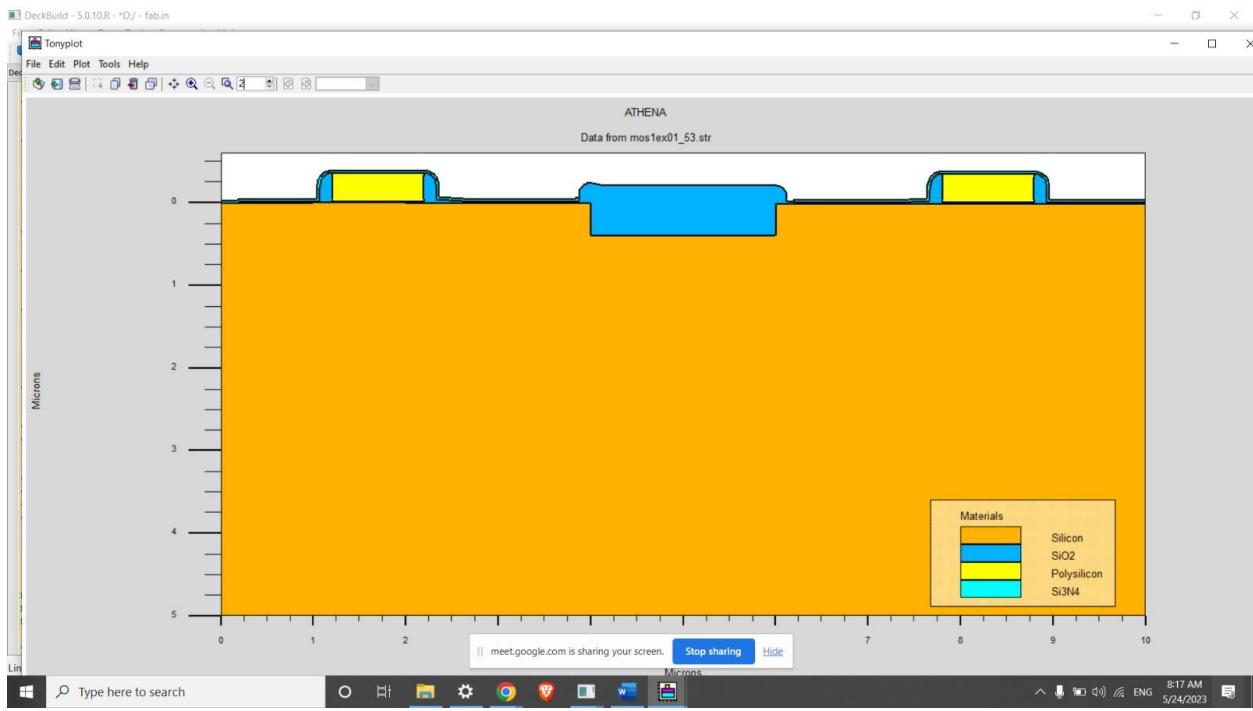
```



```

#etch
etch Ni start x=3 y = -1
etch continue x=6.2 y = -1
etch continue x=6.2 y = 0.1
etch done x=4 y =0.1
structure outfile=mos1ex01_53.str

```

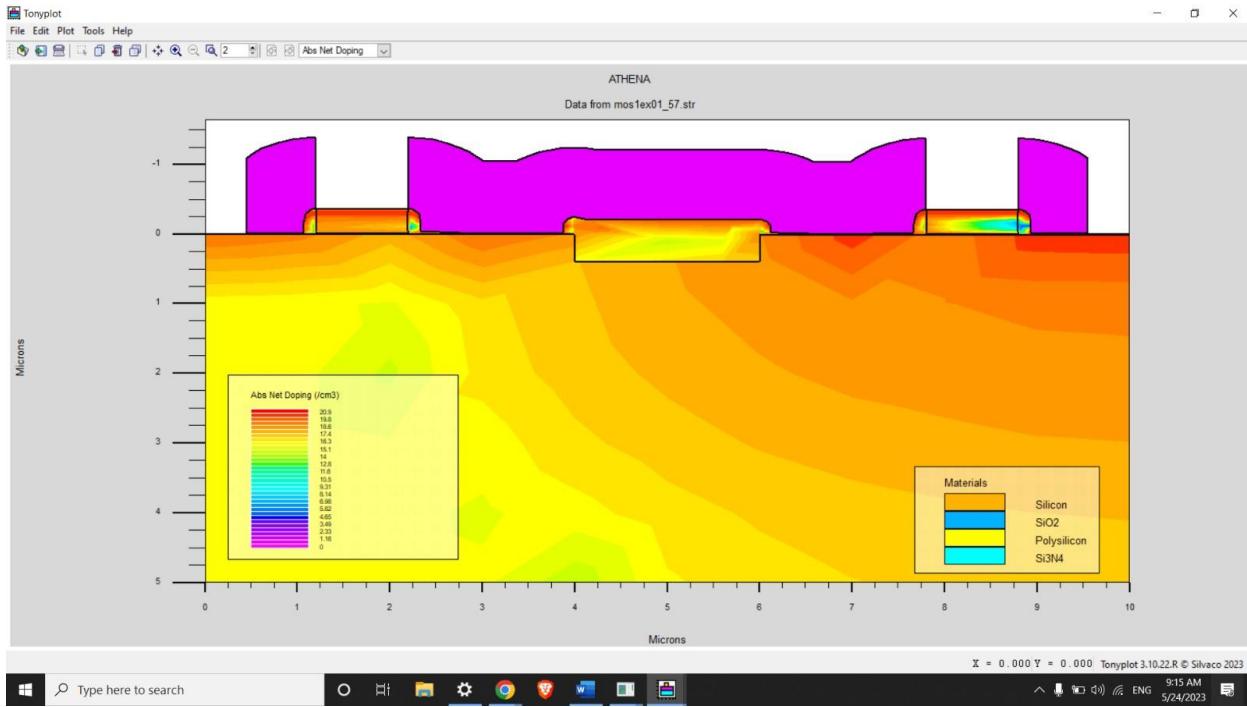


## Section XIII: First metal level formation:

```

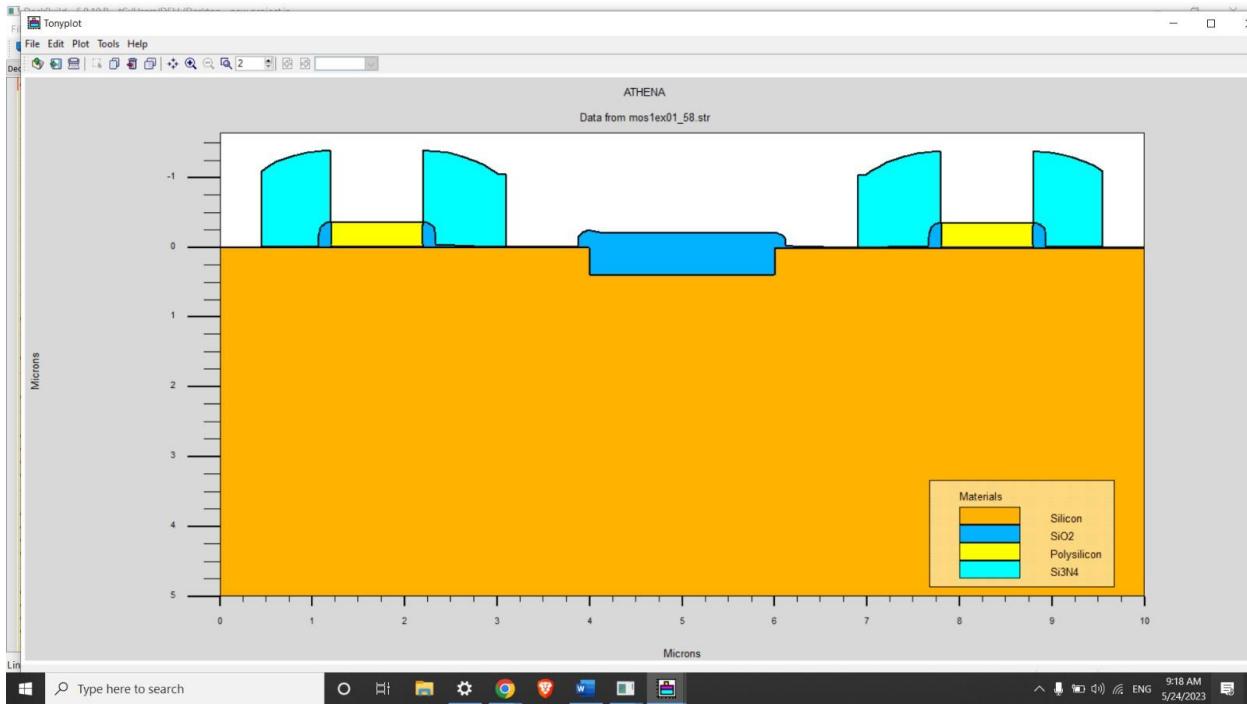
# pattern S/D contact metal
etch oxide left p1.x=0.2
deposit Ni thick=1 divi=10
structure outfile=mos1ex01_54.str
etch Ni left p1.x=0.45
etch Ni right p1.x=9.55
structure outfile=mos1ex01_55.str
#etch
etch Ni start x=1.2 y = -1.4
etch continue x=2.2 y = -1.4
etch continue x=2.2 y = 0.2
etch done x=1.2 y =0.2
structure outfile=mos1ex01_56.str
#etch
etch Ni start x=7.8 y = -1.4
etch continue x=8.8 y = -1.4
etch continue x=8.8 y = 0.2
etch done x=7.8 y =0.2
structure outfile=mos1ex01_57.str

```



#etch

```
etch Ni start x=3.1 y = -1.4
etch continue x=6.9 y = -1.4
etch continue x=6.9 y = 0.2
etch done x=3.1 y =0.2
structure outfile=mos1ex01_58.str
```

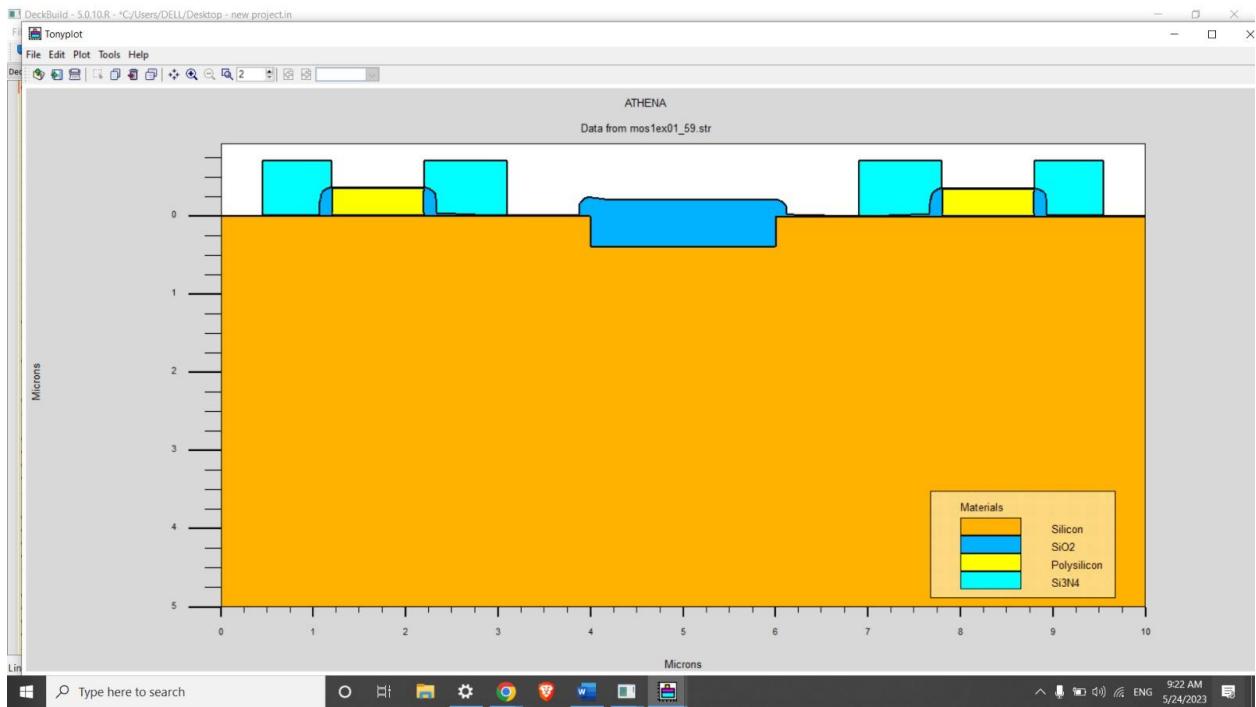


#etch

```

etch Ni start x=0 y = -1.4
etch continue x=10 y = -1.4
etch continue x=10 y = -0.7
etch done x=0 y =-0.7
structure outfile=mos1ex01_59.str

```



## Section XII: References:

- Barzdenas, V., Grazulevicius, G., & Vasjanov, A. (2019). TCAD tools in Undergraduate Studies: A laboratory work for learning deep submicron CMOS processes. *The International Journal of Electrical Engineering & Education*, 57(2), 133–163.  
<https://doi.org/10.1177/0020720919846811>