180 NM PMOS DESIGN

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Introduction:

The MOSFET (Metal Oxide Field Effect Transistor) is a type of transistor that is used in amplification and switching applications. It has 3 components: Source, Drain, and Gate.

There are 2 types of work modes for MOSFET: enhancement mode and depletion mode. Enhancement mode occurs when an inversion layer is formed when gate voltage is applied. The depletion mode occurs when the inversion layer exists in absence of the gate voltage. There are 2 types for the MOSFET according to the dopant:

- NMOS (the channel, source, and drain contain n-type dopant)
- PMOS (the channel, source, and drain contain p-type dopant)

In this project, PMOS enhancement mode transistors will be tested at 2 conditions: long channel (at channel length L = 1 um) and short channel (at channel length L = 180 nm).

Graphs and calculations needed will be:

- Drain Current vs gate voltage.
- Drain Current vs drain voltage.
- Subthreshold voltage.
- Electron density.
- Electric Field in Longitudinal direction.
- Electric Field in Transverse direction.
- Capacitances (Low and high Frequencies).
- Cross section for the transistor.
- Meshing.
- Absolute net doping concentration.
- Potential on the cross section.
- Recombination rate.
- Threshold voltage, transconductance, and lol changes due to temperature.

Phase 1: long channel model

1. Drain Current vs VGS (gate voltage):

V_{ds}= -1.2v

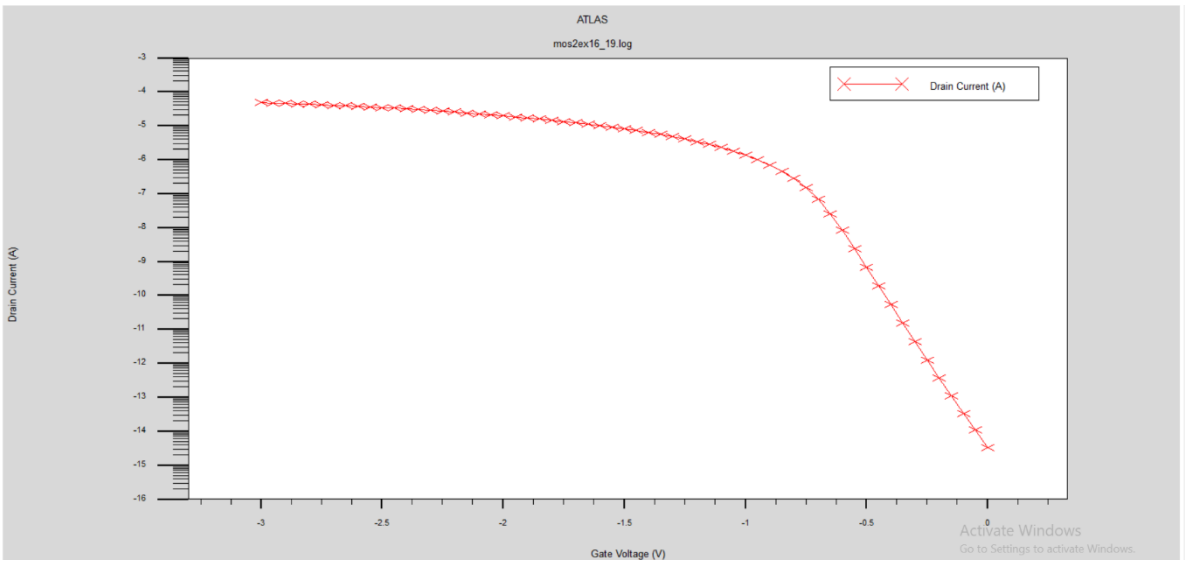

Figure 1 gate voltage vs drain current at vds= -1.2 v.

V_{ds}= -0.005v

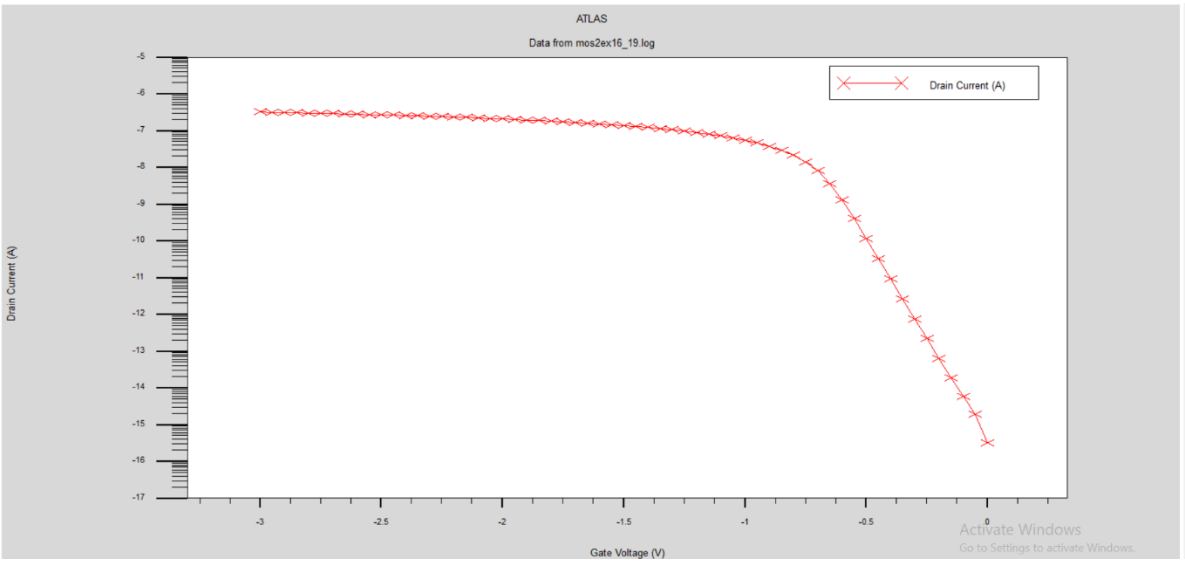

Figure 2 gate voltage vs drain current at vds= -0.005 v.

The relation between gate voltage and drain current is represented in figure 1 and 2 in two different drain voltages.

When the gate-source voltage is less than the threshold voltage, the transistor is in the cutoff region, and the drain current is close to zero. As increases beyond threshold voltage, the transistor begins to conduct. Then it enters the triode region before saturation where the drain current becomes relatively independent of gate voltage and is primarily determined by Vgs – Vth.

2. **Drain Current vs VGS (gate voltage):**

As VGS becomes more negative and approaches the threshold voltage (VTH), the transistor enters the linear region.

In the linear region, the drain current (ID) increases linearly with the increase in the magnitude of VGS.

As the magnitude of VGS increases further, the transistor enters the saturation region. In the saturation region, the drain current (ID) becomes nearly constant and is independent of the drain-source voltage (VDS).

Vg=-1.2v

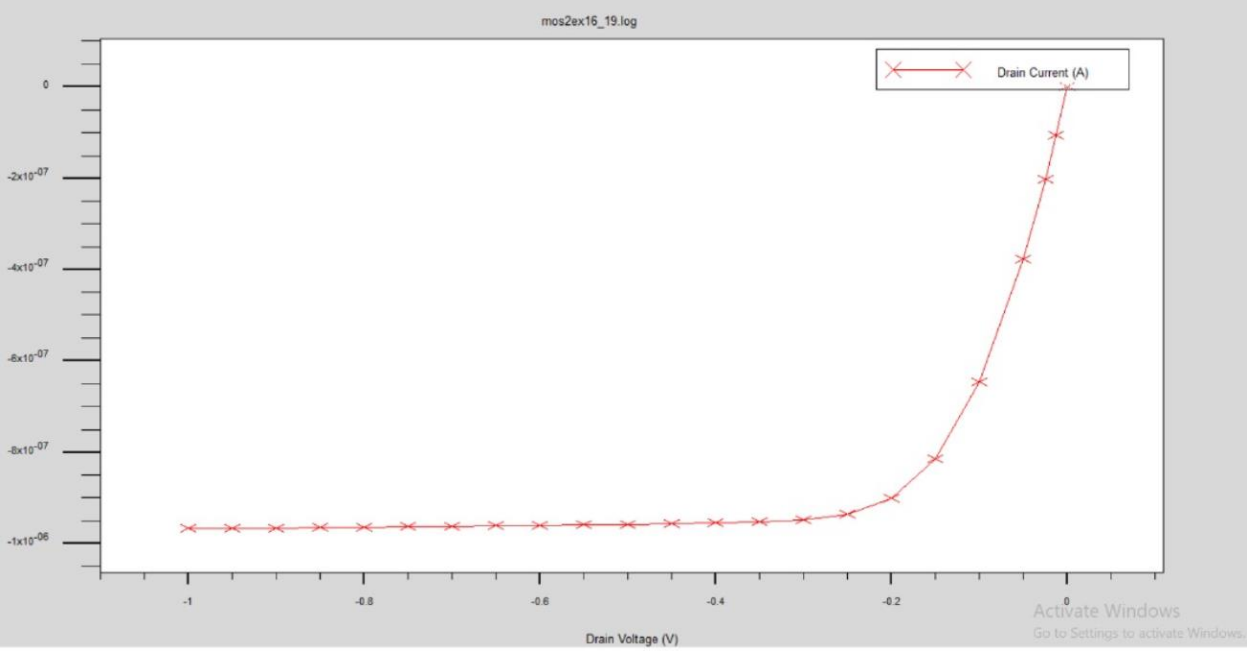

Figure 3 Drain voltage vs drain current at Vg= -1.2 v

Vg=-1v

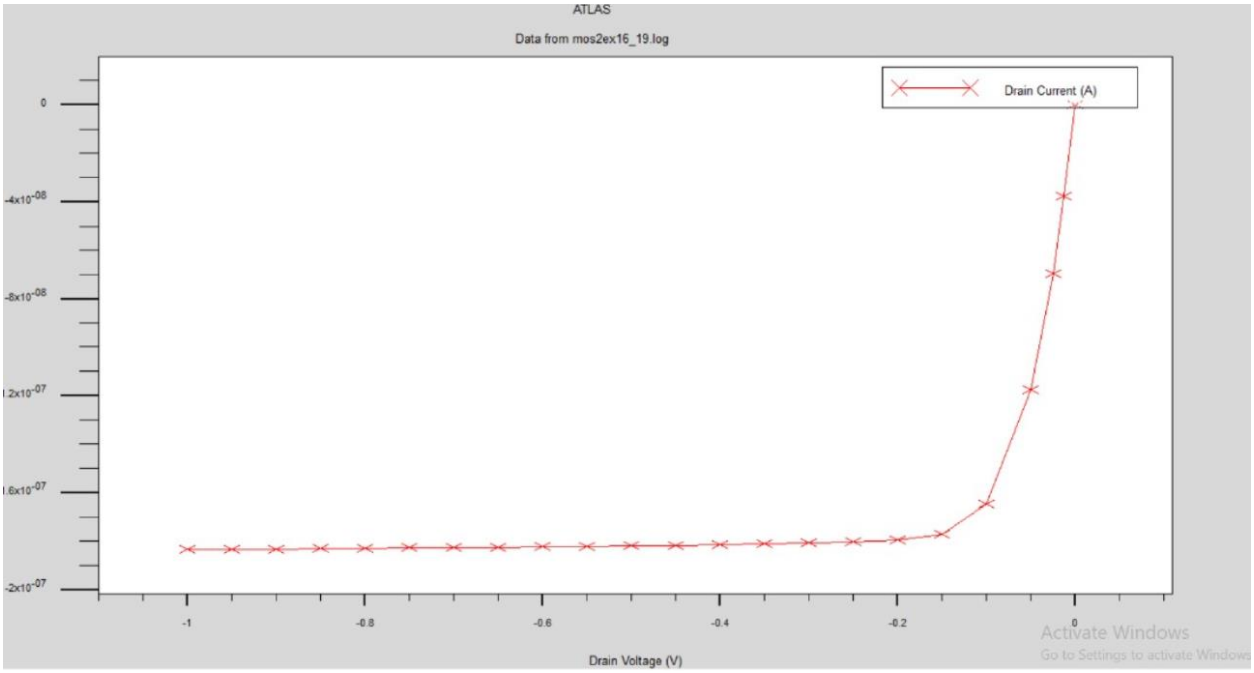

Figure 4 Drain voltage vs drain current at Vg= -1 v

Vg=-0.8v

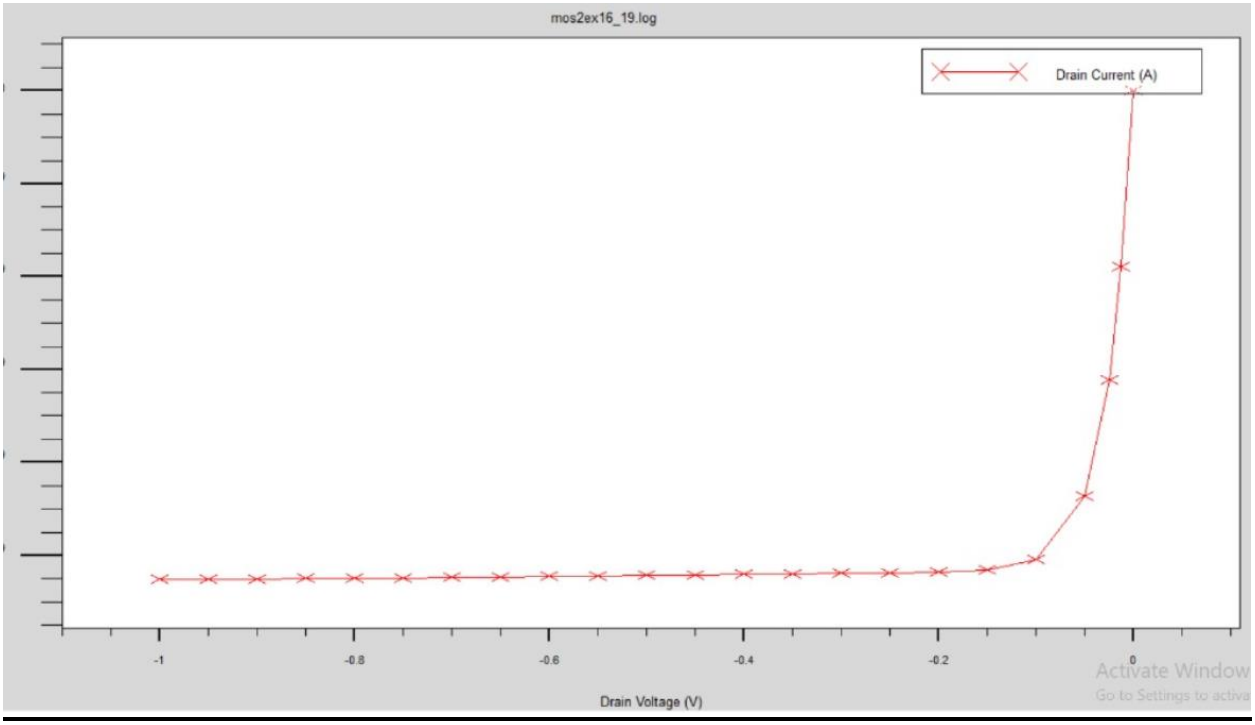

Figure 5 Drain voltage vs drain current at Vg= -0.8v

Vg=-0.5v

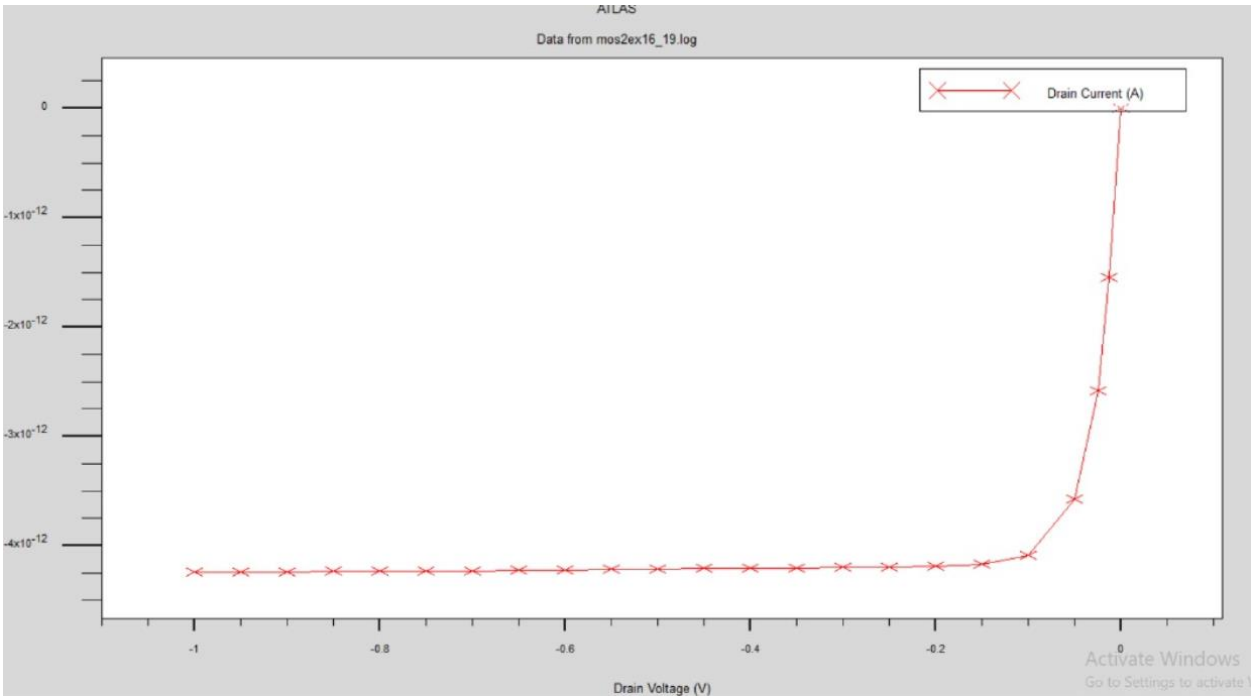

Figure 6 Drain voltage vs drain current at Vg= -0.5 v

As the gate-source voltage (VGS) of a PMOS transistor is increased (made more negative from -0.5: -1.2 v):

- The ID-VDS curve becomes steeper in the linear region, indicating a higher drain current.
- The saturation current (ID, sat) increases, causing the ID-VDS curve to shift upward in the saturation region.
- The saturation voltage (VDS, sat) decreases, as the channel becomes pinched off at a lower value of VDS.

The linear regime is from about 0 V to -0.35 V. The rest range represents the saturation regime.

3. Subthreshold swing:

The subthreshold swing is the rate of change of drain current with respect to gate voltage in the subthreshold region. The subthreshold region is the region of operation where the gate-source voltage (VGS) is below the threshold voltage (VTH) of the transistor as in this region the transistor is not fully turned on, but a small drain current still flows.

Subthreshold swing (m) = slope of log Id vs Vgs graph

$$\frac{d log\ abs(I_{D\square})}{dV_{GS}} = \frac{(-7) - (-7.9)}{-0.7 - (-0.6)} = -0.14$$

It typically decreases with increasing VGS, due to the narrowing of the energy barrier at the semiconductor-oxide interface. As the subthreshold coefficient increases, the subthreshold current increases, increasing power consumption.

4. Transconductance (gm):

Transconductance is a measure of how much the drain current (ID) changes with respect to the gate-source voltage (VGS) at a constant drain-source voltage. It's given by slope of Id vs Vgs curve:

$$gm = \frac{d(I_{D\square})}{dV_{GS}}$$

At Vds=50mV as shown in figure7:

$$gm = \frac{d(I_{D\square})}{dV_{GS}} = \frac{(-2 * 10^{-6}) - (-1.4 * 10^{-6})}{-2 - (-1.5)} = 1.2 * 10^{-6}$$

At Vds=Vdd, gm decreases due to channel length modulation effects and reduced control over the drain current as the transistor approaches saturation. As when Vds=50mV, gm is higher compared to when VDS=VDD as the transistor is operating in the linear region with a larger gate-source voltage swing available for controlling the drain current.

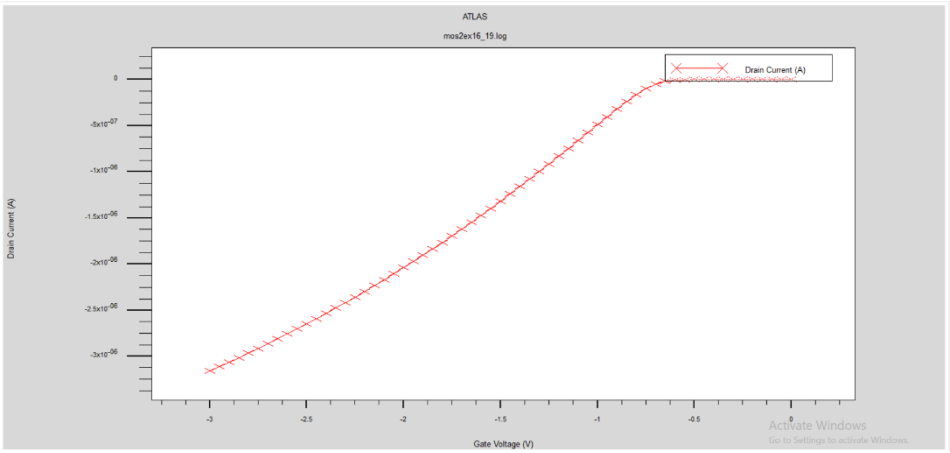

Figure 7 Vgs vs Id at Vds=-50mv

5. Output conductance(gd):

Output conductance represents the change in drain current (*I*D) with respect to drain-source voltage (*V*DS) at a constant gate-source voltage (*V*GS)
It's given by slope of Id vs Vds curve:

$$gm = \frac{d(I_{D\square})}{dV_{ds}}$$

It is responsible for leakage current and affects the transistor's output impedance. Gd will increase when vds=vdd indicating higher leakage currents and potentially higher output conductance due to weaker control of the drain current by the gate voltage.

6. Threshold voltage (Vds=50mv):

Linear region:

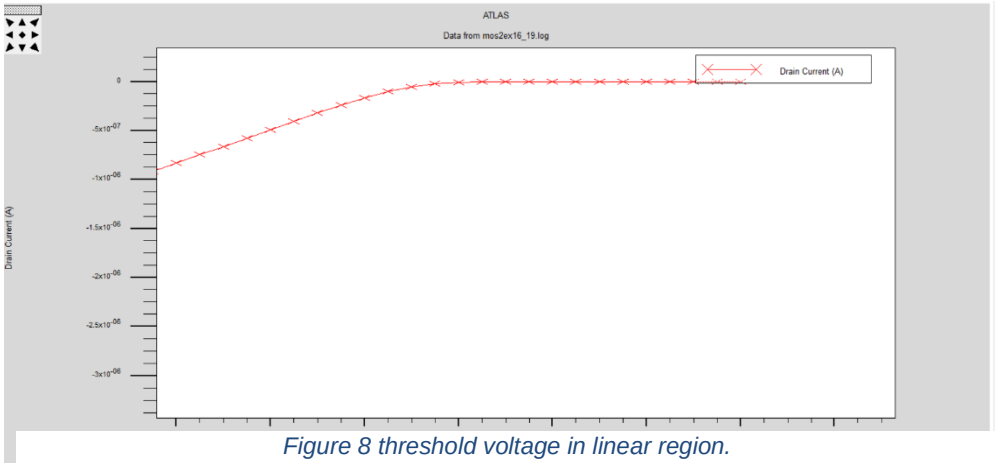

Figure 8 threshold voltage in linear region.

From figure8, the zoomed in VG vs ID curve shows that threshold voltage is nearly at -0.68 v.

Saturation region:

Figure9, shows the relation between Vd and root ID curve that hives threshold voltage is about -0.73v.

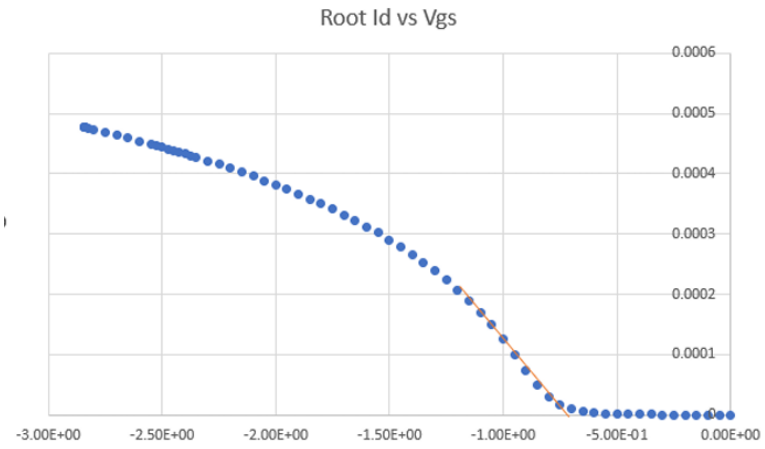

Figure 9 root id vs vgs.

7. Gate oxide Tunneling:

Gate oxide tunneling occurs by passing charge carriers into the gate oxide by overcoming the energy barrier of the oxide. As shown in figure 10, the absolute of tunneling increases by increasing the absolute of gate voltage as the increase in the voltage gives the charge carriers more energy, thus increasing the probability of tunneling.

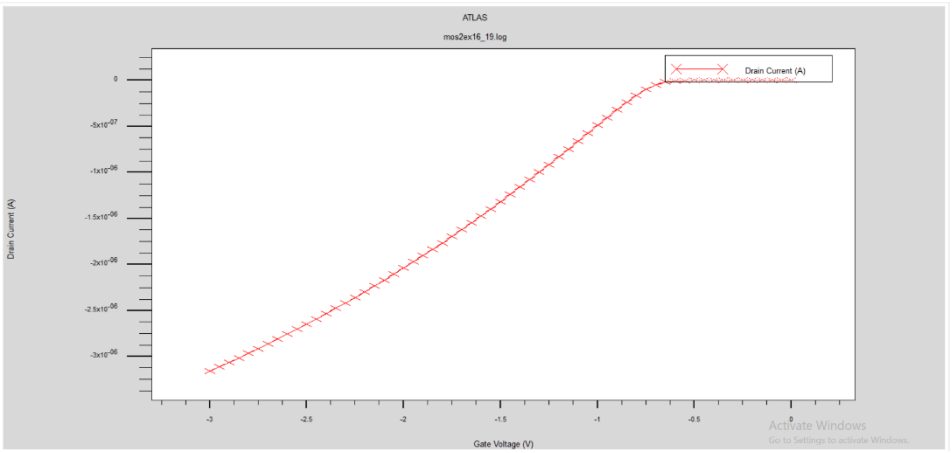

Figure 10 vg vs id to show gate oxide tunneling.

8. Electron density:

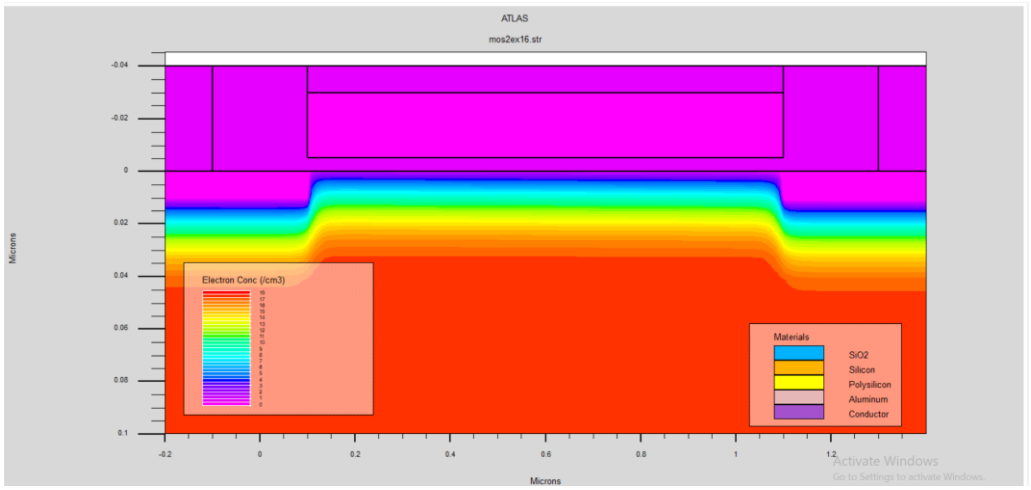

Figure 11electron density.

The electron density changes according to the doping, the type of the material, the temperature, and electric field.

9. Holes density:

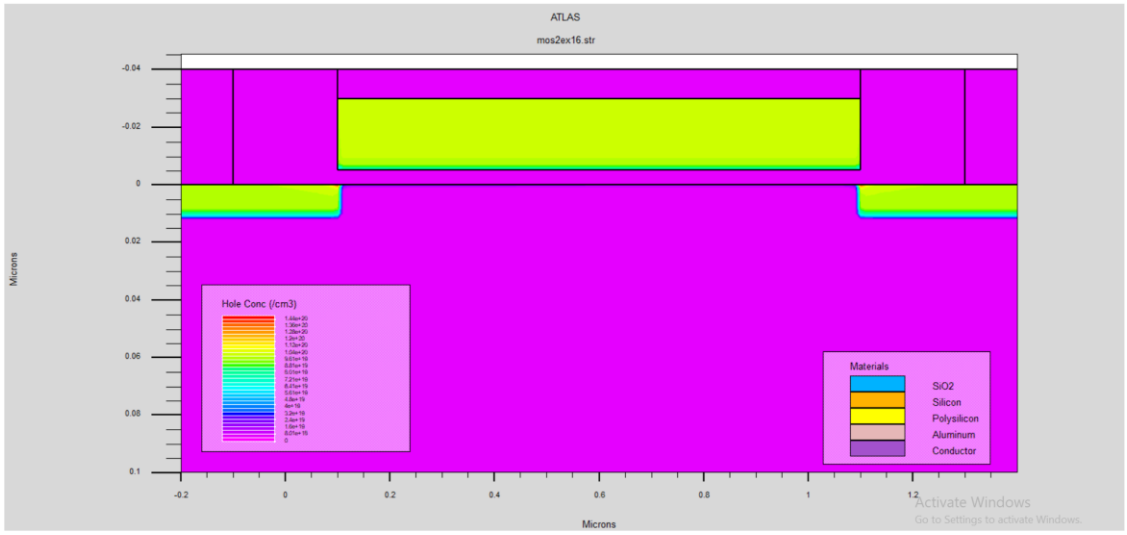

Figure 12 holes density.

The hole density depends on doping and applied voltages (either drain or gate voltages).

10.Electric field longitudinal:

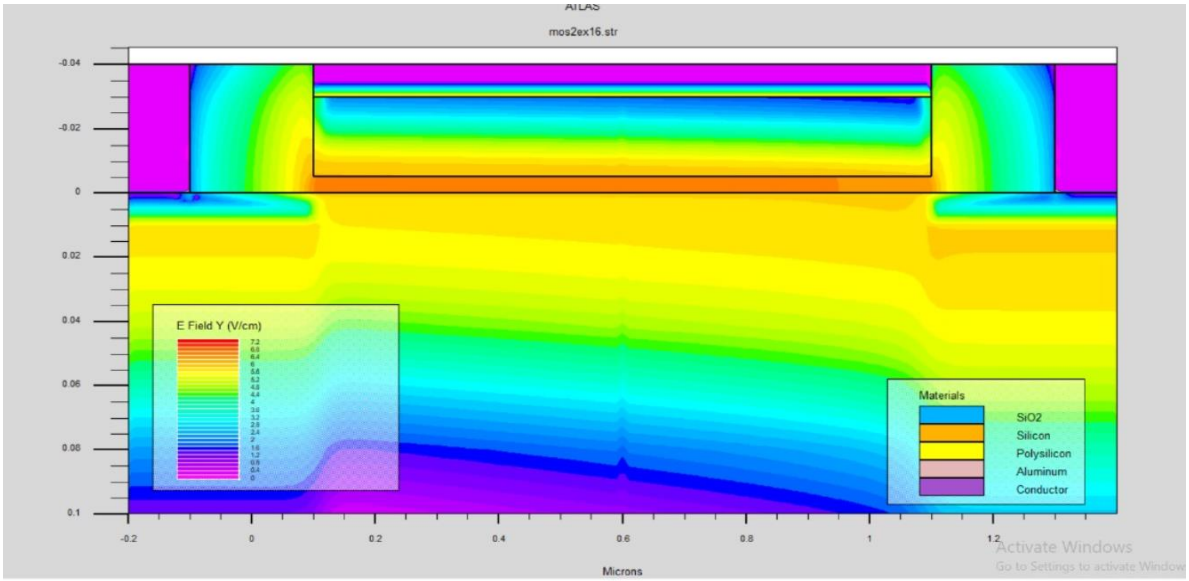

Figure 13 longitudinal electric field.

The electric field in x direction is nearly constant at the channel. The field is at max value at the source and drains parts**.**

11.<u>Electric field transverse:</u>

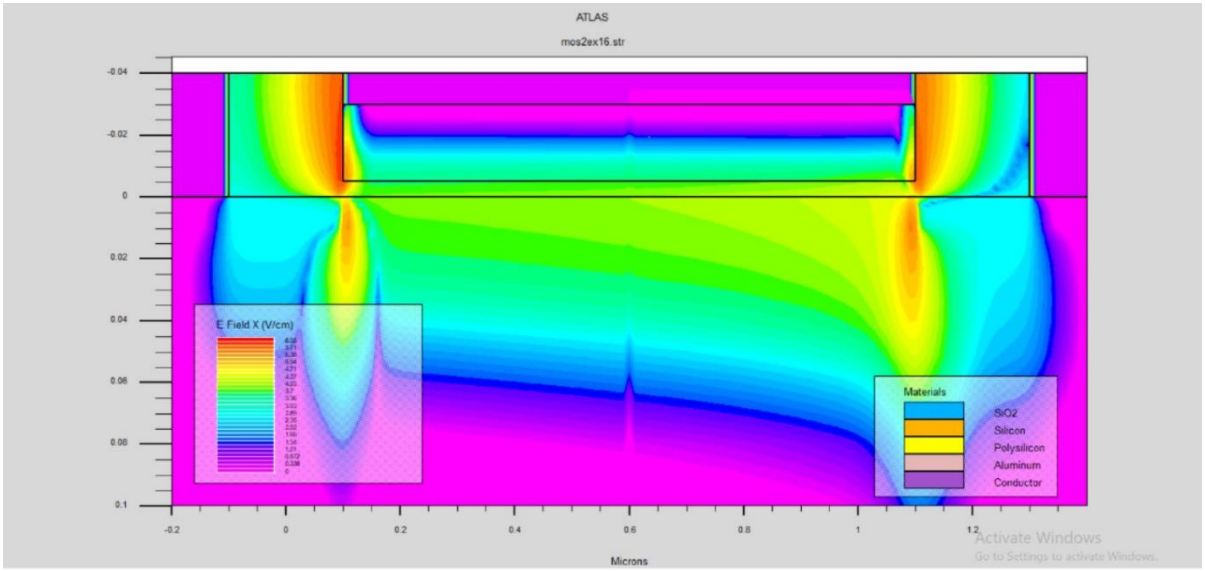

Figure 14 transverse electric field.

The electric field at y direction is high at the source, drain, and channel due to the concentration of holes. The field is nearly constant at the channel.

12. Capacitances (High Frequency):

Gate capacitance (Cg)

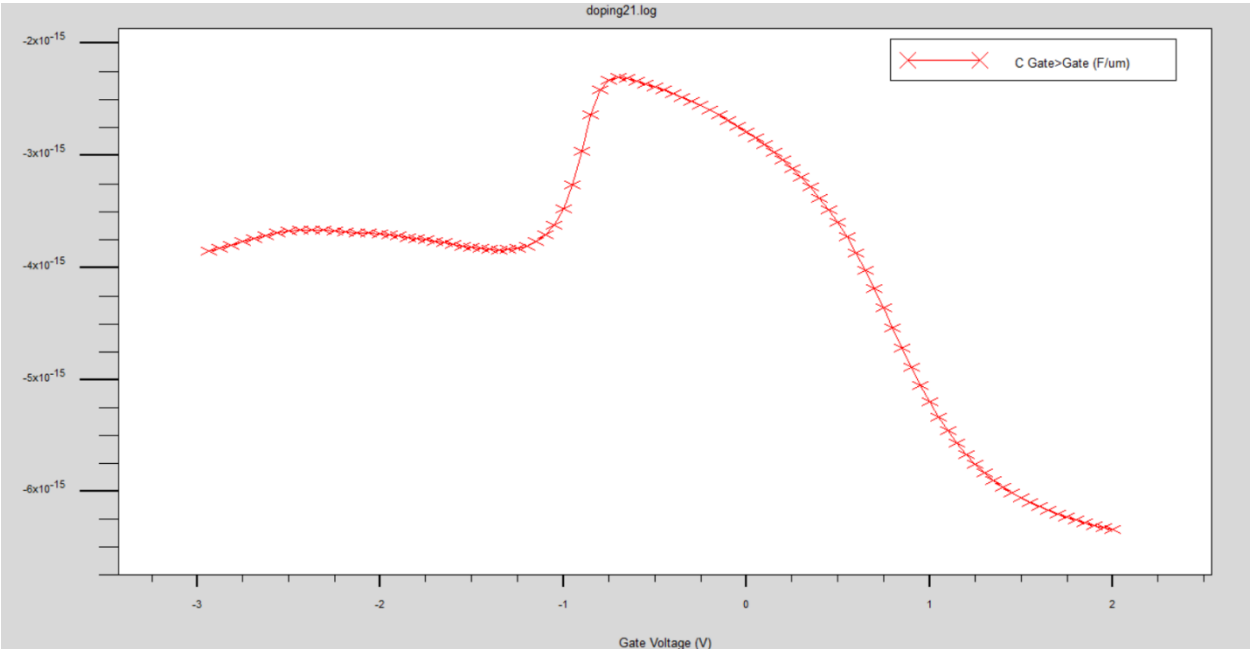

Figure 15 gate voltage vs gate capacitance.

From figure 15, V_built in = peak voltage = 0.728 V.

Source capacitance (Cgs)

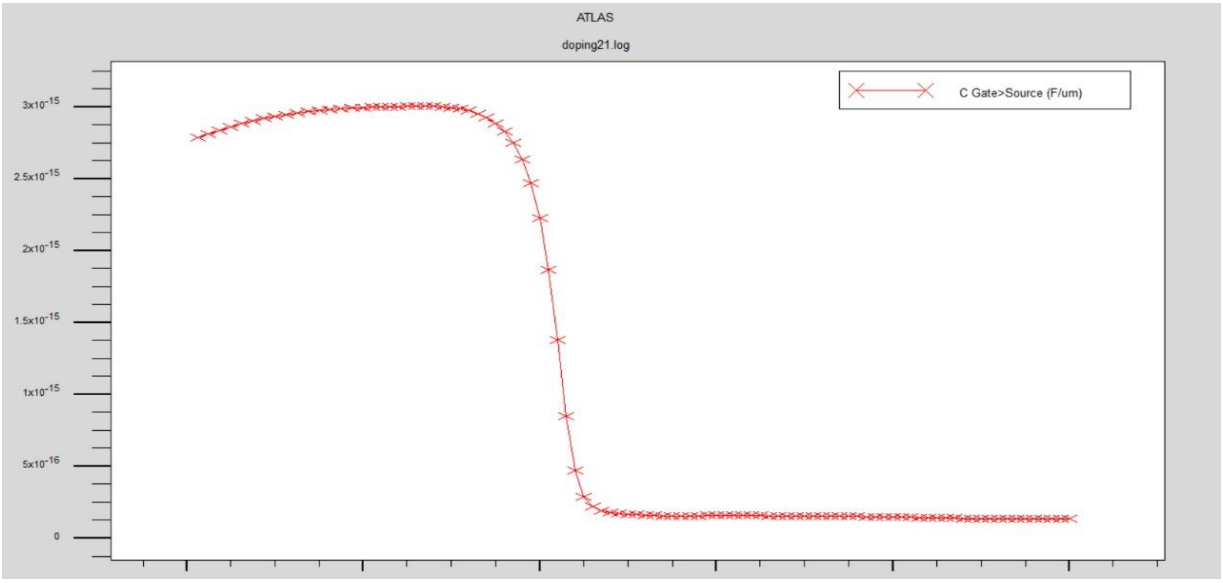

Figure 16 gate voltage vs source capacitance.

At low frequencies, Cgs is mainly influenced by the overlap capacitance between the gate and source regions, as well as the channel capacitance when the transistor is in the linear region. Cgs = C_ox * W * L_overlap (where L_overlap is the overlap length, W is the channel width, and C_ox is the oxide capacitance per unit area).

Drain capacitance (Cd)

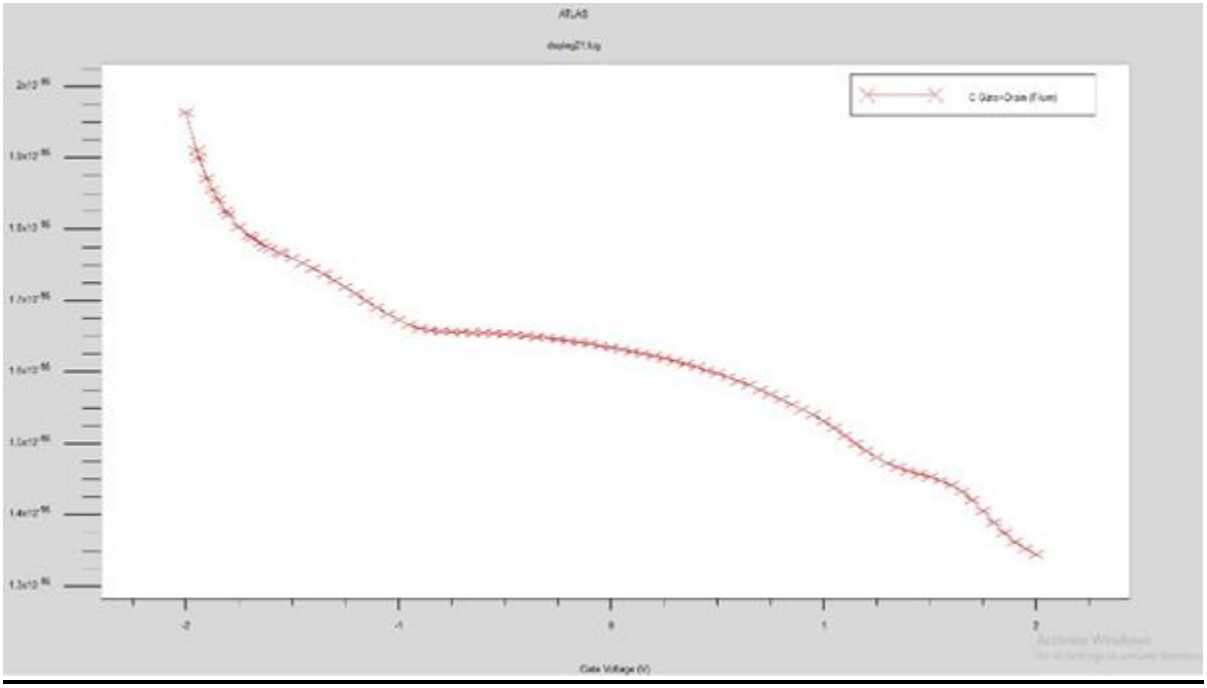

Figure 17gate voltage vs drain capacitance.

Like Cgs, Cgd includes both the overlap capacitance and the channel capacitance. In the saturation region, Cgd is reduced because the channel pinch-off point moves away from the drain. Cgd = C_ox * W * L_overlap, but it is generally less than Cgs in saturation due to the channel modulation.

13. Capacitances (Low Frequency):

Gate capacitance (Cg)

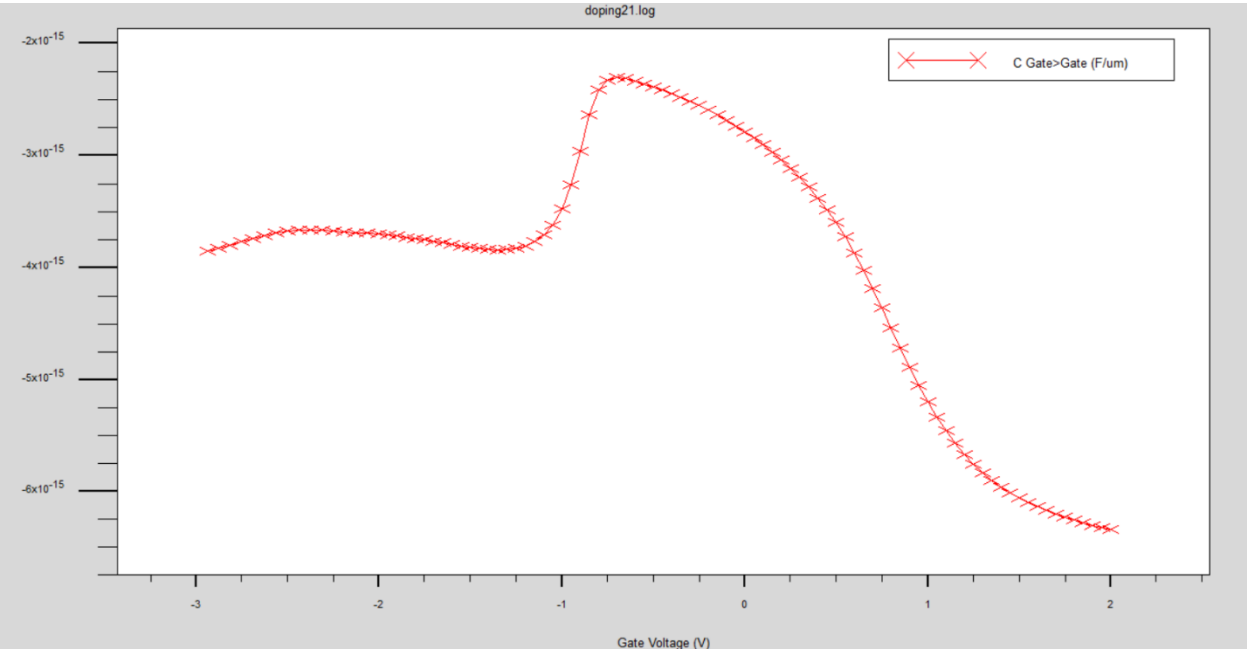

Figure 18 gate voltage vs gate capacitance.

From figure 18, V_built in = peak voltage = 0.728 V.

Source capacitance (Cgs)

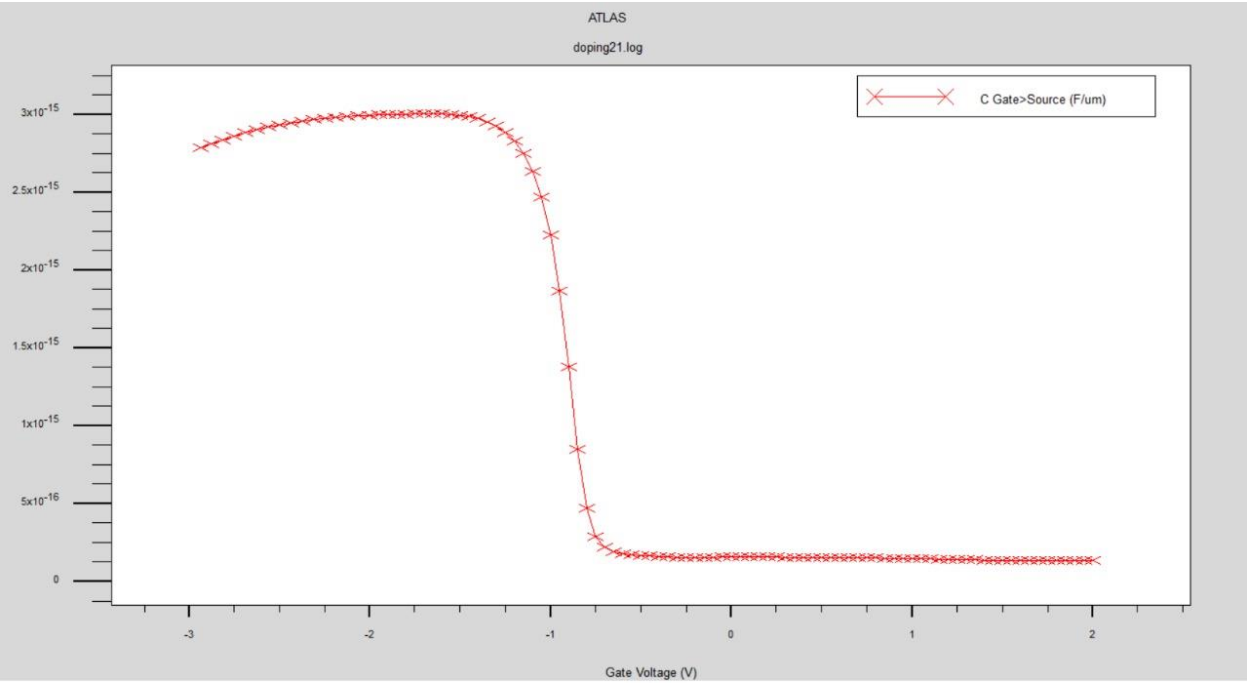

Figure 19 gate voltage vs source capacitance

At high frequencies, the overlap capacitance remains the same, but the channel capacitance component decreases because the channel cannot follow high-frequency signals. Therefore, Cgs is mainly determined by the overlap capacitance: Cgs ≈ C_ox * W * L_overlap

Drain capacitance (Cd)

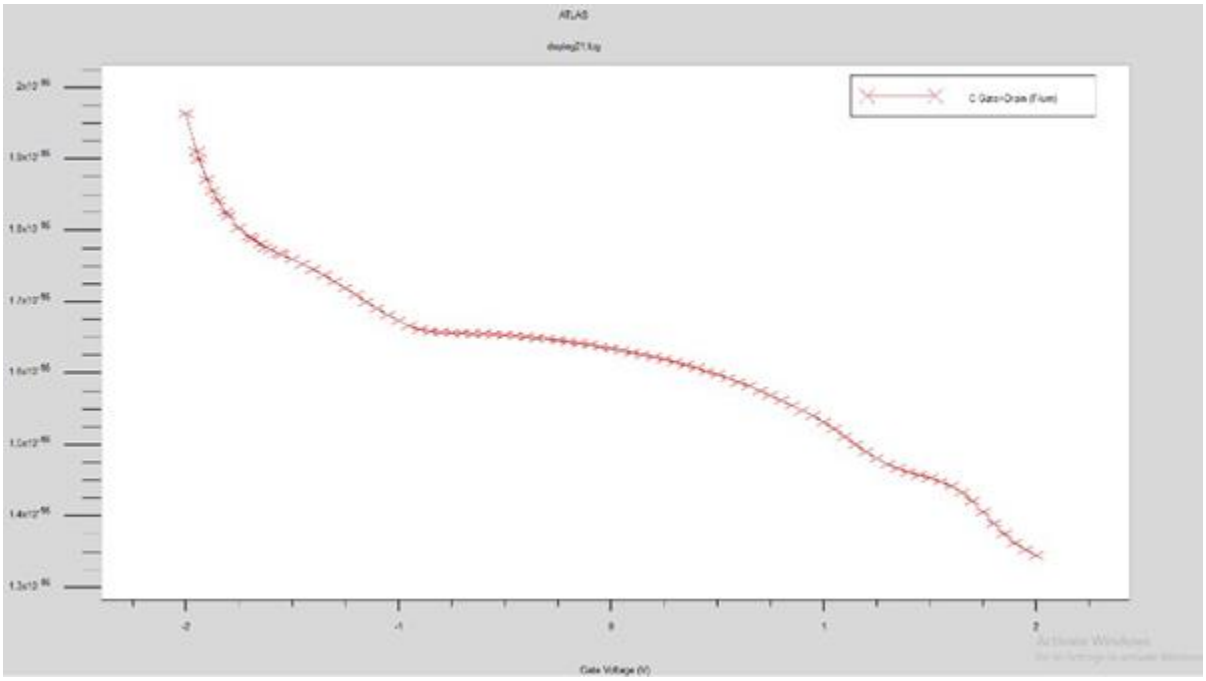

Figure 20 gate voltage vs drain capacitance.

At high Frequency: All capacitance components (oxide, depletion, and diffusion) are significant. Suitable for analog and low-speed digital applications where precision is key.

In conclusion, the choice of frequency for evaluating the capacitance of a PMOS MOSFET depends on the application requirements. Analog and precision applications benefit from low-frequency measurements, while high-speed and RF applications benefit from high-frequency characterization.

14.Cross section for the transistor:

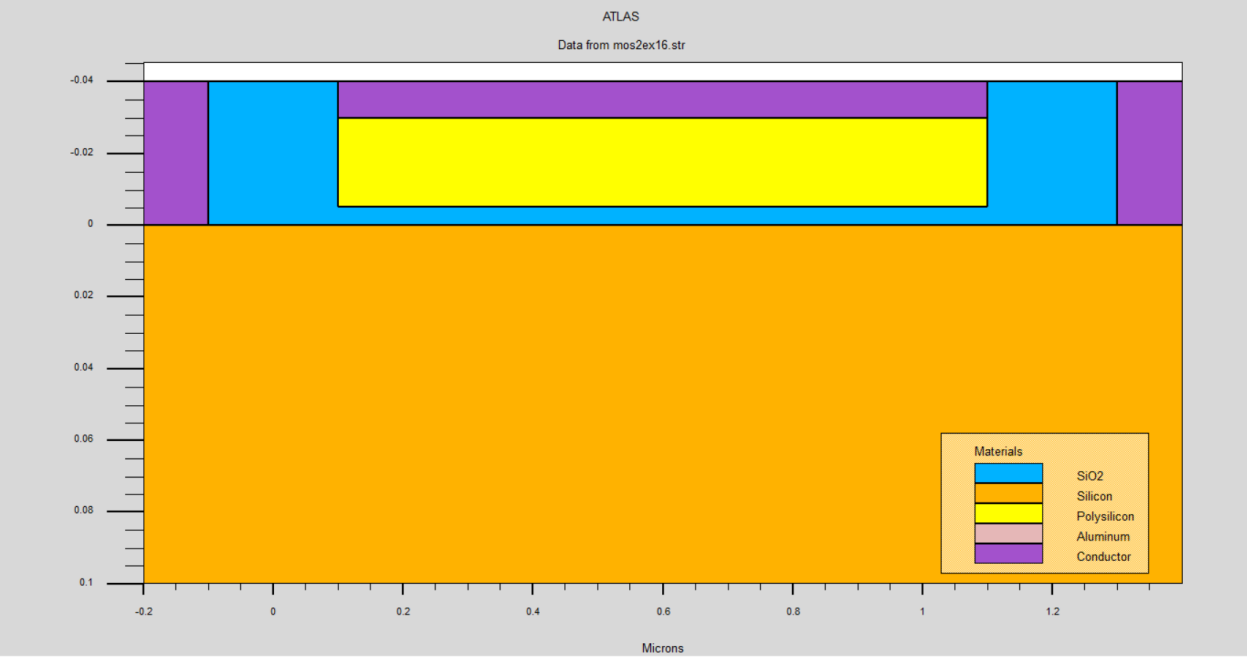

Figure 21 cross section of long channel structure.

15.Meshing:

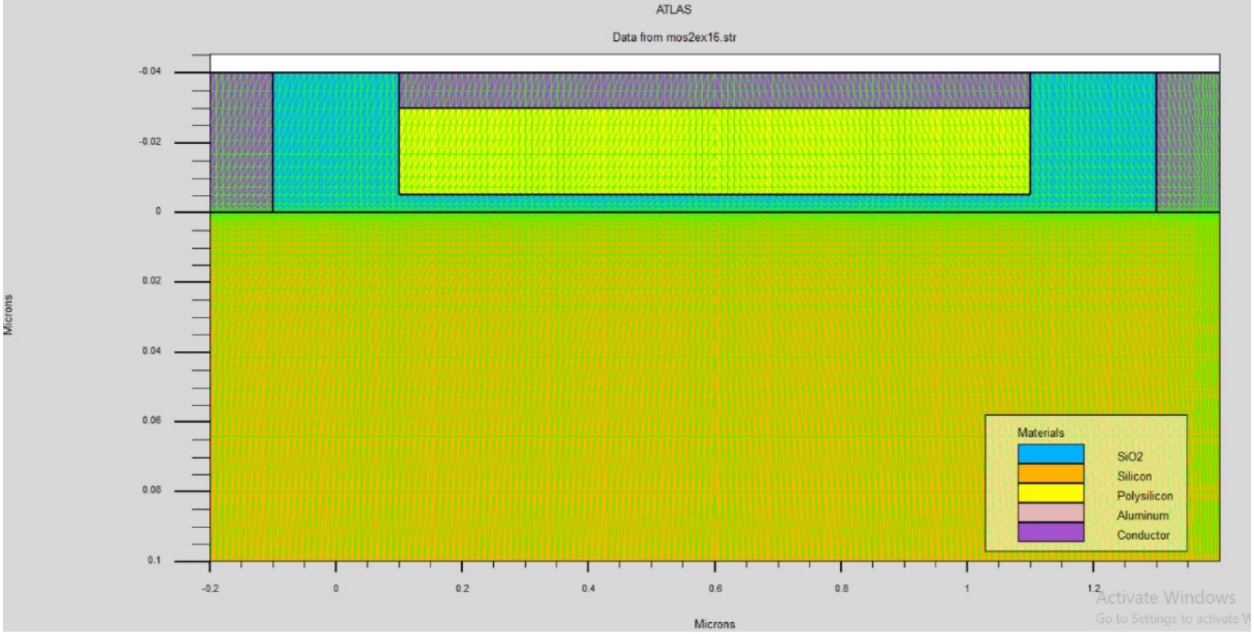

Figure 22 Meshing.

16.Doping concentration:

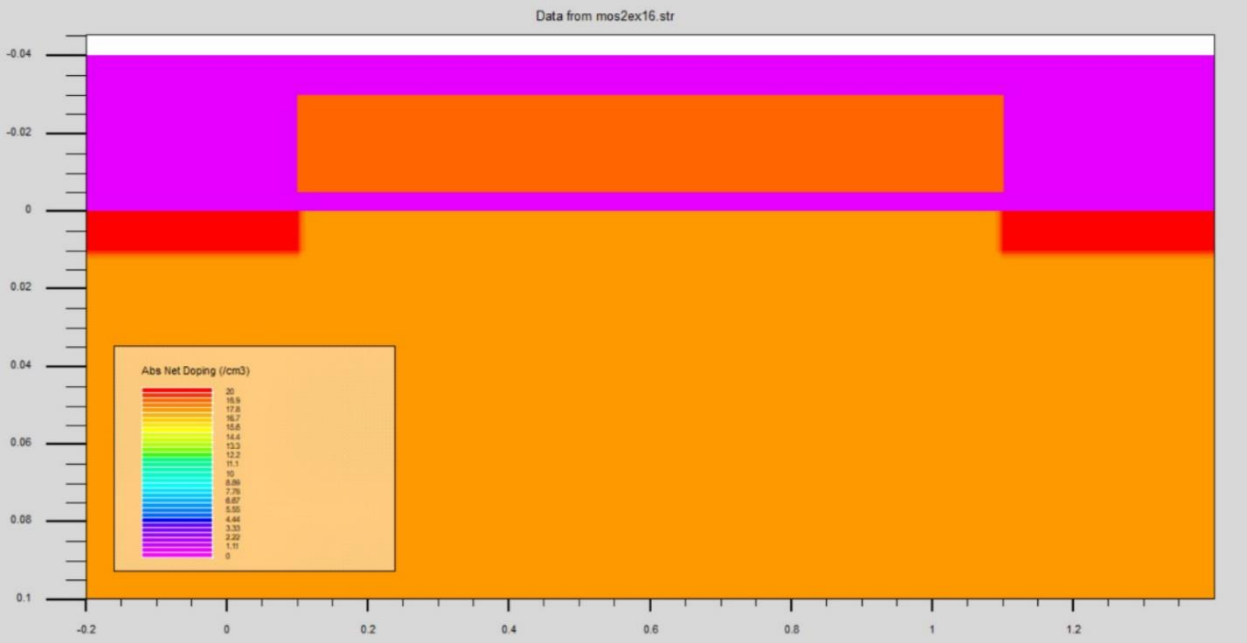

Figure 23 doping concentration.

17.Absolute net doping concentration:

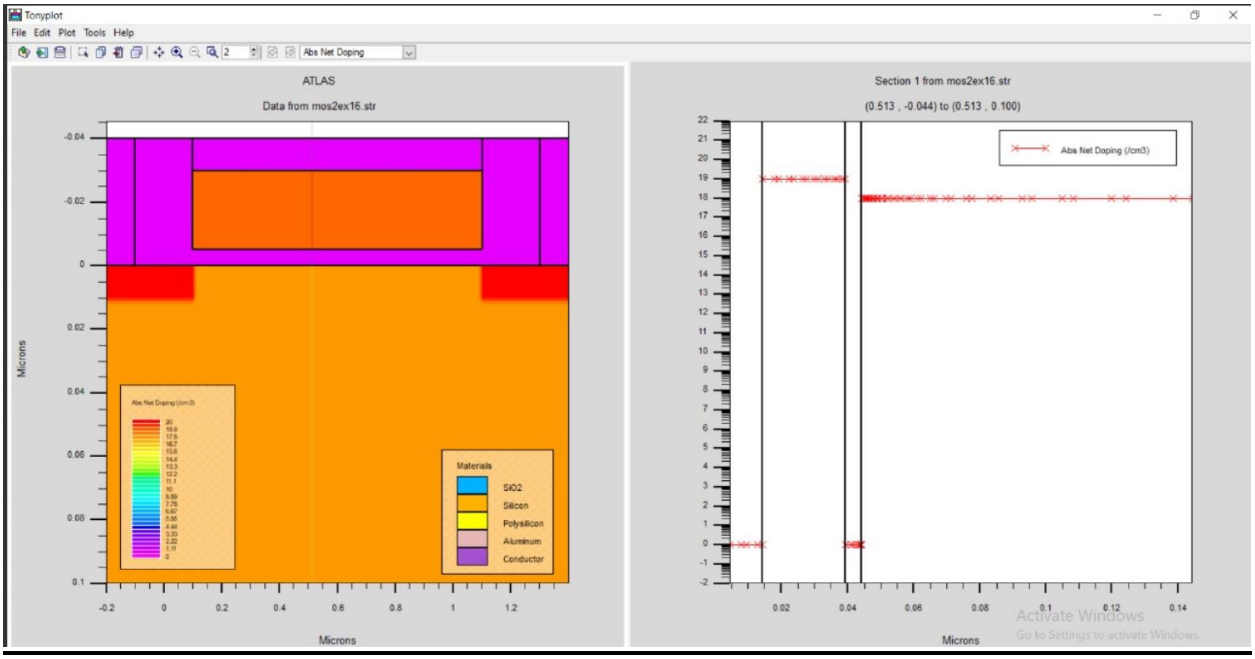

Figure 24 Absolute net doping concentration.

18.Electric field:

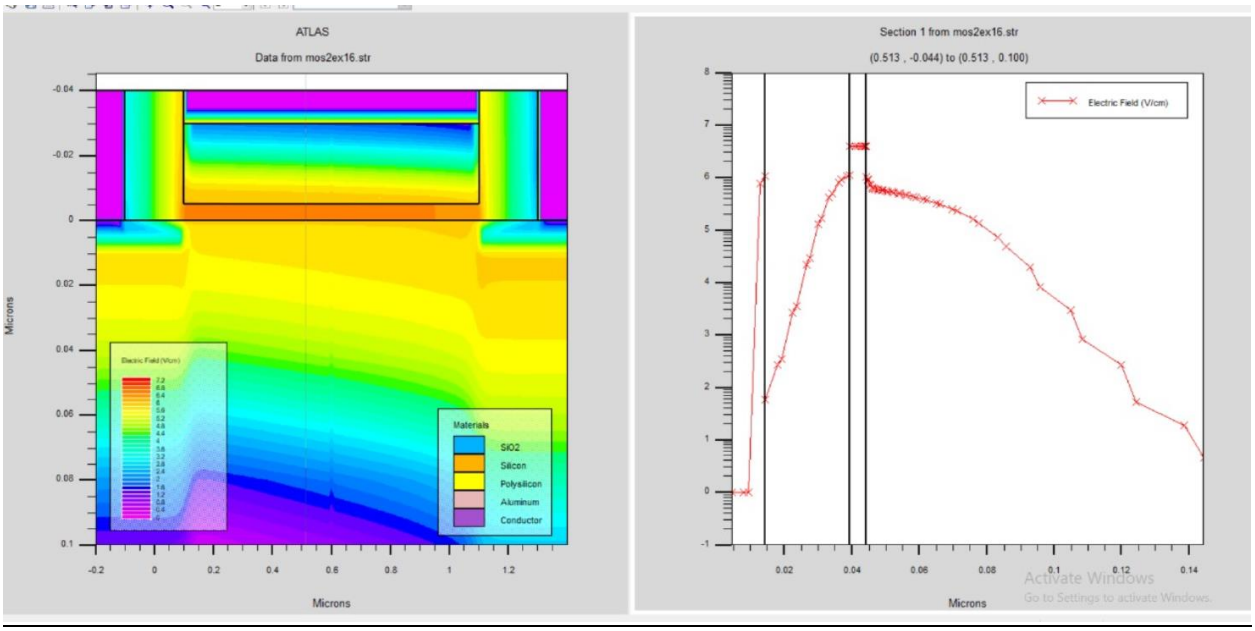

Figure 25 electric field.

19.Potential

The electrostatic potential within the gate region is established by the gate voltage. When a positive Vgs is applied, it attracts electrons from the source region. This process leads to the formation of an inversion layer in the channel region, causing a decrease in the overall potential.

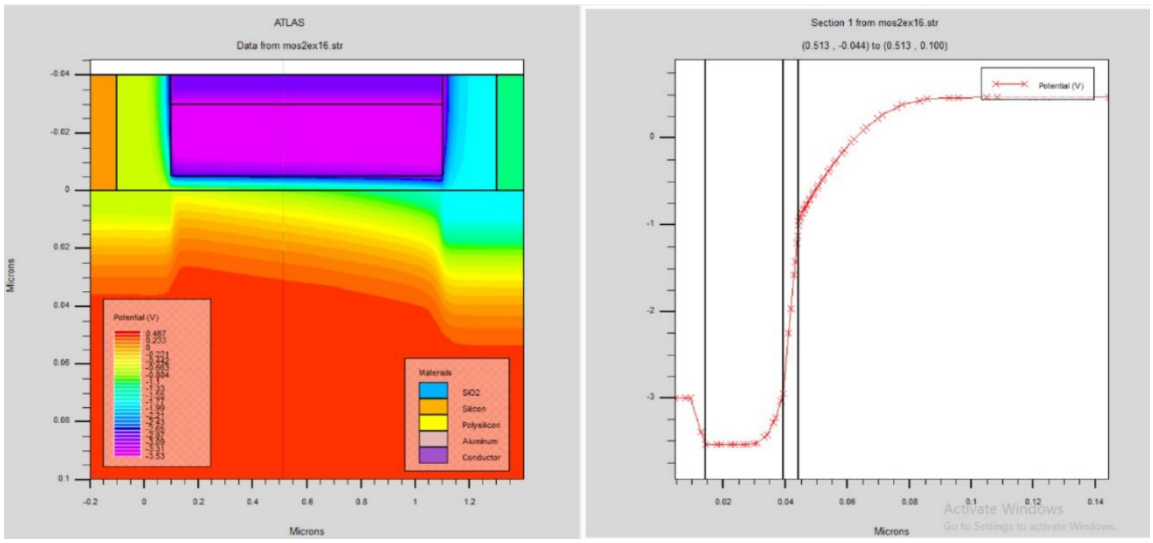

Figure 26 potential.

20.Recombination Rate:

The recombination rate within a MOSFET device represents the speed at which minority carriers (holes in an n-type MOSFET or electrons in a p-type MOSFET) combine with majority carriers (electrons in an n-type MOSFET or holes in a p-type MOSFET) within the channel region. Recombination can arise from different mechanisms, including Shockley-Read-Hall recombination.

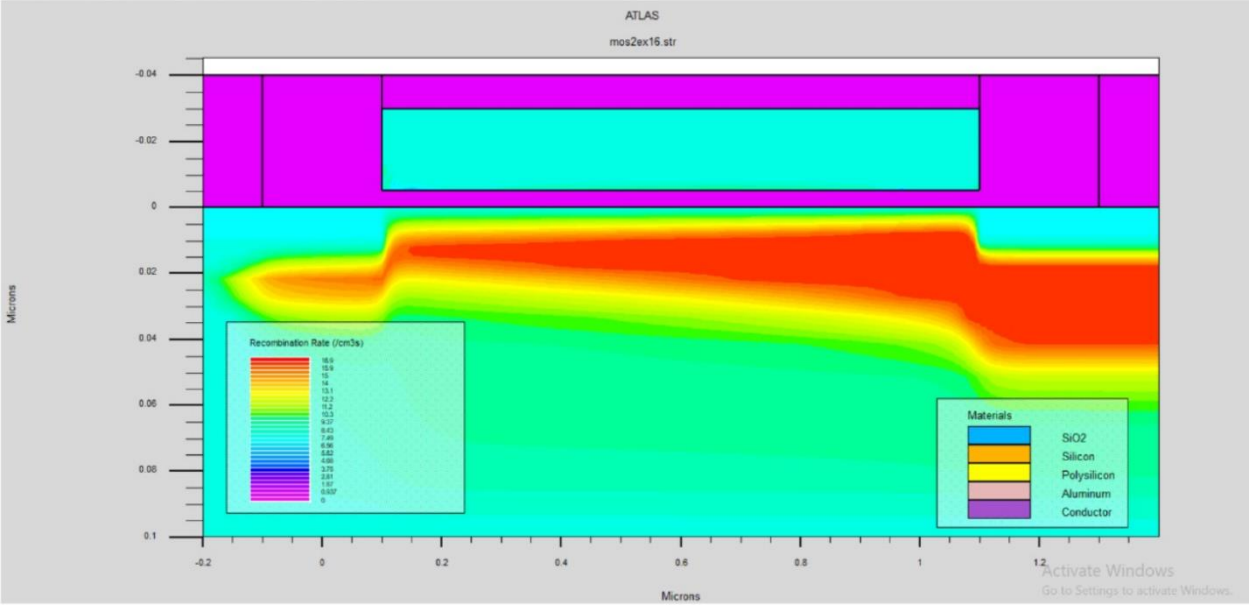

Figure 27Recombination rate.

21.Changes due to temperature:

The threshold voltage: It is solved by takes 2 points from Id vs Vgs curve at different temperatures and solving for VT using the following equation:

$$\frac{I_{ds1}}{I_{ds2}} = \frac{(V_{gs1} - V_T)^2}{(V_{gs2} - V_T)} = 2$$

VT at T = 300 K: -0.7807 V

VT at T = 400 K: -0.7141 V

VT at T = 500 K: -0.6322 V

Transconductance (gm): It is solved by taking 2 points from Id vs Vgs curve at different temperatures and taking the slope at the liner region.

At T = 300 K: $7.96 * 10^{-7}$

At T = 400 K: $1.25* 10^{-6}$

At T = 500 K: $1.65 * 10^{-6}$

Output resistance (channel conductance gd): It is solved by taking 2 points from Id vs Vds curve at different temperatures and taking the slope at the liner region.

At T = 300 K: $7.27 *10^{-6}$

At T = 400 K: $6.49* 10^{-6}$

At T = 500 K: $6.33 * 10^{-6}$

Phase2: Short channel Model

In short channel PMOS structure, the scaling factor used is **K=0.18** and these are the parameters after scaling:

Parameter and value in long channel	Value	Scaling ratio	Value after scaling
Channel length (L)	1um	k	180nm
Width (W)	10L	k	1.8um
Gate conductor thickness	10um	k	1.8nm
Source & drain conductors' lengths	40nm	k	7.2nm
Gate oxide thickness	3nm	k	7.2nm
Polysilicon Gate	25nm	k	4.5nm
Junction depth 60 nm	10nm	k	1.5nm
Doping concentration	1*10^20	1/k	5.6*10^20
Polysilicon doping	1*10^19	1/k	5.6*10^19
Substrate doping	1*10^18	1/k	5.6*10^18
Body depth	100nm	k	18nm

I. Drain current vs gate voltage.

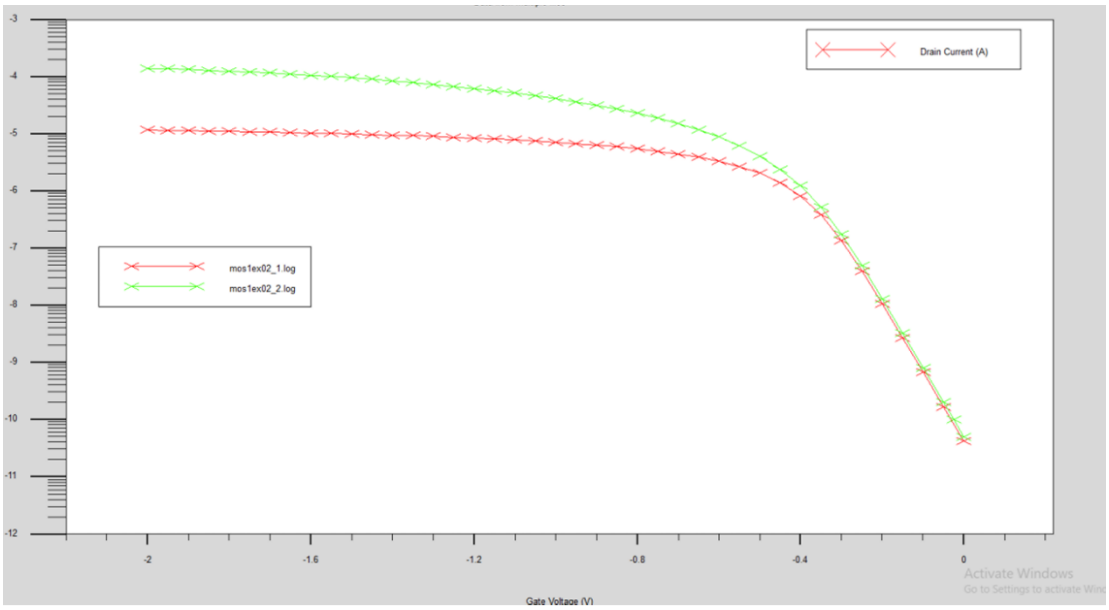

Figure 28Vg vs ID at two vds values.

In figure 29, green curve represents Vds = -0.005 V and red represents Vds = -1.2 V.

II. Drain current vs vds.

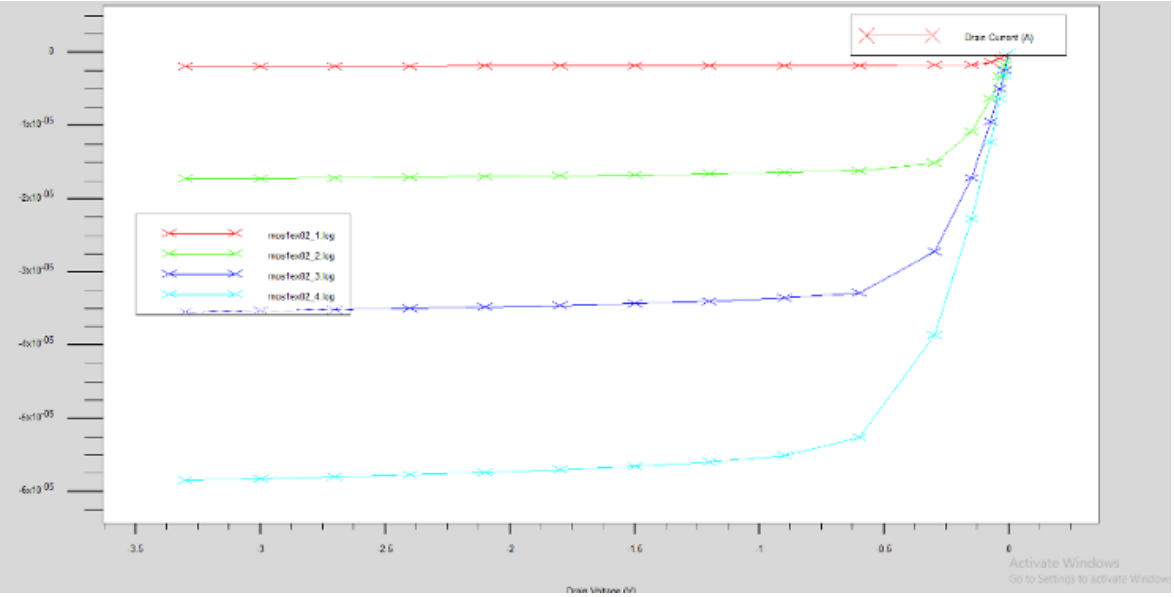

Figure 29 Drain current vs vds.

In figure 30, the red curve is -0.5 v, green is -0.8 v, blue is -1v, cyan is -1.2v.

III. Saturation region limitation

Using Id vs Vds graph at Vgs = -1.2 in figure 31, the saturation part is examined. Since the
saturation region has a nearly linear slope, then the region is influenced by the velocity saturation, not the pinch off point. This is due to the presence of horizontal electric field of range 10^4 V / cm.

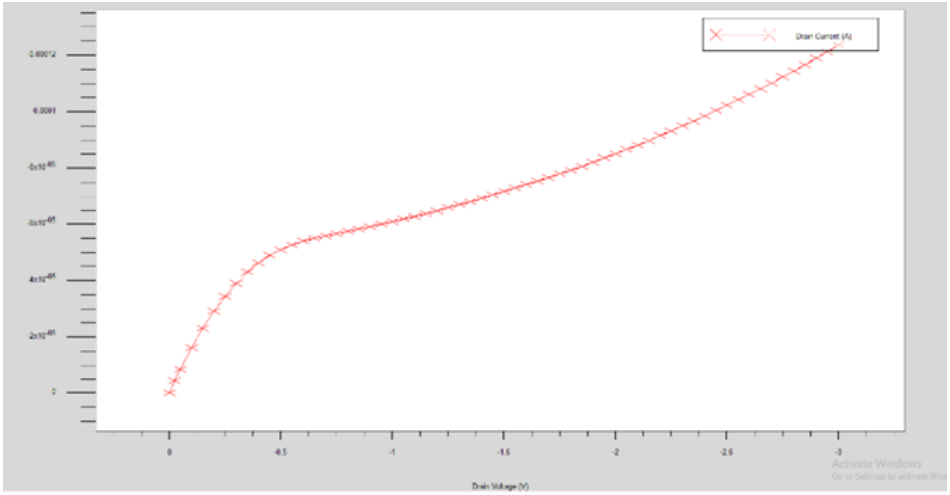

Figure 30 ID vs VGS at -1.2 v

IV. Subthreshold swing

The subthreshold swing is the rate of change of drain current with respect to gate voltage in the subthreshold region.
It's determined by the slope of the log Id vs Vgs graph (figure 29), through the following equation:

$$\frac{dlog\ abs(I_D)}{dV_{gs}} = \frac{(-6.391)-(-6.381)}{-0.379-(-0.38)} = -10$$

V. Threshold voltage

To get the threshold voltage in saturation region, we plotted the relation between root(id) and vgs, to get that the threshold voltage is nearly **-0.26v** as shown in figure 32.

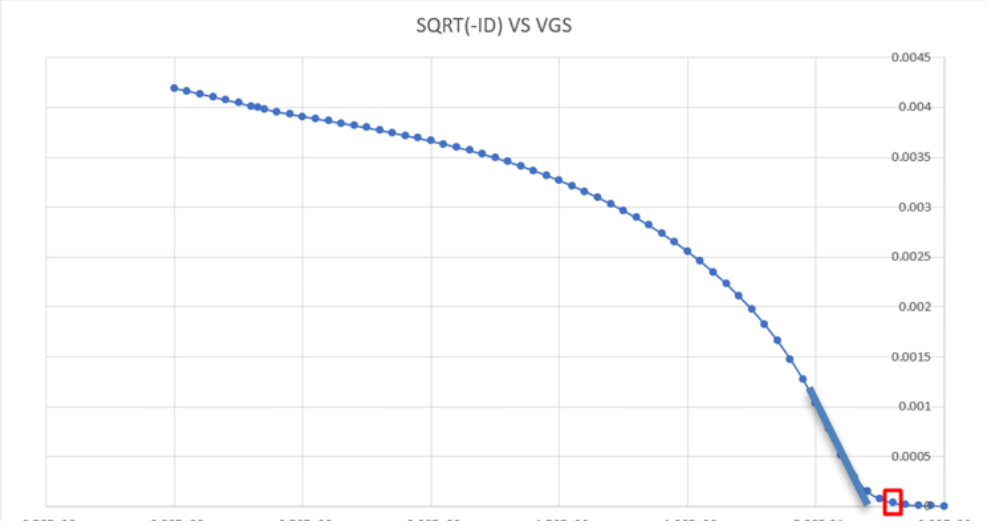

Figure 31 SQRT(-id) vs Vgs at vds= -0.005v.

To get the threshold voltage in linear region, we observe the threshold voltage form the relation between id and vgs as shown in figure 33, Vth nearly equals **-0.5v**.

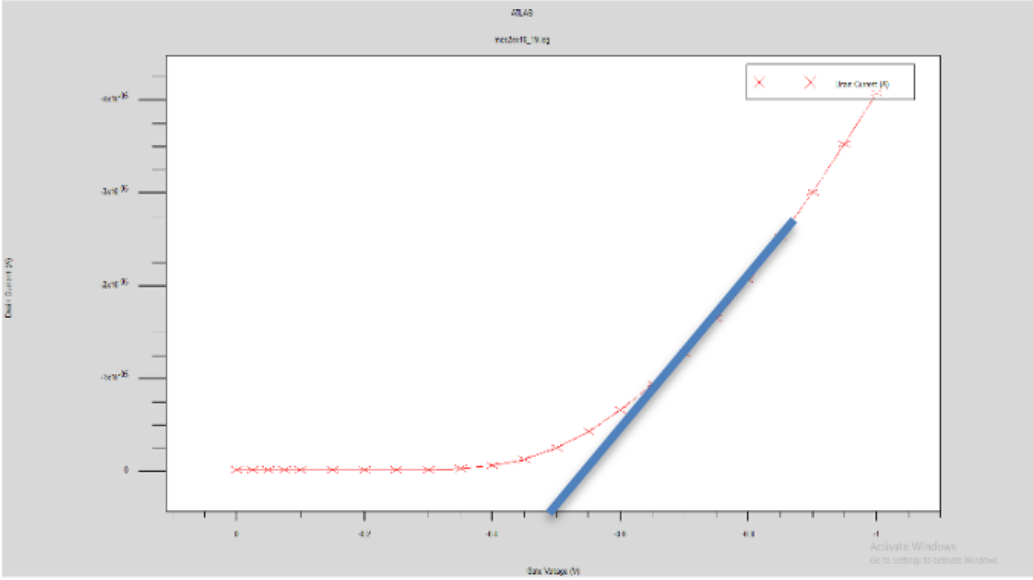

Figure 32 Id vs VGS.

VI. Gate oxide tunneling

Gate oxide tunneling occurs by passing charge carriers into the gate oxide by overcoming the energy barrier of the oxide. As shown in figure 34, the absolute of tunneling increases by increasing the absolute of gate voltage as the increase in the voltage gives the charge carriers more energy, thus increasing the probability of tunneling.

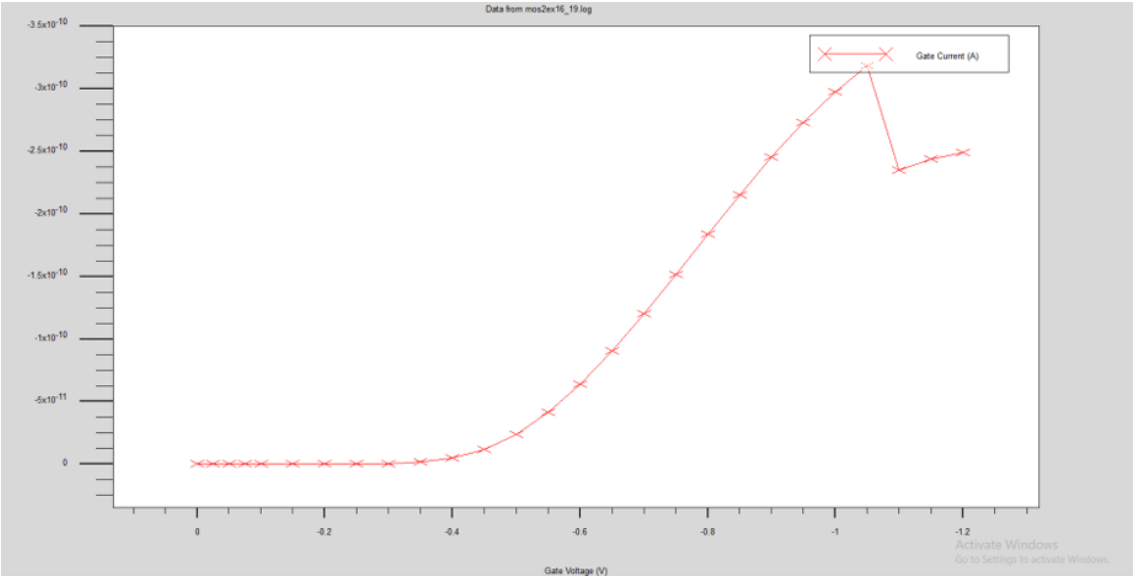

Figure 33 vg vs id to show tunneling effect.

VII. Holes density

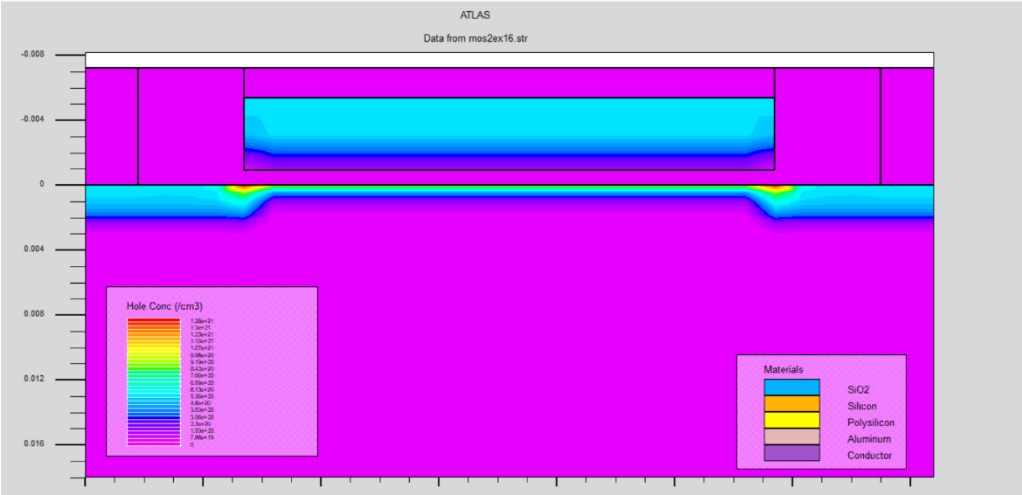

Figure 34 holes concentration.

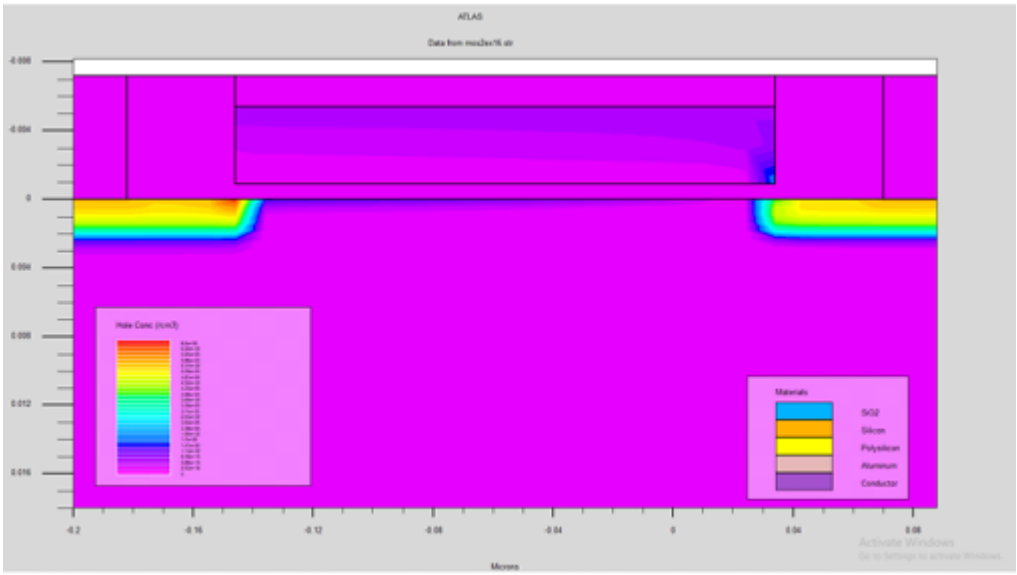

Figure 35 hole concentration.

Figure 35 is the hole concentration at vgs of -0.005 V and Vg of -1V and figure 36 is the hole concentration at V drain = -1.2 V and Vgate = -1 V. Since Vth = -0.25 V, then Vdrain > (Vgate – Vth). This caused change in equivalent channel length due to channel length modulation.

VIII. DIBL (Drain-Induced Barrier Lowering).

It's the is the contribution of the drain voltage to reduce the barrier between the source and drain and the phenomenon where the drain voltage (VDS) affects the effective threshold voltage (VTH) of the transistor.

It's calculated by the relation:

$$DIBL = \frac{(Vth1 - Vth2)}{(Vds1 - Vds2)}$$

If we take any two values as vd1 = -50 mV, vth1 = -0.247, vd2 = -1.2 V, vth2 = -0.315 V.

DIBL =0.059

In general, a lower DIBL value is desirable, as it indicates better short-channel effect control and improved transistor performance.

IX. Channel length modulation parameter.

The effective channel length is also bias dependent and is modulated by VDS. Channel length modulation is the change of the effective channel length by the shifting of the pinch off point more towards the source. This occurs if the drain voltage increases to more than the saturation drain voltage. The Channel length modulation parameter is calculated using the Id vs Vds graph at saturation region as shown in figure 37.

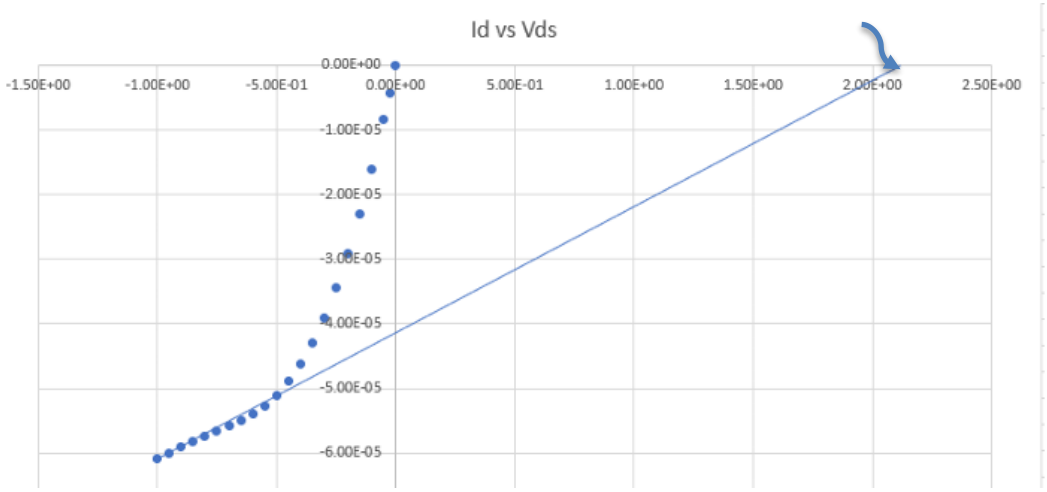

Figure 36 Id to Vds to show CLM.

Graph 37 helps us get the value of early voltage (Va) to calculate the CLM coefficient $\lambda = \frac{1}{Va} = \frac{1}{2.1} = 0.476\ 1/v$

The effect of that modulation is mostly not effective in the long channel as the distance of the shift of the pinch off is very low compared to the long channel. However, It becomes effective in the short channel. As the change in the channel length increases, the effective length decreases, increasing the drain current.

X. Channel effective mobility.

The mobility is how easy the charged particle to move. In short channel MOSFETs, the mobility variates due to the electric field due to gate voltage (this is called coulomb interaction). As the gate voltage increases, the electric field increases, decreasing the mobility of the charge carriers (holes in PMOS).

Mobility varies with gate voltage, as surface scattering is the positive fixed oxide charge near the oxide-semiconductor interface will further reduced mobility due to the additional coulomb interaction.

Mobility vs Vgs

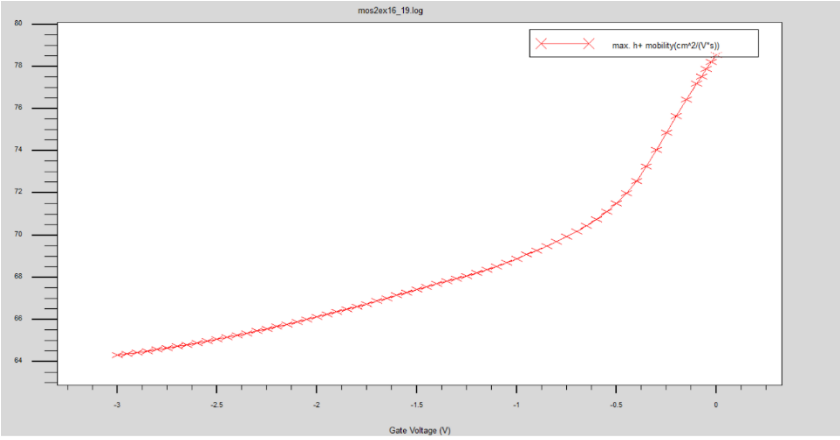

Figure 37 mobility vs gate voltage.

In short-channel PMOS transistors, mobility decreases with increasing gate voltage due to the increased vertical electric field causing surface scattering. At high $V\ g$ Vg, mobility reduction is further compounded by velocity saturation effects. These variations can be described using empirical models that account for field-dependent mobility degradation and short-channel effects.

Mobility vs vds:

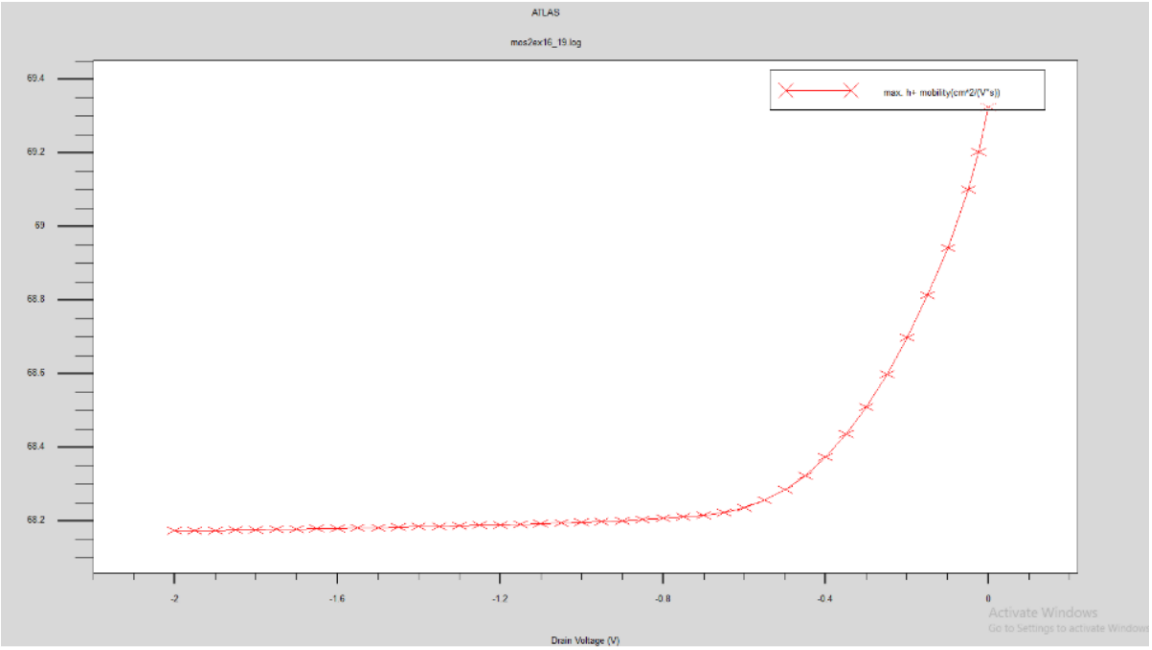

Figure 38 mobility vs vds.

As the drain voltage increases, the electric field in the channel increases, decreasing the mobility limiting the carriers' acceleration.

This variation is critical in designing and optimizing short-channel PMOS transistors for high-speed and high-frequency applications, where understanding and mitigating mobility degradation is essential for improving device performance.

XI. Junction depth changes

First, the provided values (20 nm, 30 nm, 60 nm, 90 nm) should be scaled according to the technology mode. K = 0.18

Depth before scaling	Depth after scaling
20 nm	3.6 nm
30 nm	5.4 nm
60 nm	10.8 nm
90 nm	16.2 nm

The threshold voltage did not change and is the same in all 4 depths: the junction depth does not change the number of charge carriers in the channel (no doping changes). In addition to that, no electric field change occurs.

Figure 40 shows the gate voltage and Id relation which is the same for the 4 depths as threshold voltage is nearly -0.5V.

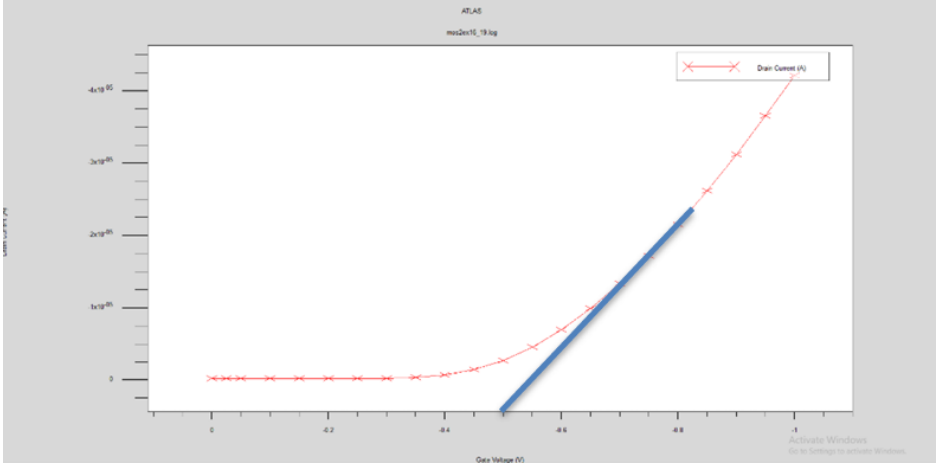

Figure 39 id vs vg.

XII. Low frequency capacitances

At low frequencies, charge carriers have sufficient time to respond to changes in the gate voltage, and the capacitances reflect both the intrinsic device characteristics and any additional short-channel effects.

Gate capacitance:

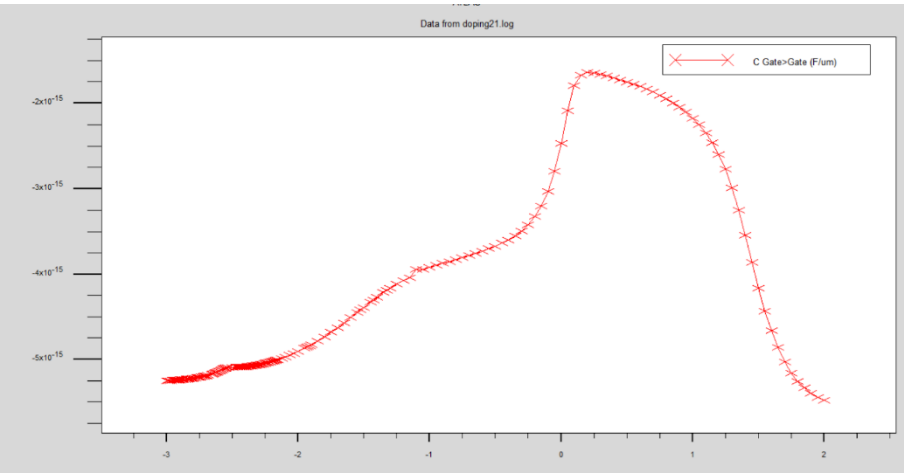

Figure 40 Gate capacitance.

Source capacitance:

Overlap Capacitance: This component remains the same as in long-channel devices and is due to the overlap of the gate with the source region.

Channel Capacitance: In the linear region, the channel capacitance is significant and changes with Cox is the oxide capacitance per unit area, W is the channel width, and L is the channel length. Due to short-channel effects, the effective channel length L might be reduced.

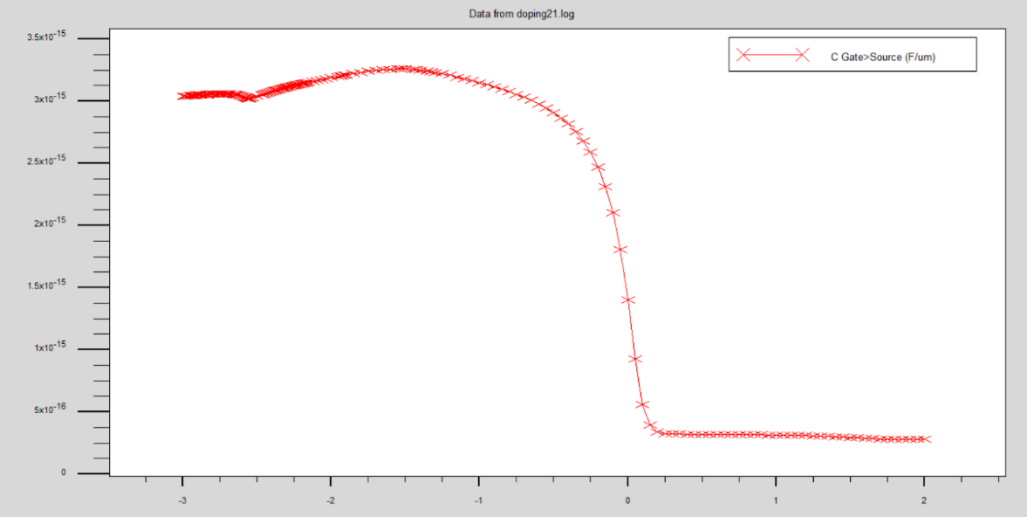

Figure 41 Source capacitance.

Drain capacitance:

Overlap Capacitance: As with Cgs, this component remains similar to the long-channel case.

Channel Capacitance: In the saturation region, the channel pinch-off reduces the channel capacitance component, but in short-channel devices, this reduction is less pronounced due to the proximity of the drain to the source.

Miller Effect: In short-channel devices, the Miller capacitance can be significant due to high gains and can modify the effective Cgd.

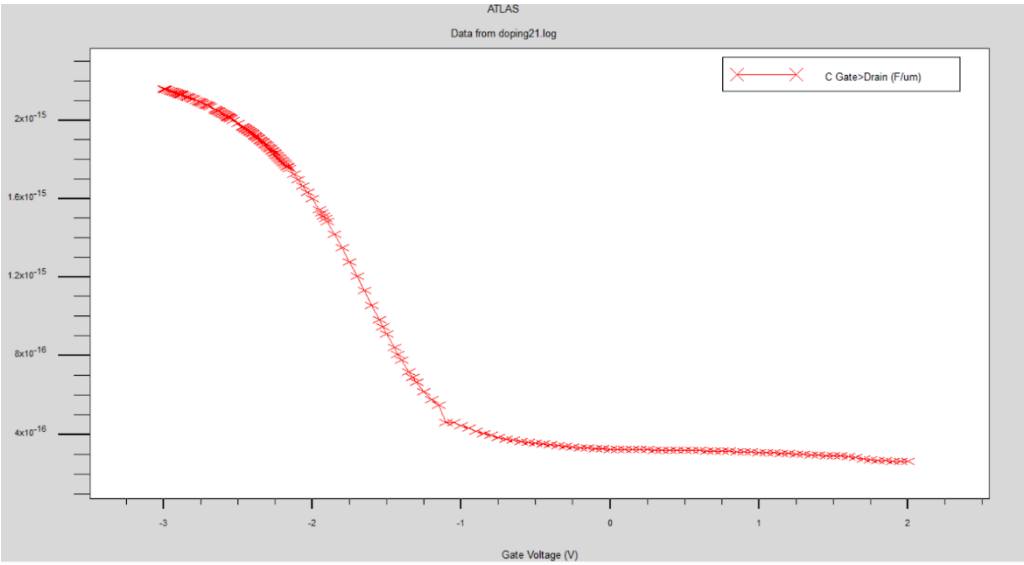

Figure 42 Drain capacitance.

XIII. High frequency capacitances

At high frequencies, the dynamic response of the charge carriers is limited, and the capacitances reflect primarily the geometric overlaps and the immediate response to the gate voltage changes.

Gate capacitance:

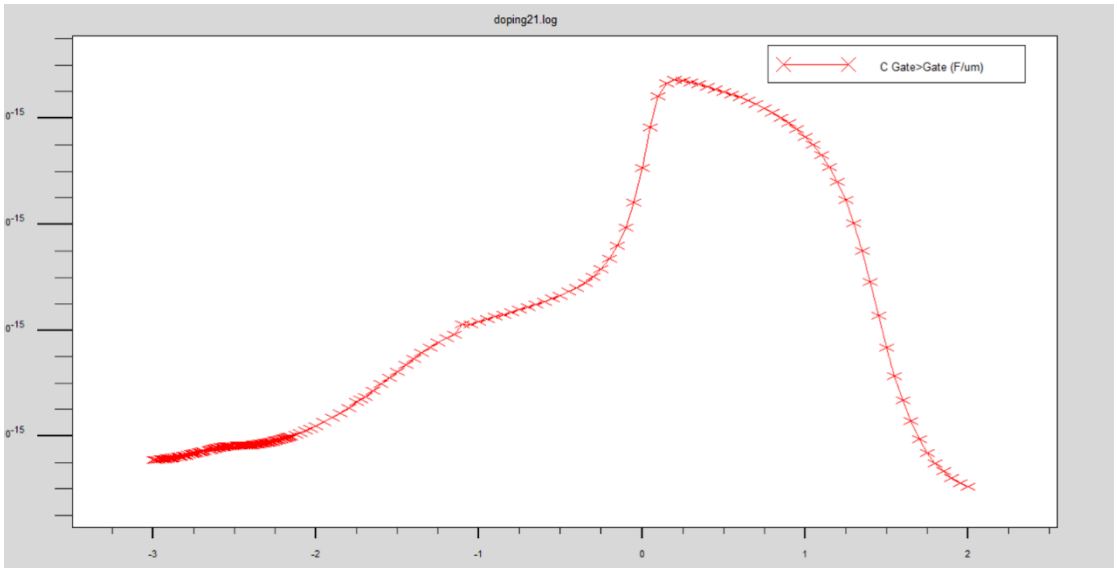

Figure 43 Gate capacitance.

Source capacitance:

Overlap Capacitance: Dominates at high frequencies, like the long-channel case. Reduced Channel Contribution: The channel capacitance is less significant because the carriers cannot respond quickly enough.

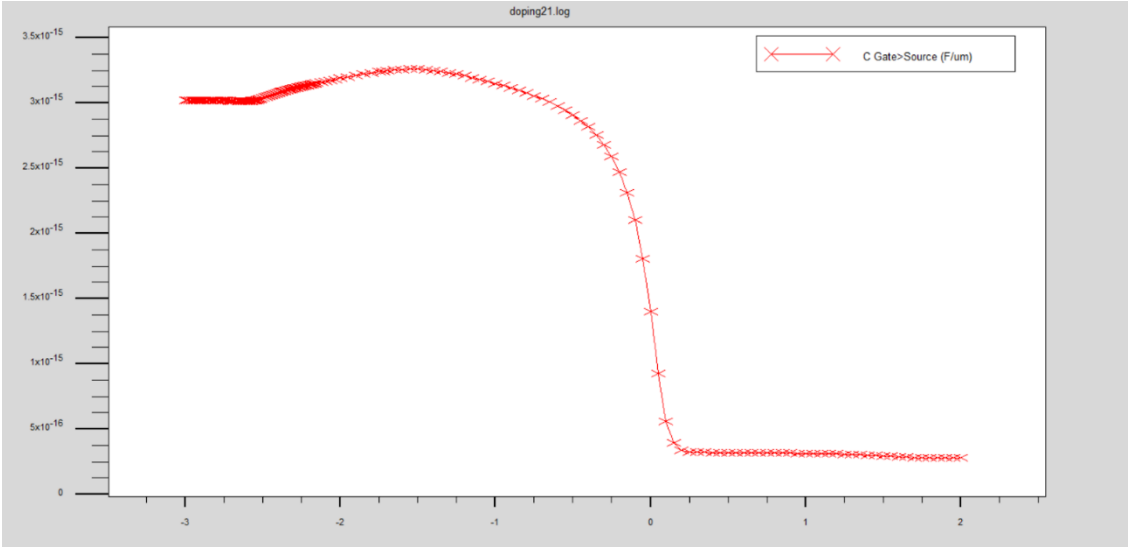

Figure 44 Source capacitance.

Drain capacitance:

Overlap Capacitance dominates.

Reduced Miller Effect: The high-frequency response limits the impact of the Miller effect, but in short-channel devices, this effect might still be more pronounced than in long-channel devices due to higher intrinsic gains.

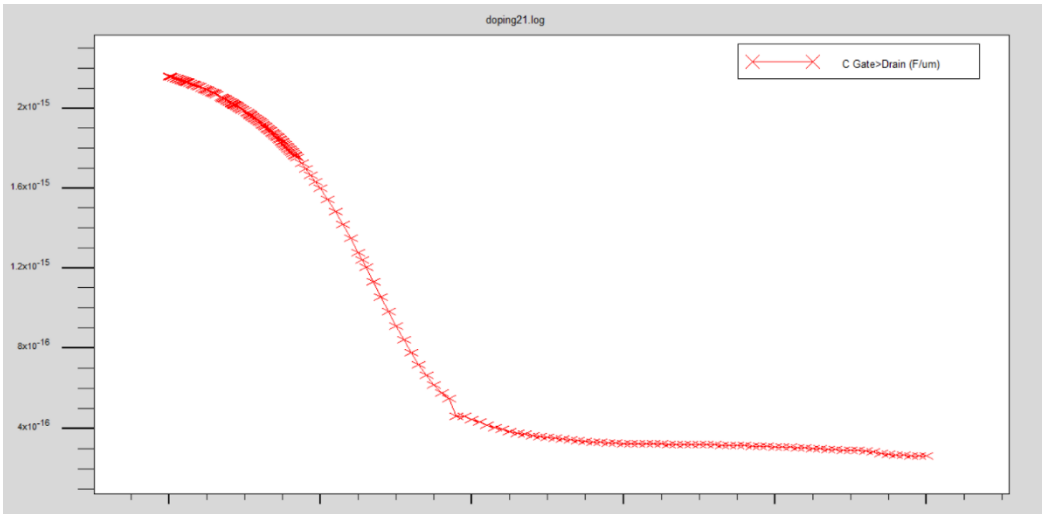

Figure 45 Drain capacitance.

XIV. Tunneling

The absolute of tunneling increases by increasing the absolute of gate voltage as the increase in the voltage gives the charge carriers more energy, thus increasing the probability of tunneling.

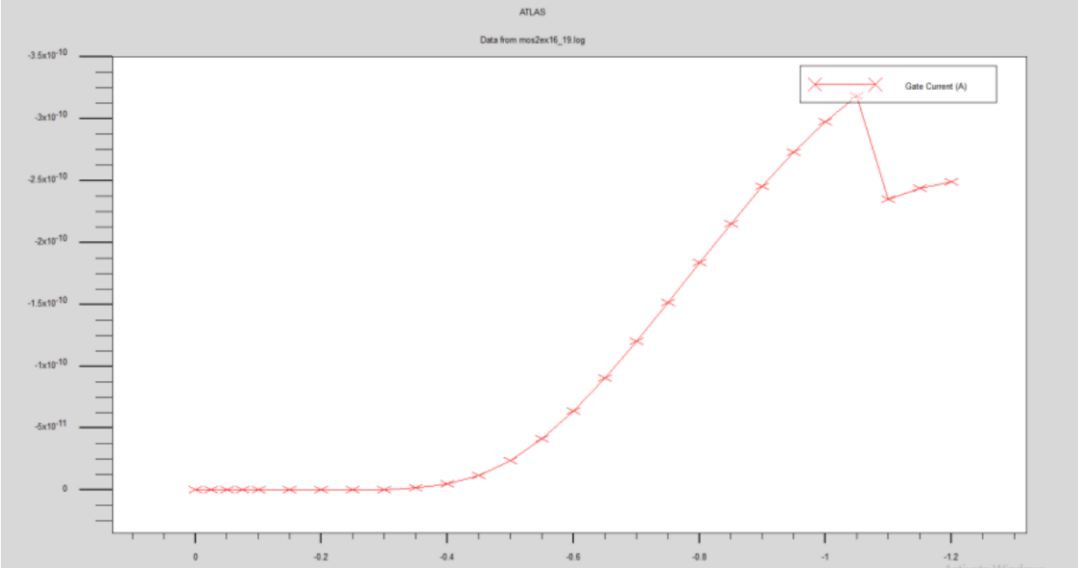

Figure 46 tunneling effect.

XV. Cross section structure

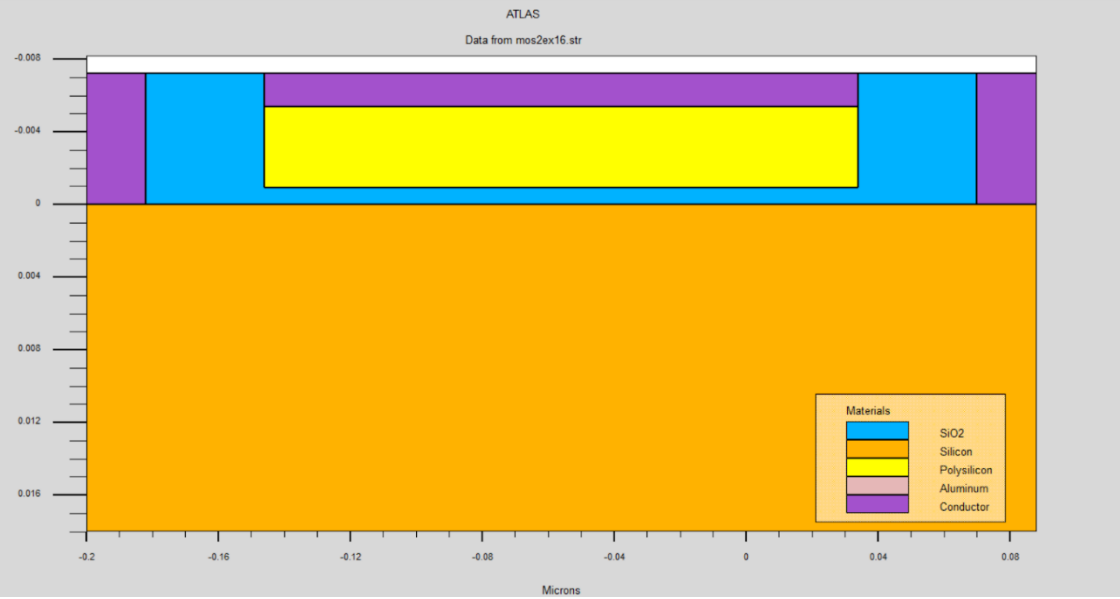

Figure 47 structure.

XVI. Meshing

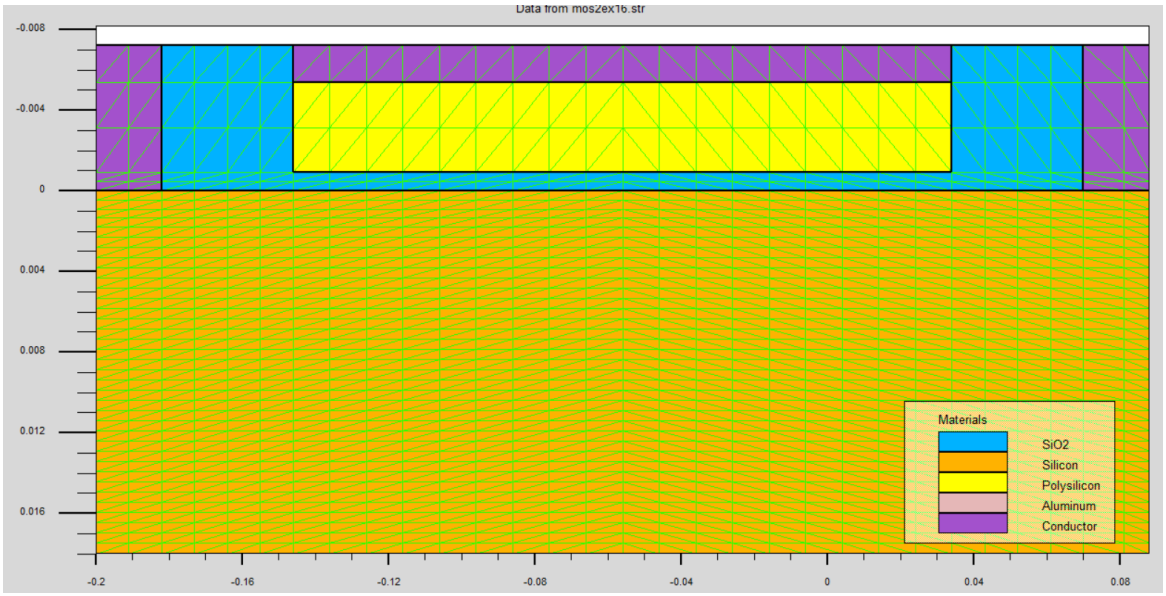

Figure 48 Meshing.

XVII. Potential

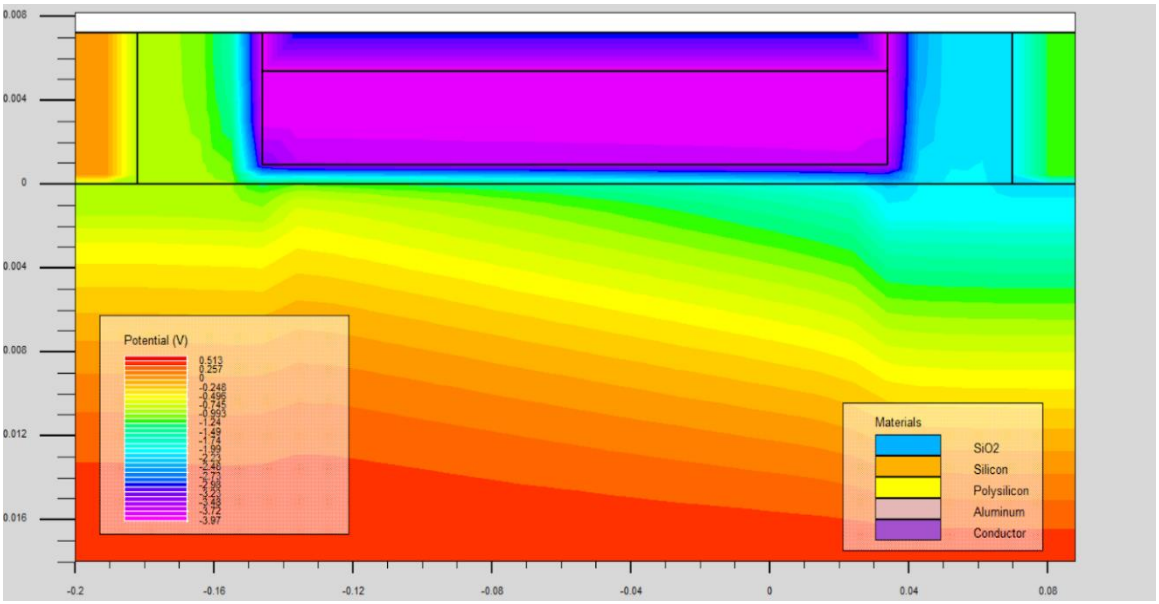

Figure 49 Potential.

XVIII. Electric field

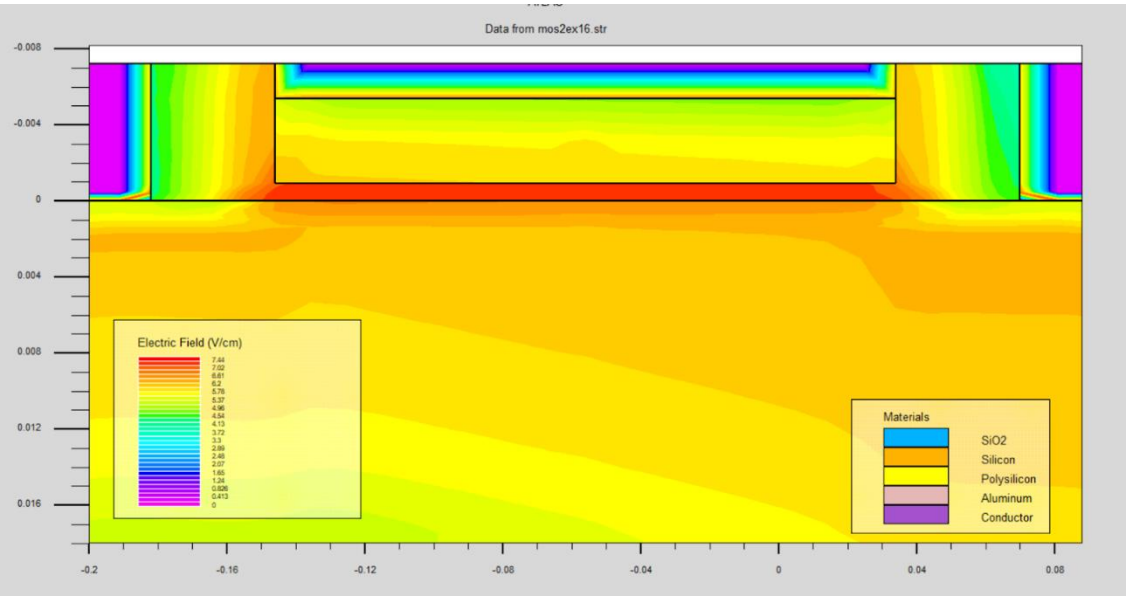

Figure 50 Total Electric field.

XIX. Recombination rate

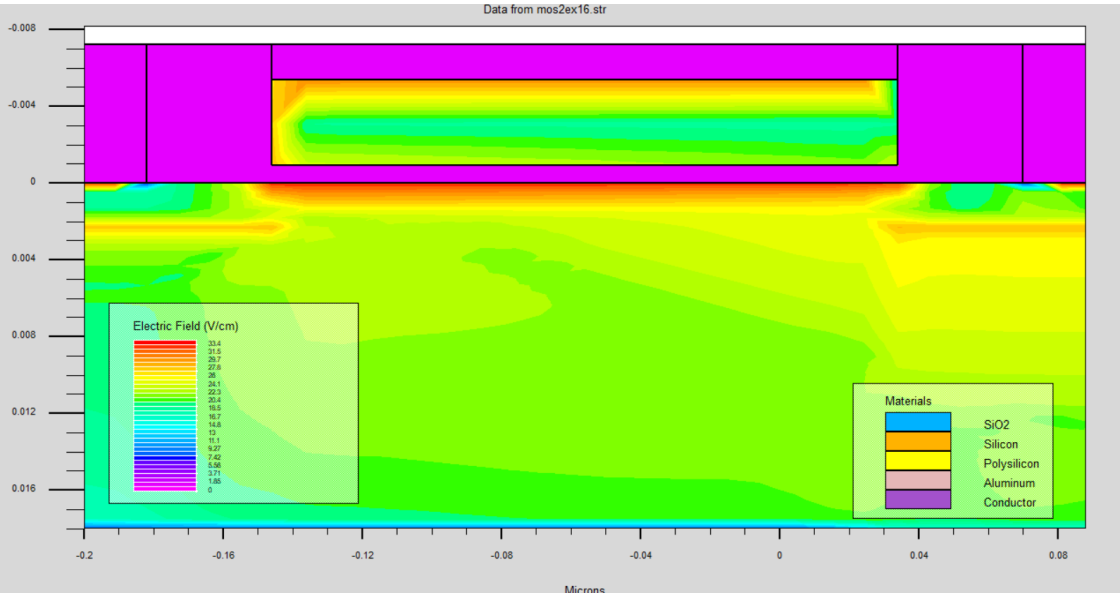

Figure 51 Recombination rate.

XX. Abs net doping

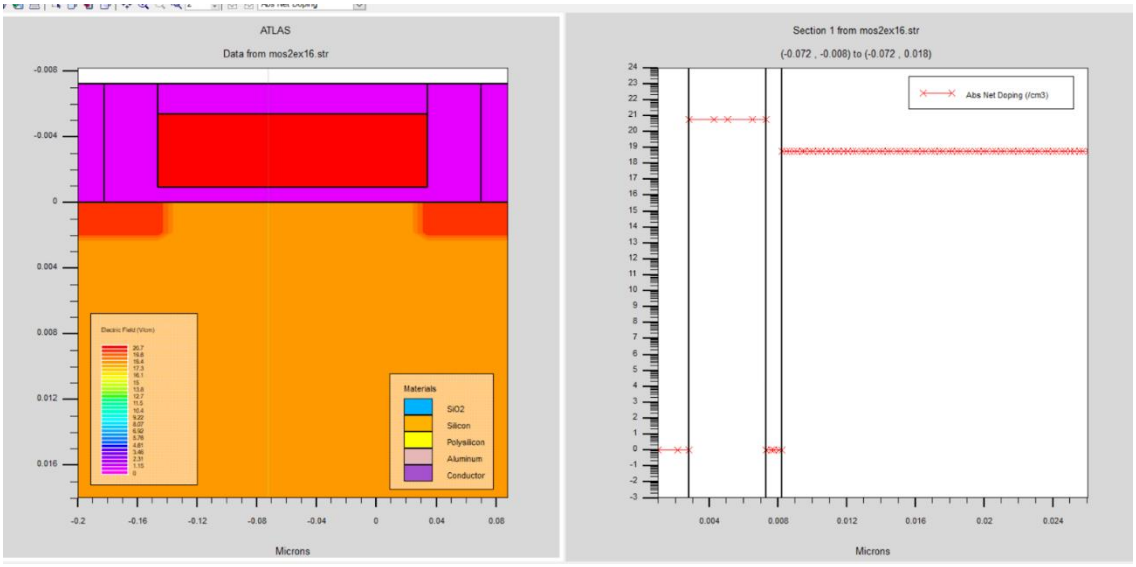

Figure 52 Abs net doping.

XXI. Transverse electric field

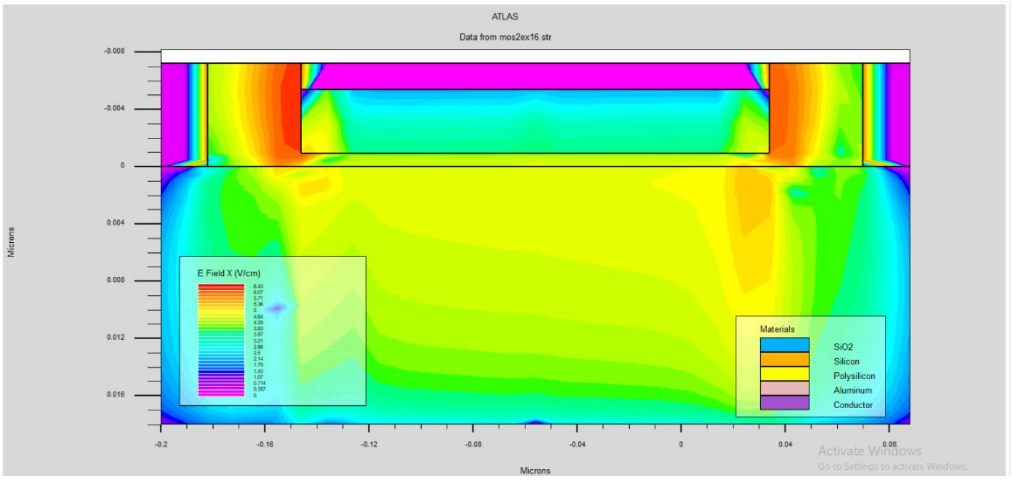

Figure 53transverse electric field.

XXII. Longitudinal electric field

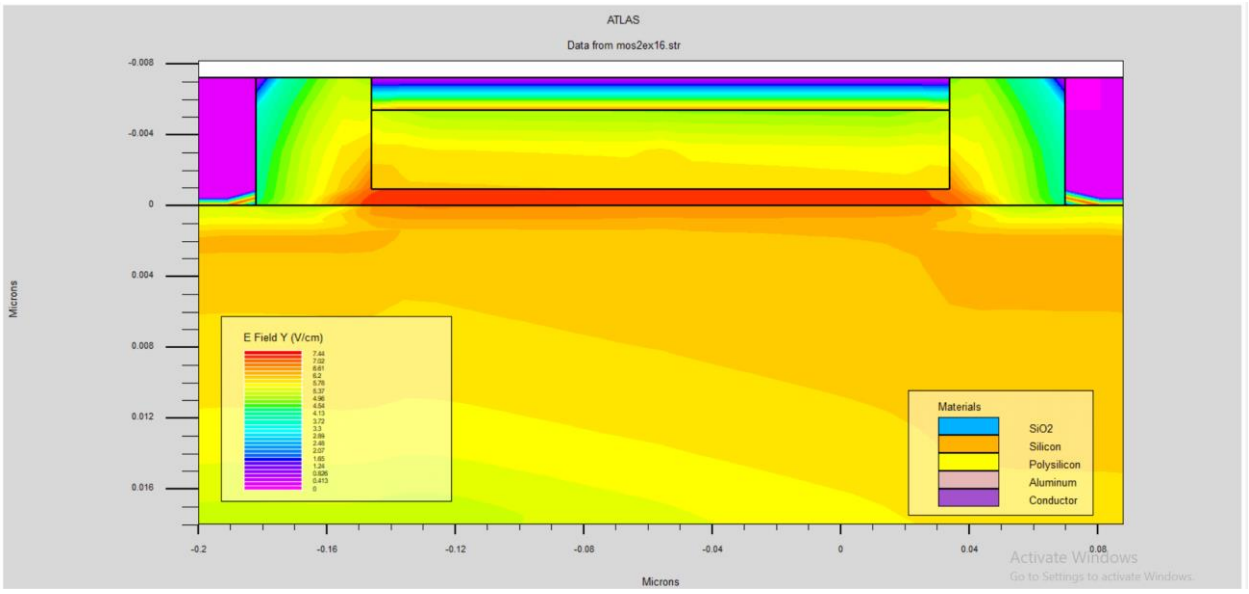

Figure 54 longitudinal electric field.

XXIII. Current density

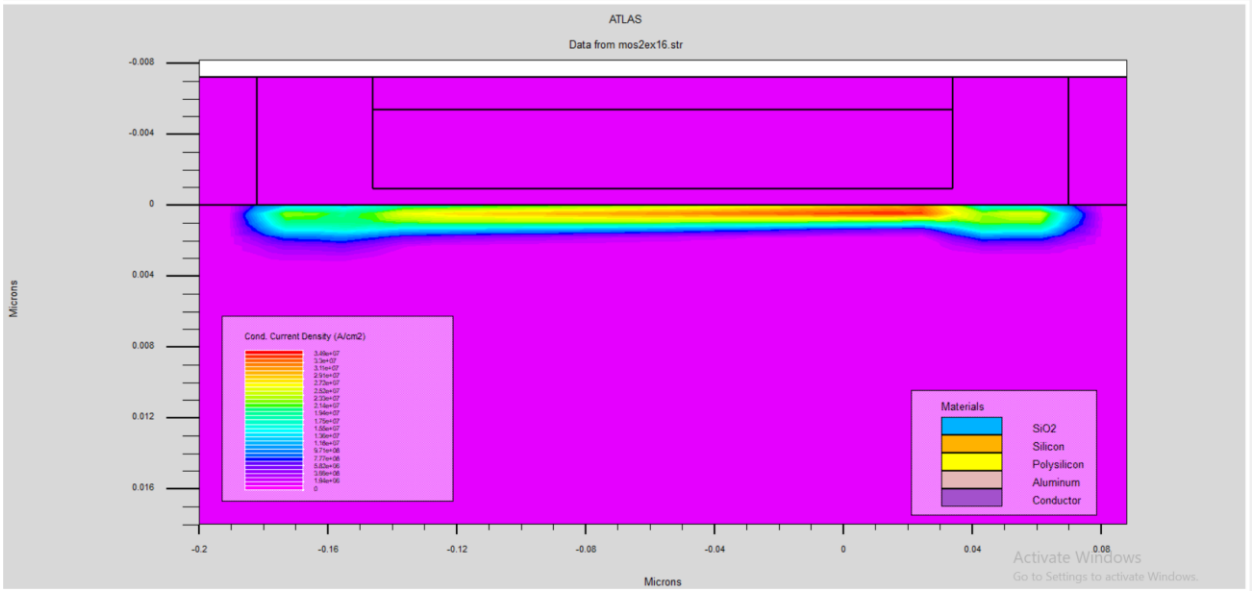

Figure 55 conduction current density.

The combination of DIBL and CLM in short-channel PMOS transistors causes the highest conduction current density to be in the region near the drain-channel junction, specifically on the drain-side of the channel.

Changes due to temperature

The threshold voltage: It is solved by takes 2 points from Id vs Vgs curve at different temperatures and solving for VT using the following equation:

$$Ids1Ids2 = (Vgs1 - VT)2(Vgs2 - VT)2$$

VT at T = 300 K: -0.7807 V

VT at T = 400 K: -0.7141 V

VT at T = 500 K: -0.6322 V

Transconductance (gm): It is solved by takes 2 points from Id vs Vgs curve at different temperatures and taking the slope at the liner region.

At T = 300 K: 7.96 * 10 -7

At T = 400 K: 1.25* 10 -6

At T = 500 K: 1.65 * 10-6

Output resistance (channel conductance gd): It is solved by taking 2 points from Id vs Vds curve at different temperatures and taking the slope at the linear region.

At T = 300 K: 7.27 *10-6

At T = 400 K: 6.49* 10-6

At T = 500 K: 6.33 * 10-6

References

[1] D. A. Neamen, SEMICONDUCTOR PHYSICS & DEVICES: BASIC PRINCIPLES, FOURTH EDITION, New York: McGraw-Hill, 2012.