**Analog Integrated Circuit Design - FALL 2023/2024**

# Two-Stage CMOS operational amplifier Report

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**Introduction:**

In this project we deign a two-stage CMOS operational amplifier, as the two-stage operational amplifier consists of a differential amplifier at the. input stage, while the second stage is a high gain stage biased by the output of the differential amplifier.

This design has to achieve some specifications in 65 nm technology shown in table 1:

| | |
|---|---|
| $V_{DD}$ | 1.2 V |
| GND | 0 V |
| Bias current of $M_{12}$ | 80 µA |
| $C_L$ | 0.2 pF |
| Nominal input common-mode (input DC level) | 0.6V |
| Nominal output common-mode (output DC-level) | 0.6 ± 0.1 V |
| Overall power consumption (including bias circuit) | ≤ 1 mW |
| Output peak-to-peak Swing | 0.7 V |
| Low-frequency differential to single-ended gain | ≥ 60 dB |
| Unity gain frequency | ≥ 900 MHz |
| Phase Margin | ≥ 60° |
| Slew rate | ≥ 5 V/µs |
| Maximum length of transistors | $5\times L_{min}$ |

Table (1). Requirements

And this is the circuit show in figure1:

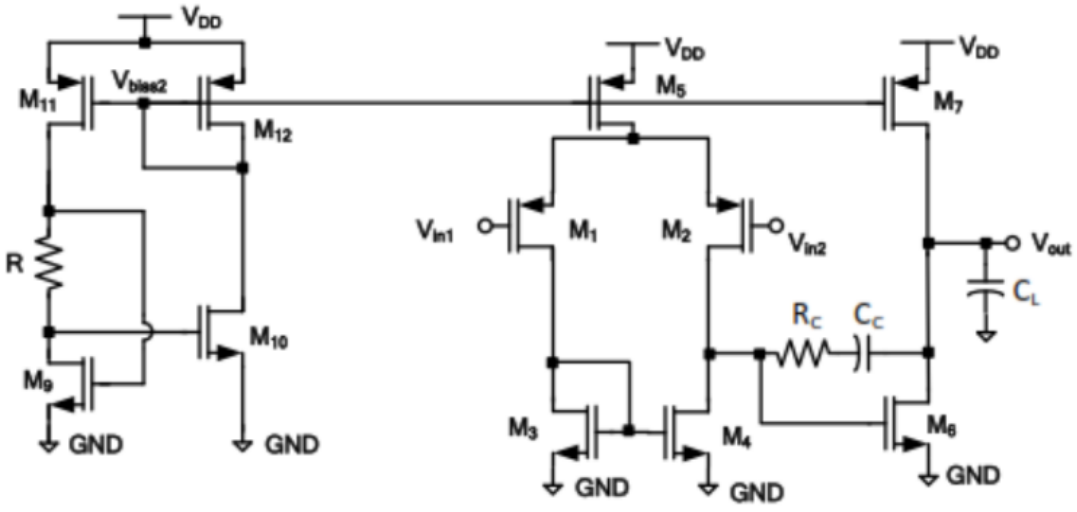


Fig (1). Two-stage op amp circuit

**Schematic:**

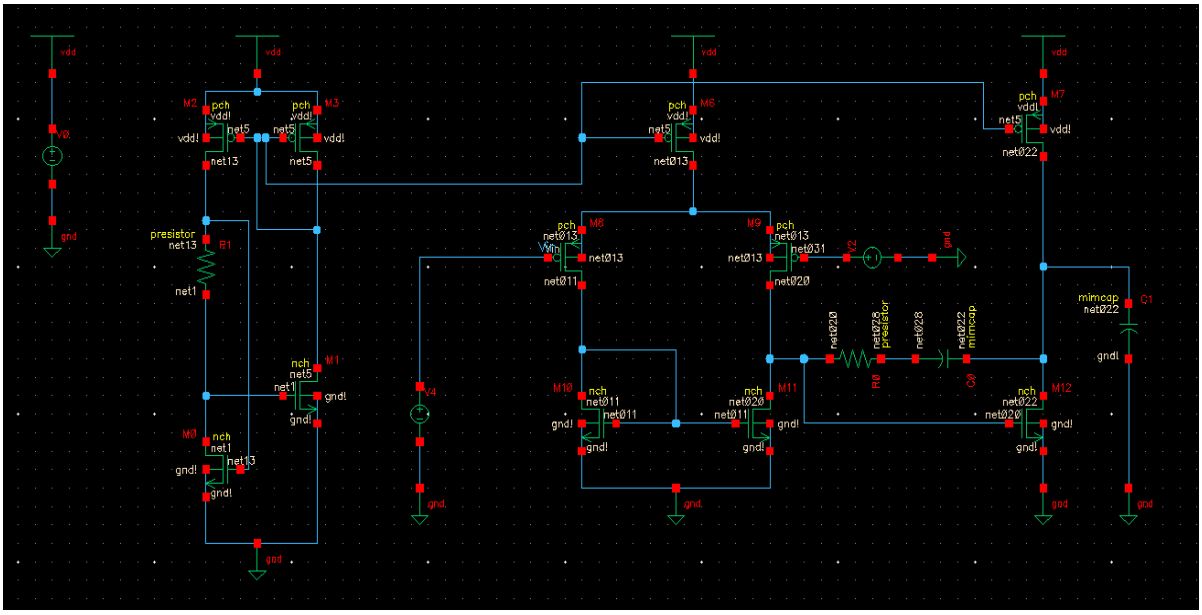


Fig (2). Schematic of whole circuit

**Current source bias circuit:**

This circuit is required to produce nearly 80 uA current with Vdd of 1.2 V, so our design was to put the suitable widths and length of the transistors to get the desired output current, so these are the used parameters after manipulations:

- Resistance used is polyresistance equals 1k ohms.
- The length of all the transistors is 5*$l_{min}$ = 325 nm.
- M2 and M3 PMOS have width of 9 um.
- M0 width is 3u.
- M1 width is nearly 6.3u.

Both the PMOS transistors have the same width, but there is a difference in the widths of the NMOS transistors to allow current flow and to produce output current of nearly 80 uA as shown in the $I_d$ of M1.

All the transistors are checked to be in the saturation region (region 2) as shown in figure 3.

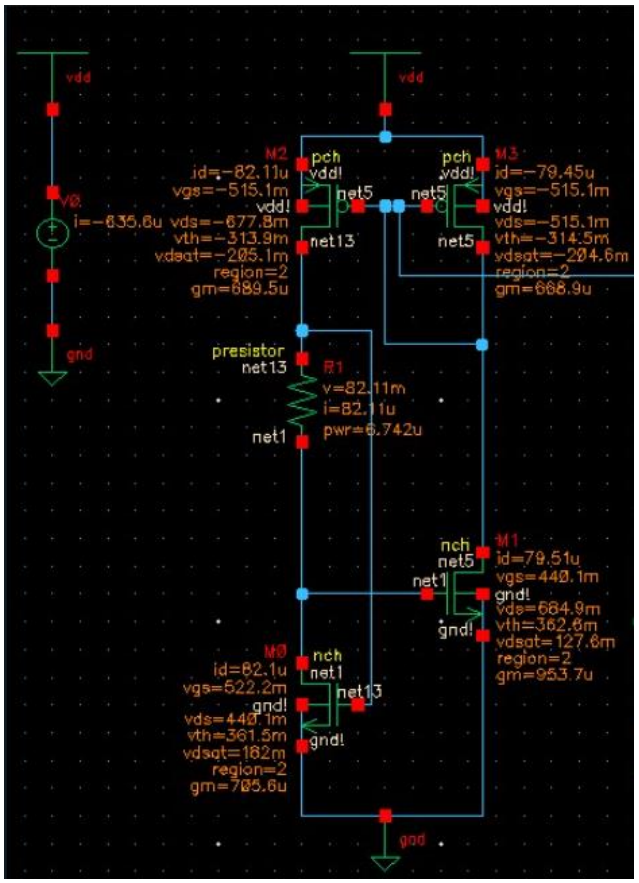


Fig (3). Current source circuit

**Amplifier stages:**

The first stage in the operational amplifier is considered as the stage to produce gain and the second stage is the one for the swing.

To reach the desired widths and lengths of the transistors we used the gm/id methodology to get the dimensions of the transistors (PMOS or NMOS) through the relation between gm/id and gm/gds and I/W.

**PMOS gm/id methodology curves:**

this is the curve for the relation between gm/gds and gm/id, as after the required analysis (shown in figure 6) the used curve is the blue one at 325 nm length that will give the desired gain and the width is gotten form I/W relation shown in figure (5).

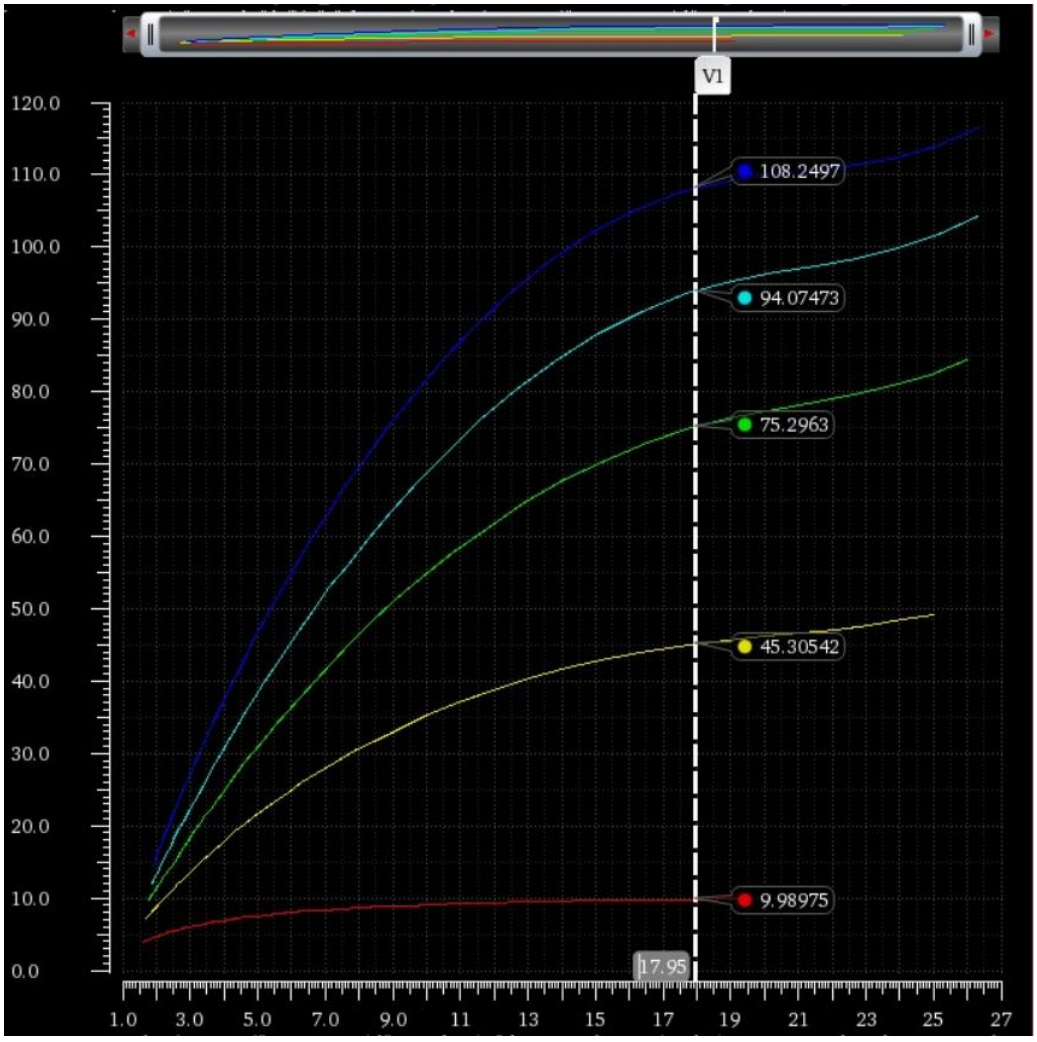


Fig (4). gm/id is at 17.95

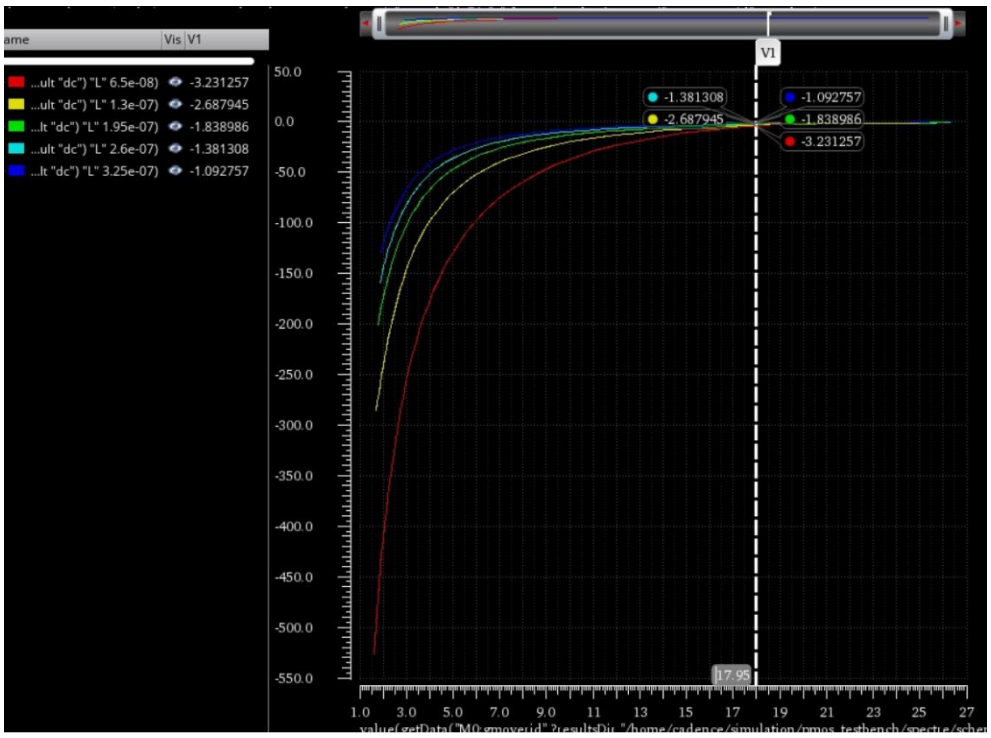


Fig (5). Relation with Id/w

So, from figure 5, Id/w suitable for our analysis equals 1.092757. Figure 6 will show the hand written analysis to get the length and width for the PMOS (M8 and M9) transistors as the length is 325 nm and width is 32 ums.

PMOS [M8, M9]

$\therefore GBW \geq 900\ MHz$

Let $\rightarrow \frac{g_{m1}}{2\pi C_c} = 1000\ MHz$ $\quad \because C_c = 0.1\ pF$

$\therefore g_{m1} = (1000)(2\pi)(0.1\ pF)$

$= 628.3\ \mu S$

Let $\rightarrow$ Slew Rate $= \frac{700\ V}{\mu S} = \frac{I_{B1}}{C_c}$

$\therefore I_{B1} = 70\ \mu A$

$I_{D1} = 35\ \mu A$

$\therefore \frac{g_{m1}}{I_D} = 17.95$ $\quad \therefore \frac{I_D}{W} = 1.092757$

$\therefore W = 32\ \mu m$ at $L = 325\ n$

Fig (6). Hand Analysis

**NMOS gm/id methodology curves:**

The same happened in PMOS is done here in the NMOS and the analysis shown in figures 7) and length of M10 and M11 transistors is 25 nm and the width is 1.02 um.

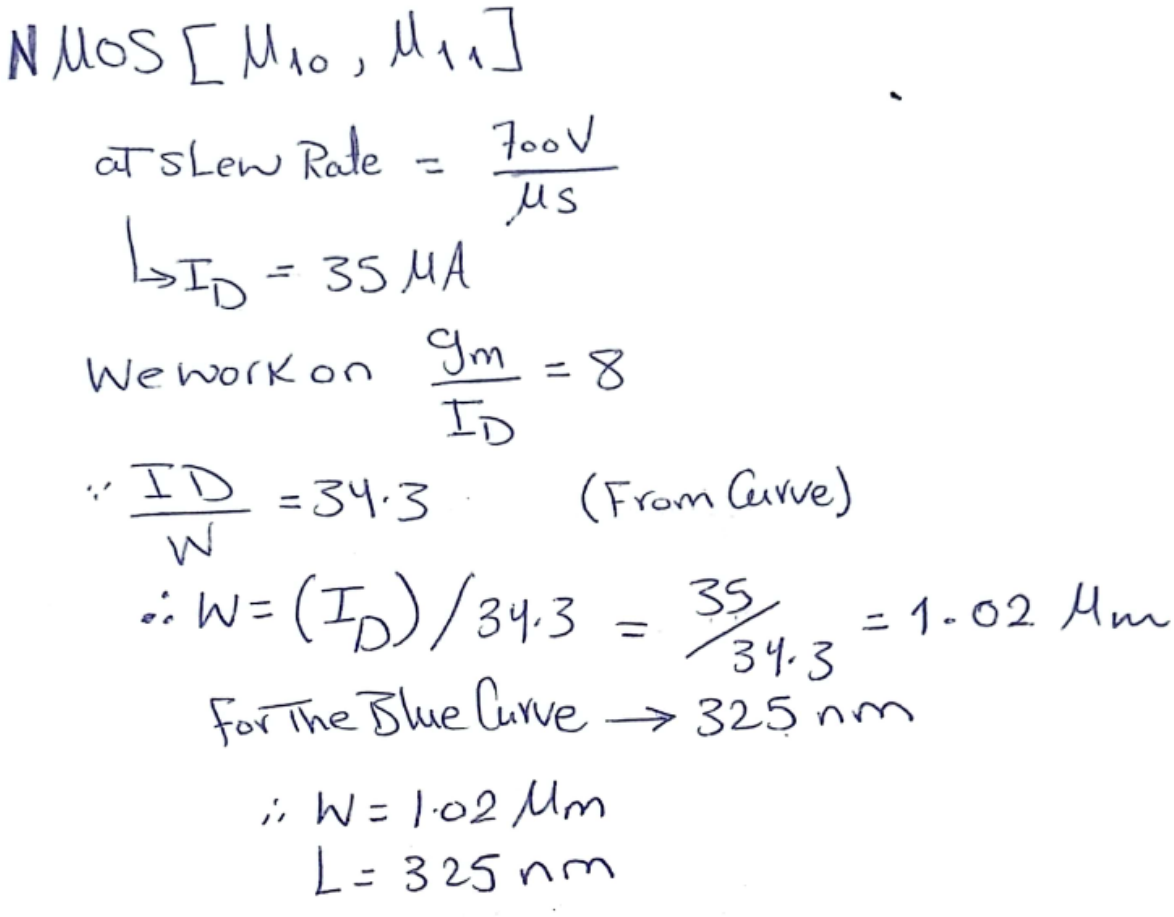


Fig (7). Hand Analysis

The remaining transistors dimensions is manipulated to reach the desired gain and to get all the transistors in the saturation region.

- The length of all the transistors is set to be 325 nm.
- M6 width is the same as M2 and M3 equals 9um.
- M7 width is made to be 5 times the width of M6 to be 45 ums, this will lead to $I_d$ of nearly five times in M7 than M6.
- M12 is made to be 11 um width to reach the gain and the saturation.
- C1 equals 0.2 pF

- C0 equals 0.5*C1 = 0.1pF.
- R0 equals 1K ohms.

Figure 8 shows the whole schematic and the regions check.

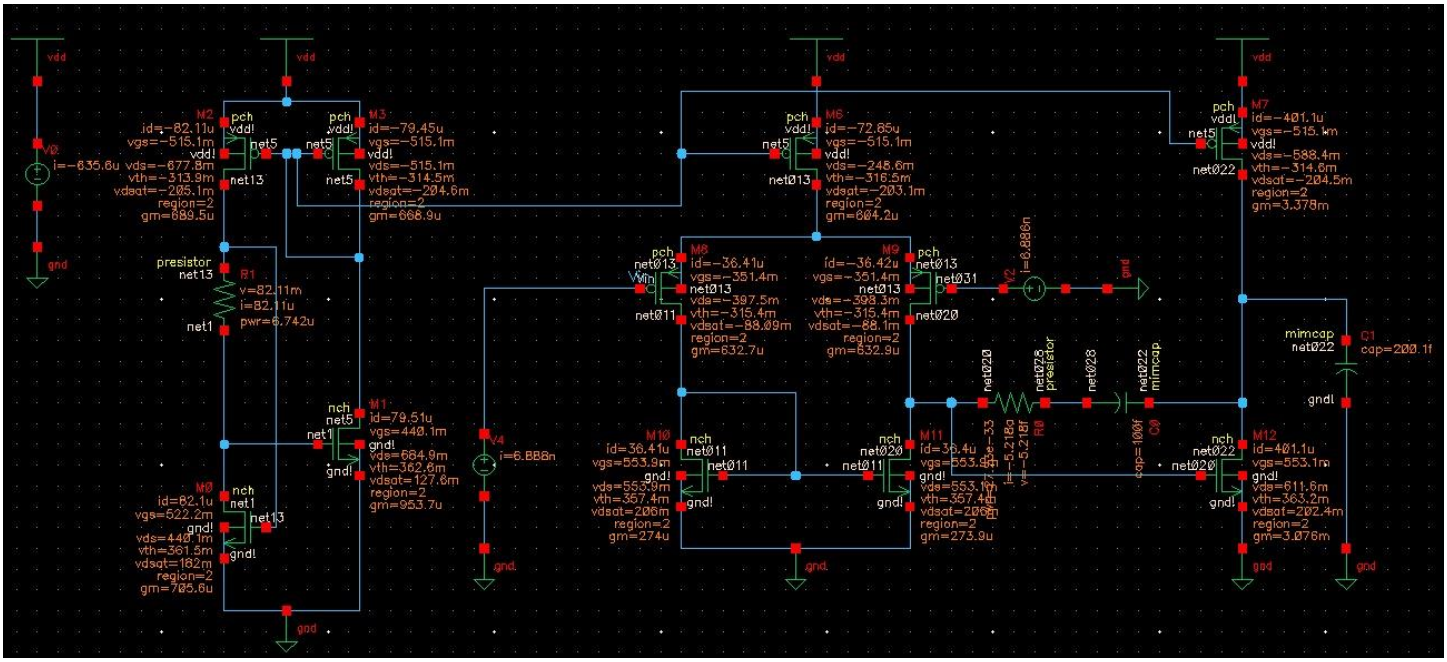

Fig (8). Final schematic

## Checking parameters:

### Gain:

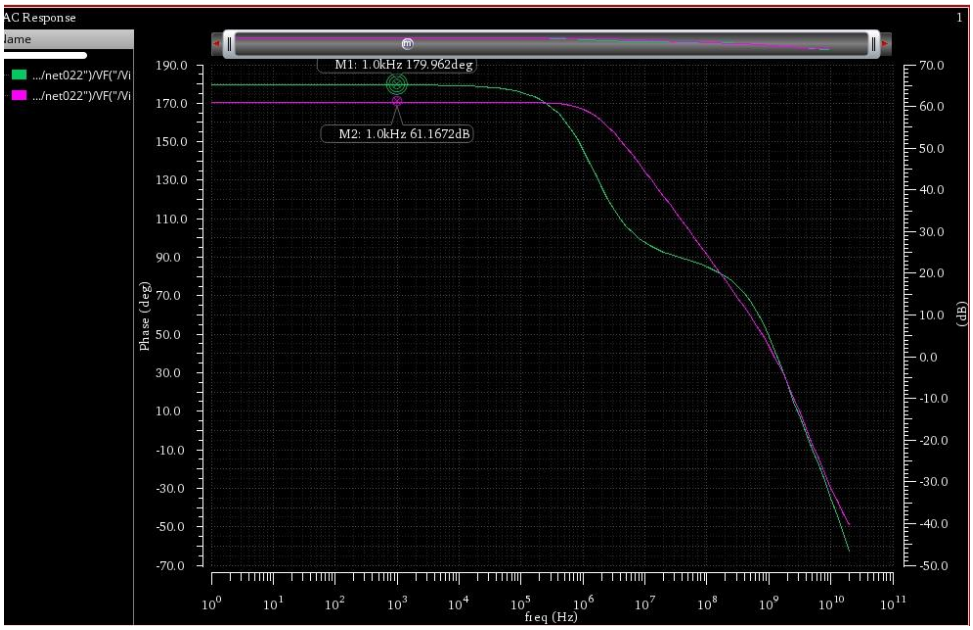


Fig (9). Gain

**Table 2 shows the results of the other parameters extracted from the designed circuit.**

| | Name/Signal/Expr | Value |
|---|---|---|
| 1 | Phase margin | 180 |
| 2 | Gain | 61.17 |
| 3 | band width | 1.26G |
| 4 | output common mode | 563.8m |
| 5 | slew rate | 5.259M |
| 6 | swing | 799.1m |

Table (2). Parameters check

Now all the required parameters are checked and the schematic is ready for the layout.

## LAYOUT

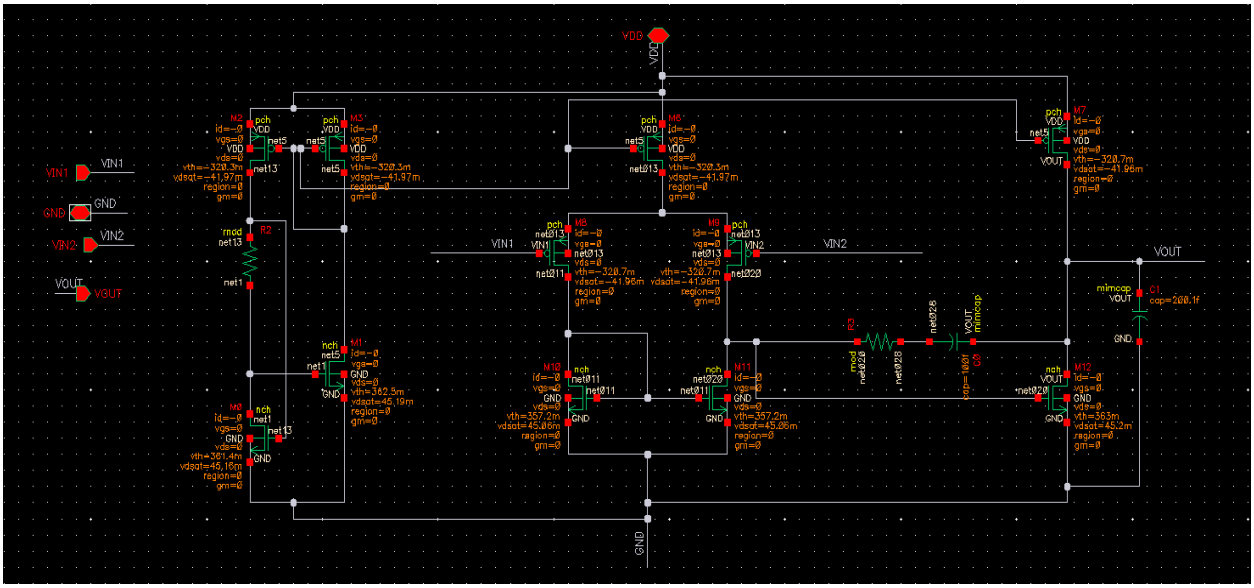


Fig (10). preparation for layout

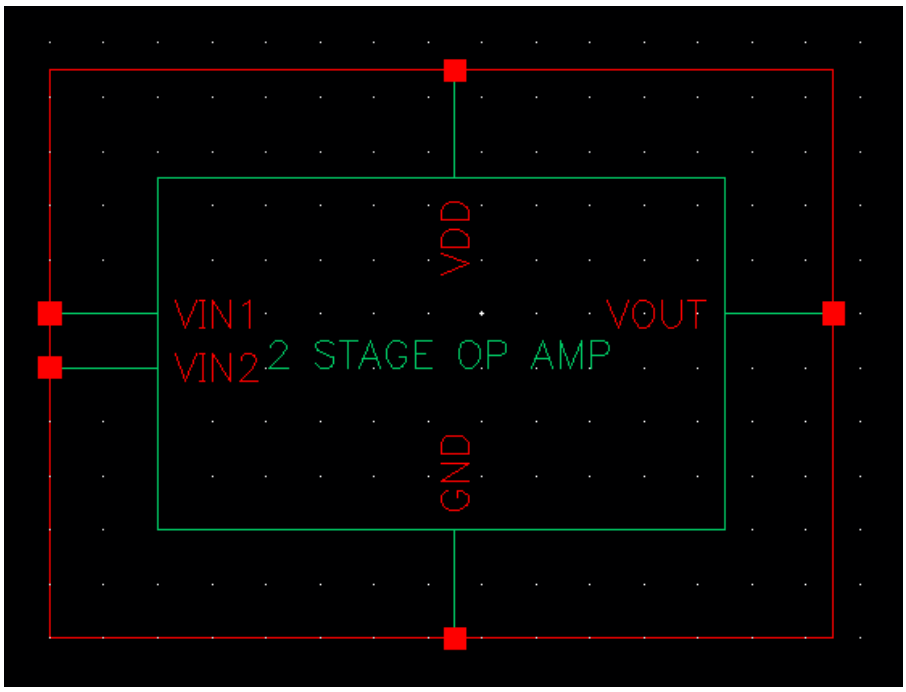


Fig (11). Symbol of two stage op amp

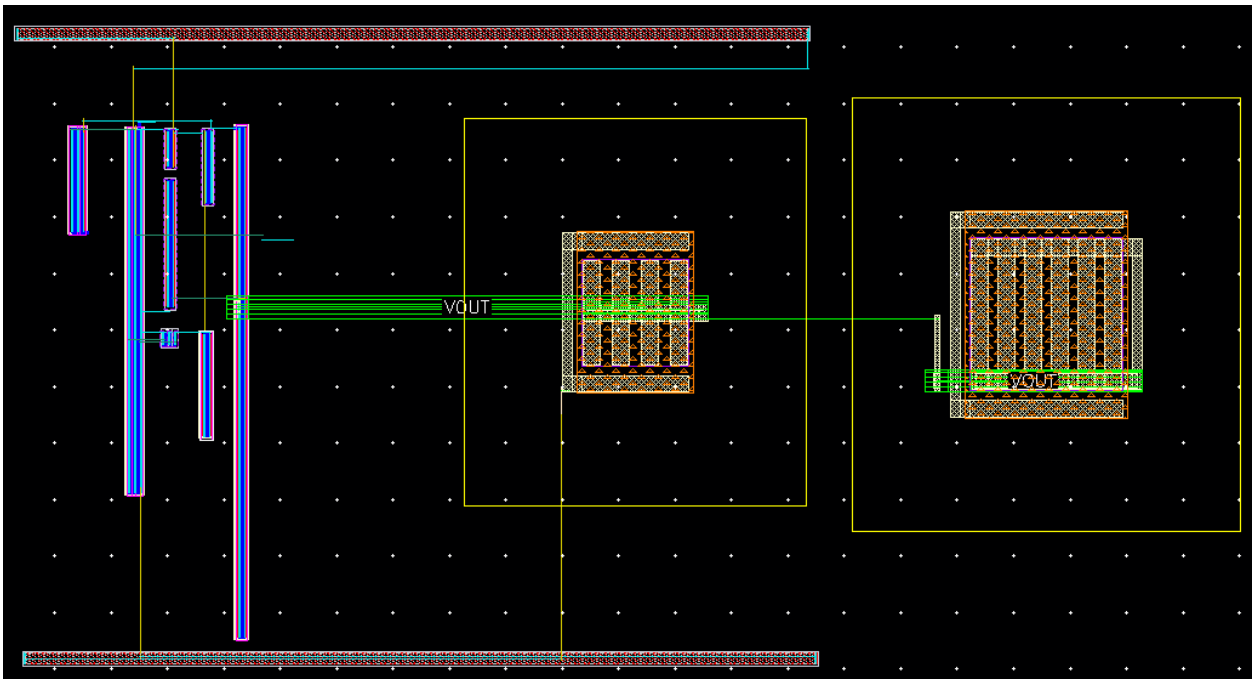


Fig (12). Layout

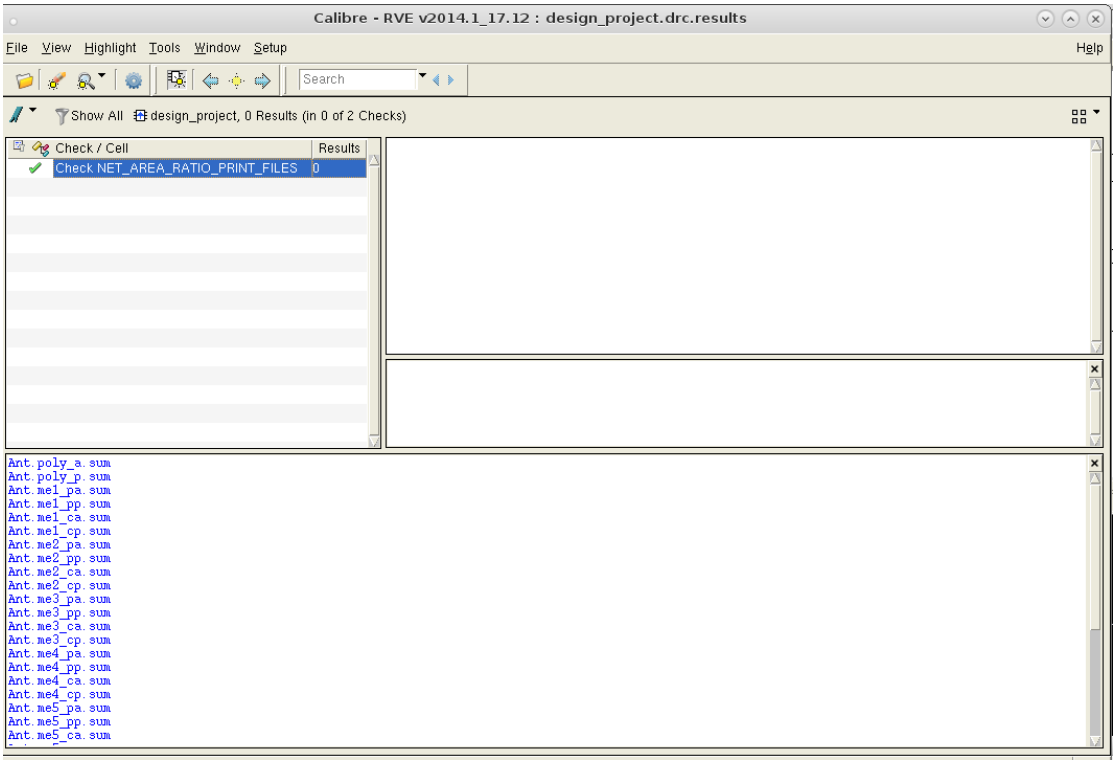


Fig (13). DRC check

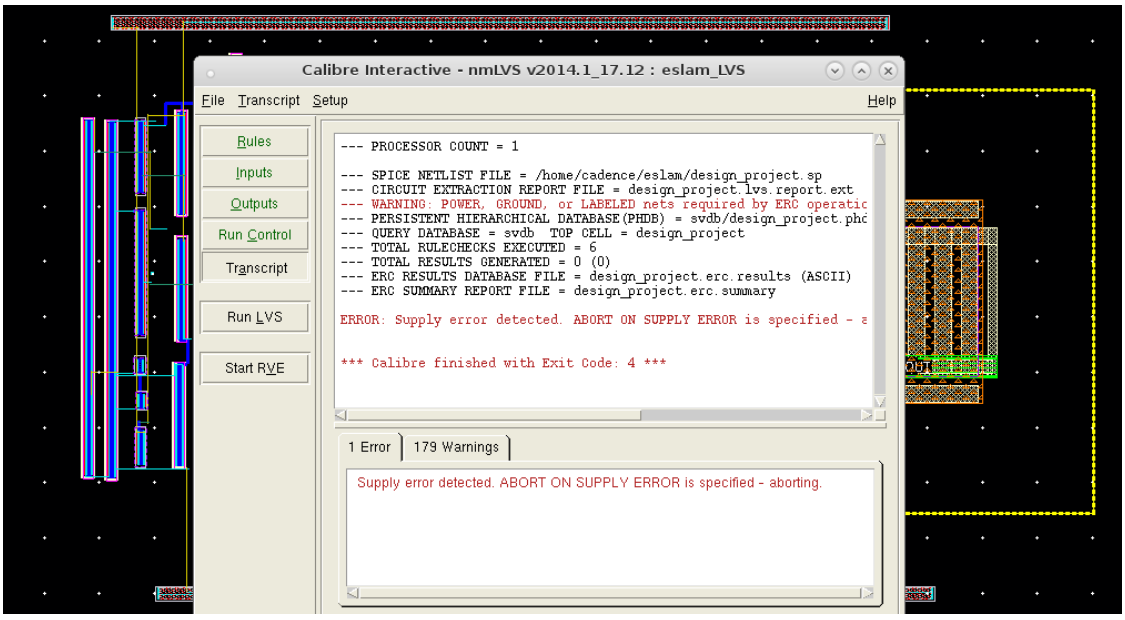


Fig (14). LVS check

**Comment:**

- There is an error in operating the LVS test due to problems in the connections with the GND and VDD and the DRC test passed.
- The resistance used in the layout is Rnod with the same values from TSMC65 library to appear in the layout not like the poly resistance used while we were doing the schematic.