

Computer Architecture  
Lab 3

You are required to build the following:

- A register file which contains 4 registers, each register has 16-bits widths. The register file has 1-read address and 1- write address. It also has 1- read ports and 1-write port. It also has a write enable and a reset signal. (What is the size of address bus? What is the size of data bus?)
- Use the given registers (DFF) to create the register files.
- Create testbench to do the following:
  - Reset all registers, set all read addresses to zero
  - Write in Reg(0) 0xF00F
  - Write in Reg(1) 0x1001
  - Read Reg(1) and **write 0x0003 Reg(0)**
  - Read Reg(2) and Don't write anything
  - Read Reg(0) and **Write in Reg(2) 0xA00A**
  - Read Reg(1) and **Write in Reg(3) 0xB000B**
  - Read Reg(2) and don't write anything

**Assignment:**

- Create the same register file using memory arrays instead of DFFs.
- Test your new register file using the same testbench.
- Use Quartus to generate RTL view for both designs to compare between them.

CYCLE#	Read Port 0
1	0
2	F00F
3	F00F

<b>4</b>	<b>1001</b>
<b>5</b>	<b>0000</b>
<b>6</b>	<b>0003</b>
<b>7</b>	<b>1001</b>
<b>8</b>	<b>A00A</b>