Cairo University

CMPN 301

Computer Architecture

Faculty of Engineering
CHS

Project Phase-I

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Instruction Format

- **Instruction Bit Details**

31 - 26	25	24 - 22	21 - 19	18 - 16	15 - 0
6 bits	1 bit	3 bits	3 bits	3 bits	3 bits
Op code	Immediate value check	Rsc1	Rsc2	Rd	Immediate value

- **Instructions Opcode**

Instructions	OpCode
BRANCHING (000)	
JZ	000
JC	001
Always Taken (Different Bit)	
JUMP	010
CARRY OPERATIONS (001)	
SETC	000
CLRC	001
MOV (010)	
MOV	000
LDM	001

ALU OPERATIONS (011)	
0:2	
NOT	000
INC	001
DEC	010
3:4	
AND	011
OR	100
5:7	
SUB	101
ADD	110
IADD	111
NO-OP (100)	
NOP	000
IN	001
OUT	010
DATA MEMORY (101)	
LDD	000
STD	001
STACK MEMORY (110)	
POP	000
PUSH	001
ROUTINE (111)	
CALL	000
RETURN	100
RTI	111
Forced NOP	001

- **Control Signal Tables**

Control Signals			
INSTRUCTIONS		WRITE BACK	
		current RET/RTI	Freeze Fetch
BRANCHING (000)		0	0
carry operations (001)		0	0
mov (010)		0	0
Alu Operations (011)		0	0
NOP (100)		0	0
Data Memory (101)		0	0
Stack Memory (110)		0	0
ROUTINE (111)			
CALL	000	0	0
RETURN	100	1	1
RTI	111	1	1

Control Signal						
INSTRUCTIONS	EXECUTION					
	ALU ENABLE	IMM/ SRC SELECTOR	Branching Operation	PART SELECTOR (2 BITS)	OP SELECTOR (3 BITS)	Call Operation
Categories						
NP-OP (100)	0	x	0	x	x	0
DATA MEMORY (101)	0	x	0	x	x	0
STACK MEMORY (110)	0	x	0	x	x	0
ROUTINE (111)						
CALL	0	x	0	x	x	1
RETURN	0	x	0	x	x	0
RTI	0	x	0	x	x	0
BRANCHING (000)						
JZ	1	x	1	00	000	0
JC	1	x	1	00	001	0
JUMP	1	x	1	00	010	0
CARRY OPERATIONS (001)						
SETC	1	x	0	01	000	0
CLRC	1	x	0	01	001	0
MOV (010)						
MOV	1	x	0	10	000	0
LDM	1	1	0	10	001	0
ALU (011)						
NOT	1	x	0	11	000	0
INC	1	x	0	11	001	0
DEC	1	x	0	11	010	0
AND	1	0	0	11	011	0
OR	1	0	0	11	100	0
SUB	1	0	0	11	101	0
ADD	1	0	0	11	110	0
IADD	1	1	0	11	111	0

Control Signal								
INSTRUCTIONS	MEMORY							
	Read Address Selector	Write Address Selector	Data Written Selector	MEM OP	MEM READ	MEM WRITE	Data Bus Selector	propagated RET/RTI
NP-OP (100)	x	x	x	0	x	x	x	0
Branching (000)	x	x	x	0	x	x	x	0
Carry (001)	x	x	x	0	x	x	x	0
Mov (010)	x	x	x	0	x	x	x	0
ALU (011)	x	x	x	0	x	x	x	0
DATA MEMORY (101)								
LDD (000)	0	x	x	1	1	0	0	0
STD (001)	x	0	1	1	0	1	0	0
STACK MEMORY (110)								
POP (000)	1	x	x	1	1	0	0	0
PUSH (001)	x	1	1	1	0	1	0	0
ROUTINE (111)								
CALL (000)	x	1	0	1	0	1	0	0
RETURN (100)	1	x	x	1	1	0	0	1
RTI (111)	1	x	x	1	1	0	1	1

Control Signals						
INSTRUCTIONS		WRITE BACK				
		REG FILE ENABLE	FLAG ENABLE	DATA SELECTOR	FLAG SELECTOR	IN DATA SELECTOR
BRANCHING (000)						
JZ	000	0	1	x	0	x
JC	001	0	1	x	0	x
JUMP	010	0	0	x	x	x
CARRY OPERATIONS (001)						
SETC	000	0	1	x	0	x
CLRC	001	0	1	x	0	x
MOV (010)						
MOV	000	1	0	0	x	0
LDM	001	1	0	0	x	0
ALU OPERATIONS (011)						
NOT	000	1	1	0	0	0
INC	001	1	1	0	0	0
DEC	010	1	1	0	0	0
AND	011	1	1	0	0	0
OR	100	1	1	0	0	0
SUB	101	1	1	0	0	0
ADD	110	1	1	0	0	0
IADD	111	1	1	0	0	0
NO-OP (100)						
NOP	000	0	0	x	x	x
IN	001	1	0	x	x	1
OUT	010	0	0	x	x	x
DATA MEMORY (101)						
LDD	000	1	0	1	x	0
STD	001	0	0	x	x	x
STACK MEMORY (110)						
POP	000	1	0	1	x	0
PUSH	001	0	0	x	x	x
ROUTINE (111)						
CALL	000	0	0	x	x	x
RETURN	100	0	0	x	x	x
RTI	111	0	1	x	1	x

Design

https://drive.google.com/file/d/18ZOQ17pb-gTuv2SYxonlB-z9uLjafBDG/view

Please Find the design.drawio in the submitted Folder

Pipeline Registers

	Size / Inputs
IF/ID	16 bits PC 32 bit Instruction
ID/EX	9 bits Execution 8 bits Memory 5 bits Wb 16 bits PC 16 bits RD data 16 bits RS1 data 16 bits RS2 data 16 bits Immediate value 3 bits flags 3 bits Rd address
EX/MEM1	8 bits Memory 5 bits Wb 16 bits PC 16 bits RS1 data 16 bits RS2 data 16 bits Alu result 3 bits flags 3 bits Rd address

MEM1/MEM2	8 bits Memory 5 bits Wb 16 bit Alu result 16 bit data to be written 16 bit write address 16 bit read address 3 bits flags 3 bits Rd address
MEM2/WB	5 bits Wb 16 bit memory data read 3 bits flags read 16 bit Alu result 3 bits flags 3 bits Rd address

Hazards

- **Structural Hazard**
  Between Mem1 / Mem2
  Sol : Hazard Detection Unit .

- **Data Hazard**
  Operands & Flags Dependencies
  Sol : 2 Forwarding Units 1 for data and the other for flags (between ID/EX , EX/MEM1 , MEM1/MEM2).

- **Control Hazard**
  Interrupt , Branching and Call operations
  Sol : Static Prediction always not taken.