

INSTRUMENTATION ELECTRONICS FOR AN INTEGRATED  
ELECTROPHYSIOLOGY DATA ACQUISITION  
AND STIMULATION SYSTEM

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The Neurobiology Engineering Laboratory at Western Michigan University has need of an electrophysiology instrumentation system combining generation of multiple arbitrary stimulation waveforms and recording of action potentials on multiple channels. Electronics for an instrumentation system with the capability of generating four unique stimulation waveforms and recording action potentials on eight channels were developed and implemented on a printed circuit board. Collaboration with fellow graduate student, Mr. Kyle Batzer, who developed firmware and software for the instrumentation system as described in his thesis, was essential for successful realization of the instrumentation system. Knowledge gained and reported by previous students working in the Neurobiology Engineering laboratory also contributed to the development. This system was used to perform a standard electrophysiology experiment on earthworm giant axon action potentials using only instrumentation electronics and software developed by students at Western Michigan University.

INSTRUMENTATION ELECTRONICS FOR AN INTEGRATED  
ELECTROPHYSIOLOGY DATA ACQUISITION  
AND STIMULATION SYSTEM

by

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## Foreword

This thesis and the companion Master of Science in Computer Engineering thesis by Mr. Kyle Batzer describes a complete hardware and software instrumentation system for conducting electrophysiology experiments. The developed system features multiple channels that can be used for measurement and stimulation of biological electrical activity. These theses represent the culmination of many previous projects in the Western Michigan University Neurobiology Engineering Laboratory. This foreword provides a brief history of those previous projects to provide context for these two theses.

The original motivation for this line of research was the availability of microelectrode arrays (MEAs) from companies such as Multi Channel Systems ([www.multichannelsystems.com](http://www.multichannelsystems.com)). MEAs are essentially culture dishes with an array of implanted electrodes that enable monitoring and stimulation of neuron and neuronal network electrical activity. Reference [1] provides an excellent overview of studying learning in neuronal networks using MEAs. I was first introduced to MEAs via an article provided by Dr. John Gesink, Emeritus Chair of the WMU Department of Electrical Engineering. My first steps into this area included submission of an unfunded grant *From Artificial to Naturally Intelligent Systems: Computing with Neuron Cell Cultures* and auditing Dr. John Jellies' outstanding Advanced Neurobiology course in the Spring 2006 semester.

After discussions with Dr. Frank Severance, we decided to start a new laboratory to conduct research using MEAs, and I subsequently visited with Mr. Alex Cadotte at Dr. Thomas DeMarse's lab at the University of Florida to learn more about these devices, including efforts to use neuronal networks as an intelligent closed loop controller [2, 3]. A WMU Faculty Research and Creative Activities Support Fund grant, myself, Dr. Gesink, Dr. Severance, and the WMU Department of Electrical and Computer Engineering provided funds for cell culture equipment and supplies and instrumentation components. The WMU College of Engineering and Applied Sciences configured a laboratory for cell culture work and the Neurobiology Engineering Laboratory was born. Graduate student Mr. Michael Ellinger led the challenging effort to successfully culture the first cells in the lab in Summer 2008 [14]. Estab-

lishing a cell culturing capability relied on help from many people, most notably Biological Sciences graduate student Sr. John-Mary Vianney and her advisor Dr. John Spitsbergen.

In 2007, two senior design groups [4, 5] developed an initial design for the instrumentation system based on the research literature (including the key references [6, 7]) and a commercial system from Multi Channel Systems. In particular, [6] identified challenges and solutions with recording and stimulating using the same electrode. A third senior design group [8] continued this effort, breadboarding a single analog input channel and an associated digital control circuit. Mr. John Stahl conducted research on the noise characteristics of the analog input channel, building a complete analog/digital two channel prototype [9]. Mr. Stahl then designed a printed circuit board implementation for two analog input channels. A fourth senior design group [10] made significant progress on both the instrumentation system hardware and software, including development of a printed circuit board implementation of two analog input channels with the associated digital control circuit. A fifth senior design group [11] worked on this system with a focus of using an FPGA based solution for data acquisition and control via a computer.

Mr. Squires, working with Mr. Stahl, built on these previous accomplishments to produce the instrumentation design presented in this thesis. His design features a modular system consisting of a “mother board” into which up to eight analog input channel cards (designed by Mr. Stahl) can be inserted. Mr. Batzer, leveraging his previous work as a member of the fourth senior design group, completed the design of an FPGA based solution for data acquisition and control of the instrumentation system via a computer, including a scripting language, as his thesis. A key laboratory accomplishment was using the developed instrumentation system to conduct a standard experiment that measures earthworm giant axon nerve impulses [9, 12, 13, 14] as described in this thesis.

I thank the many students that have worked in the lab over the years. I also thank my colleagues for their unselfish help in these projects, and in particular Dr. Frank Severance, who co-directs the lab, and Drs. Bazuin and Gesink. Finally, I thank the WMU College of Engineering and Applied Sciences, the Department of Electrical and Computer Engineering, the Lee Honors College, the Office of the Vice President for Research, and the NASA

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# 1 Introduction<sup>1</sup>

An Integrated Electrophysiology Data Acquisition and Stimulation System to support electrophysiology research has been developed by building on previous work at WMU [4, 8, 9, 10, 14], studying commercial systems [16], and reviewing the research literature [3, 6, 17]. The developed prototype provides a real-time platform for measurement and stimulation of biological electrical activity and a PC application for controlling the real-time platform and visualizing cellular activity. The system can accommodate up to eight measurement channels and four stimulation channels, and the design can be expanded for up to 64 channels to support future research at the Western Michigan University (WMU) Neurobiology Engineering Laboratory.

The developed prototype is viable for a wide array of electrophysiology experiments, completely fulfilling the instrumentation needs of [12, 13, 18] and partially fulfilling the requirements for [1, 2, 3]. In particular, a standard electrophysiology experiment was performed on earthworm giant axon action potentials to validate system functionality. The prototype is also intended for studying software and hardware principles required for performing research using cells cultured on a Microelectrode Array (MEA), e.g. [16]. A cell culture protocol has been developed [14] and previous work on such a system [4, 8, 10], including low noise amplification, has been completed [9]. Initial analytical algorithms have also been developed [14].

# 2 Specifications<sup>1</sup>

The Data Acquisition and Stimulation System (DASS) is expected to provide the following functionality:

1. Provide a platform for performing electrophysiology experiments with earthworms as described in [12, 13]
  - (a) Produce a voltage-controlled square wave stimulation pulse with widths from

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<sup>1</sup>This section is co-authored with Kyle Batzer, [15].

0.01ms to 100ms and amplitudes from 0.1V to 10V

- (b) Produce single stimulation pulses or multiple pulses at rates from 1Hz to 10Hz
  - (c) Provide at least one differential recording channel
  - (d) Record an action potential voltage from the time of a stimulation pulse for a minimum duration of 20ms
  - (e) Plot the recorded voltage
  - (f) Store the recorded voltage to a non-proprietary, standard file format
2. Provide a platform for stimulation and recording of neuron cell culture electrical activity via MEA electrodes
- (a) Provide at least four recording channels
  - (b) Store data from recording channels continuously
  - (c) Provide at least four voltage-controlled arbitrary stimulation channels
  - (d) Output single-ended stimulation signals on recording electrodes and add culture voltage offset to the stimulation signal
  - (e) Provide an interface that can specify stimulation waveforms, locations, and intervals that can be updated based on data from the recording electrodes
3. Utilize Low-Noise Amplifier described in [9]
- (a) Connect to each Low-Noise Amplifier channel with a PCI-Express card edge connector
  - (b) Provide  $\pm 7\text{ V}$  to  $\pm 15\text{ V}$  analog voltage supplies and ground via the card edge connector
  - (c) Provide ability to independently switch four digital inputs for each channel,  $0_{IH} = 0.8\text{ V}$  and  $1_{IL} = 2.4\text{ V}$
  - (d) Route differential analog input to the card edge connector for each channel
  - (e) Convert the 20Hz to 14.6kHz analog output signal [9] to digital samples

- (f) Route a single-ended stimulation signal to each channel
4. Additional requirements
    - (a) Employ proven, effective circuit design and layout best practices

### 3 Terminology

**Analog to Digital Converter (ADC)** A device for converting an analog voltage to a digital code. The ADC on the Electrophysiology Interface is an Analog Devices AD7606.

**Complex Programmable Logic Device (CPLD)** Non-volatile programmable logic device that is used to allow limited outputs from the FPGA to control many more digital input lines required by multiple Preamp boards connected to the Electrophysiology Interface. The CPLD on the Electrophysiology Interface may be a Xilinx® XC9536XL or a XC9572XL (the devices are pin compatible).

**Data Acquisition and Stimulation System (DASS)<sup>2</sup>** System intended for electrophysiology experiments described in this thesis and corresponding thesis [15]. The DASS includes all hardware, software, and firmware.

**Data Acquisition and Simulation Control Center (DASCC)<sup>2</sup>** PC application, described in [15], for controlling and transferring data to and from the RTSC.

**Differential Output Amplifier** A custom designed operational amplifier configuration on the Electrophysiology Interface that provides gain and offset to an input from the DAC and provides two output signals where one signal is the inverse of the other signal, with respect to ground (0V).

**Digital to Analog Converter (DAC)** A device for converting a digital code to an analog voltage. The DAC on the Electrophysiology Interface is an Analog Devices AD5678.

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<sup>2</sup>This item is co-authored with Kyle Batzer, [15].

**Electrophysiology Interface**<sup>3</sup> Subsystem that provides the RTSC with an interface to biological systems. It consists of a custom PCB described in this thesis.

**Field Programmable Gate Array (FPGA)** Volatile programmable logic device that performs the majority of the real time control functions on the RTSC. The FPGA on the RTSC is a Xilinx® Spartan-3 XC3S500E.

**Real Time System Controller (RTSC)**<sup>3</sup> Subsystem that implements the real-time functions of the system. It consists of a Digilent® Nexys™ 2 development board [19, 20], with custom firmware described in [15].

**Preamp**<sup>3</sup> Low noise instrumentation amplifier with stimulation dc bias addition for MEA experiments. Designed by Mr. John Stahl as described in [9].

**Printed Circuit Board (PCB)** A fiberglass board with thin layers of copper that are etched and drilled allowing electronic components to be mounted and connected in a compact, professional-looking package for an electronic circuit.

## 4 Data Acquisition and Stimulation System Hardware

A digital platform that interfaces with analog signals is an effective and flexible instrumentation strategy for electrophysiology experiments that require arbitrary stimulation signals and recording action potentials. A digital to analog converter (DAC) can convert a digitally represented waveform to an analog signal that can be used to stimulate experimental subjects, and a analog to digital converter (ADC) can convert analog voltages to digital data that can be saved in readily available digital formats.

The user interface of the platform needs to be flexible to accommodate the various electrophysiology experiments it will perform. Custom PC software allows the user to control the complex capabilities of the platform while also providing access to data storage space; however, PC hardware is not capable of interfacing directly with DAC and ADC circuits.

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<sup>3</sup>This item is co-authored with Kyle Batzer, [15].

To save development complexity, real time control of the DAC and ADC is accomplished with a Digilent® Nexys™ 2 field-programmable gate array (FPGA) development board. The DAC and ADC, along with related circuitry, are implemented on a custom designed printed circuit board (PCB).

An overview of the Data Acquisition and Stimulation System (DASS) is shown in Figure 1. Custom user interface software on the PC communicates to the Digilent® Nexys™ 2 Real Time System Controller (RTSC) board over USB and serial RS232 interfaces. An RS232 level converter chip converts the PC's RS232 logic levels to FPGA compatible TTL logic levels and vice-versa. A microcontroller on the RTSC provides the USB physical layer (PHY) and is capable of controlling the Joint Test Action Group (JTAG) bus to load a FPGA configuration file into the FPGA or save the configuration to a flash memory device capable of storing the configuration on the board without power and loading the configuration into the FPGA upon power-up. The JTAG bus also allows a configuration to be loaded into the Complex Programmable Logic Device (CPLD), which can be programmed with logic to allow the FPGA to control the multiple digital inputs on the Preamp boards with fewer output pins. A DRAM chip on the RTSC stores stimulation waveform data. The FPGA outputs stimulation waveform data to the DAC on the Electrophysiology Interface board and controls the ADC. Data from the ADC is sent to the microcontroller, which has customized firmware that transfers data to the PC over the USB interface.

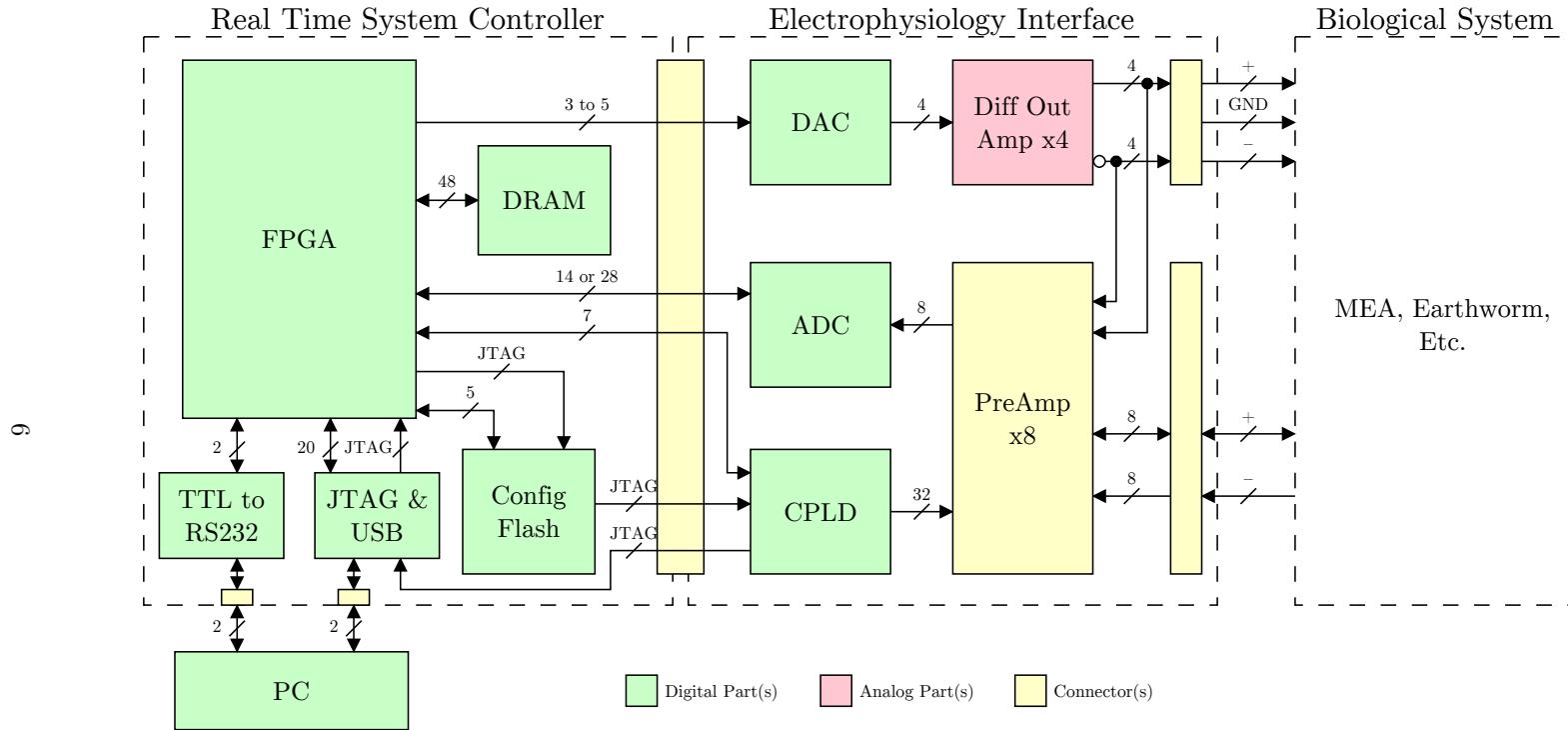


Figure 1: The Data Acquisition and Stimulation System consists of a PC, the Real Time System Controller Board, which is a Digilent® Nexys™ 2 FPGA development board [19, 20], and the Electrophysiology Interface board, which is based on previous work as described in the text.

The analog operating ranges of the DAC and ADC are not compatible with the voltages used in electrophysiology experiments, so a differential output amplifier circuit conditions the DAC output, and connectors are provided to allow previously developed low-noise amplifier boards [9] (Preamp) to condition low-voltage action potentials for input into the ADC. The Preamp boards have the capability of outputting a provided analog stimulation signal on the recording electrode; digital inputs control whether the Preamp is in stimulation or recording mode.

Typical use of the DASS involves the following: connecting the Electrophysiology Interface board stimulation and data acquisition channels to the biological portion of the electrophysiology experimental setup; powering the Electrophysiology Interface and RTSC boards, which causes the FPGA to be configured based on the data in the flash memory configuration chip; using the PC application to send commands over the RS232 interface to the FPGA for configuring the stimulation and data acquisition channels [15]; running a script on the PC application that sends commands to the FPGA over the RS232 interface to load stimulation waveform profiles in the DRAM, sets the Preamp boards to stimulation or recording mode, causes the DAC to output the stimulation waveform, collects data from the ADC, and transfers data collected from the ADC to the PC for storage and analysis [15]. Waveforms from the DAC output are amplified and conditioned by the Differential Output Amplifier before being routed to the biological system either to independent stimulation electrodes or through the Preamp boards to the recording electrodes. The response from the biological system is observed on the recording electrodes as analog electrical signals which are routed to the Preamp boards for amplification and filtering before being routed to the ADC for conversion to digital information.

This thesis describes the relevant circuitry on a Digilent® Nexys<sup>TM</sup> 2 FPGA development board that is necessary to implement a RTSC board, and it describes the design of the Electrophysiology Interface board. The design of the PC software, microcontroller firmware, and programmable logic configurations is described in [15].

## 4.1 Power Supply

The hardware for the Data Acquisition and Stimulation System requires several supply voltages to power the digital integrated circuits (ICs) in addition to dual analog power supplies for amplification circuitry. Consequently, there are several options for providing power to the Real Time System Controller Board and Electrophysiology Interface board. Figure 2 summarizes the power needs of the ICs and circuit blocks along with the power input connectors and voltage regulators.

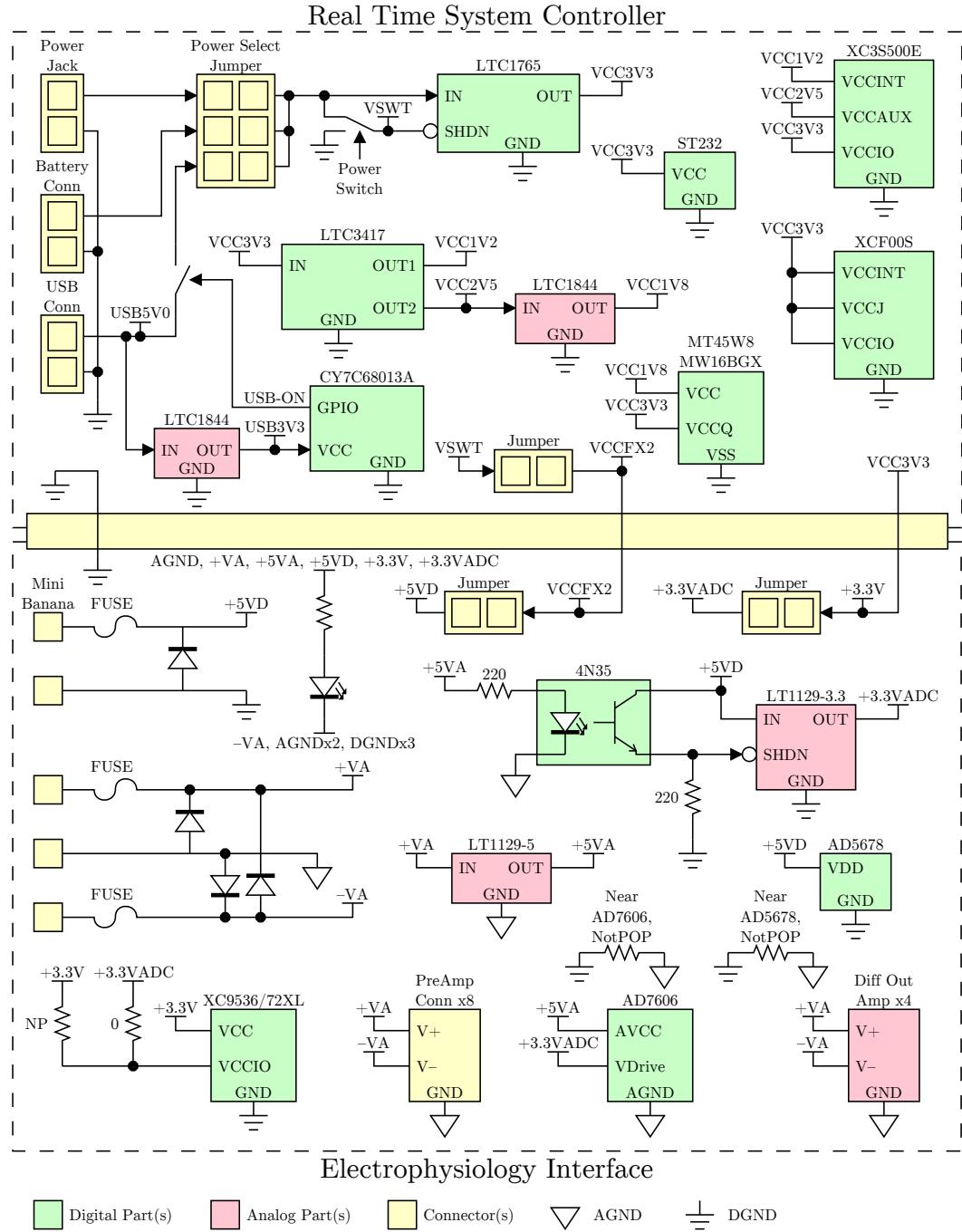


Figure 2: Power connectors and IC power connections on the Real Time System Controller Board [19, 20] and the Electrophysiology Interface board

#### 4.1.1 Real Time System Controller Power

The RTSC has selectable input power options configured by placing a jumper connecting the desired power connector to a LTC1765 switching voltage regulator. The power jack and battery connector both connect directly to the regulator, but the CY7C68013A Cypress microcontroller, which requires a +3.3 V supply and acts as the USB PHY, draws power exclusively from the USB interface, so a LTC1844 linear regulator is included to regulate the +5.0 V USB input voltage to the required value. When a USB cable is connected to the RTSC and a PC, the Cypress microcontroller informs the PC that more than 100 mA of current will be drawn over the USB interface; then, the USB-ON signal switches a NMOS transistor, connecting USB power, which can supply up to 500 mA of current, to the power selection jumper [19, 20]. The power consumption of the RTSC will vary based on the configuration of the Xilinx® XC3S500E FPGA, clock speeds of the digital logic, and the power drawn from the Electrophysiology Interface board [19].

The power switch on the RTSC board connects the active low shutdown signal ( $\overline{\text{SHDN}}$ ) of the LTC1765 regulator to either the power selection jumper (to enable the regulator output) or to ground (to disable the regulator output) [21]. Setting the power switch to the off position does not disconnect USB power from the Cypress microcontroller but does disconnect the main power jumper from VCCFX2 if the jumper is in place to connect the VSWT to VCCFX2 [20].

Most of the circuits on the RTSC board are powered by the VCC3V3 supply, which is why a LTC1765 high-efficiency switching regulator is used for the supply. The ST232 RS232 level shifting IC and the Xilinx® Platform Flash XCF00S configuration flash memory require only 3.3V [22, 23]. The Xilinx® Spartan 3E XC3S500E FPGA requires a significant amount of current at +1.2V for its internal core, VCCINT, and requires +2.5 V for its auxiliary supply voltage, VCCAUX, so a LTC3417 high-efficiency dual-output switching regulator provides the needed supply voltages [19, 24]. Also, the MT45W8MW16BGX 128Mb DRAM module alone requires a 1.8 V core voltage, with a maximum current of 25 mA at 66 MHz and 45 mA at 133 MHz, along with an IO voltage supply equal to the FPGA IO voltage [25]. Thus, a LTC1844 linear regulator is provided for the specialized VCC1V8 voltage supply, and

since linear regulator efficiency is directly proportional to the magnitude of the voltage drop across the regulator, it is powered by the voltage supply that will require the least voltage drop, VCC2V5 [20].

#### 4.1.2 Electrophysiology Interface Power

To isolate analog devices from the noise generated by digital devices, it is preferable to have separate power supplies and ground for the digital and analog devices on the Electrophysiology Interface board. In addition, the Preamp boards connected also draw power from the analog voltage supplies on the Electrophysiology Interface board.

The integrated circuits requiring a digital voltage supply are the Analog Devices AD5678 DAC, the Xilinx® XC9536/72XL CPLD, and the logic supply, VDrive, of the AD7606 ADC. The nine LT1124 dual op-amp ICs of the differential output amplifier blocks require dual analog voltage supplies, and each Preamp requires dual analog voltage supplies for its LT1167 instrumentation amplifier, LT1124 dual op-amp, LT1125 quad op-amp, and ADG202 analog switch ICs. Complicating the analog voltage supply requirements is the Analog Devices AD7606 ADC, which requires a  $+5.0\text{V} \pm 0.25\text{V}$  analog voltage supply, AVCC [26].

Five 2mm banana (also known as mini-banana) connectors are provided on the Electrophysiology Interface board to connect analog voltage ( $\pm\text{VA}$ ) and ground (AGND) and digital voltage ( $+5\text{VD}$ ) and ground (DGND). The magnitude of  $+\text{VA}$  should be a close as possible to the magnitude of  $-\text{VA}$ . Table 1 shows the acceptable voltage range of the power supply inputs. The minimum and maximum values of  $+5\text{VD}$  are determined by the AD5678 requirements, but it should be noted that the maximum DAC output voltage will be equal to the supply voltage [27]. The minimum value for the  $\pm\text{VA}$  supply is determined by the dropout voltage of the LT1129-5 regulator (0.45 V at 100 mA load current [28]), and the maximum value for the  $\pm\text{VA}$  supply is limited by the requirements of the LT1167 instrumentation amplifier and ADG202 analog switches on the Preamp boards [29, 30].

Fuses and protection diodes will protect the circuits on the Electrophysiology Interface board if the supply leads are reversed. If the supply leads are reversed, one or more of

Supply	TYP (V)	MIN (V)	MAX (V)
+5VD	5.0	4.5	5.5
± VA	9.0	5.5	15.0

Table 1: Electrophysiology Interface power supply voltages

the protection diodes will be forward biased, allowing a large amount of current to flow between the reversed supply leads causing a fuse to blow and the dangerous voltage to be disconnected from the rest of the board. The fuses on the Electrophysiology Interface board are surface mount fuses in 0805 packages that have the advantage of taking up very little board space but have the disadvantage of having a high series resistance of  $0.7\Omega$  (measured). When one of the fuses blows, it is not visually distinguishable from a non-blown fuse. To ensure a low resistance connection, the ground connection does not go through a fuse, which will present a problem if a power lead is connected to a ground connector that creates a large voltage difference between the analog and digital grounds.

The 3.3 V supply from the RTSC board is used to power the core of the CPLD and may be used to power the IO buffers of the CPLD and ADC by connecting the jumper from +3.3 V to +3.3VADC, in which case the LT1129-3.3 should not be populated. Alternatively, the IO buffer of both the ADC and CPLD or the ADC alone may be powered by a LT1129-3.3 linear regulator that converts the +5VD voltage to 3.3 V. To ensure that the IO buffers of the ADC are powered only when the ADC's AVCC is powered and to preserve analog and digital isolation, a 4N35 opto-isolator, with its input driven by the +5VA supply, controls the operation of the linear regulator. Since other signals from the CPLD and DAC violate analog and digital isolation, as discussed in section 4.1.4, the opto-isolator is excessive, but it illustrates the concept of analog and digital isolation.

Both the AD5678 DAC and the AD7606 ADC recommend analog and digital ground and power isolation, but when analog and digital grounds are to be connected at some point, the connection should be as close as possible to the AD5678 as recommended by [27], and the connection should be as close as possible to the AD7606 as recommended by [26]. To accommodate this conflicting information, pads for  $0\Omega$  resistors are provided near the

DAC and ADC for testing analog and digital ground connections. Although, with all of the signals that connect analog and digital powered devices, as discussed in section 4.1.4, a single  $0\Omega$  resistor may not be sufficient for routing signal return currents.

The +5VD supply may be configured to be powered by the main input bus of the RTSC board by connecting the jumper on the RTSC the connects VSWT to VCCFX2 and the jumper on the Electrophysiology Interface board that connects VCCFX2 to +5VD. The reverse should not be practiced: using +5VD to power the RTSC could result in the +5VD power supply being shorted to ground by the power switch that connects VSWT to the main input bus or to ground. If the USB interface is used to power the RTSC and the Electrophysiology Interface boards, care must be taken to ensure that no more than 500 mA is drawn from the USB interface. A typical configuration of the FPGA may cause the RTSC, itself, to draw 300 mA of power from the USB interface [19]. The AD5678 draws only 2.6 mA of quiescent current with its internal voltage reference on, but the AD5678 output amplifiers draw varying amounts of current based on input resistance of the Differential Output Amplifier blocks [27]. The CPLD's power consumption varies depending on its configuration and clock speed. With a configuration consisting entirely of 16-bit counters, a XC9536XL can draw between 15 mA and 65 mA of current from the +3.3 V power supply, and a XC9572XL can draw between 25 mA and 125 mA [31, 32]. The resulting current drawn from the USB interface depends on the power efficiency of the LTC1765, which varies from 75% to 87% depending on output current [21].

LEDs are provided to give a visual indication for each power supply to which they are connected. The LEDs are driven by the power supply rail through a resistor to limit the current through each LED. The magnitude of the resistance is determined based on the desired current in the LED and the forward voltage of the LED. Red surface mount LEDs from Kingbright are used that have a rated forward current of  $I_F = 20\text{ mA}$  with a forward voltage of  $V_{FTyp} = 2.0\text{ V}$  [33]. A forward current of  $I_F = 5\text{ mA}$  is bright enough for an indicator. Using the constant-voltage-drop model of the diode, a resistance values is calculated, using

$$R = \frac{(V_{\text{supply}} - V_F)}{I_F}, \quad (1)$$

to produce the desired forward current based on the power supply voltage,  $V_{\text{supply}}$ , and the typical forward voltage of the diode,  $V_F$ . For example, the power supplies with a nominal voltage of  $V_{\text{supply}} = +5.0 \text{ V}$ , using  $I_F = 5 \text{ mA}$  and  $V_F = V_{FTyp} = 2.0 \text{ V}$  yields a resistance of  $R = 600 \Omega$ . A standard value resistor that is  $560 \Omega$ , which is close to  $600 \Omega$ , is populated on the Electrophysiology Interface board for the LEDs that indicate the  $+5\text{VD}$  and  $+5\text{VA}$  supplies are on. For the  $\pm\text{VA}$  supplies, a resistance value is populated that will yield forward currents below the maximum specified for the part for the range of input voltages specified in Table 1.

#### 4.1.3 Linear Regulator Thermal Consideration

To produce the  $+5.0 \text{ V}$  analog voltage required by the AD7606, an LT1129-5 linear regulator is provided. The LT1129-5 produces a  $+5.0 \text{ V} \pm 150m\text{V}$  voltage that meets the requirements of the AD7606 [28]. Linear regulators offer excellent noise characteristics and circuit simplicity compared to switching regulators; the trade off is low efficiency, which can result in a significant amount of heat in the regulator that must be considered. The maximum allowed junction temperature of the LT1129 series is  $125^\circ \text{ C}$  [28]. To estimate the junction temperature, the junction-to-ambient thermal resistance of the IC package,  $R_{\text{TH}}$  given in  $^\circ \text{C/W}$ , is multiplied by the power dissipation of the part [28]. Two equations describe the amount of power (heat) dissipated in a voltage regulator. The power dissipated due to the current drawn by the circuit connected to the regulator output is

$$P_{\text{drop}} = I_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}}), \quad (2)$$

which, according to Kirchoff's Current Law, has to come from the input, and

$$P_{\text{gnd}} = I_{\text{GND}} \times V_{\text{IN}} \quad (3)$$

is the power dissipated by the current flowing from the input to ground where  $I_{GND}$  is estimated based on performance curves in [28].

Since the AD7606 is the most significant current draw on the output of the LT1129-5, the supply current given in the AD7606 data sheet is used to estimate the current draw on the LT1129-5. The AD7606 data sheet specifies that, when the device is operational, the maximum supply current is 27mA [26]. Thus, the expected maximum power dissipated in the LT1129 is  $P_{drop} + P_{gnd} = 276\text{ mW}$  based on one eight channel AD7606 drawing 27 mA for  $I_{OUT}$ ,  $V_{IN}$  provided by +VA at the maximum 15 V, and  $I_{GND}$  estimated to be 0.6 mA based on performance curves in [28].

The junction-to-ambient thermal resistance depends on the IC package and the area of copper in the PCB that will spread the heat away from the IC [28]. Taking the worst thermal characteristic package, 8-pin SOIC with  $100\text{ mm}^2$  of copper on the top side of the board and  $2500\text{ mm}^2$  on the bottom side of the board with  $R_{TH} = 69^\circ\text{ C/W}$  [28], yields a temperature rise of  $276\text{ mW} \times 69^\circ\text{ C/W} = 19.0^\circ\text{ C}$ , which means that, in the worst case scenario, the junction temperature of the LT1129 will only be  $19.0^\circ\text{ C}$  warmer than the ambient temperature. Since the ambient temperature would have to be above  $106^\circ\text{ C}$  to yield a junction temperature that could damage the part, it is safe to choose the 8-pin SOIC package for the +5VA regulator.

#### 4.1.4 Grounding

Fast switching digital signals have a wide bandwidth that causes RF energy to be injected in the power supplies and radiated from that portion of the circuit. Also, the high instantaneous current drawn by a switching digital signal can cause a voltage potential between the ground connections of the circuit and the ground at the power supply due to the non-zero resistance and inductance of ground planes, traces, and power supply leads. Thus, it is desirable to have electrically isolated power and ground supplies for the analog and digital portions of the circuit.

Figure 3 shows one possible power supply configuration of the RTSC and Electrophysiology Interface boards and shows analog (ASIG) and digital (DSIG) signal paths which

connect an IC grounded to the analog plane (AGND) to a IC grounded by the digital ground plane (DGND). The RTSC board is powered by the USB interface of the PC, which may or may not connect DGND to earth ground of the building electrical distribution system. Digital signals from the FPGA are routed to the Electrophysiology Interface board over the Hirose FX2 connector, which also makes multiple connections between DGND on the Electrophysiology Interface board and the ground plane of the RTSC board. The digital circuits on the Electrophysiology Interface board are powered by an isolated +5.0 V fixed output bench-top power supply and are connected to the DGND plane. The analog circuits are powered by the isolated variable outputs of the bench-top power supply and are connected to the AGND plane. The AD5678 DAC is powered by the digital supply, and its analog output signals are connected to the differential output amplifier blocks that are powered by the analog supplies. The AD7606 ADC communicates with the digital signals of the FPGA, and its IO buffers are powered by a digital supply, but its main power supply is analog. The Preamp boards receive analog power from the PCI-Express connectors, and their digital signals are controlled by the CPLD powered by the digital supply.

The communication between parts powered by the analog and digital supplies requires that the signals be referenced to a common node. Thus, the analog and digital grounds are connected near the bench-top power supply. This has the effect of minimizing ground-bounce by directing the current return of most of the fast switching digital signals through the digital power supply lead, but it directs the signal return current, from signals that cross the ground planes, to the bench-top power supply before it can return to the signal source, yielding a large signal loop that increases radiated emissions [34].

Both the AD5678 and AD7606 recommend that, if analog and digital ground connection is needed, it should be close to the the respective IC [26, 27]. Near the AD5678 and near the AD7606, pads for  $0\Omega$  resistors may be populated to allow a shorter signal current return path, but if multiple signals switch at once, the actual non-zero resistance of the resistor, via, and trace connecting the ground planes will be out of balance with the signal trace resistance and may allow signal return current in the ground planes to divert back to the bench-top power supply.

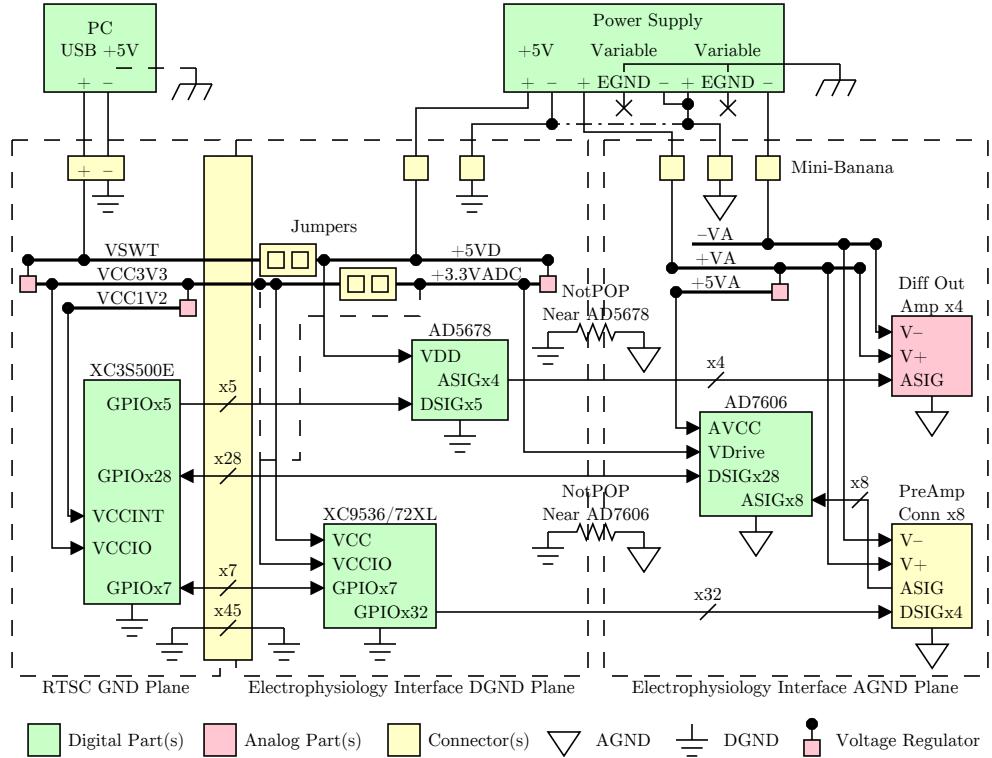


Figure 3: Ground planes

Future designs should consider suggestions in [34] for completely isolating analog and digital power and ground using opto-isolators or isolation transformers for digital signals that need to communicate between analog and digital circuits, or an alternative is to bridge analog and digital planes under signals that interface with analog and digital circuits.

#### 4.1.5 Decoupling Capacitors

Capacitors are populated on the RTSC board and the Electrophysiology Interface board for the purpose of maintaining quality power supply voltages in the presence of high switching currents and radiated and conducted electromagnetic interference (EMI). Capacitors connected to the power and ground planes perform three functions: decoupling which provides a source of DC power near components that meet demand for short duration power surges and keeping RF energy generated by components from propagating into the power

supply network, bypassing which provides a low impedance path to ground for high frequency noise that may interfere with components, and bulk capacitance that is used to maintain a constant DC voltage for situations that cause a large  $di/dt$ , such as all digital signals switching simultaneously [34].

Ideal capacitors with large capacitance values yield a low impedance at high frequencies and store more energy than low capacitance values, but the electrolytic and tantalum constructions that allow large capacitance values in small volumes have comparatively large equivalent series resistance (ESR) and equivalent series inductance (ESL) that limit their usefulness at higher frequencies and for large  $di/dt$ . Thus low ESR, ESL, and value ceramic capacitors are often used in parallel with electrolytic or tantalum capacitors to provide the required capacitance for decoupling and bypassing [34]. The capacitors are also placed as close as possible to the component that needs bypassing and decoupling to limit the added inductance in the length of PCB trace between the capacitor and the component. Because of resonance effects with parallel capacitors, their values should be separated by at least two orders of magnitude (i.e. the value of the electrolytic capacitor should be at least 100 times greater than the value of the ceramic capacitor) [34]. Power and ground planes, themselves being two parallel plates, also act as capacitors with the advantage of having effectively no ESR and very low ESL and may provide sufficient capacitance, with closely spaced planes for slow switching frequency and slew rate circuits, but the planes should be spaced by less than 0.1 in and vias limit the effective capacitance of the parallel planes [34].

On the Electrophysiology Interface board, a capacitor that performs decoupling and bypass functions is populated for each power supply pin of a component and each power pin of a connector, and the capacitor is placed as close as possible to the pin. One  $0.1 \mu\text{F}$  ceramic capacitor is used, if no recommendation is given by the part's data sheet. The AD5678 data sheet recommends a  $10 \mu\text{F}$  capacitor in parallel with a low ESR  $0.1 \mu\text{F}$  capacitor [27]. If a surface mount ceramic capacitor is available with the recommended capacitance, a ceramic capacitor is used even if the data sheet suggests using a tantalum or electrolytic capacitor. One large value electrolytic capacitor is available for each of the +5VD, +VA, and -VA power supplies to provide bulk capacitance.

## 4.2 Programmable Logic Configuration

The Xilinx® XC3S500E FPGA is a volatile programmable logic device, meaning that the configuration of the FPGA is lost when power is removed. The Xilinx® XC9536/72XL CPLD is a non-volatile programmable logic device. Configuration files that describes the state of the FPGA and CPLD are produced by the Xilinx® ISE Design Suite. A mechanism must be in place to load the configuration into the FPGA after every power cycle. The CPLD configuration only needs to be loaded once; it will retain its configuration between power cycles.

Two configurations options are available on the RTSC to load a configuration to the FPGA. A jumper selects whether the FPGA will be configured using the Joint Test Action Group (JTAG) interface or the Xilinx® XCF00S Platform Flash EEPROM. The connections between the FPGA and the Platform Flash and the jumper options are shown in Figure 4.

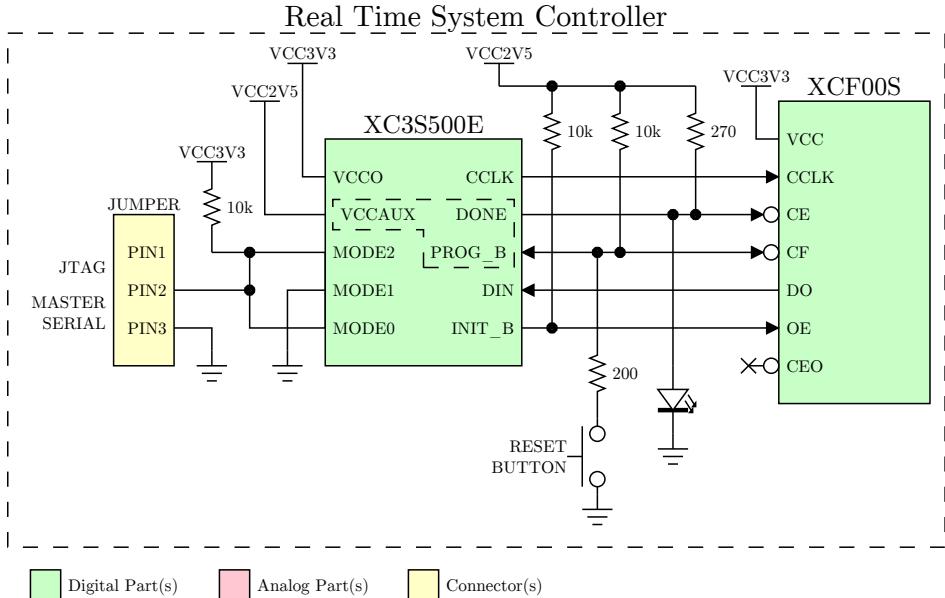


Figure 4: Connection of the Platform FLASH Configuration PROM to the FPGA [19, 20]

There are three pins on the FPGA that control the configuration mode. These pins are labeled MODE[0:2]. The FPGA is capable of several configuration modes, but the modes available on the RTSC are shown in Table 2.

MODE[0:2]	Configuration mode
[0 0 0]	Master Serial (Platform Flash)
[1 0 1]	JTAG Mode

Table 2: FPGA configuration modes from a table in [35]

#### 4.2.1 Master Serial

Xilinx® has created a line of flash ICs that make on board configuration very simple. Using the Platform Flash ICs, the Spartan 3E FPGA can configure itself in Master Serial mode where the FPGA controls the serial data clock and enables the flash chip [35]. The XCF04S 4Mbit Platform Flash device provides enough storage for one configuration file for the XC3S500E [35].

Upon power up, the INIT\_B and DONE open-drain IO pins and the PROG\_B input pin are pulled high. INIT\_B going high causes the FPGA to sample the MODE[0:2] pins, and if Master Serial is the mode selected, INIT\_B is pulled low, resetting the Platform Flash while the configuration is cleared, after which INIT\_B is allowed to go high. DONE is pulled low, enabling the Platform Flash, and the FPGA begins to generate a clock on CCLK, causing the Platform Flash to present data on its DO pin. After configuration is complete, DONE is allowed to go high, and by virtue of the resistor and LED connected to the pin, the LED will turn on and DONE and  $\overline{CE}$  voltage will be at  $V_F$  of the LED [35].

Pulsing PROG\_B low for at least 500 ns will cause the FPGA to clear the configuration memory, pull INIT\_B low, and sample the MODE[0:2] pins when INIT\_B goes high [35]. The reset button on the RTSC will cause the FPGA to clear its configuration and reconfigure itself or wait for the JTAG interface, depending on the status the MODE[0:2] pins.

#### 4.2.2 JTAG

A method of testing interconnects between integrated circuits (IC) on a PCB called Boundary Scan is commonly implemented on digital ICs. The Boundary Scan standard was developed by the Joint Test Action Group (JTAG) and later adopted as an IEEE standard with the designation IEEE Std. 1149.1. Boundary Scan, which is commonly referred to as

JTAG [36].

The JTAG interface also provides in-circuit programming capabilities which is the feature that is used to configure the FPGA, Platform Flash, and CPLD. Multiple devices can be daisy-chained in a single JTAG interface. The list of signals is in the Table 3, which is based on [36].

Abbreviation	Signal	Description
TCK	Test Clock	Clock signal bussed to all devices in the chain
TMS	Test Mode Select	Mode signal bussed to all devices in the chain
TDI	Test Data In	Data to be shifted into device JTAG logic from the previous device in the chain. Sampled on rising edge of TCK
TDO	Test Data Out	Data to be shifted out of device JTAG logic to the next device in the chain. Updated on falling edge of TCK

Table 3: JTAG signal names and descriptions [36]

To program the FPGA, Platform Flash, or CPLD, a JTAG programming cable available from Digilent®, Xilinx®, or another vendor may be connected to the JTAG header, or the JTAG capabilities of the Cypress microcontroller may be utilized with the Digilent® ADEPT PC software. Details of the JTAG connections, which are based on [20], are shown in Figure 5. The resistors on the TCK, TMS, and XC3S500E TDI lines are required to be  $> 68\Omega$  for 3.3 V JTAG interfaces ( $0\Omega$  for 2.5 V interface) [35]. Reference [20] uses  $200\Omega$  resistors.

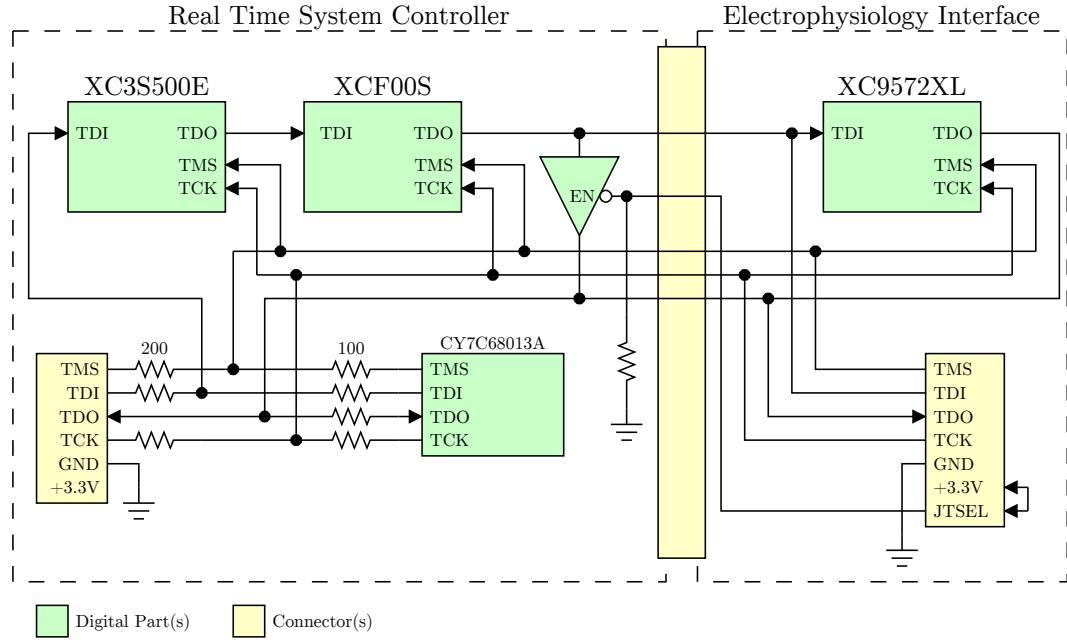


Figure 5: Signals in the JTAG scan chain; RTSC connections based on [20]

The RTSC routes the JTAG scan chain through the FPGA, then the Platform Flash, and finally over the Hirose FX2 connector. If a peripheral board connected to the FX2 connector does not connect to the RTSC's JTAG scan chain, a tri-state buffer, with its active-low output-enable pin pulled low, routes the TDO signal of the Platform Flash to the Cypress microcontroller and JTAG programming cable header. To enable the CPLD on the Electrophysiology Interface board to be programmed through the JTAG scan chain of the RTSC, the TDO signal from the Platform Flash is routed to the TDI pin of the CPLD, the TDO pin of the CPLD is routed to the Cypress microcontroller and JTAG programming header on the RTSC, and the TMS and TCK signals are bussed to the CPLD. A header on the Electrophysiology Interface board allows probing of the JTAG signals, or if the board is not connected to the RTSC, a JTAG programming cable may be connected to the header to program the CPLD. The output-enable pin of the tri-state buffer is routed to the JTSEL signal on the Electrophysiology Interface board. To prevent the tri-state buffer and CPLD from acting as an output on the same signal, connecting JTSEL to +3.3 V on the header on

the Electrophysiology Interface board will disable the output of the tri-state buffer. Thus, simply connecting the Electrophysiology Interface board to the RTSC board will put the CPLD in the RTSC's JTAG scan chain.

Steps for configuring the FPGA or CPLD or loading a configuration file into the Platform Flash in JTAG mode:

1. Set the configuration jumper on the RTSC to JTAG Mode
2. If the Electrophysiology Interface board is connected to the RTSC, configure the power supplies so that the CPLD's VCC and VCCIO pins will be powered
3. Connect the USB cable to the RTSC, or connect the JTAG programming cable to the JTAG header on the RTSC
4. Turn on power to the RTSC and Electrophysiology Interface, if it's connected
5. Follow the steps required in the PC software for the programming cable to load the configuration file onto the FPGA, Platform Flash, or CPLD

### 4.3 Real Time System Controller Board Circuit Design

This section describes the relevant circuitry on the Digilent® Nexys™ 2 FPGA development board that is utilized by the Data Acquisition and Stimulation System (DASS) as the Real Time System Controller (RTSC) Board. Replacing the Nexys™ 2 FPGA development board with a custom RTSC Board or designing a system based on the DASS with more channels, as described in section 8, would require the duplication of the following circuitry or the design of new circuitry that would perform similar functions.

#### 4.3.1 Cypress Microcontroller

The Cypress CY7C68013C EZ-USB® microcontroller on the RTSC provides a USB interface to the FPGA and provides JTAG programming capabilities without the need for separate JTAG programming hardware [19]. Unlike a general purpose microcontroller or FPGA, the Cypress microcontroller can connect directly to the USB signal lines with

its integrated USB transceiver [37]. Figure 6 shows the connections between the Cypress microcontroller and the FPGA on the RTSC.

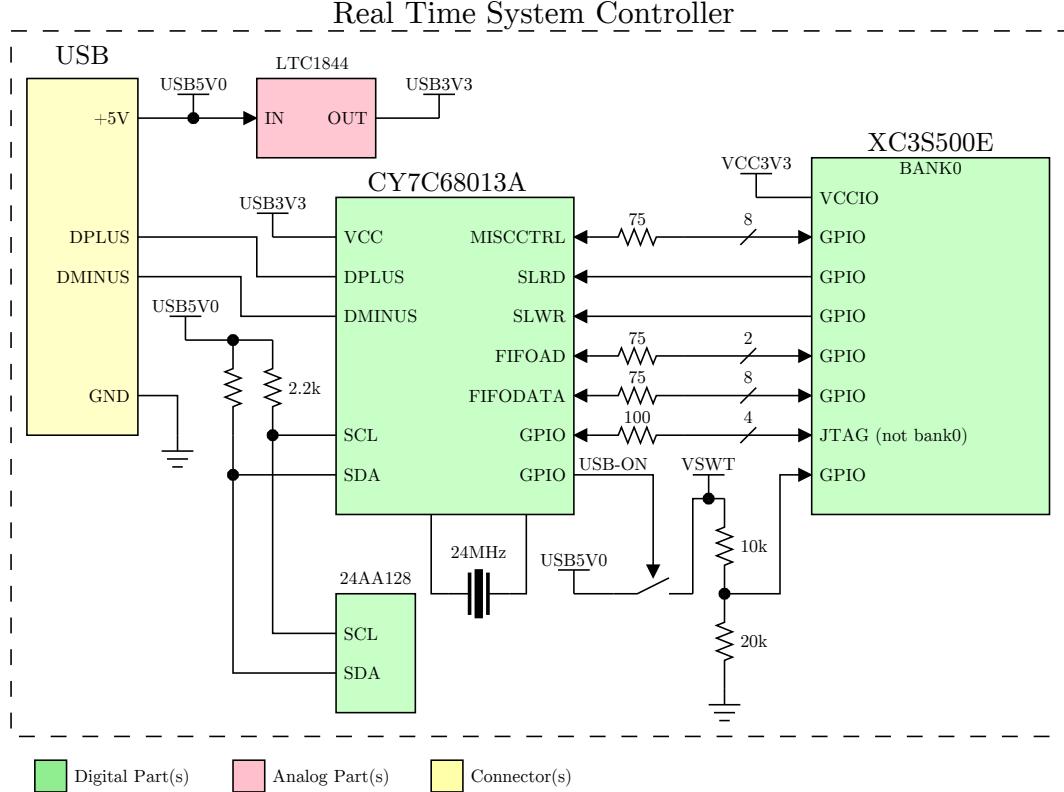


Figure 6: Connections for the USB interface on the RTSC board [19, 20]

A USB peripheral must not draw more than 100mA from the host until it has negotiated the full power capabilities of the bus. The Cypress microcontroller receives 3.3V power from a regulator connected directly to the 5V USB supply. The rest of the RTSC board can be powered from the USB supply, but if the entire RTSC board is to be powered by the USB supply voltage, it must not power all of its circuits immediately upon connection because the board would draw more than 100mA [19]. When the Cypress microcontroller has negotiated the full power capabilities of the bus, the USB-ON signal, which is connected to the gate of a NMOS transistor, is toggled connecting the USB5V0 voltage to the rest of the board [19].

Connections between the Cypress microcontroller have series resistors where the Cypress microcontroller signal can be an output. This is to limit the current in the case of the FPGA

pin being setup as an output simultaneously with the Cypress microcontroller.

Data transfer from the FPGA to the USB host is facilitated by a first in, first out (FIFO) buffer in the Cypress microcontroller. A FIFO acts as a dual port memory allowing a device to push data into the memory; the FIFO will keep track of the memory address to be written. The same device or a second device can then read from the memory and the FIFO will fetch the oldest data in memory that has yet to be read. In this way, two devices, operating on different clocks or with other tasks to complete, can share data without being synchronized, or one device can store a stream of data and retrieve the data stream in the order written without the need for memory addressing logic.

Eight of the data connections between the Cypress microcontroller and the FPGA carry the FIFO data that can be written or read by the FPGA (FIFODATA). The Cypress microcontroller internally reads or writes to the other side of the FIFO with data to or from the USB bus [37]. A 24MHz crystal provides a dedicated clock to the Cypress microcontroller. A 12pF capacitor is required from each terminal of the crystal to ground to stabilize the oscillation [19]. A 24AA128 EEPROM, that contains the Digilent® firmware, is connected to the I<sup>2</sup>C pins of the Cypress microcontroller, which are open-drain outputs and hysteresis inputs that must be pulled up to 3.3V even if unconnected [37]; although, the RTSC pulls these signals to USB5V0 [20].

#### 4.3.2 RS232 Control Interface

Control signals can be communicated separately from the USB interface using the serial port on the RTSC. PC serial ports conform to the RS232 standard which uses signaling voltages that are incompatible with the 3.3VTTL/CMOS logic of the FPGA [38]. The ST232 level shifting IC converts logic LOW and HIGH of LVTTL/CMOS voltages to RS232 compatible voltages without the need for higher voltage supplies [22]. Table 4 shows the logic voltage levels compatible with the Xilinx® XC3S500E FPGA IO pins configured for LVTTL and logic voltages compatible with the RS232 standard [24, 38].

RS232 communication is asynchronous and full duplex with separate receive (often labeled as RX or R) and transmit (often labeled as TX or T) data lines and without a

Logic	LOW <sub>min</sub>	LOW <sub>max</sub>	HIGH <sub>min</sub>	HIGH <sub>max</sub>
LVTTL	-0.5 V	+0.8 V	+2.0 V	+3.8 V
RS232	+3.0 V	+25.0 V	-25.0 V	-3.0 V

Table 4: FPGA and RS232 logic voltage level comparison

dedicated clock signal. The signals other than RX and TX are not necessary for simple communication between one host and peripheral [38].

As shown in Figure 7, the ST232 level shifting IC is between the FPGA’s GPIO pins being used for RX and TX signals that can be connected to a PC via the standard pinout D-Subminiature 9 pin (DB9) connector. The ST232 is capable of passing two separate RS232 communication busses (R1/T1 IN/OUT and R2/T2 IN/OUT), but only one set is used by the FPGA.

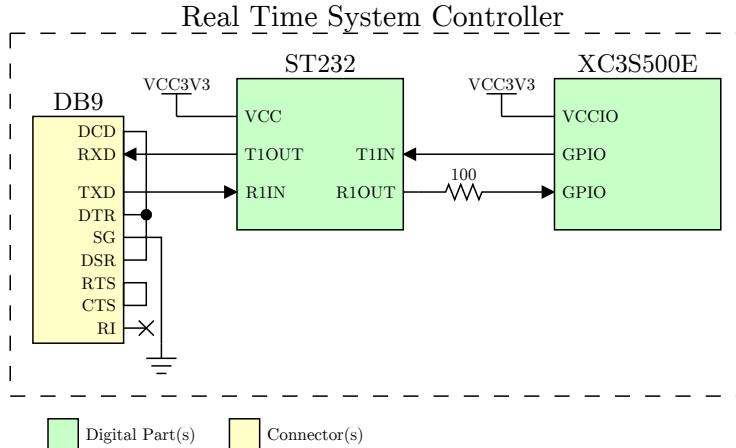


Figure 7: RS232 level shifter that allows a PC serial port to communicate with the FPGA [19, 20]

For a future design, an alternative to provide PC communication is to use an TTL-232RG cable from FTDI that connects to a USB port and provides a virtual serial port to the PC while providing a TTL serial UART compatible interface to connect to the FPGA, directly [39].

### 4.3.3 DRAM

The RTSC board contains a 54-pin, ball grid array (BGA) packaged MT45W8MW16BGX 128Mbit DRAM IC from Micron® with its address and data bus connected in parallel with a JS28F128 128Mb Flash ROM from Intel® [19]. The DRAM is used by the configuration on the FPGA to store stimulation waveform data, and the Flash ROM is not used [15]. Figure 8 shows the connections between the Xilinx® XC3S500E FPGA and the DRAM and Flash ROM on the RTSC board.

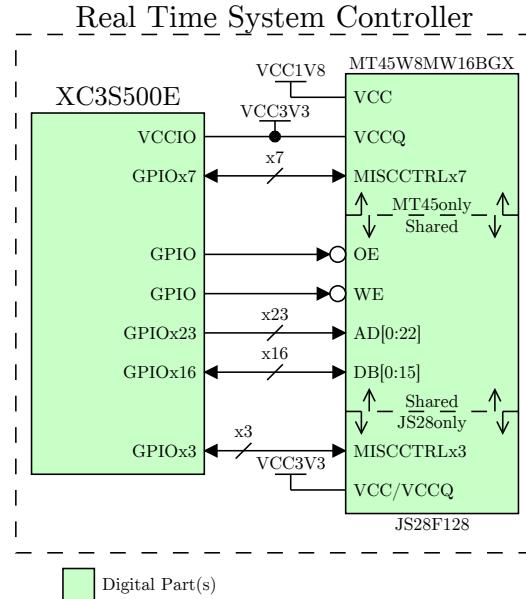


Figure 8: Connections between the FPGA and the DRAM and Flash memory ICs on the RTSC board [19, 20]

The DRAM requires a +1.8 V power supply for its internal circuitry and has a dedicated supply pin for interface logic as described in section 4.1.1. Seven control signals are connected exclusively between the FPGA and DRAM IC. The 23-bit wide address bus, 16-bit bi-directional data bus, output enable ( $\overline{OE}$ ) signal, and write enable ( $\overline{WE}$ ) signal are connected to both the DRAM and Flash IC. The Flash IC has a 25-bit address bus, but its MSbit and LSbit are pulled LOW [20]. Three control signals are connected exclusively between the FPGA and Flash ROM IC.

## 4.4 Electrophysiology Interface Board Circuit Design

This section describes and documents the design of the custom circuitry on the Electrophysiology Interface Board. These circuits were implemented on a custom printed circuit board (PCB), described in section 5. The circuit designs in this section could also be used in the creation of a 64 channel system, as proposed in section 8, for use in microelectrode array (MEA) electrophysiology experiments.

### 4.4.1 Digital to Analog Converter

The Analog Devices AD5678-2 was chosen to be the DAC on the Electrophysiology Interface board because of previous experience with the device in the Neurobiology Engineering Laboratory [10]. The design for the circuit shown in Figure 9 is based on a breadboarded prototype circuit [10] and recommendations in the device data sheet [27].

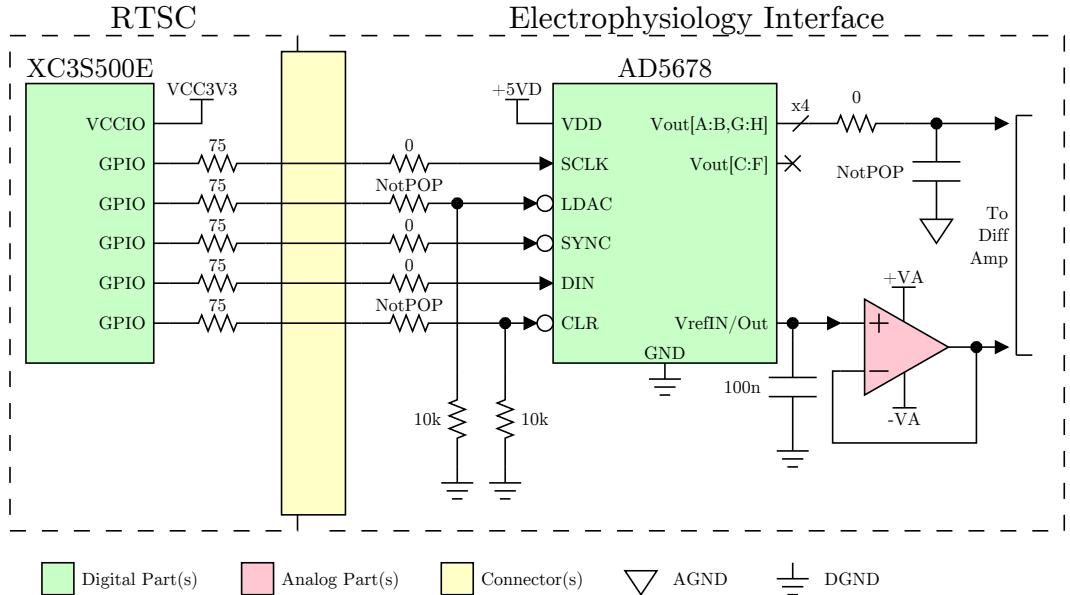


Figure 9: FPGA connections to the DAC

Signals from the Xilinx® XC3S500E FPGA on the RTSC board are routed through the Hirose FX2 connector to the Electrophysiology Interface board and the 40-pin test header, finally going through a  $0\Omega$  resistor before being routed to the digital control pins

of the AD5678. The four 16-bit DAC analog outputs are routed to the Differential Output Amplifier circuits through a resistor that may be used, in concert with a capacitor, to implement an RC-type low pass filter. The four 12-bit DAC outputs are left unconnected. The FPGA configures the AD5678 to use its internal voltage reference for DAC operations, and thus, the Vref pin acts as the output of the internal voltage reference. A 100nF capacitor is placed between the Vref pin and ground to stabilize the reference output [27], and the reference output voltage is used in the Differential Output Amplifier circuit, which requires the use of a buffer amplifier [27]. A description of each digital control pin is in Table 5.

Pin	Function
SYNC	Active low synchronization signal for input data, similar to SPI CS
DIN	Serial data input
SCLK	Serial clock input
LDAC	Updates outputs simultaneously on a low pulse, it may be tied low if unused
CLR	Falling edge triggered clear input that can set all the outputs to zero, mid-scale, or full-scale (default zero), pull down resistor keeps this from being noise triggered if unused

Table 5: AD5678 Digital Pin Functions [27]

$\overline{\text{SYNC}}$ , DIN, and SCLK are mandatory signals for executing commands and loading data into the DAC. The signals are compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards [27]. The  $\overline{\text{LDAC}}$  and  $\overline{\text{CLR}}$  signals provide additional functionality that is not used in the current version of the FPGA configuration. Thus, the  $0\Omega$  resistors are not populated on the Electrophysiology Interface board, allowing the FPGA's GPIO pins to be accessed at the test header and used for other purposes if needed, and the DAC pins are pulled to ground through  $10\text{k}\Omega$  resistors to keep the inputs at a known state that will not affect the operation of the DAC.

The AD5678 contains a power-on reset circuit that sets the DAC outputs to 0V upon power up, which due to the Differential Output Amplifier may yield a significant voltage across the stimulation electrodes, which may be incompatible with the biological setup [27]. Therefore, upon power-up, the FPGA should immediately write DAC outputs or set the

Clear Code Register and pulse the  $\overline{\text{CLR}}$  signal to set the DAC outputs to a value that will yield a voltage across the stimulation electrodes that is compatible with the experimental setup.  $\overline{\text{CLR}}$  is a falling edge triggered signal that can also be used to asynchronously set all of the outputs to the state defined in the Clear Code Register of the AD5678 [27].

#### 4.4.2 Differential Output Amplifier

The analog output of the AD5678-2, when using the internal 2.5 V voltage reference, can vary over the range of 0 V to 5 V. The output voltage is given by the equation

$$V_{\text{out}} = 2 \times V_{\text{refOut}} \times \frac{D}{2^N}, \quad (4)$$

where  $D$  is the decimal equivalent of the binary value loaded into the DAC output register and  $N$  is the resolution of the DAC (16 for the DAC outputs used on the Electrophysiology Interface board) [27]. It is desirable to have pulses as high as 10 V and with biphasic shapes to perform some electrophysiology experiments [12, 18]. Thus, some form of signal gain and offset is needed to extend the range of the output signal. It is also desirable to be able to perform experiments with differential outputs, so the single-ended output of the DAC is converted to a differential output.

The design of Differential Output Amplifier circuit as shown in Figure 11 consists of a difference amplifier circuit, implemented with operational amplifier (op-amp) OA1, to perform the gain and offset operations on the DAC output and an inverting amplifier, implemented with op-amp OA2, to create a differential output. The Differential Output Amplifier design is replicated for each of the DAC outputs to create four unique outputs that can be connected to stimulation electrodes single-endedly (between  $V_{\text{out}+}$  and AGND or  $V_{\text{out}-}$  and AGND) or differentially (between  $V_{\text{out}+}$  and  $V_{\text{out}-}$ ).

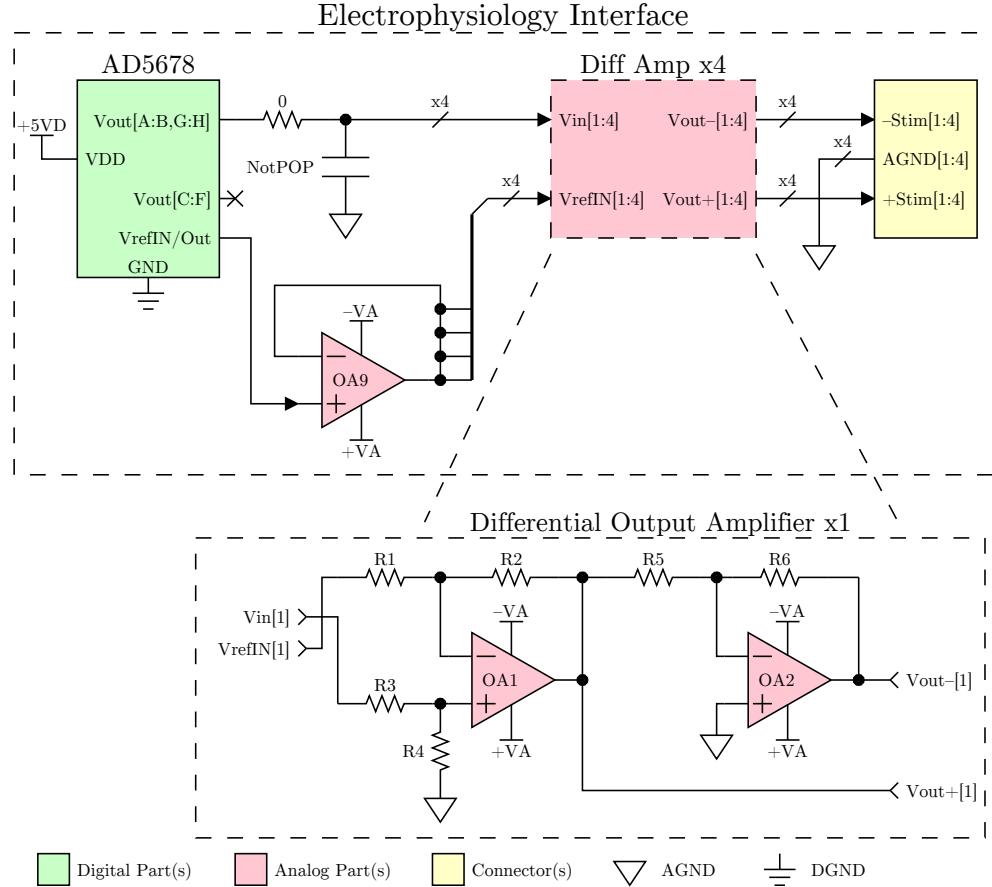


Figure 10: Differential Output Amplifier

The difference amplifier op-amp configuration is well known, with its operation described by equation

$$V_{out+} = \frac{R_2}{R_1} \frac{1 + R_1/R_2}{1 + R_3/R_4} V_{in} - \frac{R_2}{R_1} V_{refIN}; \quad (5)$$

choosing resistor values with the constraint

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \quad (6)$$

yields the simpler form

$$V_{out+} = \frac{R_2}{R_1} (V_{in} - V_{refIN}), \quad (7)$$

which has the gain and offset elements needed to fulfill the design requirements [40].

The 0 V to 5 V range of the DAC outputs can be made symmetrical around 0 V by subtracting 2.5 V, yielding a range of  $-2.5 \text{ V}$  to  $2.5 \text{ V}$ . Thus, the range of  $\text{Vout+}$  is  $-2.5 \text{ V} \times R_2/R_1$  to  $2.5 \text{ V} \times R_2/R_1$ , allowing the output range to be easily calculated and changed if needed. Since the AD5678 makes its internal 2.5 V voltage reference accessible on an external pin, using that voltage as an input to the difference amplifier eliminates the need for an external voltage reference circuit that would involve a resistor network susceptible to inaccuracies in the power supply voltage or a specialized voltage reference IC. Substituting the midscale DAC code 0x7FFF into equation (4) and (7) yields  $\text{Vout+} = 76 \mu\text{V} \times R_2/R_1$  which is very close to 0 V. Programming the AD5678 to output midscale codes on the DAC outputs after power-on reset will ensure than stimulation electrodes have a low DC voltage without having to write the DAC code at every power cycle.

An inverted output is needed to implement a differential output amplifier. This can be accomplished with an op-amp in an inverting configuration. The equation for the inverting amplifier is

$$\text{Vout-} = -\frac{R_6}{R_5} \text{Vout+}; \quad (8)$$

choosing  $R_5 = R_6$  will make  $\text{Vout-}$  the inverse of  $\text{Vout+}$  [40]. The ratio  $R_2/R_1$  is set to 3 to produce single-ended output range of  $-2.5 \text{ V} \times R_2/R_1$  to  $2.5 \text{ V} \times R_2/R_1 \Rightarrow -7.5 \text{ V}$  to  $7.5 \text{ V}$ , which will be close to the saturation voltages of an op-amp powered from  $\pm 9 \text{ V}$  supplies.

Table 6 shows resistor values chosen and calculated for the design.

Choose	$R_1$	$R_3$	$R_2/R_1$
	1 kΩ	1 kΩ	3
Yields	$R_2$	$R_4$	
	3 kΩ	3 kΩ	
Choose	$R_5$		
	1 kΩ		
Yields	$R_6$		
	1 kΩ		

Table 6: Resistor values for the Differential Output Amplifier

The dual packaged LT1124-1 precision op-amp from Linear Technology® was chosen because the LT1124/LT1125 part family was used in [9, 10], SPICE amplifier models are available for LTspice® circuit simulation software, the dual package allows the Differential Output Amplifier block with two op-amps to be implemented with only one IC, and the -1 option specifies a standard pinout 8-SO surface mount part so other op-amp models may be tested with the design [41].

According to [27], the voltage reference output should be buffered if used to drive a load, so a single op-amp in a voltage follower configuration is used to buffer the reference voltage to the Differential Output Amplifier blocks. One half of an LT1124-1 is used to be consistent with the other op-amps on the Electrophysiology Interface board. The buffer op-amp, OA9, drives current through  $R_1$  of the Differential Output Amplifier block; thus, the op-amp will need to be capable of driving current to four amplifier blocks. The maximum current the OA9 will need to provide will be determined by the maximum voltage across  $R_1$  multiplied by four. The maximum voltage across  $R_1$  will be when  $V_{in}$  equals 0 V, which would yield a maximum current of  $(V_{ref} - 0\text{ V})/R_1 \times 4 = 2.5\text{ V}/1\text{ k}\Omega \times 4 = 10\text{ mA}$ . It may be necessary to choose higher value resistors if the buffer is needed to drive more amplifier blocks or it is seen that the output voltage of OA9 changes during use.

The design of the Differential Output Amplifier was entered into the circuit simulation program LTspice®, as shown in Figure 11, to test the design of the circuit. The first test performed was a DC sweep of  $V_{in}$  to display the transfer function from the outputs  $V_{out+}$  and  $V_{out-}$ . The transfer function is shown in Figure 12. Saturation occurs at 40 mV and 4.95 V yielding saturation voltages of approximately  $\pm 7.4\text{ V}$ , allowing for almost the entire range of DAC output to be in the linear region and yielding a maximum possible output voltage, if taken differentially, of 14.8 V.

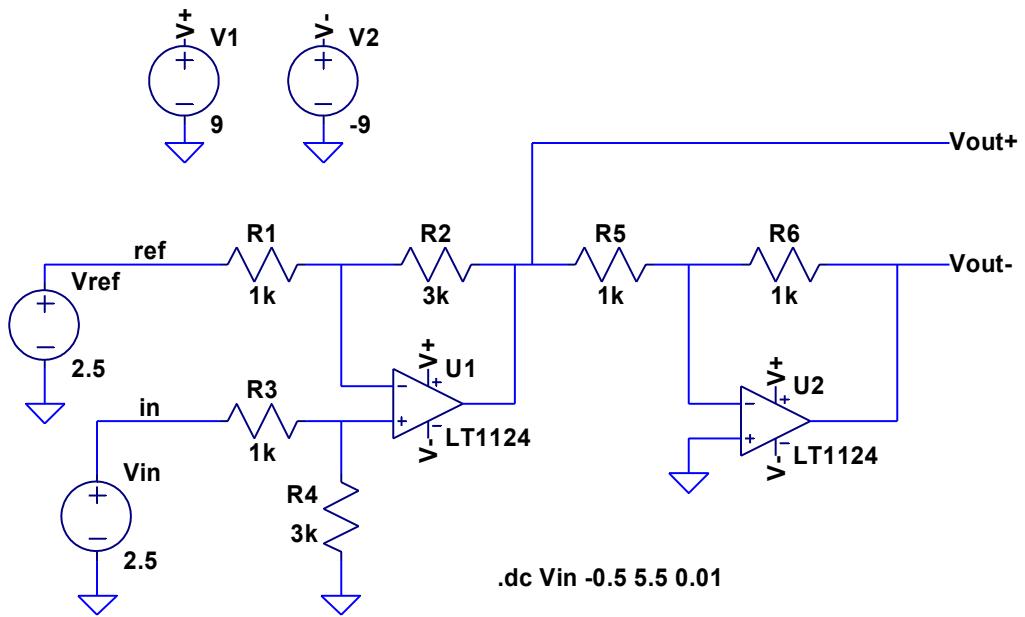


Figure 11: LTspice<sup>®</sup> schematic of the Differential Output Amplifier circuit

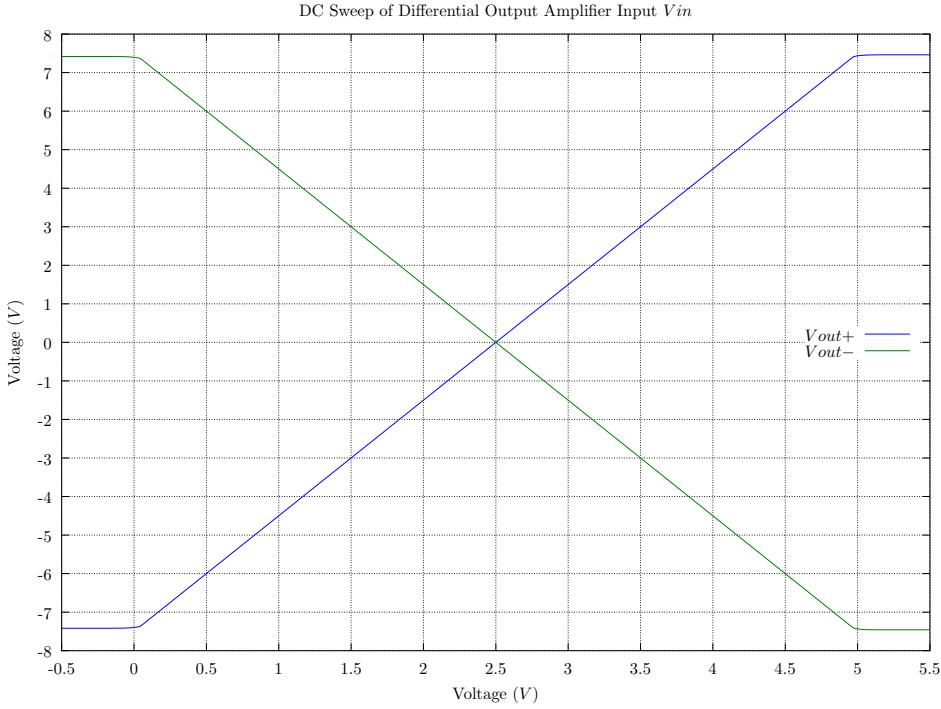


Figure 12: DC Transfer Function of the Differential Output Amplifier obtained using LTspice<sup>®</sup>

A transient simulation of a waveform used in [12] was also performed. Figure 13 shows the output connected to single-ended loads  $R_{se1}$  and  $R_{se2}$  and differential load  $R_d$ . A 0.2 ms wide pulse from midscale DAC output to an amplitude of 1.5 V with a slew rate of 1.5 V/ $\mu$ s [27] was simulated as a DAC output. The input waveform and differential and single ended outputs are shown in Figure 14.

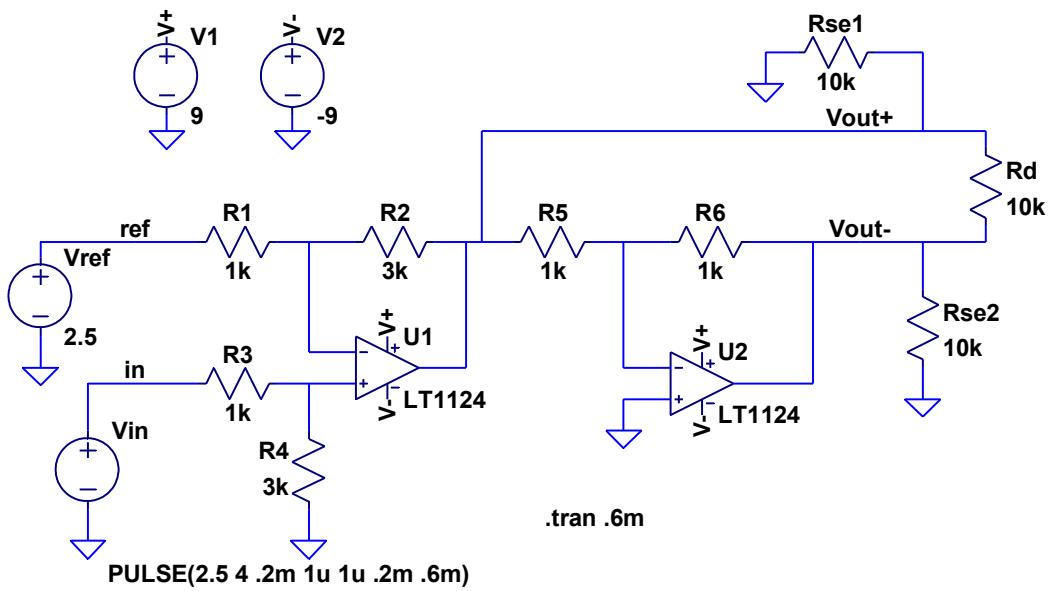


Figure 13: LTspice® schematic of the Differential Output Amplifier for transient response simulation with single-ended load resistors  $R_{se1}$  and  $R_{se2}$  and differential load resistor  $R_d$

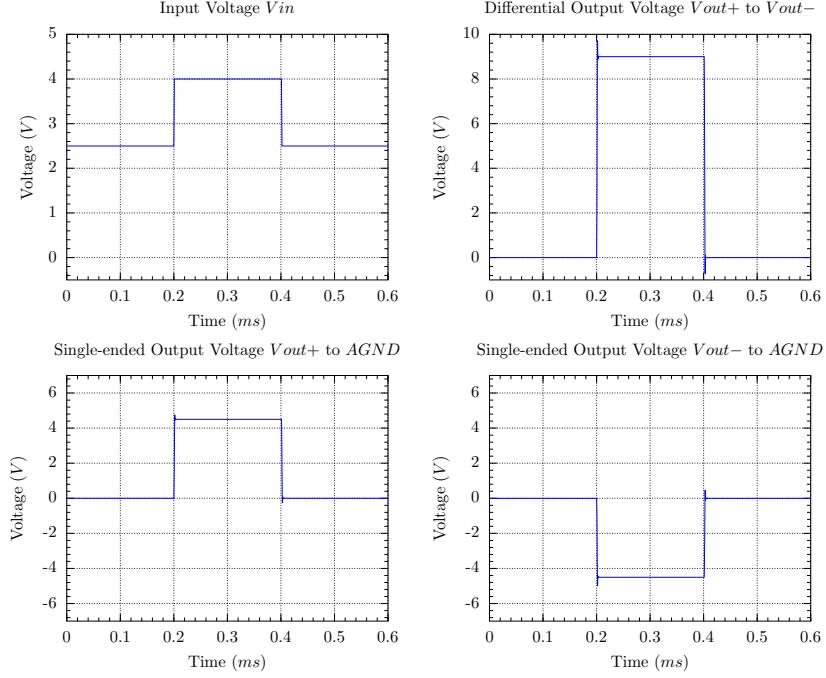


Figure 14: Differential Output Amplifier transient response to a 0.2 ms pulse from a DAC output obtained using LTspice<sup>®</sup>

#### 4.4.3 Analog to Digital Converter

The analog to digital converter (ADC) is responsible for converting the analog voltage from the output of the Preamp, which is connected to the recording electrodes in the electrophysiology setup, into digital values at regular discrete time intervals. According to the sampling theorem, the sampling frequency must be at least twice the highest frequency component of the analog signal to avoid loss of information in the analog to digital conversion [40]. The Preamp has an output bandwidth of 20 Hz to 14.6 kHz [9], which means that the minimum required sampling frequency, or Nyquist frequency, of the ADC must be  $2 \times 14.6 \text{ kHz} = 29.2 \text{ kHz}$  [40]. The AD7606 ADC from Analog Devices<sup>®</sup> offers eight analog inputs with a selectable range of  $\pm 10 \text{ V}$  or  $\pm 5 \text{ V}$  with 16 bits of resolution that sample at up to 200 kHz [26], and the AD7606 has been used previously in the Neurobiology Engineering Laboratory [10]. The AD7606 has an analog input filter with a corner frequency of 23 kHz

at  $\pm 10$  V input range and 15 kHz at  $\pm 5$  V input range [10].

Figure 15 shows the connections between the Xilinx<sup>®</sup> XC3S500E FPGA on the RTSC board and the AD7606 on the Electrophysiology Interface board. The FPGA GPIO pins connect to the digital interface of the AD7606 through the Hirose FX2 connectors and the signals are accessible on the 40-pin test header before going through a  $0\ \Omega$  resistor and finally connecting to the AD7606. Signals not used in the FPGA configuration may have their  $0\ \Omega$  resistors unpopulated allowing the unused FPGA GPIO pins to be used for other purposes and accessed on the 40-pin test header. There is a separate power supply pin, VDrive, on the AD7606 that drives the logic outputs and controls the thresholds of the logic inputs; VDrive should be powered to the same voltage as the GPIO supply of the FPGA [26].

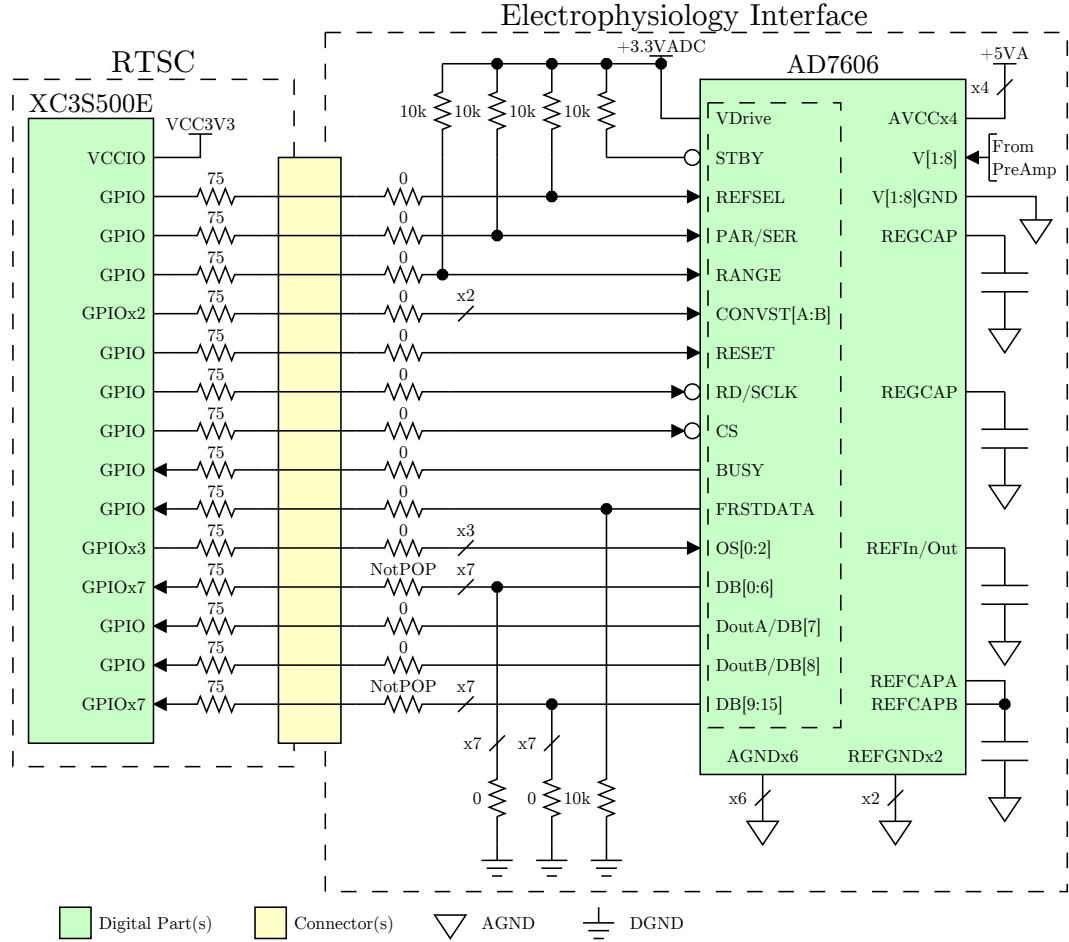


Figure 15: FPGA connections to the ADC

The single-ended outputs of the Preamps are connected to the analog voltage inputs with all channel GND pins connected to AGND. The main power supply is required to be  $5\text{ V} \pm 0.25\text{ V}$  [26], so a 5 V regulator driven by +VA provides the AVCC power. The Electrophysiology Interface board is setup for the AD7606 to use its internal voltage reference. The AD7606 requires a  $10\text{ }\mu\text{F}$  capacitor on the REFIn/Out pin for the operation of its internal voltage reference [26]. There are also a few capacitors needed for internal regulators and references; these pins have capacitors sized and placed according to the recommendation in the data sheet [26]. The details of the rest of the pin functions and connections are in

Table 7.

Table 7

Pin	Function
VDrive	Digital supply voltage. Should be the same voltage as FPGA GPIO
STBY	Puts AD7606 into low power standby mode when LOW. Tied to HIGH and not connected to FPGA
REFSEL	Selects internal, HIGH, or external, LOW, voltage reference. Pulled high through $10\text{ k}\Omega$ so $0\Omega$ resistor may be unpopulated and FPGA GPIO used for other purpose
PAR/SER/BYTESEL	Selects between serial, HIGH, or parallel, LOW, data interface. If parallel interface is selected, this is read in conjunction with DB[15] to specify 8 or 16 bit parallel interface. Pulled high through $10\text{ k}\Omega$ so $0\Omega$ resistor may be unpopulated and FPGA GPIO used for other purpose
RANGE	Sets analog input range at $\pm 10\text{ V}$ , HIGH, or $\pm 10\text{ V}$ , LOW. Pulled high through $10\text{ k}\Omega$ so $0\Omega$ resistor may be unpopulated and FPGA GPIO used for other purpose
CONVST[A:B]	Conversion Start A initiates conversions on the lower half of the analog inputs (channels 1-4 for AD7606, 1-3 for AD7606-6, and 1-2 for AD7606-4) and Conversion Start B initiates conversions on the upper half of the analog inputs. To sample on all channels simultaneously, switch both signals simultaneously. These can be shorted if both are always going to be started simultaneously, saving a FPGA GPIO pin.
RESET	Rising edge resets the AD7606. The FPGA should issue a RESET pulse to the AD7606 upon power-up
$\overline{\text{RD}}/\text{SCLK}$	Parallel data read control or serial data clock input
$\overline{\text{CS}}$	Chip select input frames data transfer
BUSY	Output rises after CONVST and falls after conversion is complete and data is ready to be clocked out
FRSTDATA	Three-state output is high-impedance when $\overline{\text{CS}}$ is HIGH, when $\overline{\text{CS}}$ is LOW, FRSTDATA is LOW except during the $\overline{\text{RD}}$ operation when channel 1 is on the parallel interface or when the 16 bits of channel 1 are being clocked out of DoutA on the serial interface (see [26] for more information). Pulled low through $10\text{ k}\Omega$ resistor to keep signal at known state when in three(tri)-state (high-impedance) mode.

*Continued on next page*

Table 7

Pin	Function
OS[0:2]	Over sampling mode select pins enables conversion a high sampling frequency and reading of the data at a lower frequency. The AD7606 then applies a digital low-pass filter before making the data available on the parallel or serial interface. Setting the mode pins to [0:0:0] disables the over sampling function. Enabling the over sampling function affects effective input bandwidth.
DB[0:6]	Three-state parallel digital input/output pins that should be tied to ground if serial data interface is used. If using the AD7606 in serial mode $0\Omega$ resistors to ground should be populated and $0\Omega$ resistors to the FPGA should not be populated. If using the AD7606 in parallel mode $0\Omega$ resistors to ground should not be populated and $0\Omega$ resistors to the FPGA should be populated.
DoutA/DB[7]	If $\overline{\text{PAR/SER/BYTESEL}}$ is HIGH, it functions as DoutA and outputs serial conversion data. Channels 1 to 4 (1 to 3 for AD7606-6, 1 to 2 for AD7606-4) first appear on DoutA. If $\overline{\text{PAR/SER/BYTESEL}}$ is LOW it's a three-state parallel digital input/output pin.
DoutB/DB[8]	If $\overline{\text{PAR/SER/BYTESEL}}$ is HIGH, it functions as DoutB and outputs serial conversion data. Channels 1 to 4 (5 to 8 for AD7606-6, 3 to 4 for AD7606-4) first appear on DoutB. Can be used as a single Dout line, the channels appear in order 5-8 then 1-4. If $\overline{\text{PAR/SER/BYTESEL}}$ is LOW it's a three-state parallel digital input/output pin.
DB[9:15]	$\overline{\text{DB[15]}}$ is also an input pin and is read if $\overline{\text{PAR/SER/BYTESEL}}$ is LOW to select between 8 bit and 16 bit interface. Three-state parallel digital input/output pins that should be tied to ground if serial data interface is used. If using the AD7606 in serial mode $0\Omega$ resistors to ground should be populated and $0\Omega$ resistors to the FPGA should not be populated. If using the AD7606 in parallel mode $0\Omega$ resistors to ground should not be populated and $0\Omega$ resistors to the FPGA should be populated.
REGCAP	Decoupling capacitors for internal regulators. Each pin should have a $1\mu\text{F}$ capacitor as close to the pin as possible with the other end connected to ground.
REFIn/Out	Voltage reference in or out. The pin should have a $10\mu\text{F}$ capacitor as close to the pin as possible with the other end connected to ground.

*Continued on next page*

Table 7

Pin	Function
REFCAP[A:B]	Reference buffer output force/sense pins. These pins should be tied together and have a $10\ \mu\text{F}$ low ESR, ceramic capacitor as close to the pin as possible with the other end connected to ground.

Table 7: Notes on AD7606 ADC pin connections and functions with information from [26]

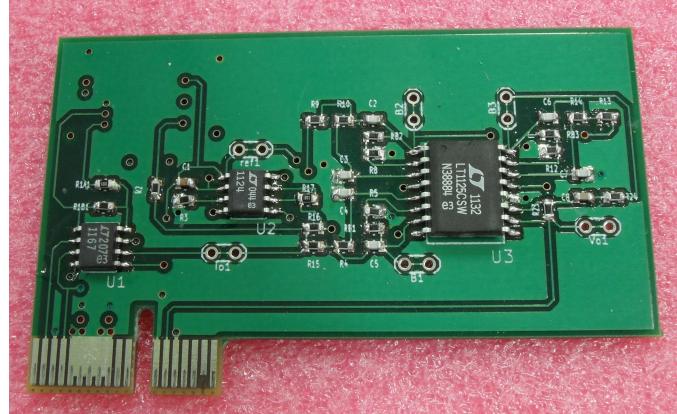
#### 4.4.4 Preamp Interface

Action potentials in electrophysiological systems are very low amplitude in the order of  $10\ \mu\text{V}$  to  $100\ \mu\text{V}$  [3]. To study the electrophysiological signals with electrical equipment, the first step is to amplify the low voltage action potentials. Previous work on this has been done in the Neurobiology Engineering Laboratory yielding a low noise amplifier design [9, 10]. Since then, the design has been adapted to fit on a PCB with a card edge connector compatible with 36-pin connectors designed for PCI-Express cards but with a custom pinout. This approach allows the tested Preamp design to be built independently of the rest of the experimental system, and eliminates the need to replicate the sensitive circuit that can be susceptible to noise. Pictures of the card edge connector version of the Preamp board, provided by John Stahl, are shown in Figure 16.

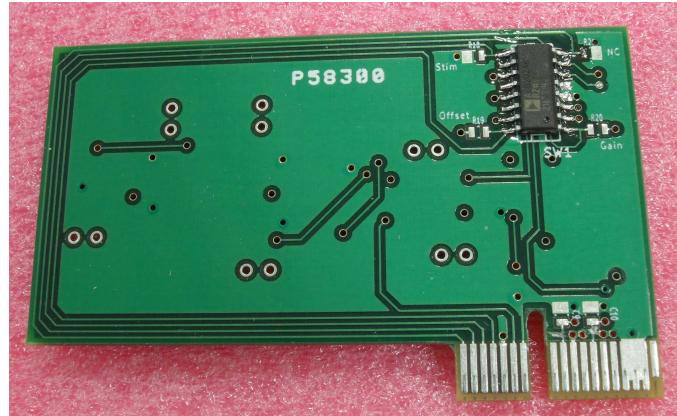
A block diagram of the Preamp board, based on [6, 9], is shown in Figure 17 along with its connection to the Electrophysiology Interface board. Not shown is the analog power and ground connections to the Preamp. A summary of the connections is shown in Table 8.

The Preamp consists of a differential input that is connected to the recording electrodes of the biological system. The low voltage signal from the electrodes is amplified by a low-noise instrumentation amplifier. An integrator connected to the instrumentation amplifier subtracts the DC part of the signal which is then passed to a 6th Order Butterworth Filter for additional gain and bandwidth reduction. A high-pass filter removes any DC component added by the Butterworth Filter circuit, and the result is a single ended output signal.

The Preamp also has the capability of outputting a stimulation signal on the non-inverting electrode with the DC offset of the electrode added to the stimulation signal [6, 9].



(a) Top side



(b) Bottom Side

Figure 16: Views of a populated Preamp Board with card edge connector, provided by John Stahl

Four digital control signals, with one not used by the Preamp, connected to analog switches and a stimulation input are needed to realize this function. CTRLO disconnects the integrator from the instrumentation amplifier output so the stimulation signal does not affect the DC offset calculation; CTRLG reduces the gain of the instrumentation amplifier to keep the amplifier from saturating when the comparatively high voltage stimulation signal is added to the electrode; an op-amp circuit adds the DC offset value, which is the integrator output divided by the instrumentation amplifier gain, to the single-ended stimulation signal, StimIn; and, finally, CTRLS connects the summing op-amp to the non-inverting electrode. The stimulation signal overpowers any biological signals on the recording electrode and allows

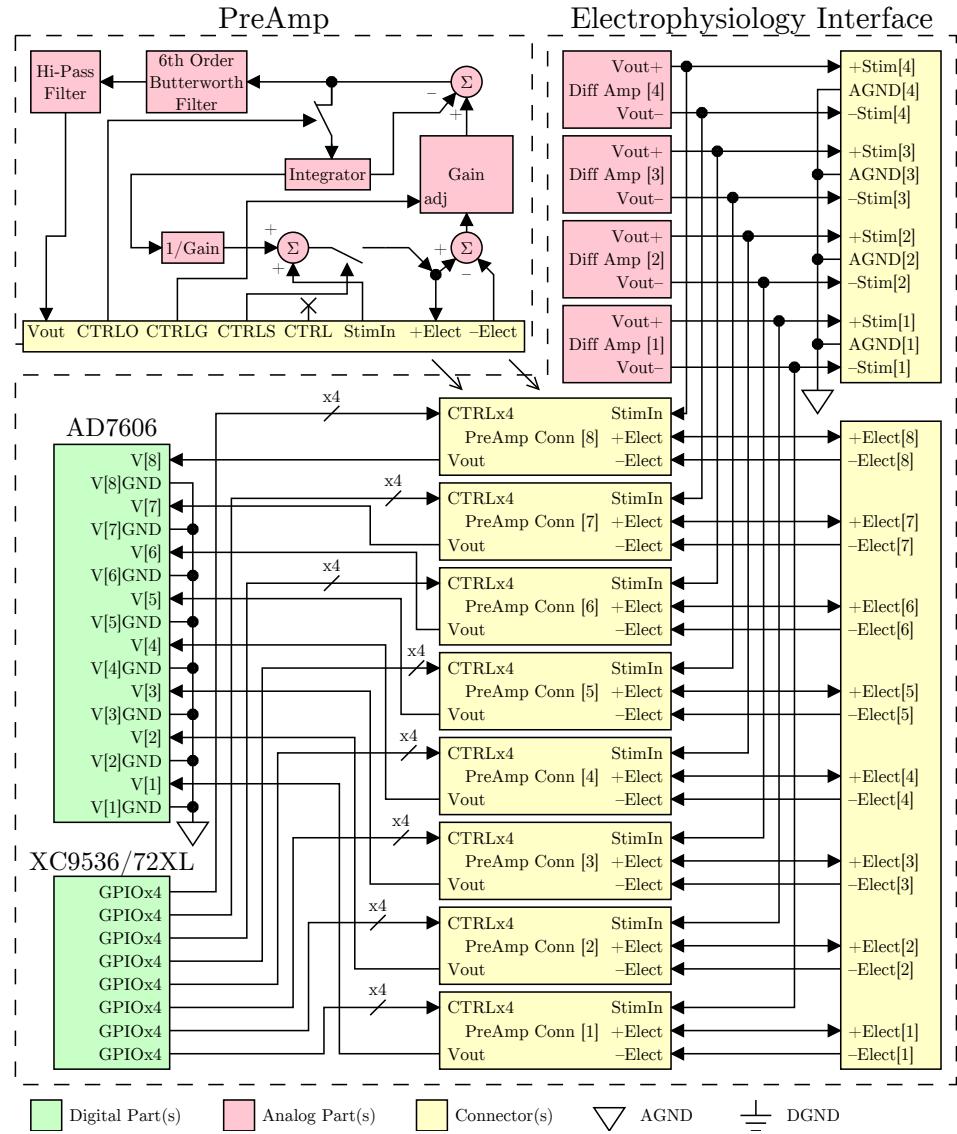


Figure 17: Preamp block diagram [6, 9] and Electrophysiology Interface board connections

an artificial signal to be applied to a biological system.

A summary of the digital signals that control the Preamp stimulation mode is in Table 9. Pull-up and pull-down resistors are included on the Preamp board to default its behavior to measurement mode. Tri-stated outputs may be connected to the Preamp's digital inputs for measurement mode. Additional work may be needed to determine the optimal relative

Signal	Connector Pin	Function
+Elect	B4	Non-inverting input of low-noise instrumentation amplifier
-Elect	B2	Inverting input of low-noise instrumentation amplifier
StimIn	A13	Single-ended stimulation input that can be routed to the non-inverting input
Vout	B13	Single-ended output of the Preamplifier
CTRLO	A15	Digital input controls AC coupling integrator
CTRLS	A16	Digital input controls connecting summing amplifier to non-inverting input
CTRLG	A17	Digital input controls gain of instrumentation amplifier
CTRL	A18	Digital input controls unused analog switch. Included for any future design needs
V+	B10	Positive analog voltage supply for Preamplifier circuits. Connected to +VA supply on Electrophysiology Interface board
V-	B8	Negative analog voltage supply for Preamplifier circuits. Connected to -VA supply on Electrophysiology Interface board
GND	All others	Remaining pins on connector are used to connect to circuit ground. Connected to AGND on Electrophysiology Interface board

Table 8: Preamplifier PCI-Express 36-pin connector signals and pinout

timing of the signals for switching modes [9].

Signal	Measurement	Stimulation
CTRLO	HIGH or tri-state	LOW
CTRLS	LOW or tri-state	HIGH
CTRLG	LOW or tri-state	HIGH
CTRL	X	X

Table 9: Preamplifier digital control for stimulation mode

A summary of how the Electrophysiology Board is connected to the Preamplifier, as shown in Figure 17, is now provided. A terminal block connects the biological system measurement electrodes to the Preamplifier electrode inputs. Differential or single-ended stimulation signals from the four Differential Output Amplifiers may be connected to the biological system using a terminal block, or the single-ended stimulation signals may be routed to the non-inverting

recording electrodes by changing the desired Preamp to stimulation mode. The output of the Preamps are connected to the analog inputs of the AD7606 ADC. Not shown in the figure are  $0\Omega$  resistors that may be used to bypass the Preamp by connecting the non-inverting electrode signal from the terminal block to the input of the ADC (this should only be done when a Preamp board is not in the PCI-Express connector). A  $0\Omega$  resistor can also be used to connect the inverting input of the Preamps to AGND. A Xilinx® XC9572XL CPLD (or the pin-compatible XC9536XL) connects to all of the control inputs of the Preamps.

#### 4.4.5 CPLD

Preamp boards have four digital inputs to set their mode for measurement or stimulation. More experimentation is needed determine optimal relative timing of these inputs [9]. The RTSC must have the ability to uniquely control each Preamp digital input, which means, for eight Preamp boards, a total of 32 external IO pins would be required of the Xilinx® XC3S500E FPGA. The Hirose FX2 connector on the RTSC exposes 40 IO pins, but many of those are needed for the DAC and ADC interfaces. Thus, a CPLD provided on the Electrophysiology Interface board, as shown in Figure 18, can act as an IO expander allowing the FPGA individual control of the four digital inputs on each of the eight Preamps connected to the Electrophysiology Interface board.

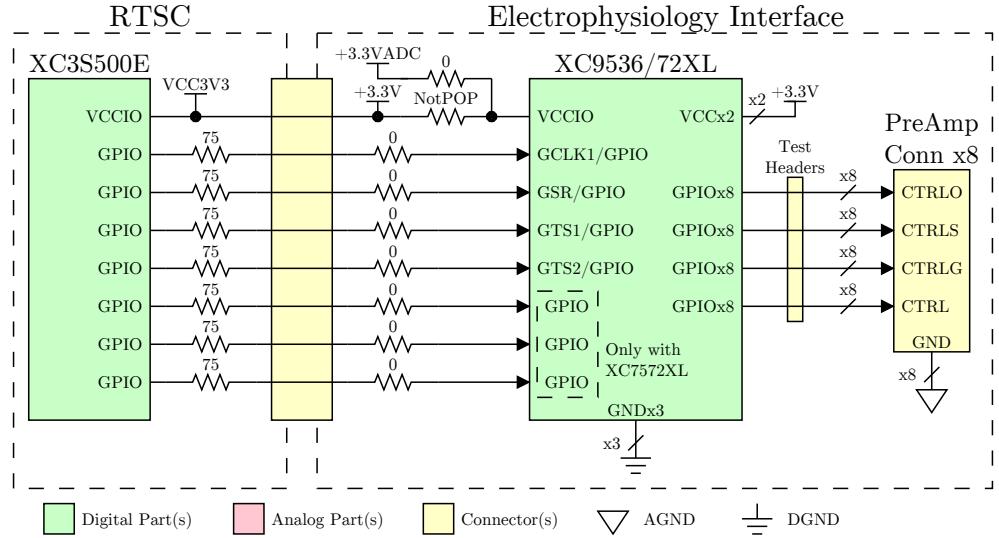


Figure 18: Connections between the FPGA on the RTSC board and the CPLD and Preamp Connectors on the Electrophysiology Interface board

A CPLD solves the problem of scarce IO very well. The configuration of the CPLD can be changed based on the needs of the system as determined by experimentation: it could be configured to simply change all of the IO pins based on a single input, or it could be configured to respond to a complex serial interface with multiple commands and a clock input. The XC9500XL series are Xilinx® CPLD devices that have adequate number of IO pins available, that can be powered with a single 3.3 V voltage supply available on the Electrophysiology Interface board from the RTSC board, that retain their configuration between power cycles, and that use the same tools from Xilinx® and Digilent® for configuration, development, and programming as the FPGA on the RTSC board [42].

The CPLD used must have enough external IO pins to connect to the eight Preamp boards plus a few IO pins for the interface with the FPGA. The DAC and ADC use 33 of the 40 available FPGA IO connections leaving seven IO connections for the FPGA to CPLD interface. Several package options are available for XC9500XL family, but the Quad Flat Pack (xQFP) variations offer the most flexibility in available parts and are relatively easy to solder by hand. The 44-pin VQFP package offers only 34 external IO pins, which, after connecting the Preamp signals, leaves only 2 pins for the FPGA interface, but

the 64-pin VQFP package offers 36 IO pins with the XC9536XL and 52 IO pins with the XC9572XL [43]. Designing the Electrophysiology Interface board for the XC9572XL in the 64-pin VQFP package will allow the XC9536XL to be used in its place for a cheaper price and lower power consumption, if the extra IO and logic gates offered by the XC9572XL are not needed. A summary of the capabilities of the XC9536XL versus the XC9572XL on the Electrophysiology Interface board are shown in Table 10, which has information from [42] and [43].

CPLD	IO Pins	Macrocells	Gates	Preamp Signals	FPGA Signals
XC9536XL	36	36	800	32	4
XC9572XL	52	72	1600	32	7

Table 10: XC9536XL and XC9572XL VQFP-64 capabilities on the Electrophysiology Interface board [42, 43]

Four of the signals from the FPGA are connected to special function pins of the CPLD. These pins provide low-latency operation for the special functions, but may be configured as general purpose IO (GPIO), if the special functions aren't needed.

Test headers provide access to the signals between the CPLD and the Preamp connectors. There are two internal power supply pins, VCC, that are connected to the +3.3 V power rail that is connected to the VCC3V3 power supply on the RTSC board. There is a separate power supply input pin for the IO buffers, VCCIO, that can be connected to +3.3 V or to the output of the 3.3 V regulator on the Electrophysiology Interface board, labeled as +3.3 VADC. VCCIO and VCC can be powered in any sequence without harming the part [43].

The digital inputs on the Preamp boards are connected to an Analog Devices ADG202A quad analog switch IC. Its digital input requirements are compared to the digital output specifications of the XC9536XL and XC9572XL, with VCCIO = 3.3 V, in Table 11, which shows that the CPLD outputs are compatible with the ADG202A inputs [30, 31, 32].

One possible situation that might cause damage to the CPLD when connected to the Preamp Board is the connection of the digital inputs on the Preamp Board to the analog voltage supplies. The XC9536XL and XC9572XL have a maximum rating on its input and

Logic	HIGH	LOW
ADG202A Input	2.4 Vmin	0.8 Vmax
XC9536/72XL Output	2.4 Vmin	0.4 Vmax

Table 11: AD202A quad analog switch and XC9536/72XL CPLD digital input and output compatibility

three-state output pins of 5.5 V [31, 32]. If the Preamp board ties a digital input to its positive analog voltage supply, the voltage on the CPLD pins could exceed their maximum rating. Tieing the digital inputs on the Preamp boards to a HIGH logic level should be accomplished with a voltage divider to ensure that the maximum voltage does not exceed 5.5 V.

## 5 Building the Electrophysiology Interface Board

To create a durable, reliable, and professional-looking implementation of the Data-Acquisition and Stimulation System hardware, it is desirable to have the Electrophysiology Interface board design implemented on a printed circuit board (PCB). To create a PCB, a layout of the circuit design is developed and converted to an industry standard file format that can be submitted to a PCB manufacturer who constructs the PCB. The complexity of the Electrophysiology Interface board circuit design necessitated a four-layer PCB construction, with internal power and ground plane layers that reduce noise emissions and susceptibility while simplifying signal routing and component placement on the top and bottom layers.

Developing the layout of the PCB requires an electronic design automation (EDA) software suite that is capable of working with a complex design implemented on a four-layer PCB and exporting the PCB design to the industry standard Gerber file format. KiCad is an open-source EDA suite that has been in development since 2006; provides schematic capture, PCB layout design, and Gerber file export at no cost; and is available for all popular operating systems. Other EDA suites were evaluated: freeware software suites are often tied to a specific manufacturer with no included Gerber file export capabilities, full-featured

software often has prohibitively expensive licensing fees or evaluation versions suitable for only small designs, and the other popular open-source suite, gEDA, does not have an official Windows binary distribution.

Advanced Circuits is the company that manufactured the Electrophysiology Interface PCB based on Gerber files created using KiCad. The manufacturer was chosen based on its location in the USA, Gerber file acceptance, and attractive student pricing that produces a four-layer board with silkscreen and solder mask for \$66 with no minimum board quantity requirement.

## 5.1 Hierarchical Schematic Capture

The first step in designing a PCB is capturing the entire circuit schematic. A circuit schematic was developed based on the designs for the Electrophysiology Interface board in section 4 and can be seen in appendix A on page 78. The schematic capture program of the KiCad EDA suite, Eeschema, handles complex, multi-sheet schematics with a hierarchical structure.

The root sheet of the schematic on page 79 contains most of the input and output connectors, such as the Hirose FX2 connector, which marries the Electrophysiology Interface board to the RTSC board, and the terminal blocks for connecting to the biological electrodes, allowing the overall signal flow to be summarized on one sheet. To add more sheets to the design, a block is added to the root sheet representing the sheet added to the design hierarchy and referencing a schematic file that defines the contents of the sheet. Figure 19 shows a hierarchical block on the root sheet that adds the sheet, PreAmpInterface, found on page 80, to the design hierarchy with its contents pulled from the file, PreAmpInterface.sch, in the project directory.

Local net labels, such as TCK on the root sheet, connect signals with the same net label without the need to draw a wire but are only valid on the same sheet. Any signal labeled TCK on another sheet will not be connected to the net on the root sheet. To connect signals between sheets, hierarchical labels may be included on the sheet. A hierarchical label, such as CPLD\_TCK on the PreAmpInterface sheet, is similar to a local net label in that its scope

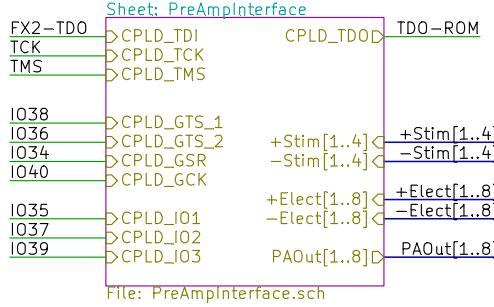


Figure 19: Example of a hierarchical block used to add sheets to the schematic

is only within the sheet but is special in that it can appear on the block symbol for the sheet. Connecting a signal to the label on the block symbol connects the signal to the net designated by the hierarchical label, such as the TCK net on the root sheet connecting to the CPLD\_TCK net on the PreAmpInterface sheet by virtue of the connection of TCK to CPLD\_TCK on the block shown in Figure 19.

Hierarchical blocks can be called from any sheet in the hierarchy, not just the root sheet, which allows for multi-level hierarchies. Figure 20 shows the hierarchical structure of the Electrophysiology Interface board schematic. Most blocks are called from the root sheet with the exception of the PreAmpInterface sheet, which itself calls several blocks.

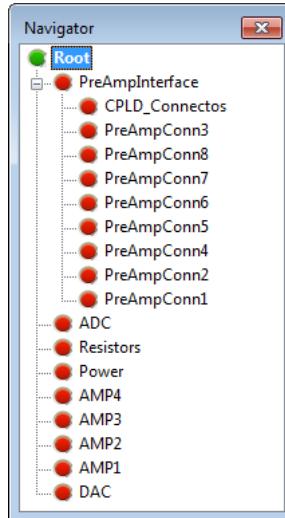


Figure 20: Sheet hierarchy in the Electrophysiology Interface board schematic

One of the advantages of hierarchical blocks is that, when parts of the circuit need to be replicated, such as in the case of the Differential Output Amplifier described in section 4.4.2, only one iteration of the circuit needs to be drawn. Multiple hierarchical block symbols can reference a single schematic file. Any changes to the circuit in one sheet will propagate to the other sheets whose blocks reference the same schematic file. Figure 21 shows how one schematic file is referenced by multiple blocks to allow four Differential Output Amplifier circuit blocks to be included in the schematic while only being drawn once.

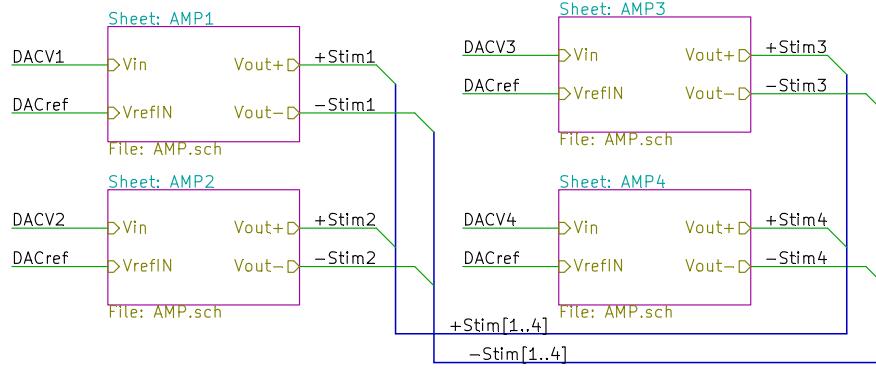


Figure 21: An example of four hierarchical blocks being used to replicate a single circuit design

The sheets AMP4 down to AMP1 on pages 93 to 96 are nearly identical, but it should be noted that the reference designators of the components on each sheet are unique. For instance, the decoupling capacitors on sheet AMP1 are labeled C24 and C25 while the decoupling capacitors on sheet AMP2 are labeled C22 and C23. Changing a reference designator on one sheet will not affect the other sheets, but adding or deleting components or drawing wires on one sheet will propagate to the other sheets.

Multiple component symbols are custom made for the Electrophysiology Interface board. Most are based on symbols from KiCad symbol library and the information contained in the respective parts data sheets. The Preamp PCI-Express connector symbol is based on a library from [44]. All custom component library files are stored in the *lib* directory under the project directory to facilitate project portability between installations of KiCad.

Test points are included for most signals to facilitate rework and voltage measurement,

with the exception of the CPLD and FPGA IO pins and JTAG signals, which are connected to header components.

## 5.2 Component Footprint Selection

The next step in designing the PCB in the KiCad EDA suite is to assign layout footprints to the components included in the schematic with the program CvPcb, which reads the netlist file created by Eeschema. Through-hole footprints are utilized for connectors, protection diodes, and electrolytic capacitors. Surface mount footprints are utilized for all other components to limit footprint size and lead length inductance [34].

Solder mount through-hole footprints with 0.1 in (2.54 mm) spacing are used for connectors with the exception of the Hirose FX2 and PCI-Express connectors. Resistors, ceramic capacitors, and LEDs use standard 0805 package outline footprints as a compromise between choosing a package that minimizes the board space requirement and one that is large enough to be easy to solder by hand. Small-Outline (SO) variations of integrated circuits are preferred when available for the component, and Quad-Flat Package (QFP) variations are used for the 64-pin count components. Test points are implemented with a square pad of plated copper which minimizes required area on the board while allowing a test probe to connect to the signal and provides an acceptable surface for soldering a wire if rework is needed.

Custom footprints not included in the KiCad suite are used for several components and are included in the *lib* directory under the main project directory. The footprints for the Preamp PCI-Express connector and the CPLD are based on libraries from [44], and the footprint for the 100-pin Hirose FX2 connector is based on a library from [45]. The footprint for the 16-pin terminal block for connecting to the recording electrodes was modified with a larger hole size to enable two 8-pin terminal blocks to be used side-by-side [46]. Guide holes were modified to be plated to be compatible with the design constraints of the manufacturer [47]. All component footprints were compared to the recommended PCB footprints in the components' respective data sheets to ensure compatibility.

CvPcb saves the footprint information to the netlist file created by Eeschema. The

name for the footprints of each component can be seen in the *Package* column on the bill of materials in Table 12 in Appendix C.

### 5.3 Layout Overview

The next step in designing a PCB is creating the layout with the program Pcbnew included in the KiCad EDA suite. The following work order is used when designing the layout of the PCB:

**Setup PCB layers** The top and bottom layers are used for signal routing; the inner layer near the top side is used for analog and digital ground planes; and the inner layer near the bottom side is used for analog and digital power planes.

**Setup design constraints** Design rules in Pcbnew are set to comply with the manufacturer design constraints in [47] and [48]. Default trace widths are set to 0.008 in with 0.016 in width for power traces on the signal layers, and to save board area, the via drill size is set to the minimum 0.015 in [47]. Blind and buried vias are not allowed [47].

**Import netlist** Pcbnew imports the netlist file created by Eeschema and CvPcb and places all of the component footprints in the layout window with vector lines representing connections between pins, creating the “rats nest” [49].

**Draw PCB outline** The board outline is drawn as a 4.75 in square, which matches the dimensions of the RTSC board.

**Place connectors** Placement of the Hirose FX2 connector is critical to ensure proper mating with the connector on the RTSC board, and the PCI-Express connectors are placed close to the recording electrode terminal block to keep the trace length short.

**Place remaining components** The remaining components are placed on the top layer with some exceptions for resistors and capacitors. Analog and digital components are placed while being mindful of the need to keep them above the analog and digital ground planes,

respectively, without overlap. Decoupling and Bypass capacitors are placed as close as possible to power pins and connectors, preferring to place the capacitors on the same side as the component.

**Draw ground and power planes** The power and ground planes are drawn on the inner layers in shapes that preserve analog and digital isolation and minimize trace length to the power and ground pins of components. Figures 22 and 23 show the ground and power planes, respectively, of the Electrophysiology Interface board. Care must be taken to ensure that the copper planes maintain the minimum clearance around component and via holes (0.010 in for inner layers) and the PCB edge (0.015 in for inner layers) while also ensuring that the plane is continuous [48]. Figure 24 shows two locations on the power and ground layers where the plane clearance is vital to maintaining continuous planes.

Figure 24a shows where the +VA plane has a through-hole connector occupying the full height of the plane. If the clearance between the plane and the hole features is too large, the plane will not be filled between the holes, disconnecting parts of the plane. Likewise, in Figure 24b, many pins on the two rows closest to the board edge need to connect to the DGND net; a large plane clearance will cut off the pins from the ground plane.

**Route critical signal traces** The signals most susceptible to signal integrity issues should be routed first. These signals include the high-frequency digital signals between the FPGA, ADC, and DAC and the noise susceptible signal from the recording electrodes. The traces should be routed with minimum length, through as few vias as possible, and on the layer adjacent to the ground plane [34].

**Route remaining traces** After the components are placed, ground planes drawn, and susceptible traces routed, the remaining signal traces may be routed. To avoid disfigurement of the trace during the etching process, narrow traces are routed so that they never form a right angle: they first turn  $45^\circ$ , then they extend at least a short distance, and finally they can make another  $45^\circ$  turn [50]. Figure 25 shows the traces and pads on the top and bottom layers of the PCB.

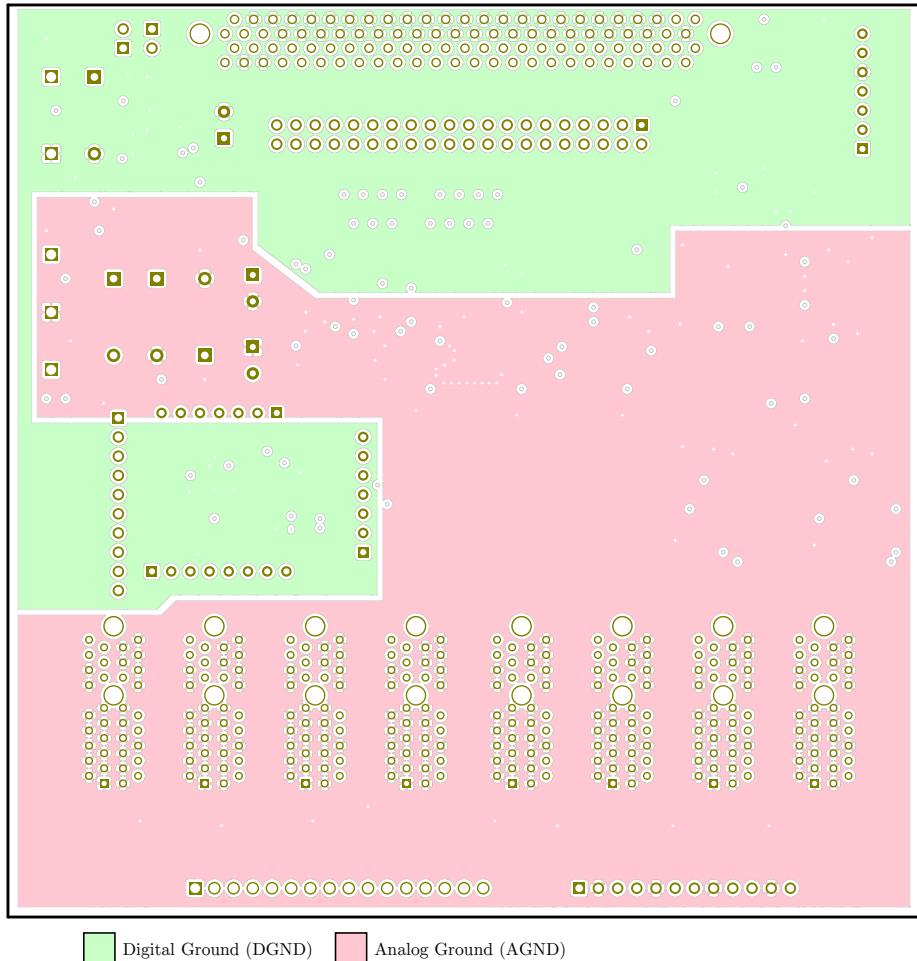


Figure 22: PCB ground plane layer

**Place test points** After the traces are routed is the best time to place the test points on the board. The placement of the test point pads is not critical for the Electrophysiology Interface board, but the size of the pad can interfere with trace routing; thus, the test points can be located last. The test point pads should be placed so as to be accessible after the components are populated.

**Iterate this procedure as needed based on signal routing** To adapt to the challenges encountered during signal routing, it is necessary to adjust ground and power planes, move components, edit component footprints, and change signal connections on the schematic.

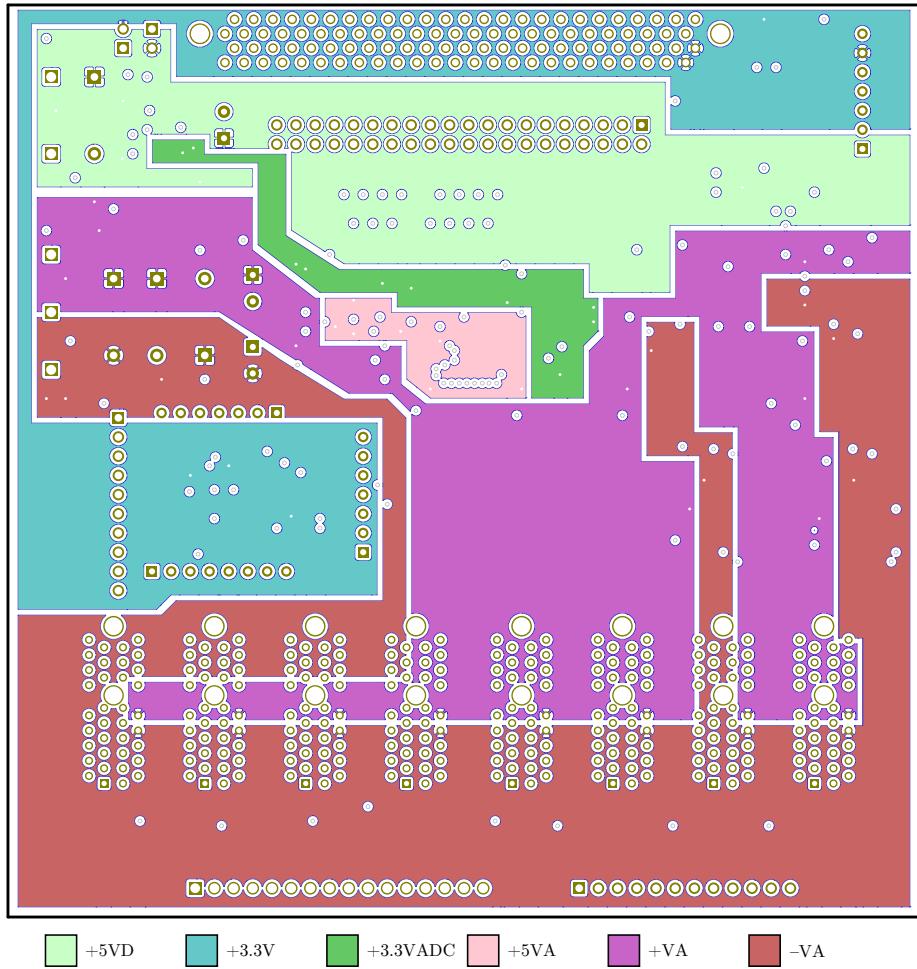


Figure 23: PCB power plane layer

For instance, the CPLD connections to the Preamp connectors are entirely based on the routing needs of the board layout.

**Move labels on the silkscreen layer** Finally, after all the signals are successfully routed, the reference designators for the individual components should be moved so that the labels are visible after the parts are populated on the board, allowing physical parts to be matched to the components in the schematic. Labels should not be located under parts or on top of exposed copper pads.

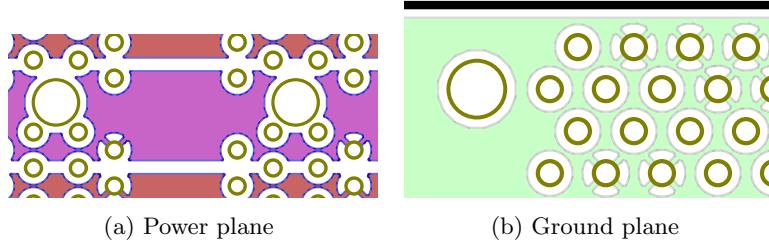


Figure 24: Close clearances on power and ground planes

## 5.4 Manufacturing and Assembly

To produce a PCB, the layout design is transmitted to a manufacturer and a finished PCB is shipped. The standard method of sharing layout design files between the designer and manufacturer is the text-based Gerber and Excellon drill file formats. Still, there are enough variations in file naming, packaging, number format, and drill files that the manufacturer's requirements and EDA suite capabilities need to be carefully scrutinized. Advanced Circuits is capable of receiving Gerber files in the newer 247X format, Excellon drill files, and Gerber FAB files [51, 52, 53]. The company also offers an automated Gerber file review and quoting service that can increase confidence in the successful manufacturing of the PCB design [53]. The procedure for creating the design files required for the Advanced Circuits manufacturing services is elucidated in Appendix B.

A PCB is useless without components with which to populate the board. Table 12 in Appendix C shows the bill of materials required to populate the Electrophysiology Interface board. Components may be ordered from electronics supplier DigiKey®, and the table includes the supplier part numbers and prices as of March 2013. Components for the Electrophysiology Interface board are sourced from DigiKey® along with samples provided by Analog Devices® and Linear Technology®.

After the PCB and components are received, assembly is required. Components are populated by soldering them to the board by hand. Logical circuit blocks, as defined in the subsections of section 4, are populated together while constantly testing for unintended short and open circuit conditions by using a resistance meter and by powering the board

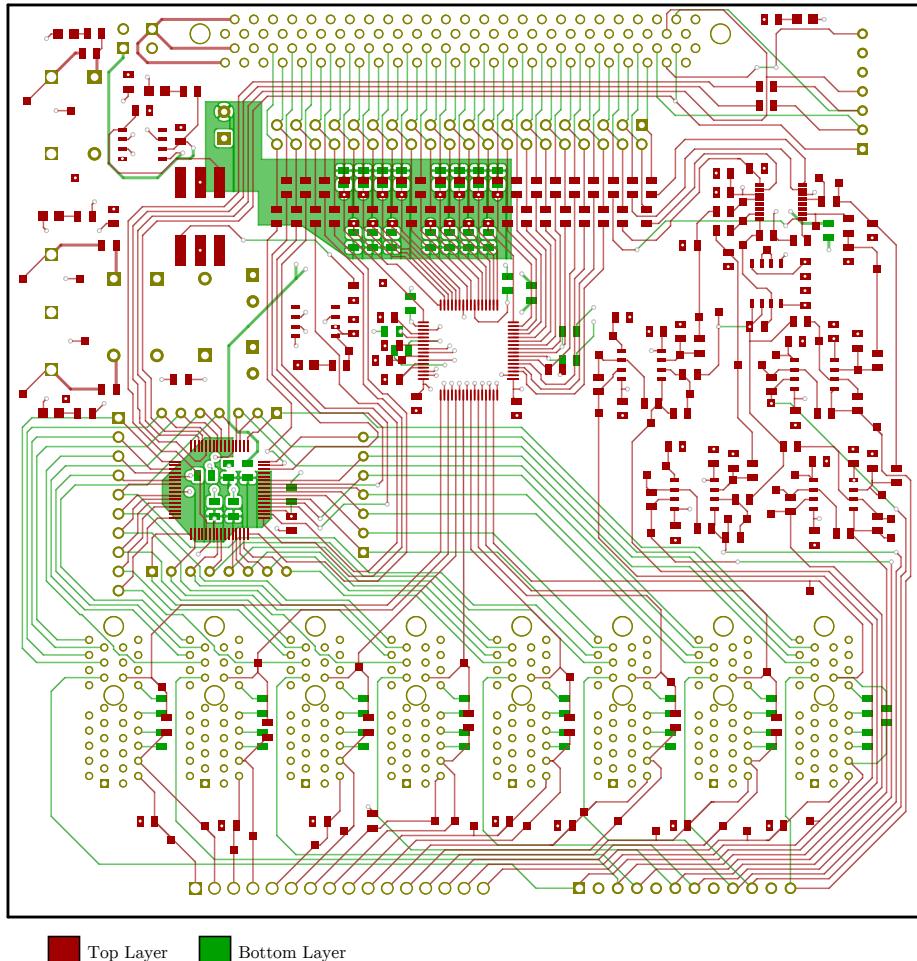


Figure 25: PCB top and bottom signal layers

after each logical block is populated. Soldering the most difficult components of the logical block first, such as ICs, is a good strategy to allow the best possible access to the hard to see and reach pins. Pictures of the assembled Electrophysiology Interface board can be seen in Figures 26 and 27.

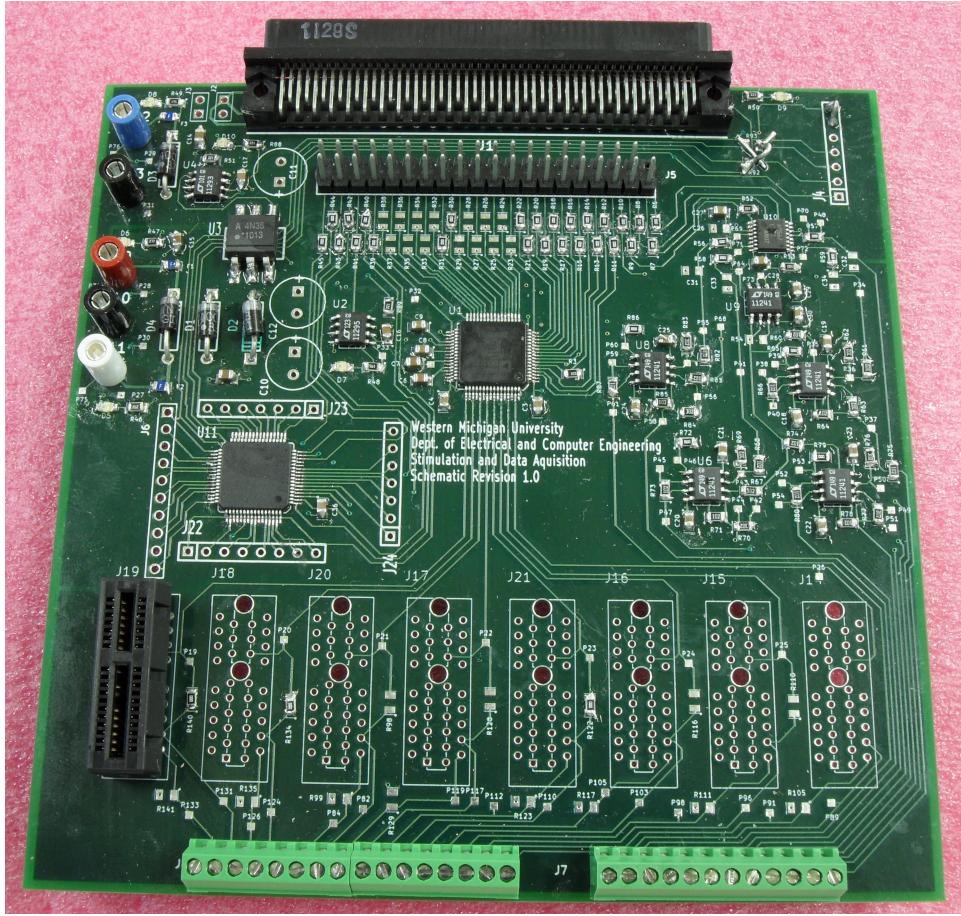


Figure 26: View of the top side of the populated Electrophysiology Interface board

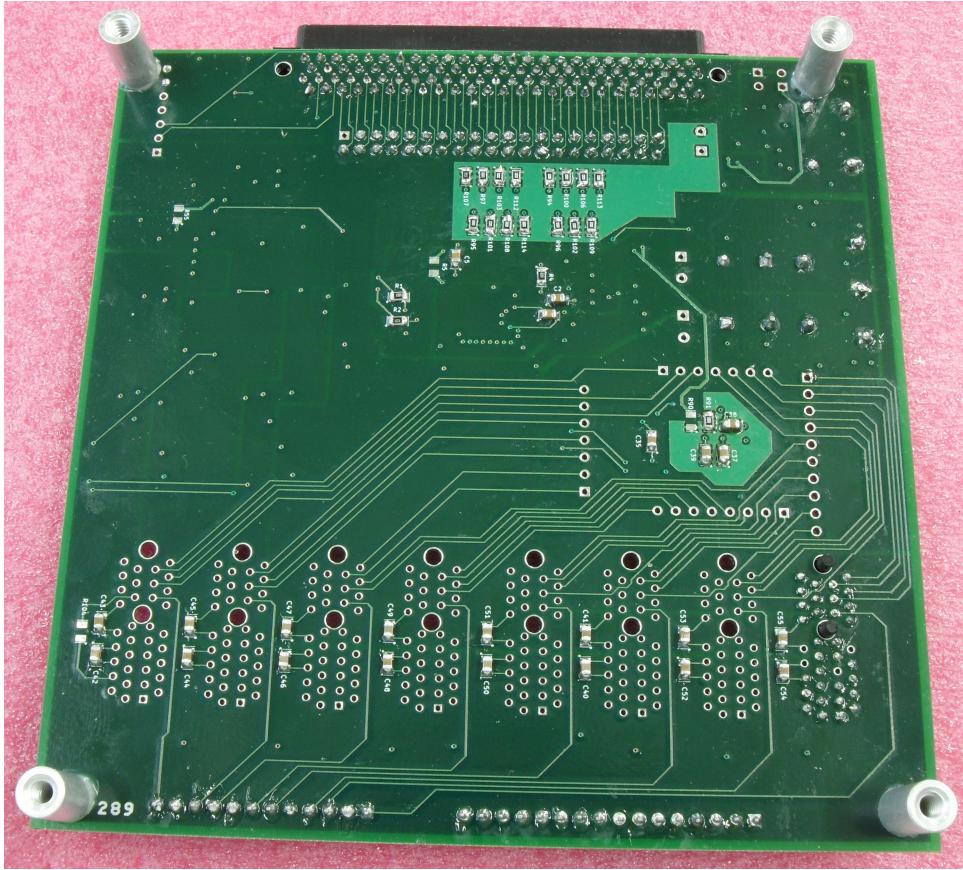


Figure 27: View of the bottom side of the populated Electrophysiology Interface board

## 6 Electrophysiology Application<sup>4</sup>

To validate the stimulation and data acquisition system design, a standard electrophysiology experiment, described in [12, 13, 14], was performed on earthworm giant axon action potentials, henceforth referred to as the Earthworm Experiment. This serves the purpose of showing that the Data Acquisition and Stimulation System is capable of being used in an electrophysiology experiment, and the procedure has been performed with previous designs, allowing the new design to be compared with previous results [9].

In the earthworm's nerve cord, there is a median giant axon and two smaller lateral giant

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<sup>4</sup>This section is co-authored with Kyle Batzer, [15].

axons on either side of the median axon. The lateral giants are connected to each other at multiple locations along the length of the earthworm which has the effect of lateral axons acting as a single giant axon [12]. A physical or electrical stimulation near the anterior or posterior ends of the earthworm will elicit a response from the earthworm in the form of an action potential that propagates along one or both of the giant axons. The propagation speed is related to the cross sectional area of the axon [13]. Varying the intensity of the electrical stimulation at the anterior end of the earthworm will show no response at low intensity, an action potential along the median axon soon after the stimulation at medium intensity, and at a higher intensity, action potentials along both the median and lateral giant axons will be visible with the median response occurring sooner than the lateral response due to the differing propagation speeds. Figure 28 shows a cross section of an earthworm based on a figure in [18] with a more detailed representation of the nerve cord based on [13].

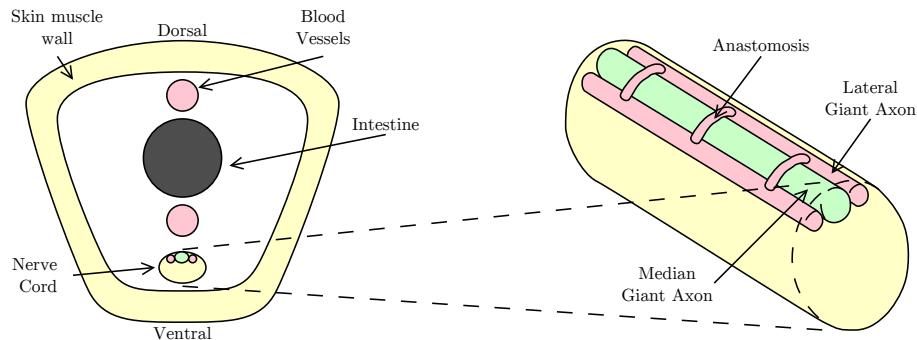


Figure 28: Cross section of an earthworm adapted from [13, 18]

Electrical stimulation is accomplished by placing two pins near the anterior end of the earthworm. Measurement of the action potentials along the axon is accomplished by dissecting the earthworm and placing two chlorided silver extracellular electrodes on the earthworm nerve cord. The extracellular electrodes measure the difference in electric potential at two points on the nerve cord. When an action potential propagates along the nerve cord, the electrodes measure a difference in voltage in time that will appear as a biphasic spike. The exact shape of the spike will depend on the placement and size of the electrodes and the

condition of the nerve cord itself [12, 13, 54].

The Data Acquisition and Stimulation System was used to perform an experiment studying earthworm giant axon action potentials with a previously developed and validated amplifier [9] and oscilloscope connected in parallel with the electrophysiology interface board, allowing the data to be compared.

## 6.1 Earthworm Setup

The dissection of the earthworm and setup of the stimulation and recording hardware is based on [12, 13, 9]. Two pins are placed near the anterior end of the earthworm. Connected to these pins is the output of the stimulation circuitry. Near the middle of the earthworm, the skin is cut and folded to expose the interior of the worm. The intestine is moved out of the way, and the nerve cord is pulled away from the fluids with two chlorided silver electrodes that are connected to the amplification and recording circuitry. Between the stimulation pins and recording electrodes, a chlorided silver wire is placed under the body of the earthworm and connected to circuit ground, which may be connected to earth ground depending on the circuit setup. Figure 29 is a diagram of the DASS connected to the earthworm

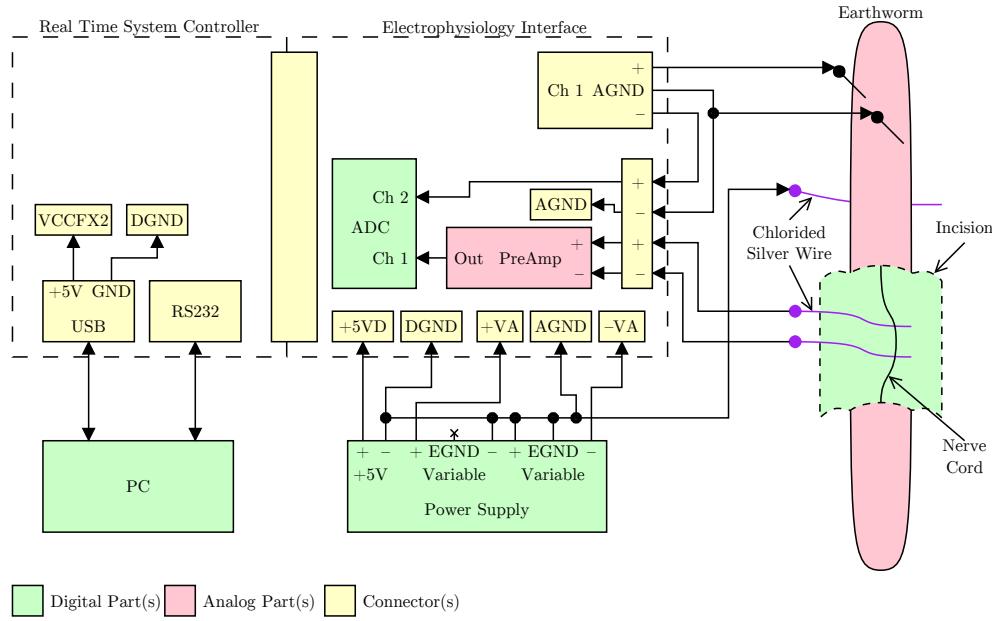


Figure 29: Diagram showing connections between the Data Acquisition and Stimulation System and an earthworm, connections to earthworm follow [12, 13]

To compare the Data Acquisition and Stimulation System with a previously validated setup, the Preamp from [9, 10], with its output connected to an oscilloscope, has its input connected in parallel with the recording electrodes as shown in Figure 30.

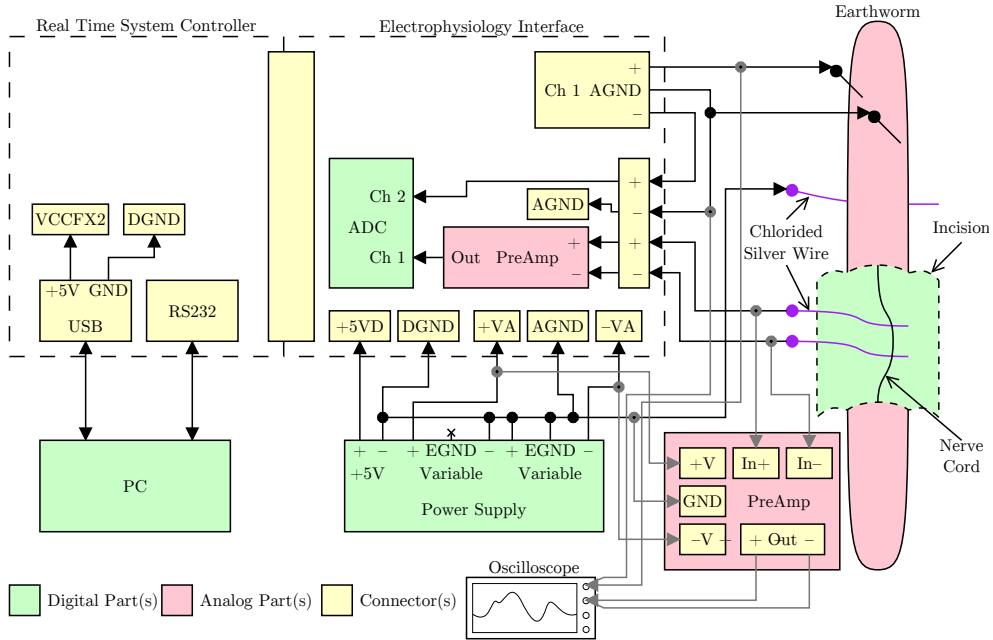


Figure 30: Diagram of the Data Acquisition and Stimulation System connected in parallel with a previously validated recording system, connections to the earthworm follow [12, 13] and connections to the standalone Preamp and oscilloscope follow [9]

## 6.2 Chloriding Silver Wire

The silver wire used for the extracellular electrodes must be coated in a layer of silver chloride. To create the coating, electroplating may be used as described in [13, 55]. A simpler method is to place the portion of the wire that will be in contact with living tissue in full-strength Clorox® bleach and leave the wire in the bleach until the wire acquires a purplish-gray tint, which should take between ten and thirty minutes [55].

## 6.3 Earthworm Experiment Procedure

The Earthworm Experiment procedure is adapted from [12, 13].

### 6.3.1 Earthworm Dissection

- Place the earthworm in a 10% ethanol solution to anesthetize it

- Leave the worm in the ethanol solution for the minimum amount of time needed to make the worm easy to work with while dissecting it; 5-10 minutes may be all that is necessary
- Rinse the earthworm in tap water and pin it, dorsal (dark) side up, on the dissecting dish
- Create a capital-letter-I shaped incision, using surgical scissors, one to two inches long, along the length of the worm, about halfway between the anterior and posterior ends of the earthworm
- Pin the skin to the dissecting dish to expose the worm internal anatomy
- Flush the cavity periodically, as needed, with worm Ringer's solution (in mM units: 102.7 NaCl, 1.6 KCl, 1.8 CaCl<sub>2</sub>, and 4 NaHCO<sub>3</sub> [13]) to make the anatomy easier to view
- Move the intestine aside, using forceps and scissors, exposing the nerve cord
- Free a few centimeters of the nerve cord from its lateral and ventral connections, using the forceps and scissors, to allow the cord to be lifted above and away from the saline and other anatomy
- Position the chlorided silver wires under the nerve cord
- Raise the fixture holding the silver wires until the wires and nerve cord are away from the saline and earthworm anatomy (a fraction of an inch is all that is necessary, blowing in the area can break up the surface tension if the saline solution is bridging the wires and cord with the rest of the earthworm)
- Moisten the nerve cord with Ringer's solution, often, throughout the experiment while making sure that the nerve cord and electrodes remain isolated from the rest of the saline and anatomy (it may be necessary to remove excess Ringer's solution)

### **6.3.2 Electrical Setup**

- Place two pins near each other in the anterior end of the earthworm
- Connect the non-inverting output of the stimulation circuit to one pin and connect circuit ground or the inverting output to the second pin
- Connect, optionally, if the inverting output is not connected to a pin in the earthworm, the inverting output of the stimulation circuit to an unused electrode input channel on the Electrophysiology Interface board; ensure that there is no Preamp board in the PCI-Express socket and bypass the socket with a  $0\Omega$  resistor. See Figures 29 and 30
- Place a chlorided silver wire under the body of the earthworm, between the stimulation pins and the exposed portion of the earthworm's body and connect the wire to circuit (which may be earth) ground
- Connect the chlorided silver recording electrodes to the Preamp inputs with the non-inverting input connected toward the anterior end of the earthworm and the inverting input connector toward the posterior end (reversing the electrodes will simply invert the signal) (connecting the electrodes may be performed before the silver wires are placed under the nerve cord, to avoid disturbing the electrodes in the process of making the connections)
- Power on the Electrophysiology Interface, first, then power on the RTSC

### **6.3.3 Software Setup**

- Update FPGA program as described in [15]
- Update Cypress EZ-USB firmware as described in [15]
- Create the script and corresponding waveform file as shown in [15]
- Launch Data Acquisition and Stimulation Control Center (DASCC)
- Select the appropriate COM port from the dropdown list

- Select the appropriate Endpoint from the dropdown list, set Packets Per Xfer to 64, and set Xfers to Queue to 64
- Select the Scripting tab and load the Earthworm Script as described in [15]
- When prepared for single stimulus and capture click the “Run Script” button. Changes to the output pulse amplitude can be accomplished by changing the 2nd line of the Waveform file as shown in [15]
- Graph data by selecting the Graphing tab and clicking the “Load File” button. Once loaded, multiple channels can be displayed at the same time using ctrl + left mouse button to select/deselect channels.
- Click “Output CSV” to export data to a comma-separated values (CSV) text file

#### **6.3.4 Stimulation and Recording**

- Stimulate the earthworm with a single, 0.2 ms wide pulse with low amplitude (less than 1.0 V)
- Repeat the stimulation while slowly increasing the pulse amplitude (in steps between 0.1 V and 0.5 V) until a response is seen between 2 ms and 8 ms after the stimulation artifact, this is the median giant response
- Save the recorded waveform
- Slowly increase the pulse amplitude, further, until a second response is seen between 6 ms and 15 ms after the stimulation artifact, this is the lateral giant response
- Save the recorded waveform

## **6.4 Results**

The Earthworm Experiment was performed with the Data Acquisition and Stimulation System connected in parallel with a preamp and oscilloscope that was validated in [9]. A

diagram of the experimental setup is shown in Figure 30. A picture of the experimental setup is shown in Figure 31.

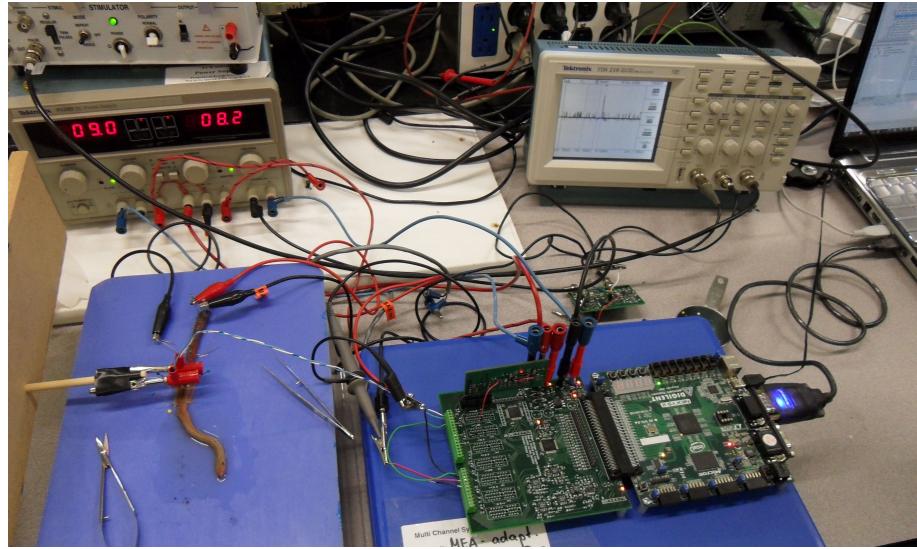


Figure 31: The Data Acquisition and Stimulation System connected in parallel with a previously validated recording system

Data recorded from a 2.0 V stimulation pulse produced a median giant response similar to those seen in [9] and [14]. Data from the previously validated Preamp and the oscilloscope was plotted on top of the data from the Data Acquisition and Stimulation System using a GNU Octave script. Data from the oscilloscope and the Data Acquisition and Stimulation System can be seen in Figure 32 and the data appears to be in very close agreement.

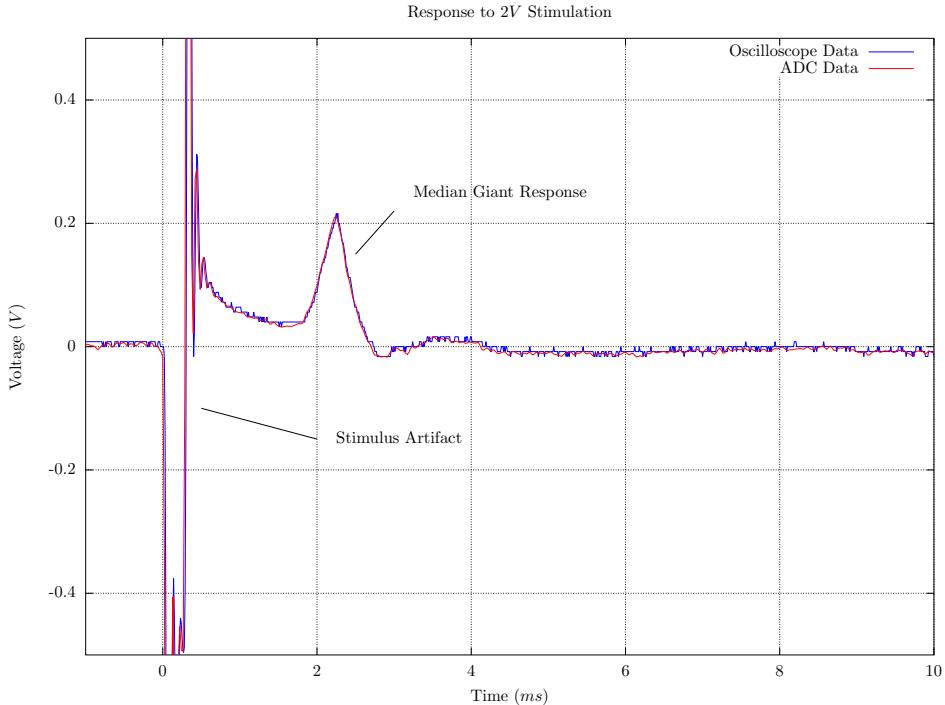


Figure 32: Earthworm response to 2.0 V stimulation pulse generated by the Data Acquisition and Stimulation System with data recorded by the oscilloscope and by the ADC on the Data Acquisition and Stimulation System

Data recorded from a 3.5 V stimulation pulse produced median and lateral giant responses similar to those seen in [9] and [14]. The data shown in Figure 33 exhibits close agreement between the Data Acquisition and Stimulation System and the previously validated Preamp.

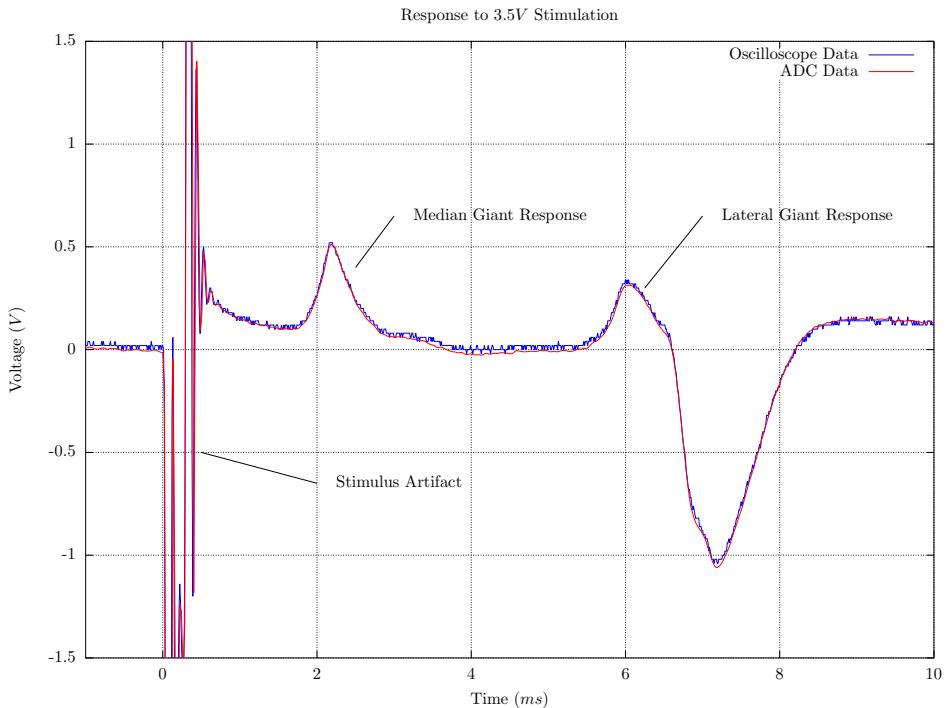


Figure 33: Earthworm response to 3.5 V stimulation pulse generated by the Data Acquisition and Stimulation System with data recorded by the oscilloscope and by the ADC on the Data Acquisition and Stimulation System

## 7 Specifications Review<sup>5</sup>

This section reviews the specifications set forth in section 2 and shows how well the Data Acquisition and Stimulation System described in this thesis meets those specifications.

1. Provide a platform for performing electrophysiology experiments with earthworms as described in [12, 13]

Successful accomplishment of the earthworm experiment is shown in section 6.4.

- (a) Produce a voltage-controlled stimulation pulse that is a square wave with widths from 0.01ms to 100ms and amplitudes from 0.1V to 10V

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<sup>5</sup>This section is co-authored with Kyle Batzer, [15]

The FPGA and Data Acquisition and Stimulation System Control Center (DASCC) are capable of defining a stimulation waveform that updates the DAC output with a period as short as  $1\ \mu s$  and storing up to 4096 waveform samples with variable sample periods from  $1\ \mu s$  to 65.536ms [15]. The DAC has a slew rates of  $1.5\ V/\ \mu s$  [27] and a differential output voltage range of  $\pm 14.8\ V$  as shown in section 4.4.2.

- (b) Produce single stimulation pulses or multiple pulses at rates from 1Hz to 10Hz

The FPGA and DASCC are capable of defining a stimulation waveform over 1s in length and repeating the waveform indefinitely [15].

- (c) Provide at least one differential recording channel

There is the potential for up to eight recording channels, each with a Preamplifier that has a differential input as shown in section 4.4.4.

- (d) Record action potential voltage from the time of the stimulation pulse for a minimum duration of 20ms

Data collected for results in section 6.4 is more than 1s in duration.

- (e) Plot the recorded voltage

The DASCC is capable of plotting recorded data [15].

- (f) Store the recorded voltage to a non-proprietary, standard file format

The DASCC is capable of exporting recorded data to a comma separated values (CSV) text file [15].

2. Provide a platform for stimulation and recording of neuron cell cultures in a portion of an MEA

Interfacing the DASS with the MEA is not yet tested

- (a) Provide at least four recording channels

Eight recording electrodes can be connected to the DASS and stored as digital samples as described in sections 4.4.3 and 4.4.4.

- (b) Store data from recording channels continuously

The data recording time limit has not been fully tested.

- (c) Provide at least four voltage-controlled arbitrary stimulation channels

The DASCC is capable of loading an arbitrary waveform as defined by a text file into the DASS, which outputs the waveform using the AD5678 with four DAC outputs shown in section 4.4.1 [15]

- (d) Output single-ended stimulation signals on recording electrodes and add culture voltage offset to the signal

The stimulation signals are routed to the Preamp boards which output the stimulation signals on the recording electrodes and add the culture voltage offset as described in section 4.4.4

- (e) Provide an interface that can specify stimulation waveforms, locations, and intervals that can be updated based on data from the recording electrodes

The DASCC provides a scripting language for defining recording intervals, stimulation waveforms, and stimulation intervals but does not have provisions for analyzing recorded data and adjusting stimulation strategy [15]

### 3. Utilize Low-Noise Amplifier described in [9]

The Low-Noise Amplifier, also known as the Preamp, is successfully utilized with the DASS; though, not all features are tested.

- (a) Connect to each Low-Noise Amplifier channel with a PCI-Express card edge connector

Eight PCI-Express card edge connector sockets are available on the Electrophysiology Interface board as described in section 4.4.4

- (b) Provide  $\pm 7\text{ V}$  to  $\pm 15\text{ V}$  analog voltage supplies and ground via the card edge connector

The Electrophysiology Interface board connects its analog voltage supply inputs, which tolerate  $\pm 7\text{ V}$  to  $\pm 15\text{ V}$ , to the Preamp connectors as described in sections 4.1

and 4.4.4.

- (c) Provide ability to independently switch four digital inputs for each channel,  $0_{IH} = 0.8\text{ V}$  and  $1_{IL} = 2.4\text{ V}$

The CPLD on the Electrophysiology Interface board enables the FPGA to control each digital input on every Preamplifier channel and voltage compatibility is shown in section 4.4.5, but a logic configuration for the CPLD is not written.

- (d) Route differential analog input to the card edge connector for each channel

The differential inputs of the Preamplifiers are routed to a terminal block for simple connection to recording electrodes as described in section 4.4.4.

- (e) Convert the 20Hz to 14.6kHz analog output signal [9] to digital samples

An AD7606 ADC converts the Preamplifier output voltage to digital samples, has an analog low-pass input filter with a corner frequency of 23kHz, and can sample at up to 200kS/s, satisfying the sampling theorem, as described in section 4.4.3

- (f) Route a single-ended stimulation signal to each channel

Four unique stimulation channels with differential outputs are connected single-endedly to the eight Preamplifier connectors as described in section 4.4.4.

#### 4. Additional requirements

- (a) Employ good circuit design and layout practices

Good design and layout practice is attempted throughout the design of the Electrophysiology Interface board and in connecting all the components of the DASS. For example, bulk and decoupling capacitors are utilized, four-layer PCB construction is used, and analog and digital power supply isolation is attempted. Although, there may be better strategies for analog and digital isolation than was used in the design of the Electrophysiology Interface board and some of those strategies are discussed in section 4.1.4.

## 8 Scaling the DASS Hardware to 60 Channels

Experiments with cultured neurons on an MEA requires the ability to stimulate and record on all 60 electrodes of the MEA. The developed Data Acquisition and Stimulation System (DASS) only has the capability of recording data on eight electrodes and outputting four unique stimulation waveforms on those electrodes. A 60-channel system could be developed by testing and refining, as needed, the hardware and software design principles used by the DASS on a portion of a MEA. Figure 34 shows one possible incarnation of the hardware for a system capable of stimulating and recording with up to 64 electrodes, which is four more channels than necessary for a 60 electrode MEA.

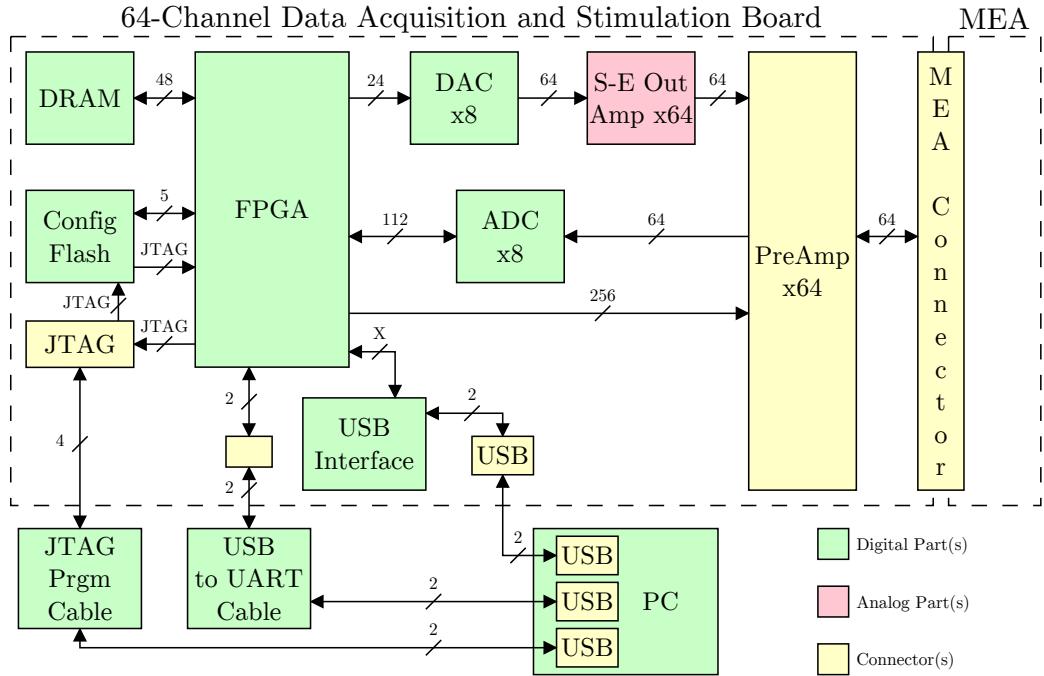


Figure 34: Block diagram of a proposed 64-channel system based on the RTSC board and Electrophysiology Interface board design

The proposed system expands on the circuit designs of the DASS. A custom PCB connects to the MEA and has a PCI-Express card edge connector socket to interface a PreAmp board to each electrode on the MEA. The PreAmp voltage output is recorded by eight AD7606 eight-channel ADC components. Eight AD5678 components contain four 16-bit

DACs and four 12-bit DACs each for a total of 64 DAC outputs, and analog amplification circuitry conditions the DAC outputs, providing 64 single-ended stimulation signals to the Preamplifier boards. An FPGA on a custom board offers many more IO pins than are available on most development kits; thus, there are likely to be enough IO pins to control the four digital inputs of each PreAmp board without the need for a CPLD for IO expansion.

The FPGA controls the eight AD7606 ADCs and eight AD5678 DACs. External RAM memory is likely needed to store stimulation waveform data. A configuration flash memory chip loads the FPGA configuration upon power-up. A JTAG programming cable eliminates the need for custom microcontroller firmware to load FPGA configurations into the FPGA or configuration flash memory. A USB to UART cable allows commands to be communicated to the FPGA from the PC with minimal circuitry on the PCB. And, a microcontroller with a USB PHY allows for fast data transfer of electrode recordings to the PC.

Information that could be acquired by testing this design with the DASS include: confirming whether 12 bits of DAC resolution is sufficient for MEA experiments, determining optimal timing of PreAmp digital control signals, determining which control signals for the ADC and DAC need to be controlled by the FPGA and which can be permanently tied to a logic level, testing data throughput for the USB interface, and, if data transfer speed is found to be insufficient, testing alternative USB2 or USB3 capable microcontrollers. One area that will need to be tested outside of the current embodiment of the DASS is PCB assembly with ball grid array (BGA) packages: the number of IO pins and logic gates required by a 64-channel system will necessitate the use of a BGA packaged FPGA.

## 9 Conclusions

The work of many students in the Neurobiology Engineering Laboratory at Western Michigan University made the completion of the Data Acquisition and Stimulation System (DASS) possible. Utilizing the documentation and knowledge gained from previous groups [4, 5, 8, 9, 10] and the concurrent efforts of fellow graduate student, Mr. Kyle Batzer [15], a custom multi-channel data acquisition and stimulation system has been developed.

oped for use in electrophysiology experiments at the Neurobiology Engineering Laboratory. Validation of the system by performing a standard electrophysiology experiment was, again, aided by the experience of students' previous design projects [9, 14].

Designing hardware for a mixed digital and analog system can be a challenge. Being able to refer to previous work reduces design time and risk. Thorough documentation in this thesis also reduces risk and aides in the subsequent use of the system. A PCB can be an expensive investment (see appendix C), and the utilization of headers and  $0\Omega$  resistors in the design of the Electrophysiology Interface board allows the few layout mistakes to be rectified, as shown in appendix D.

Application of the DASS by future students in electrophysiology experiments will require knowledge of electrical engineering. The hardware, even though it does contain some protection circuitry, can be damaged by misapplication of power or incorrect connection of inputs and outputs. The documentation in this thesis will make understanding the DASS attainable for an electrical engineering student who devotes a month or two to part-time study of the system. The documentation can also be used for a future project that would implement a system, described in section 8, with enough channels to fully exploit an Microelectrode Array (MEA) with 60 electrodes. Such a project may be too ambitious for a senior design group or graduate student to complete alone in one year, but a senior design group or graduate student that has experience working with the DASS on electrophysiology experiments before beginning such a project could realize a working 60 channel data acquisition and stimulation system.

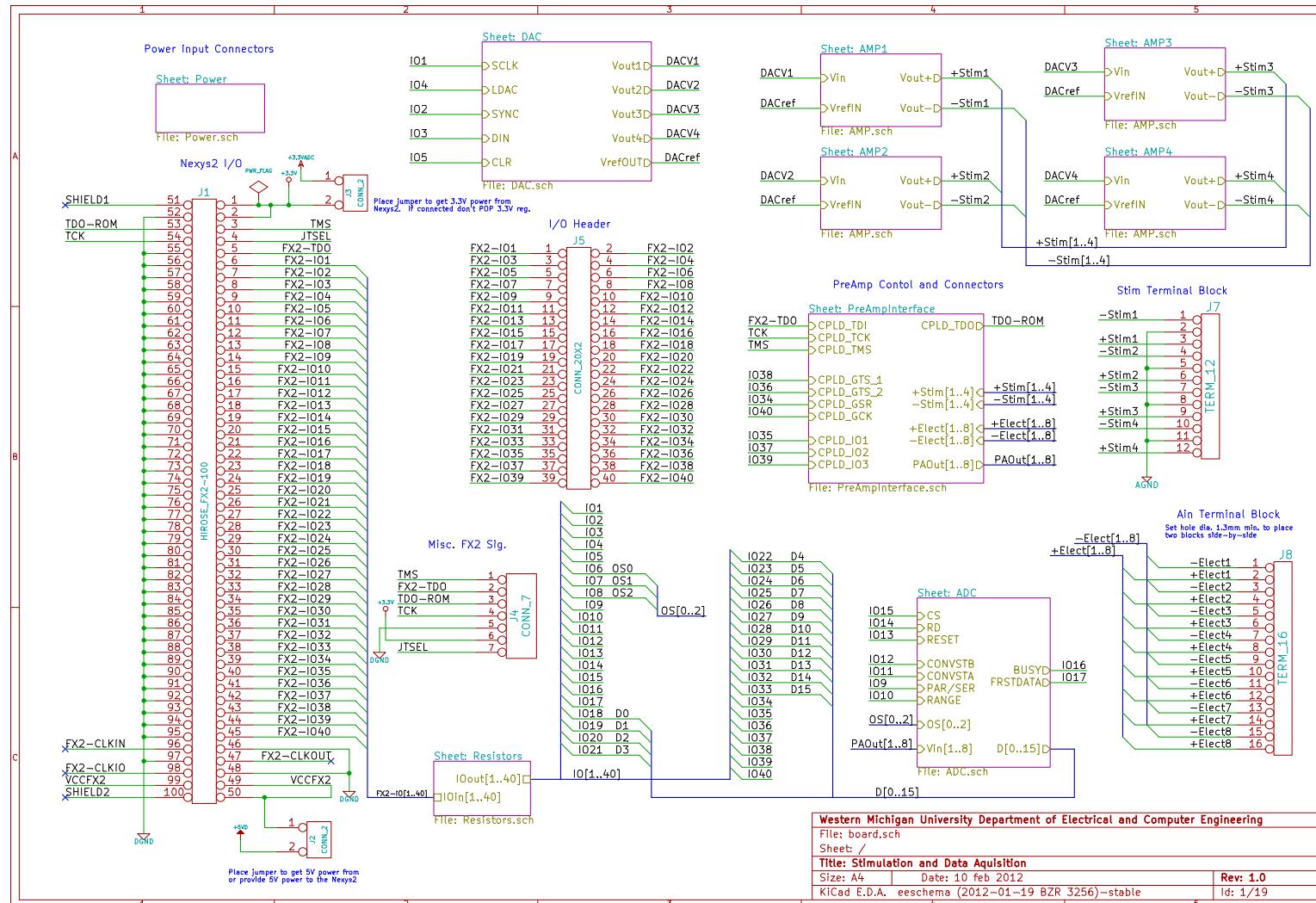
Personally, I broadened my knowledge of electronic circuit design in creating the Electrophysiology Interface board for the DASS, gained experience collaborating with a talented firmware and software designer, explored another field by learning enough neurophysiology to perform and design hardware for electrophysiology experiments, and gained confidence in my circuit and PCB design skills by having a PCB manufactured that was used successfully in an electrophysiology experiment.

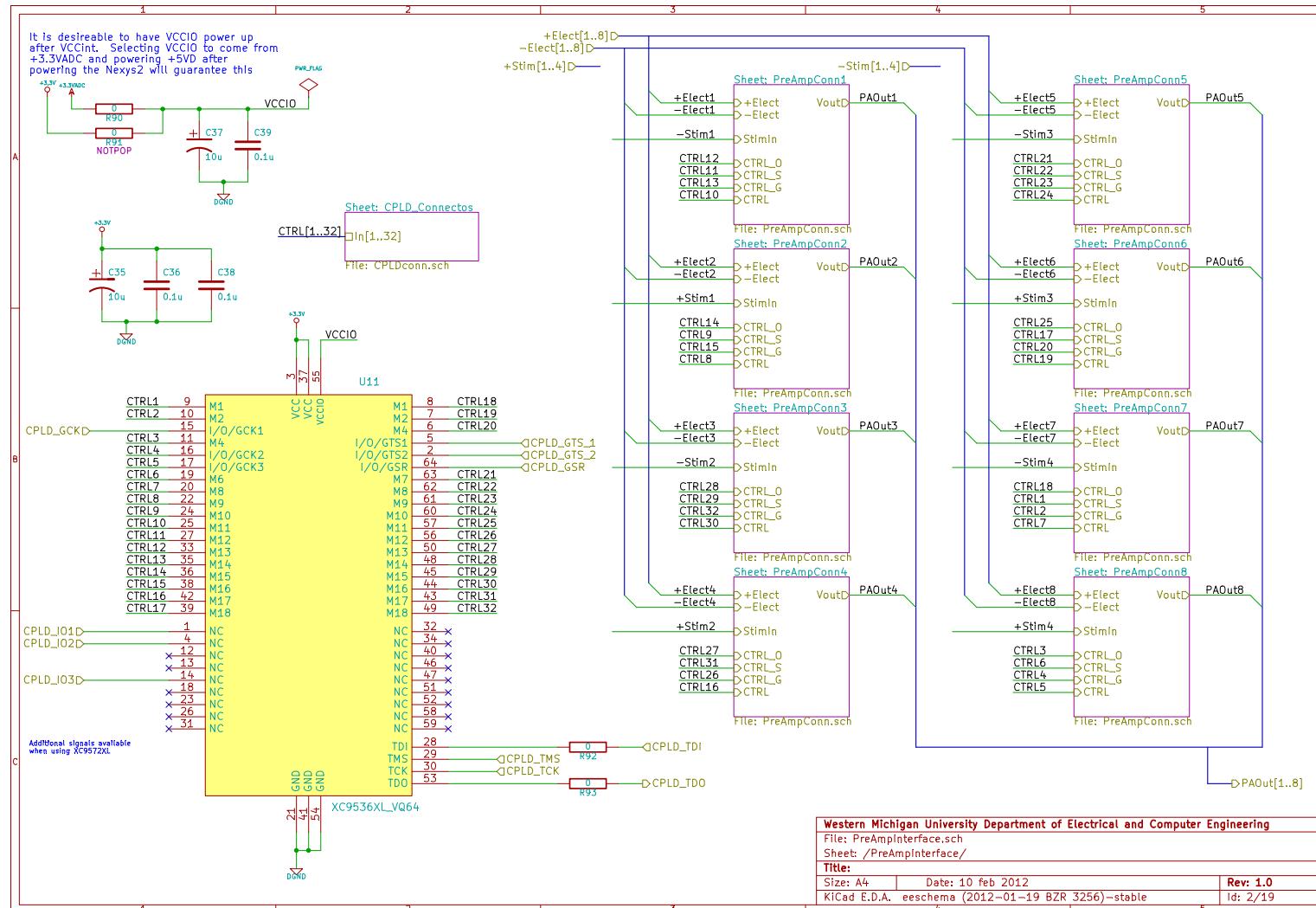
# Appendices

## A Electrophysiology Interface Board Schematic

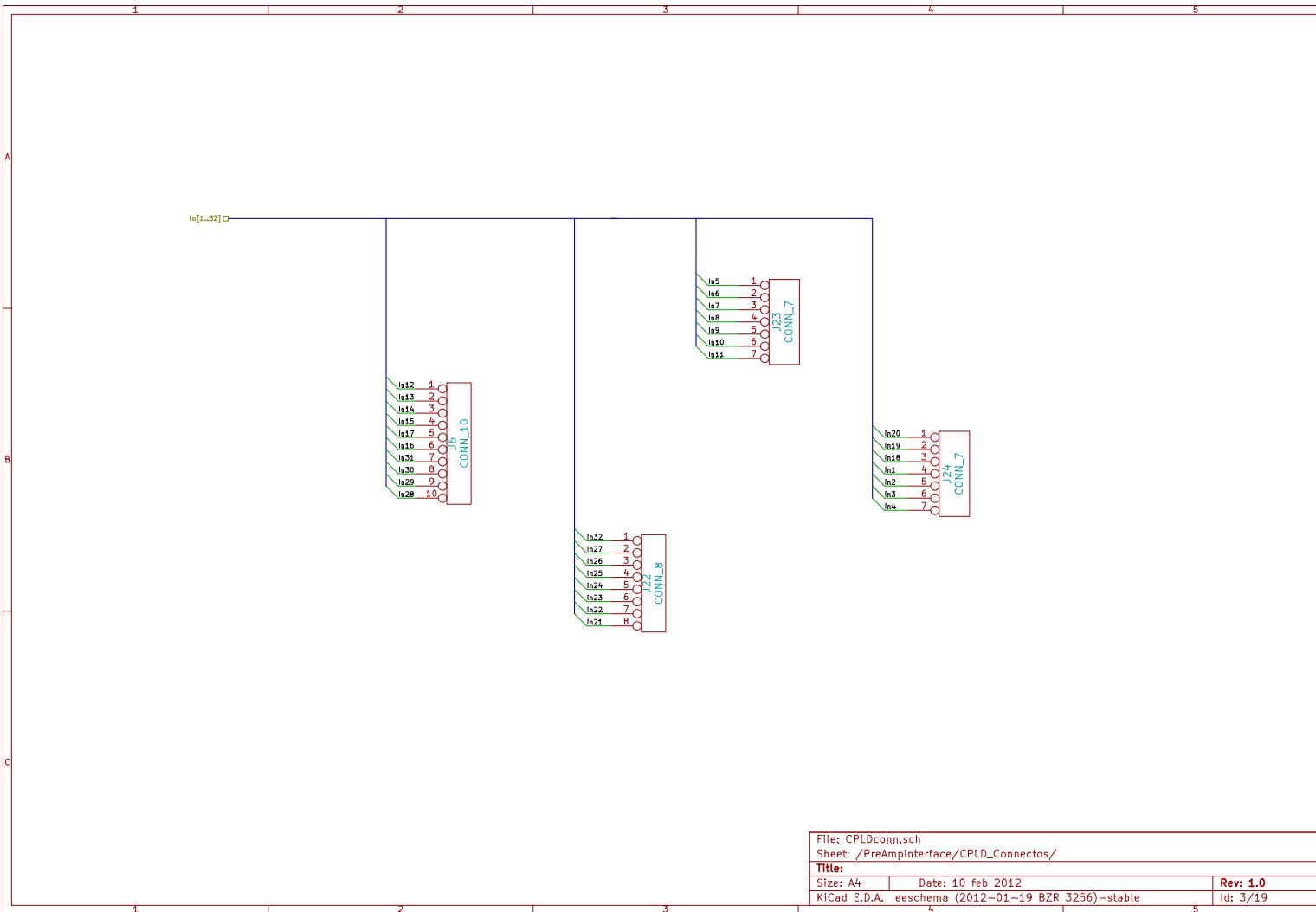
The following is the hierarchical schematic for the Electrophysiology Interface Board. The schematic was created using the KiCAD open source EDA software suite.

The first page of the schematic contains most of the connectors on the Electrophysiology Interface Board. Hierarchical blocks in the first schematic page represent following schematic pages with labels on the blocks corresponding to net names in the schematic page represented by the block. All signals have a scope only within a single schematic page save for the power supply nets, which have a global scope. The power supply input connectors are shown on page 92, and since the power nets are global, the hierarchical block on page 79 representing power input connector page, page 92, is empty of labels.

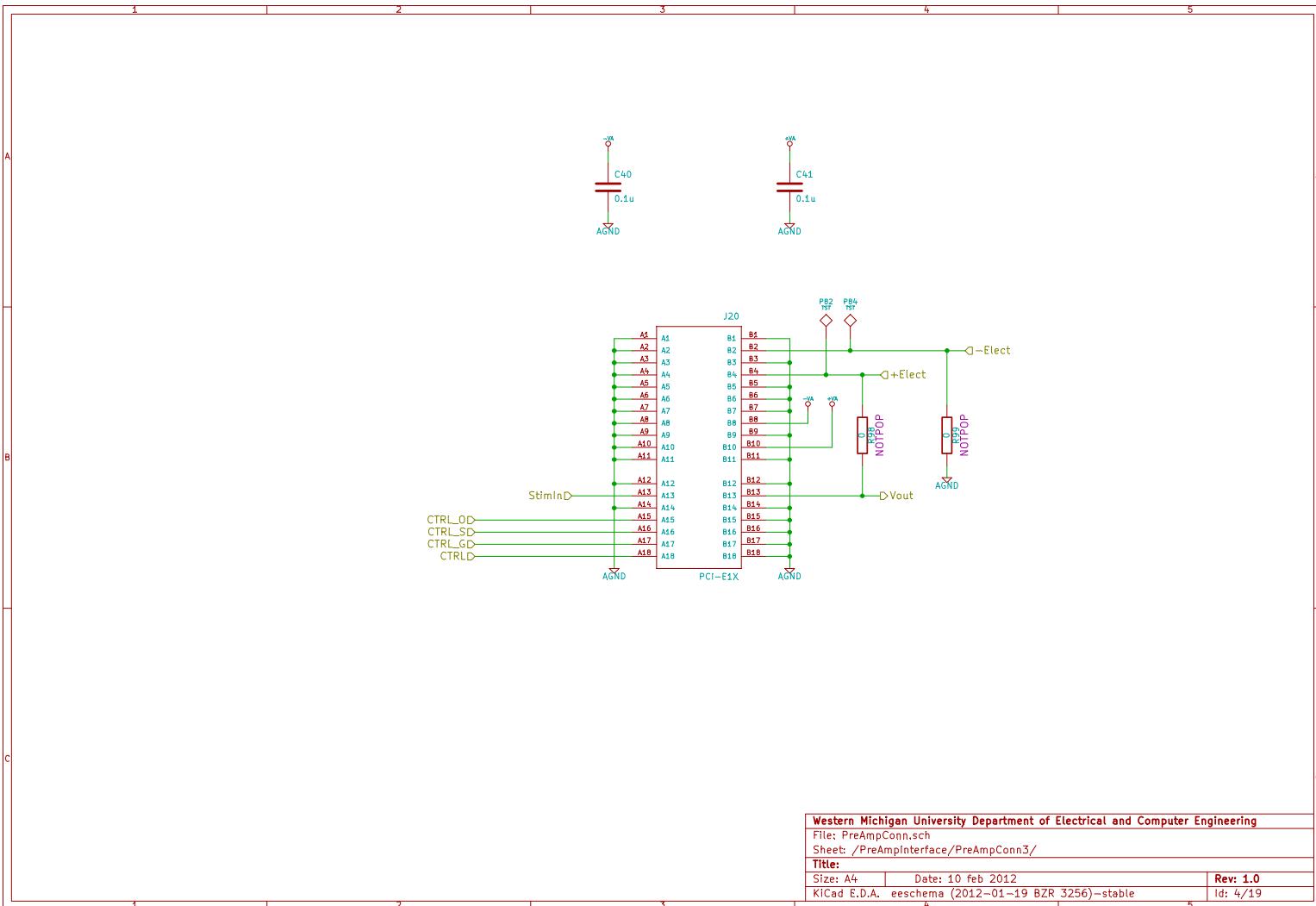




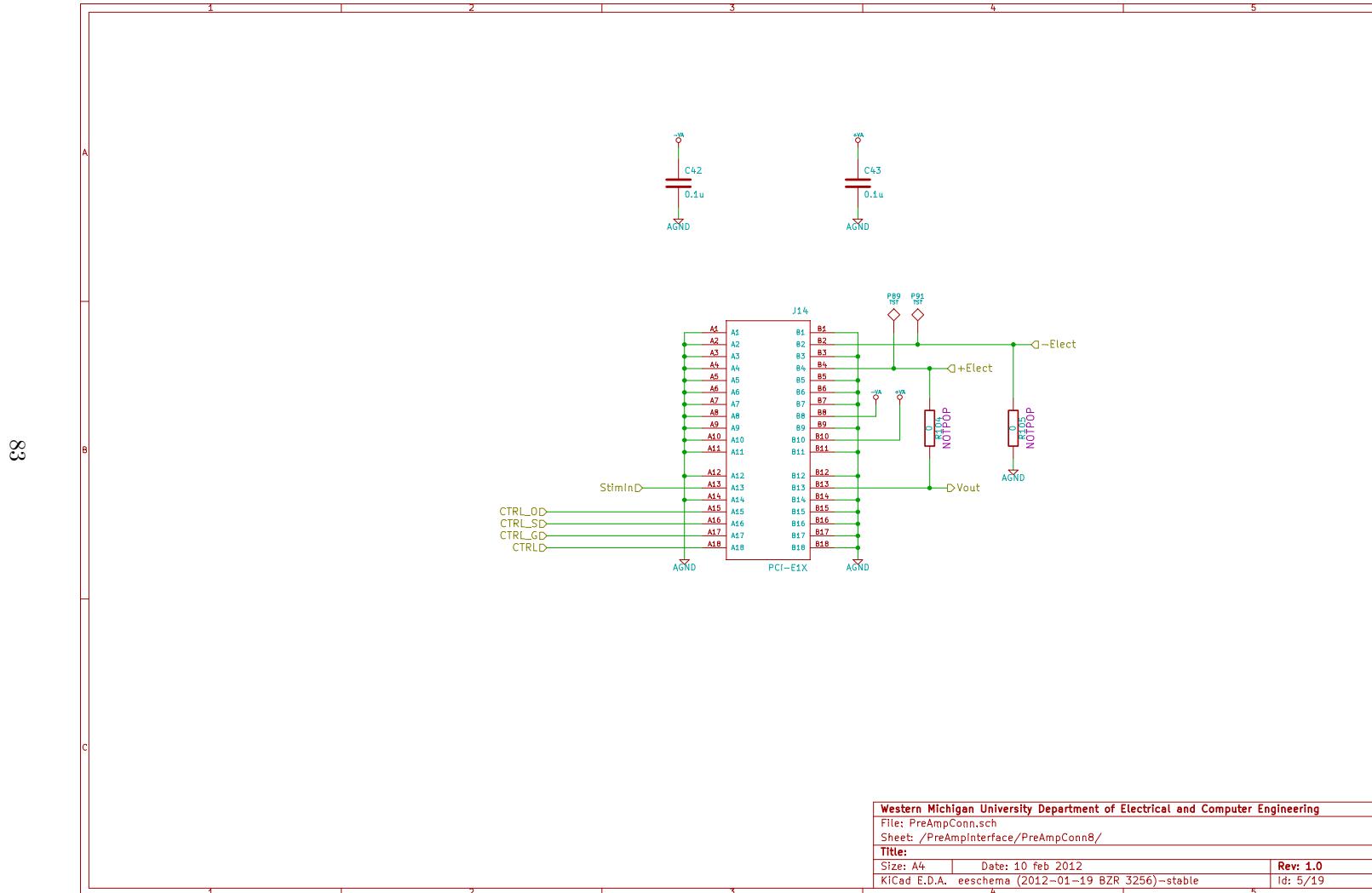
18



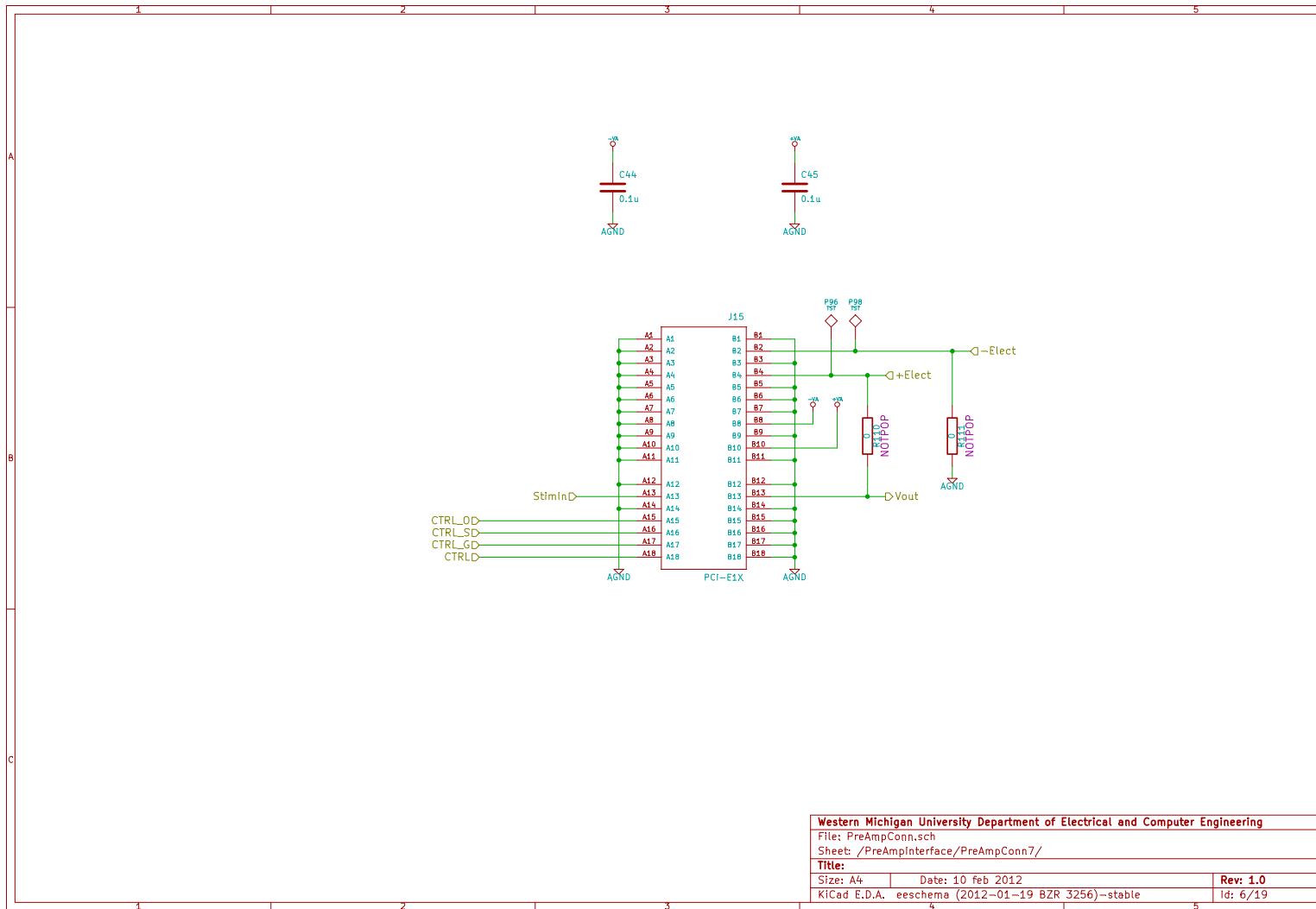
28



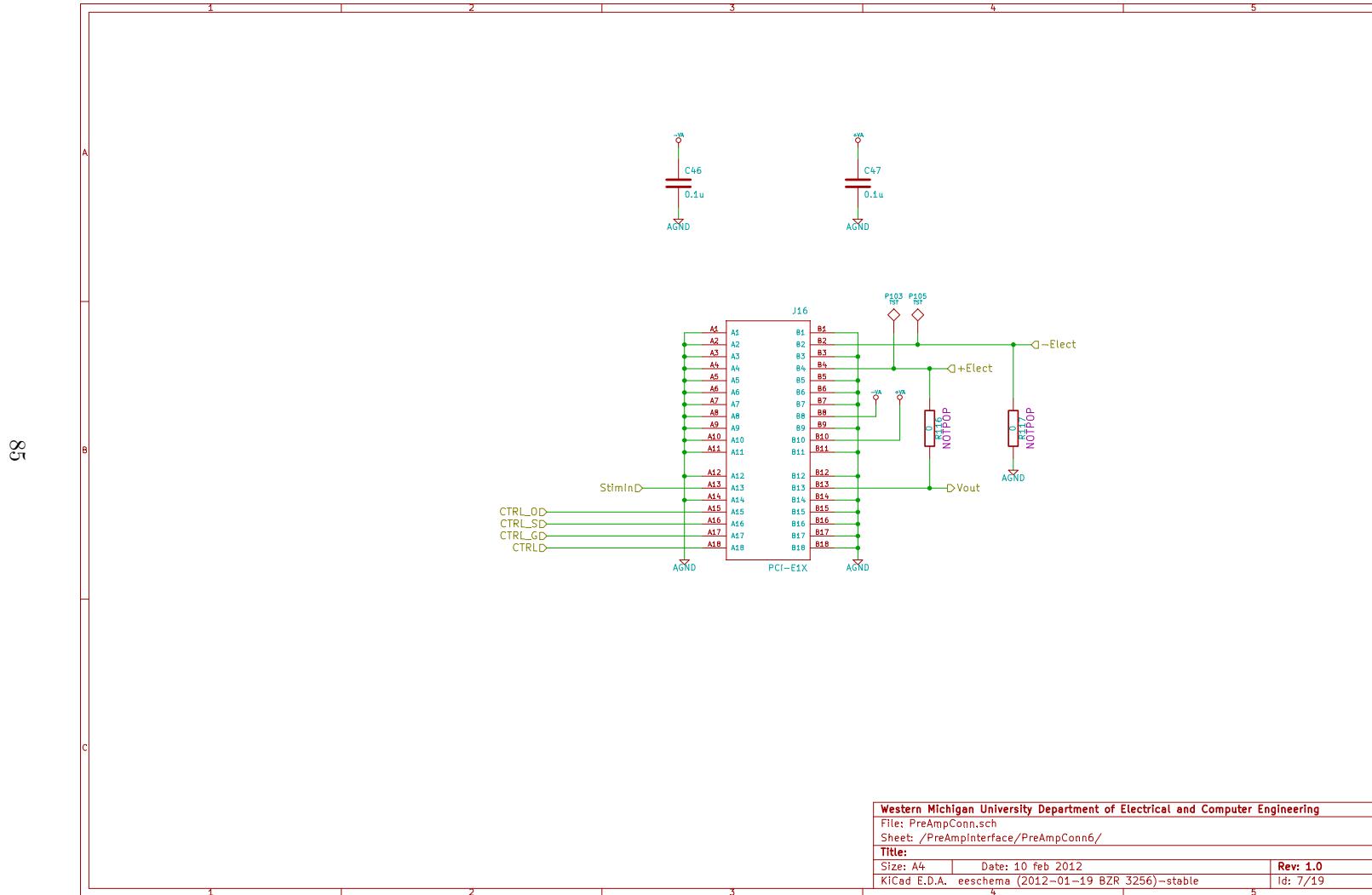
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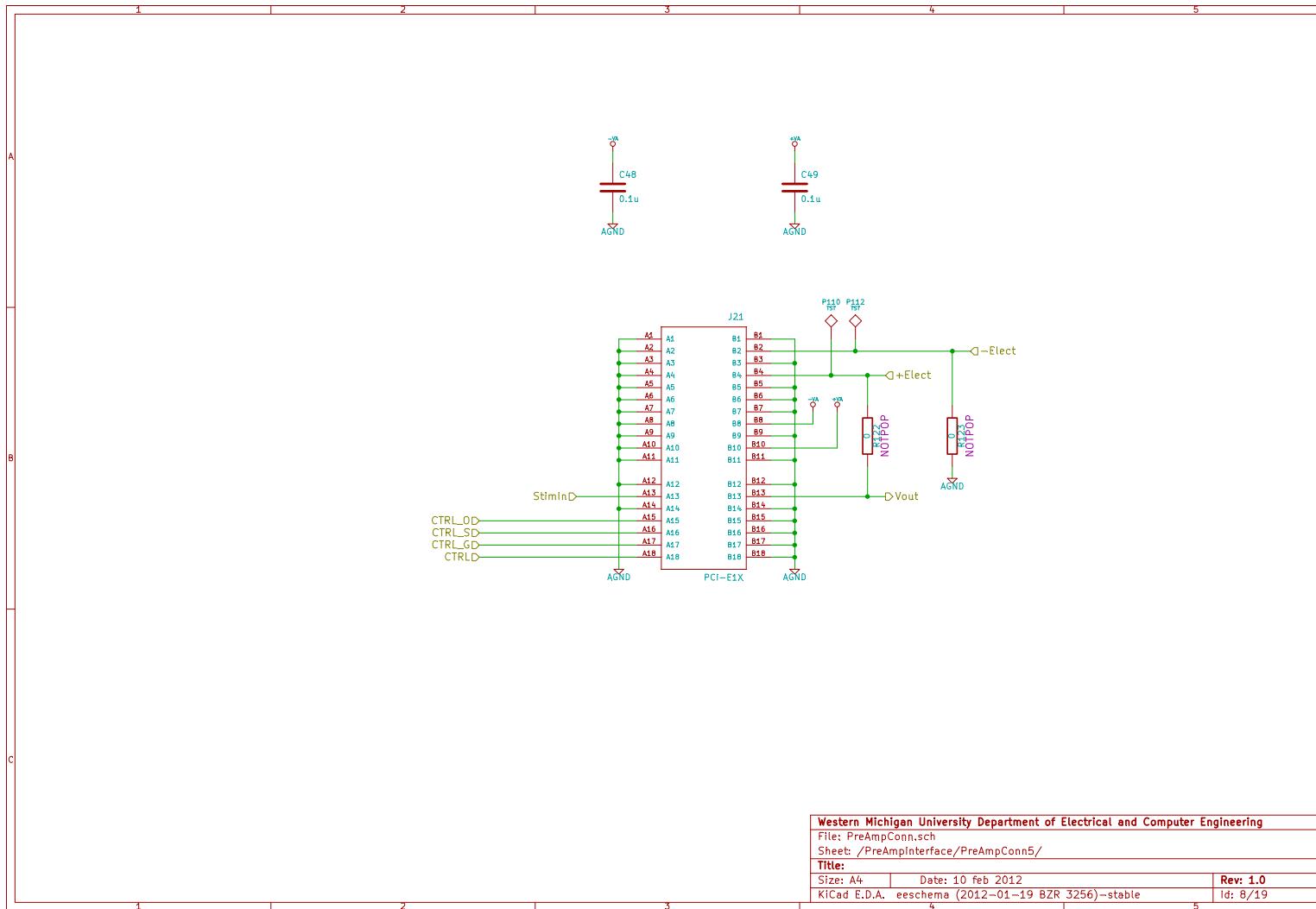
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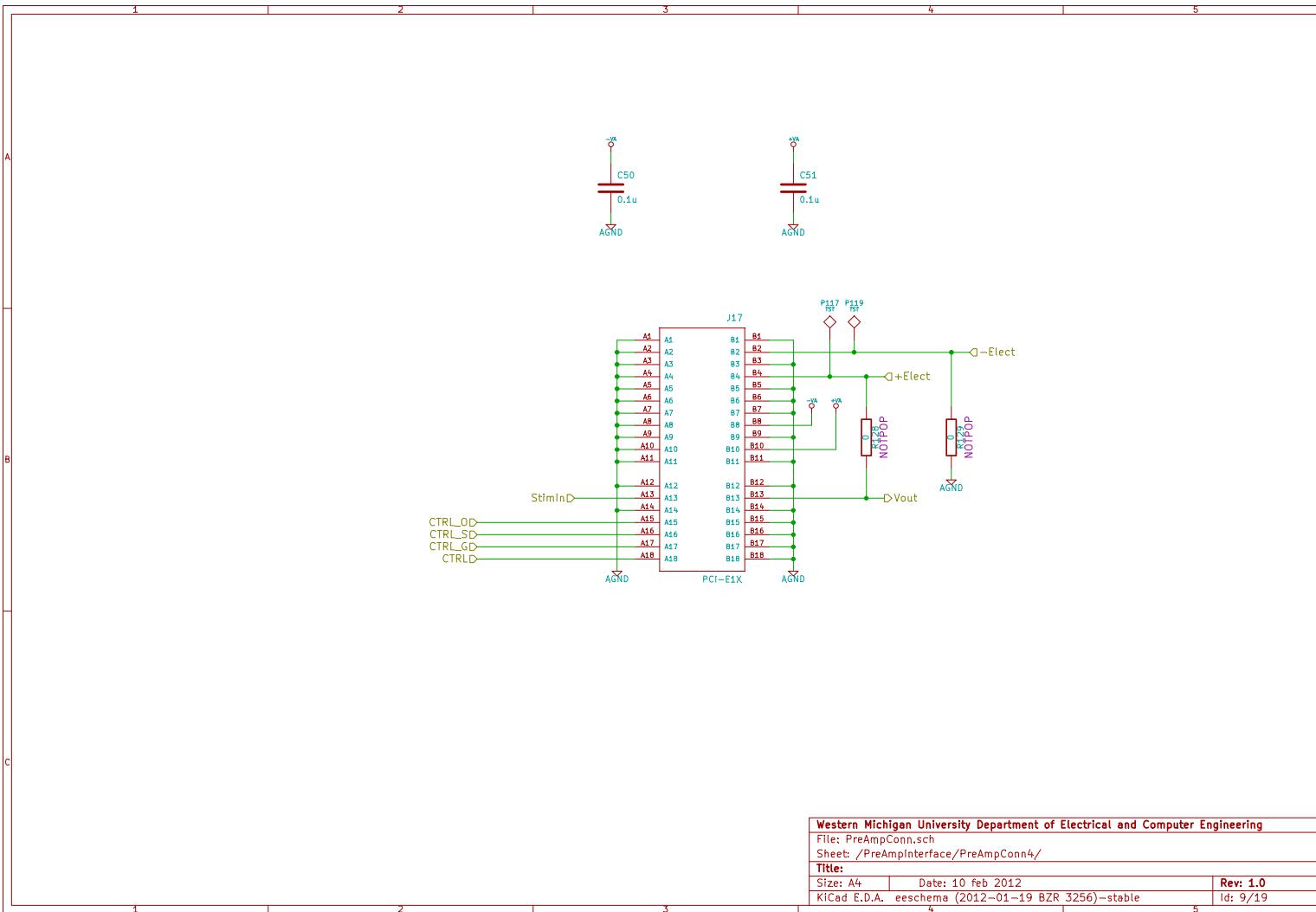
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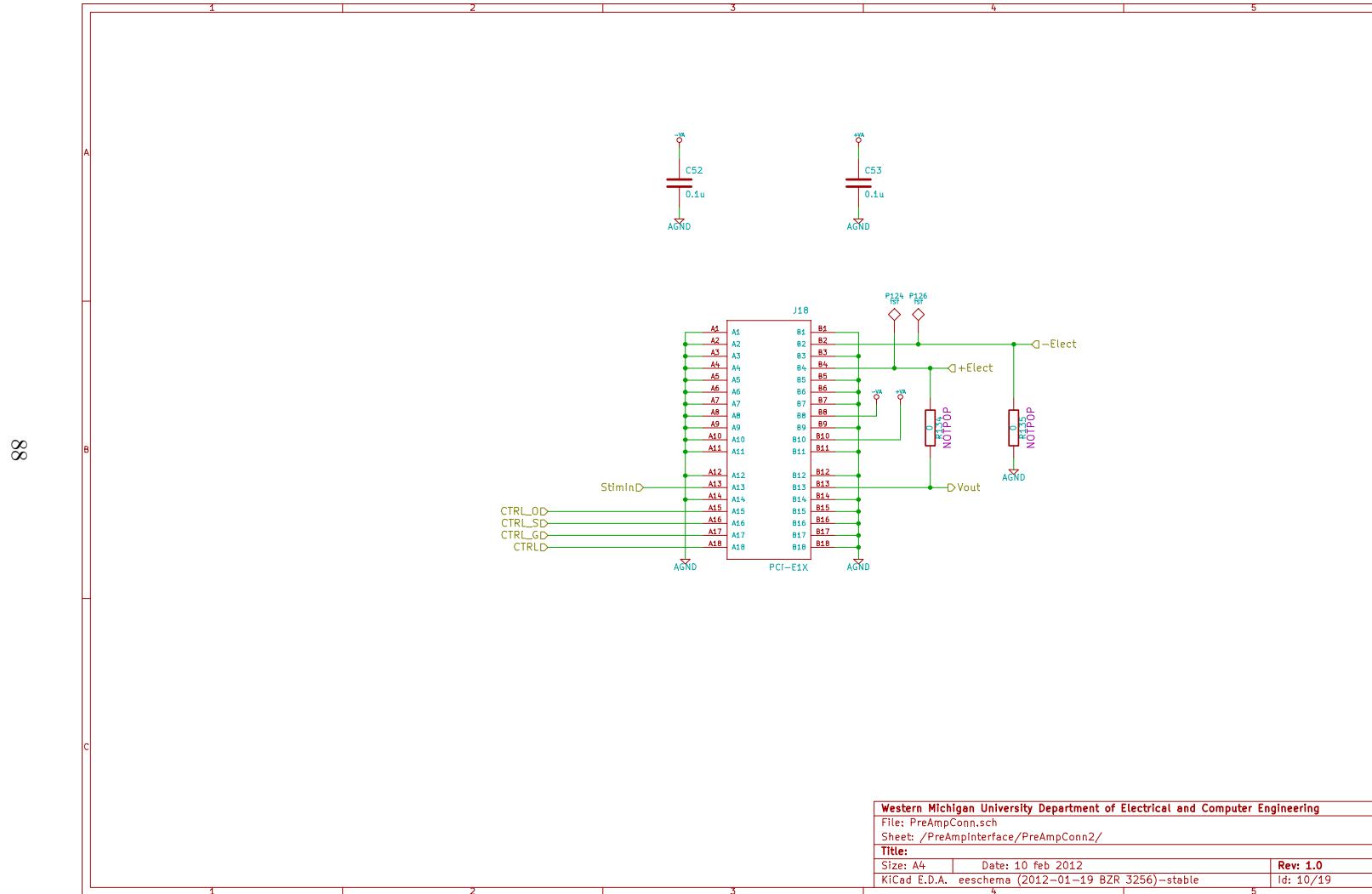
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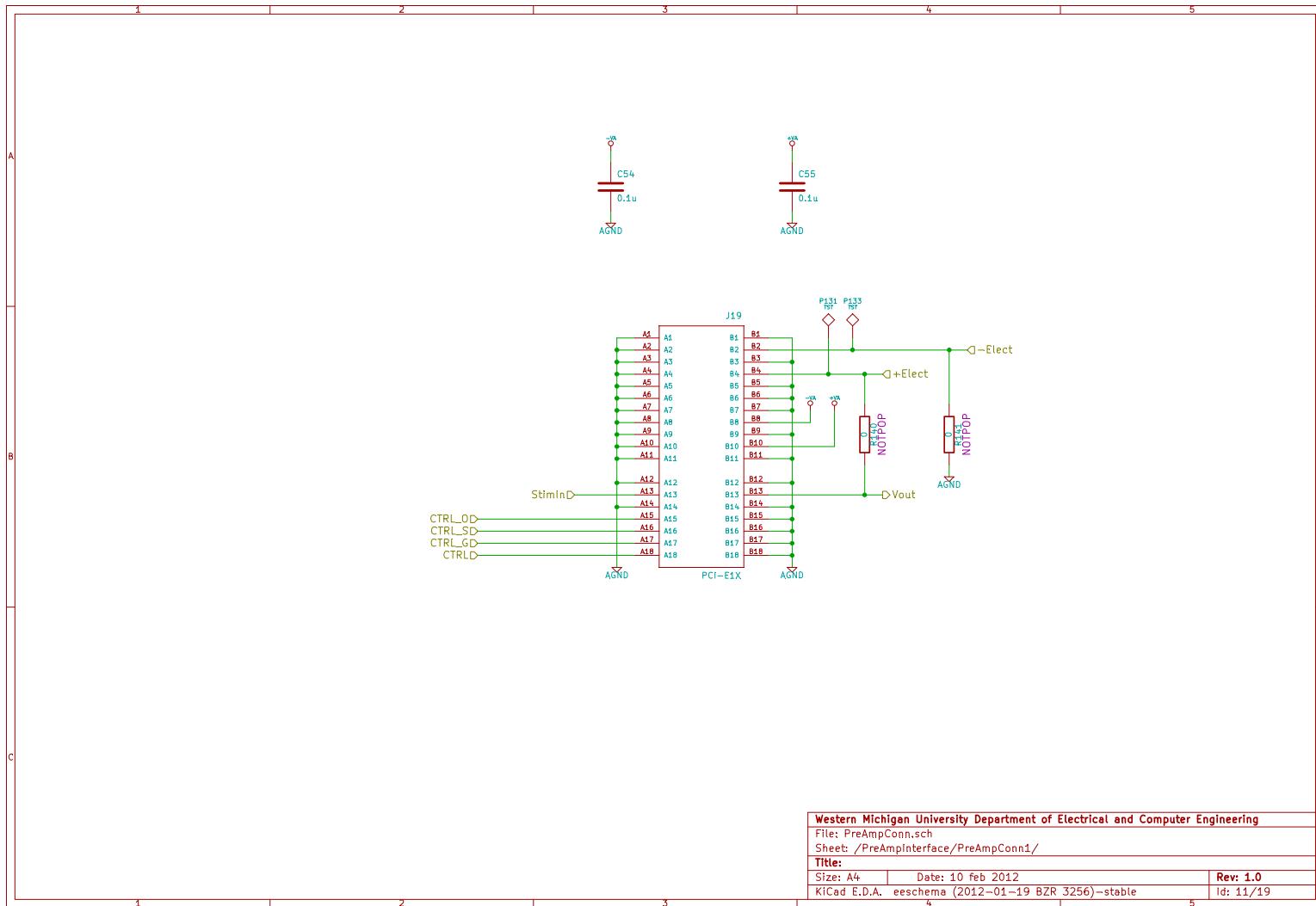
78



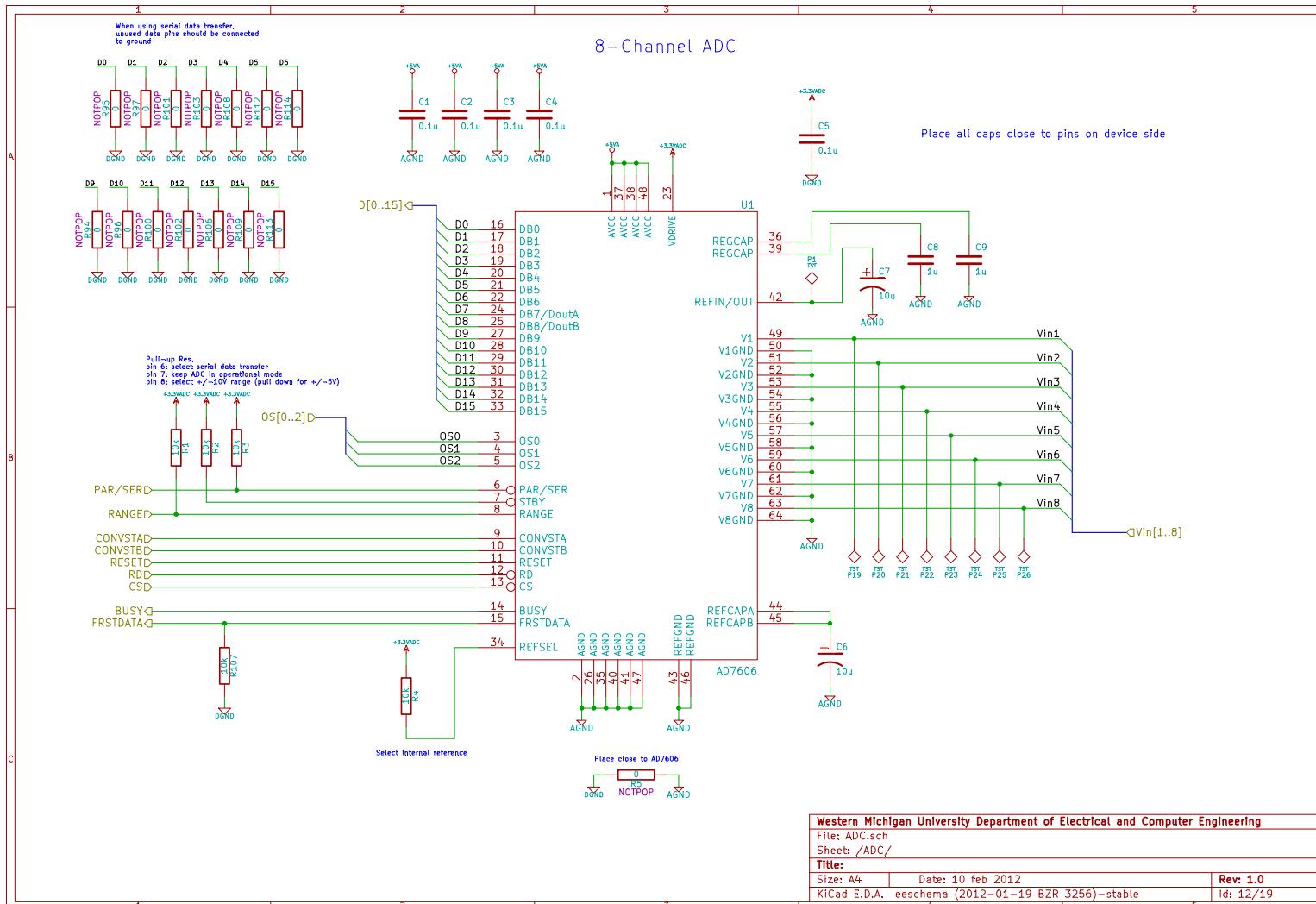
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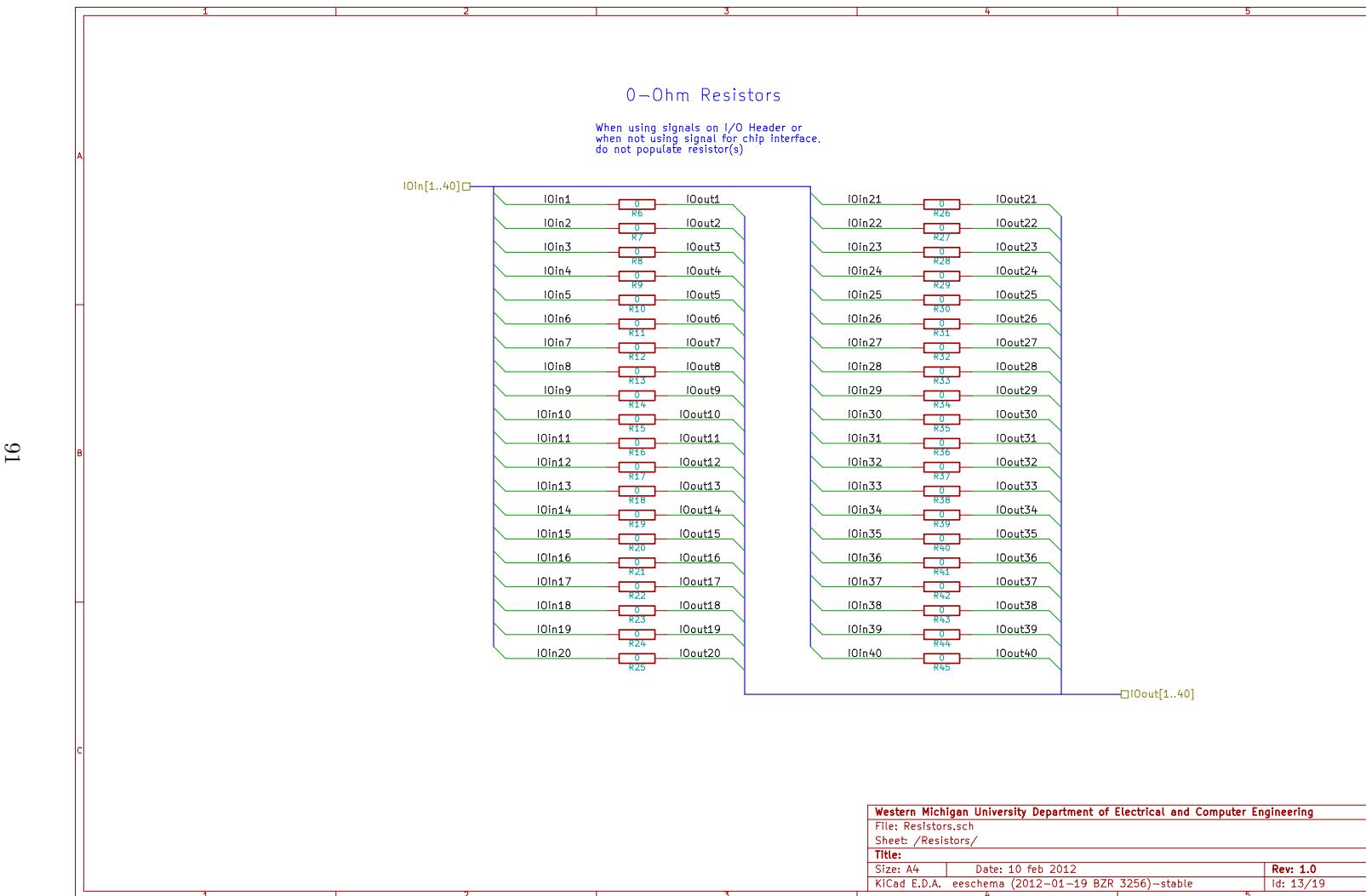


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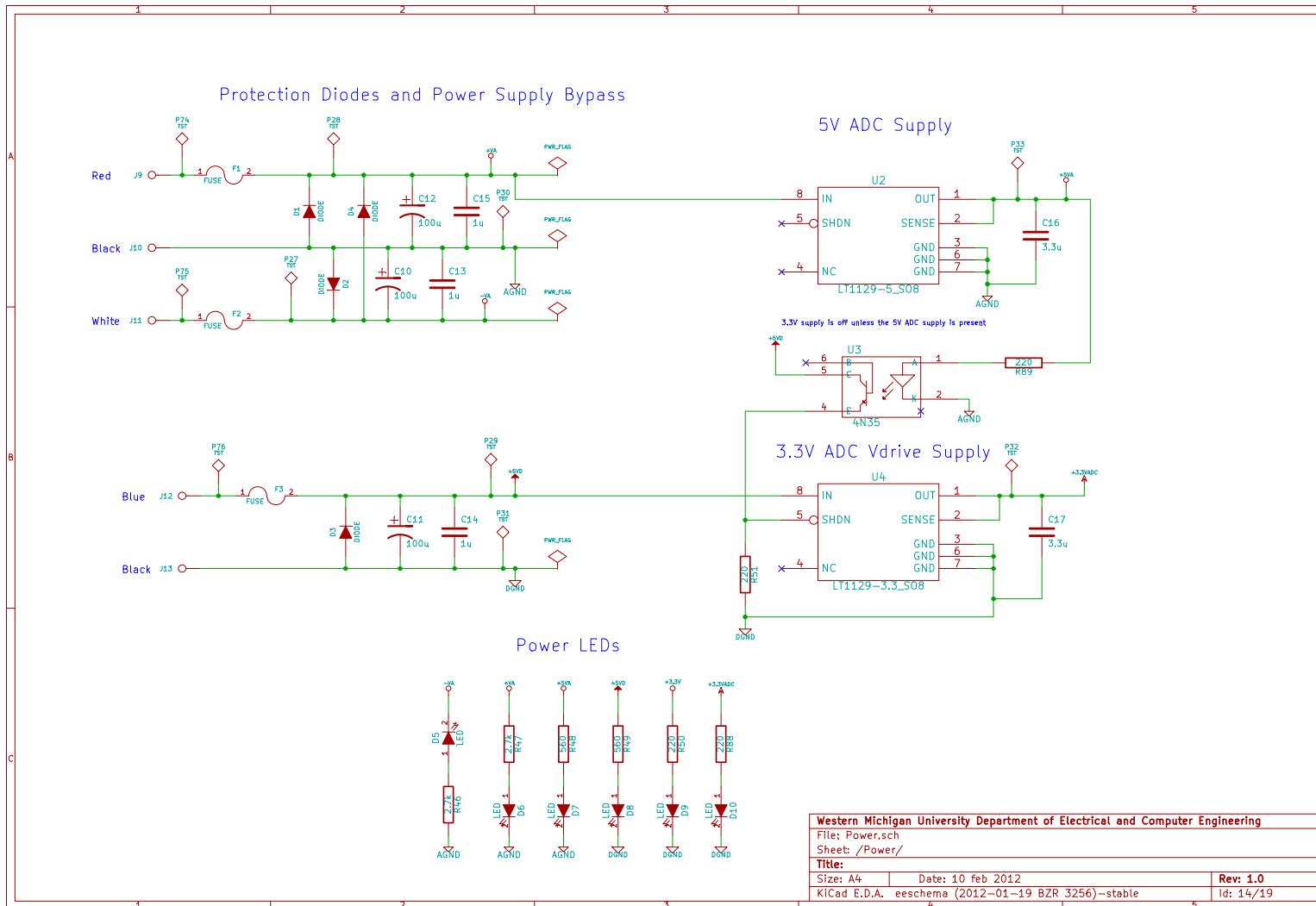


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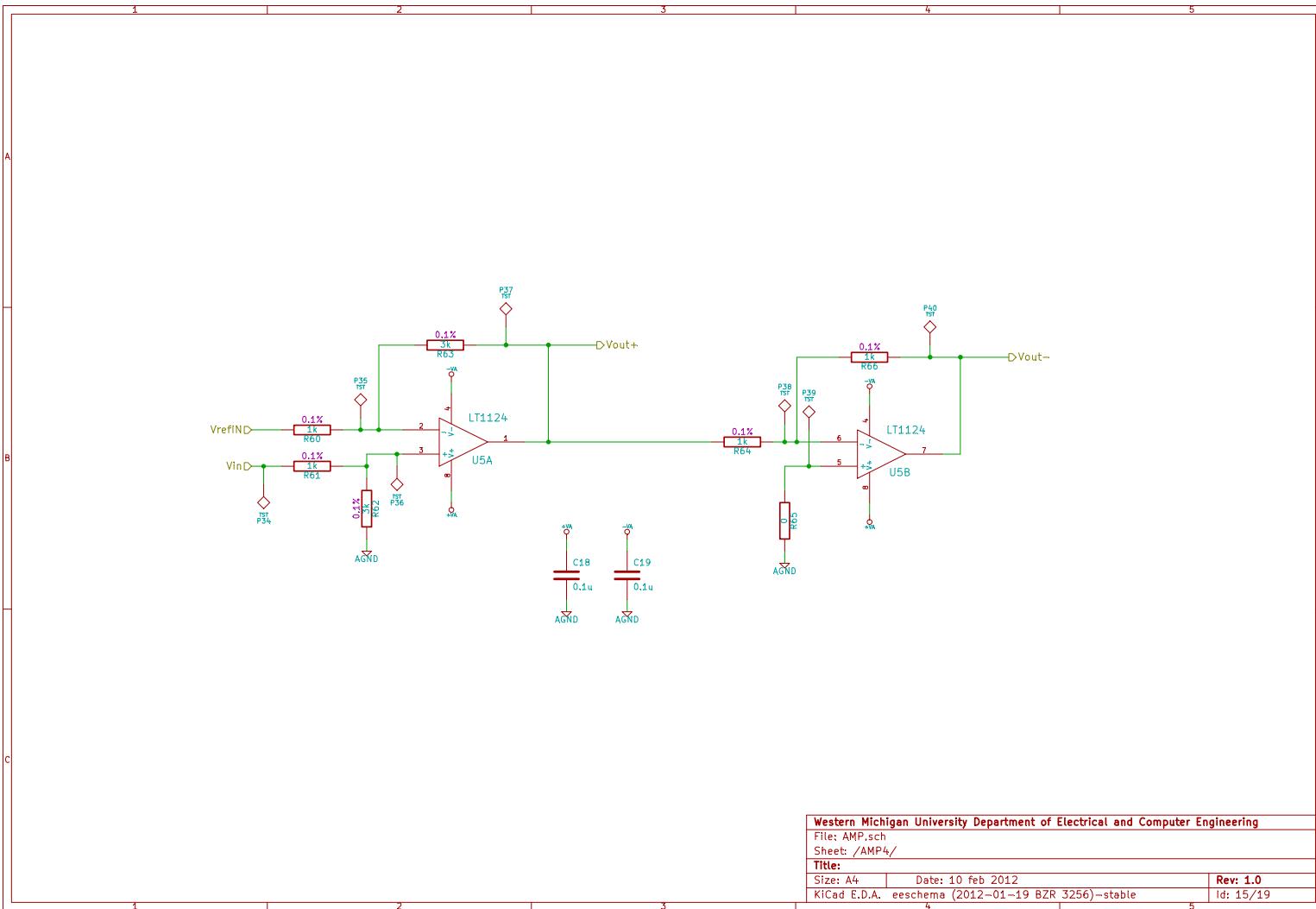




92

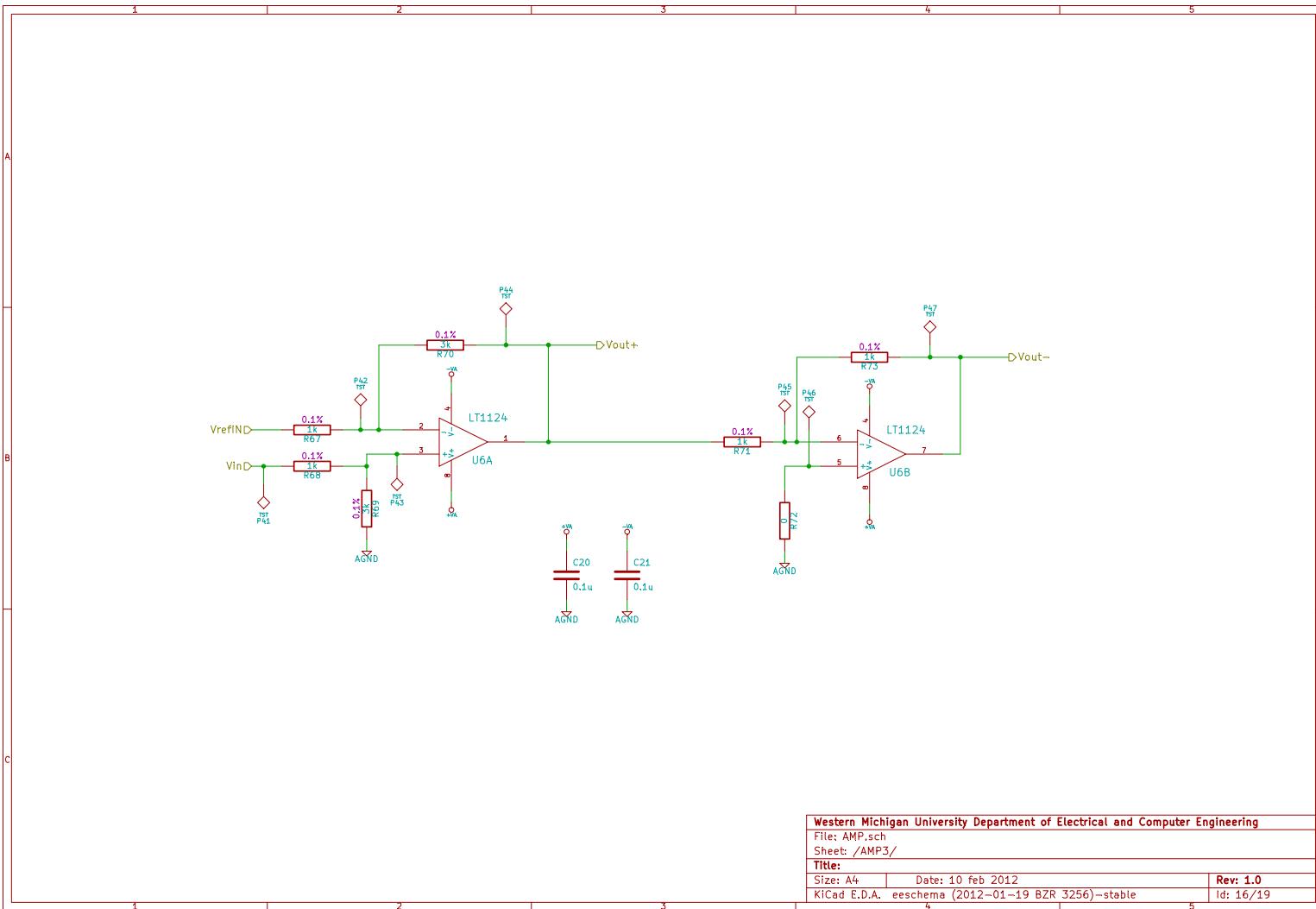


93

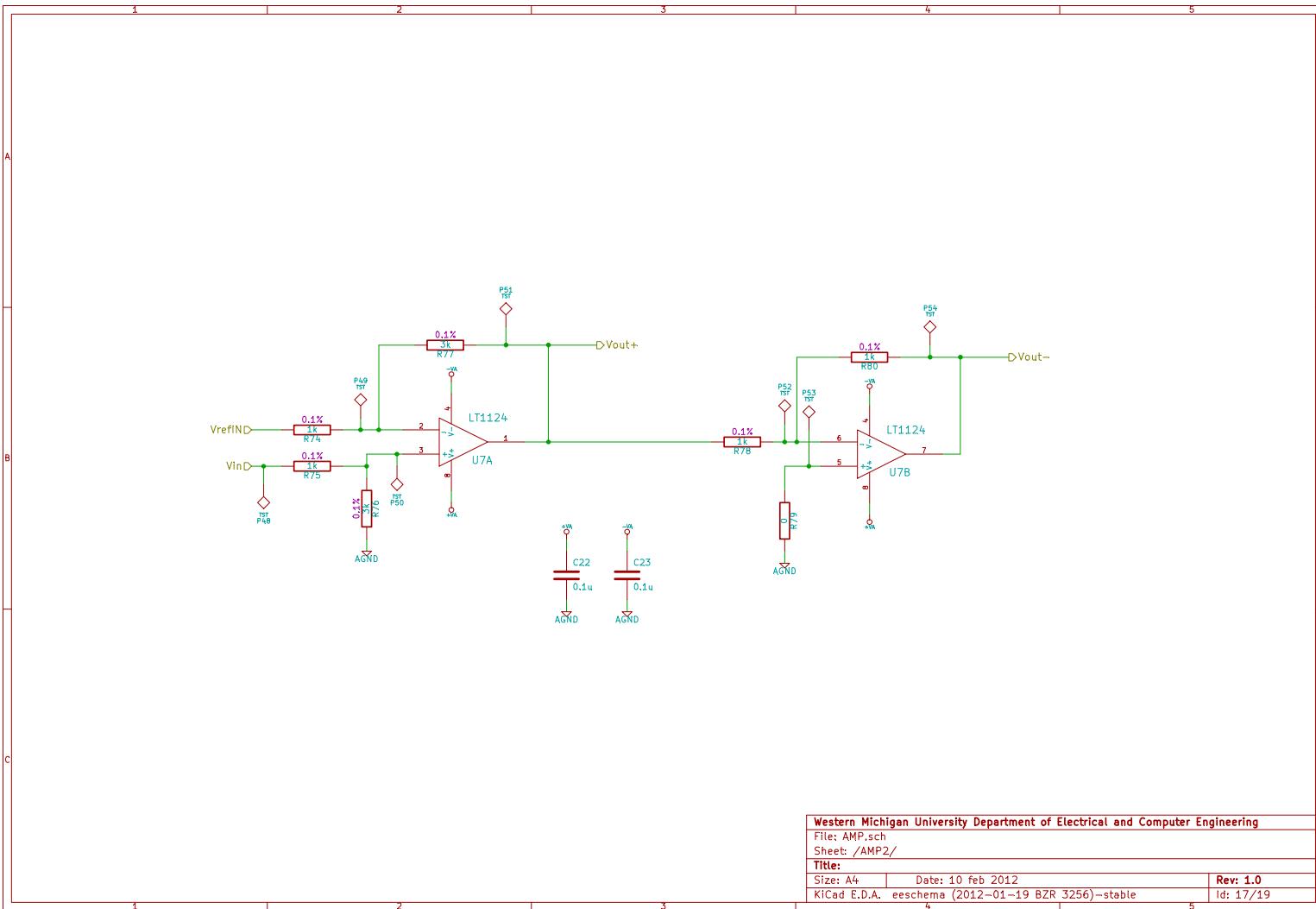


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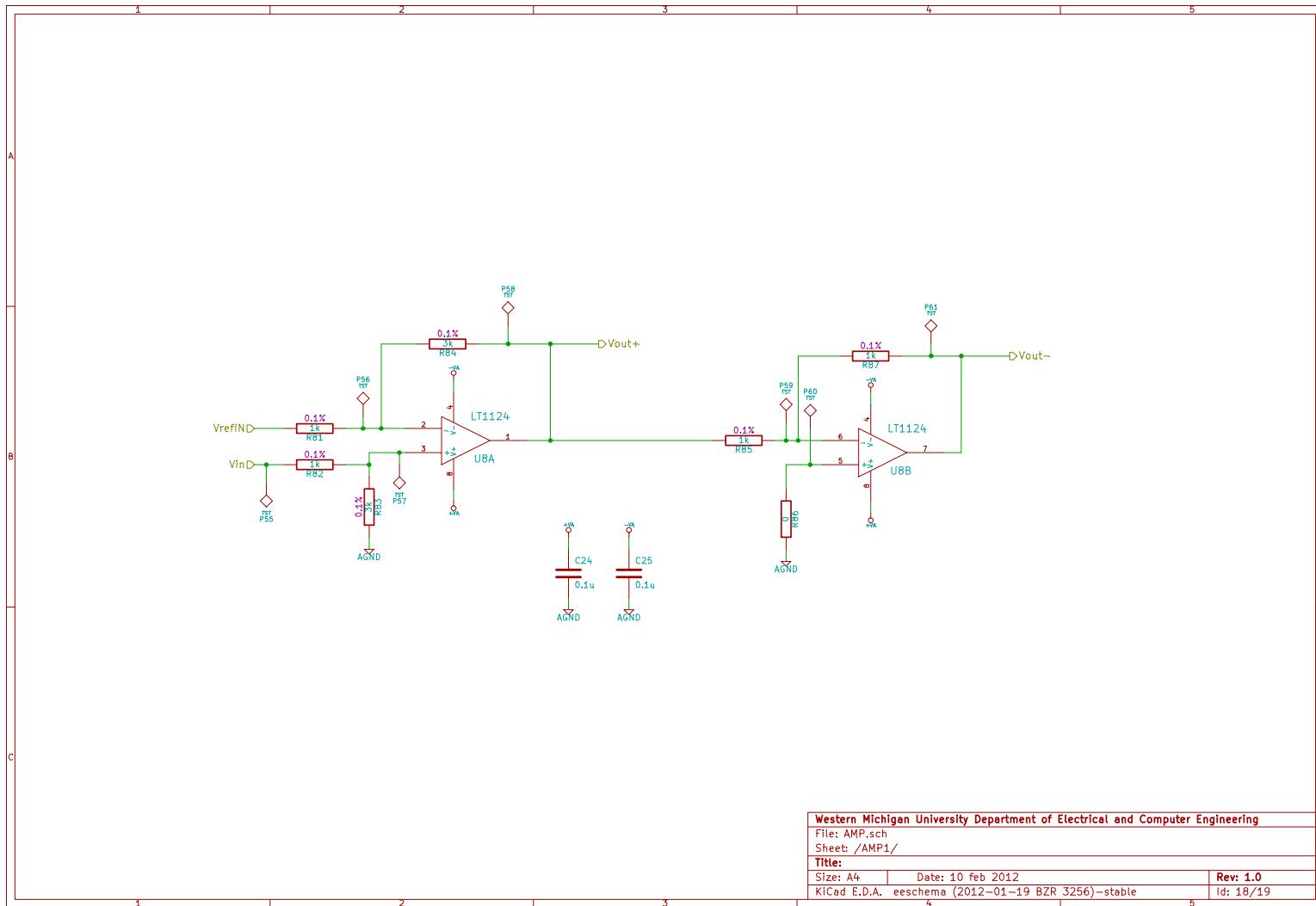
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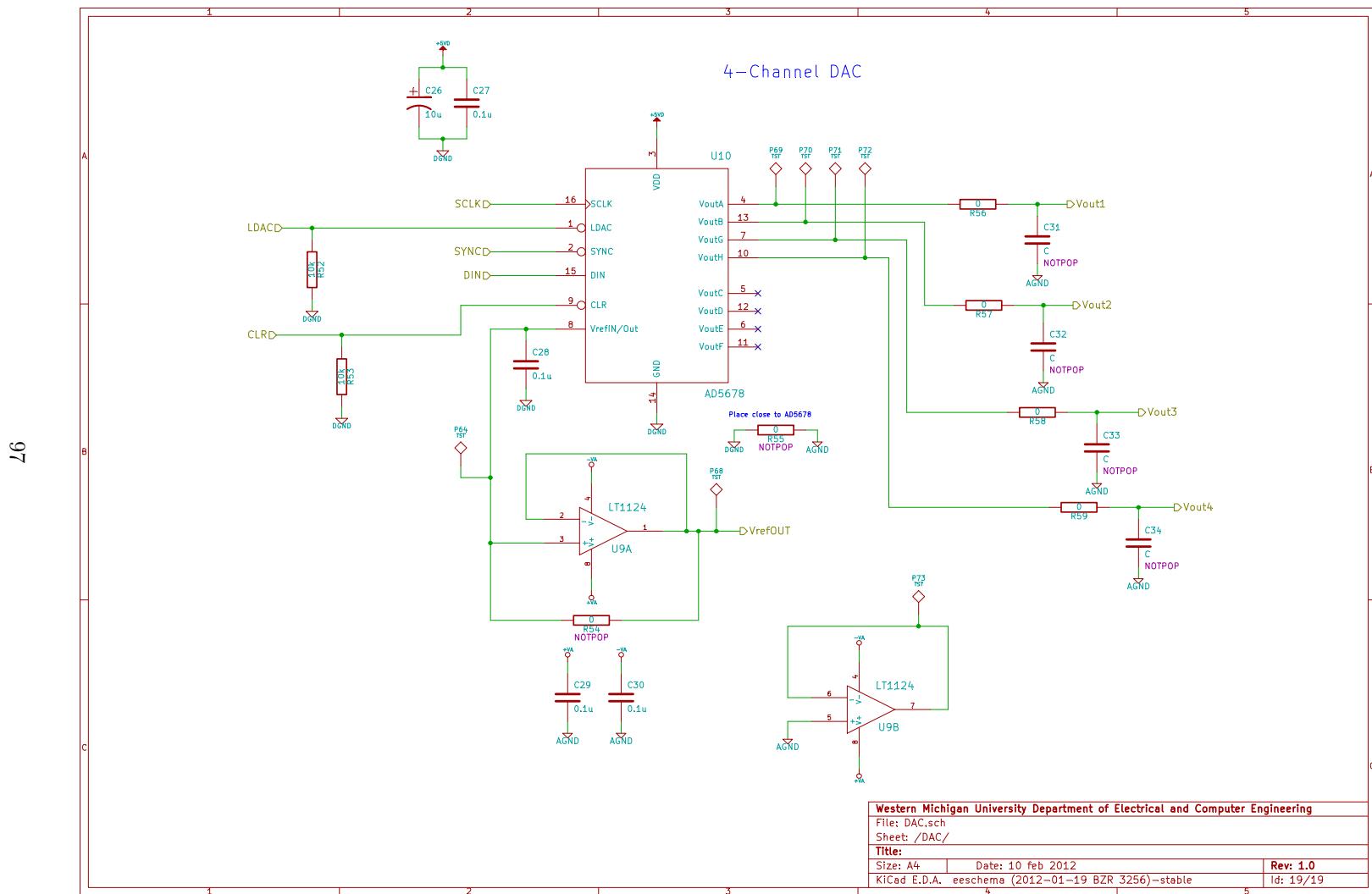


95



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## B KiCad Gerber File Export Instructions

Things to note: KiCAD produces gerber files in 274X format, so an aperture list file isn't needed. Use 8 characters for the file names. The drill map needs to be precision 2:4 with trailing zeros suppressed.

To generate the gerber and drill files, in Pcbnew, go to file->plot, see Figure 35. Notice that the copper layers, silkscreen, soldermask, and PCB\_Edges layers are selected; that "Exclude PCB Edge layer from other layers" is selected; and that "Use auxiliary axis as origin" is selected. A folder in the project directory called "gerber" keeps the plotted files organized. Press "Plot" to generate the files.

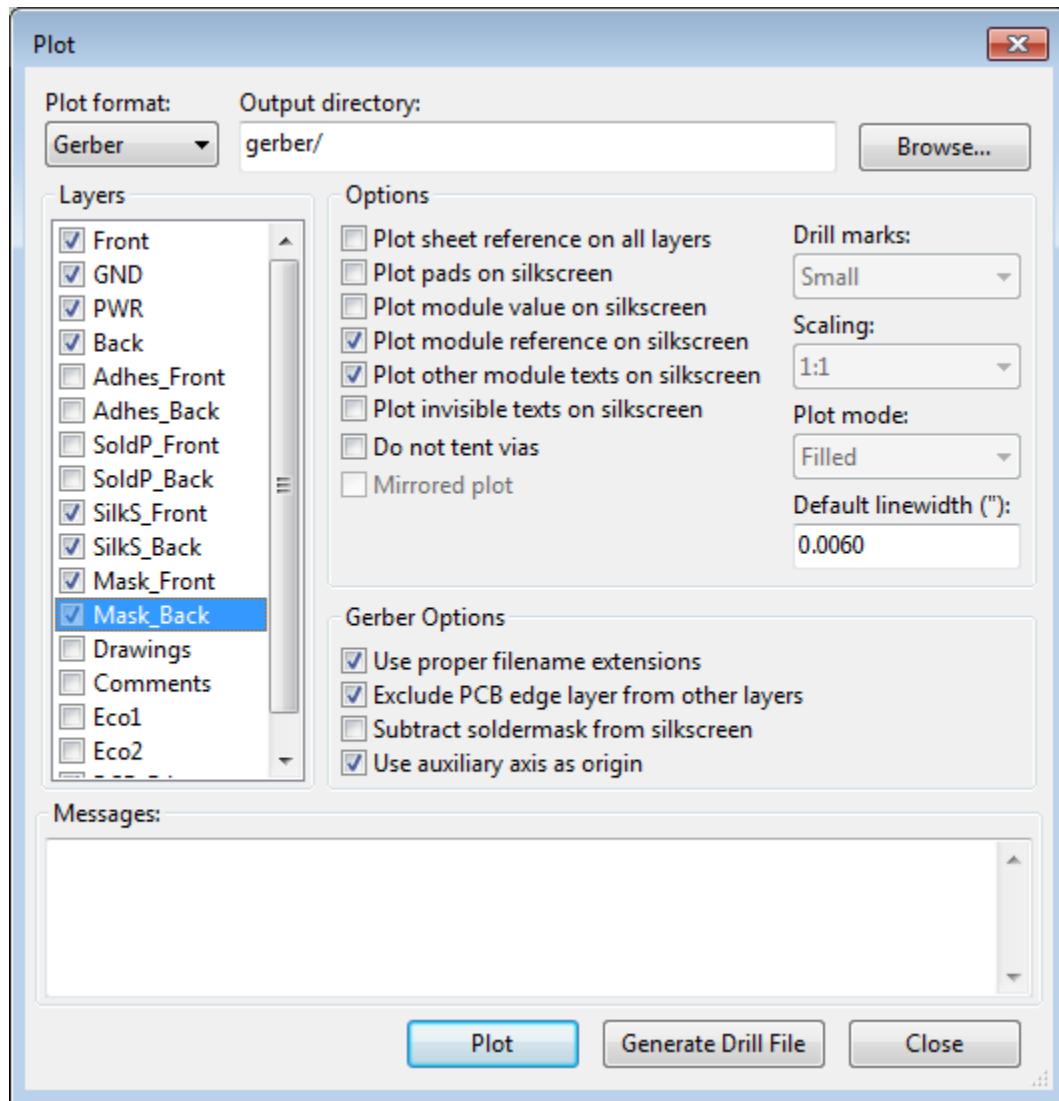


Figure 35: Pcbnew plot dialog

Advanced Circuits prefers the edge outline of the PCB to be on the silkscreen layer rather than in a separate file. As set up in Figure 35, the edges are only in the separate file. To get the edges on the front silkscreen, see Figure 36. Notice that only the front silkscreen layer is selected and this time "Exclude PCB Edge layer from other layers" is not selected. Press "Plot" to generate the new front silkscreen with the PCB edges.

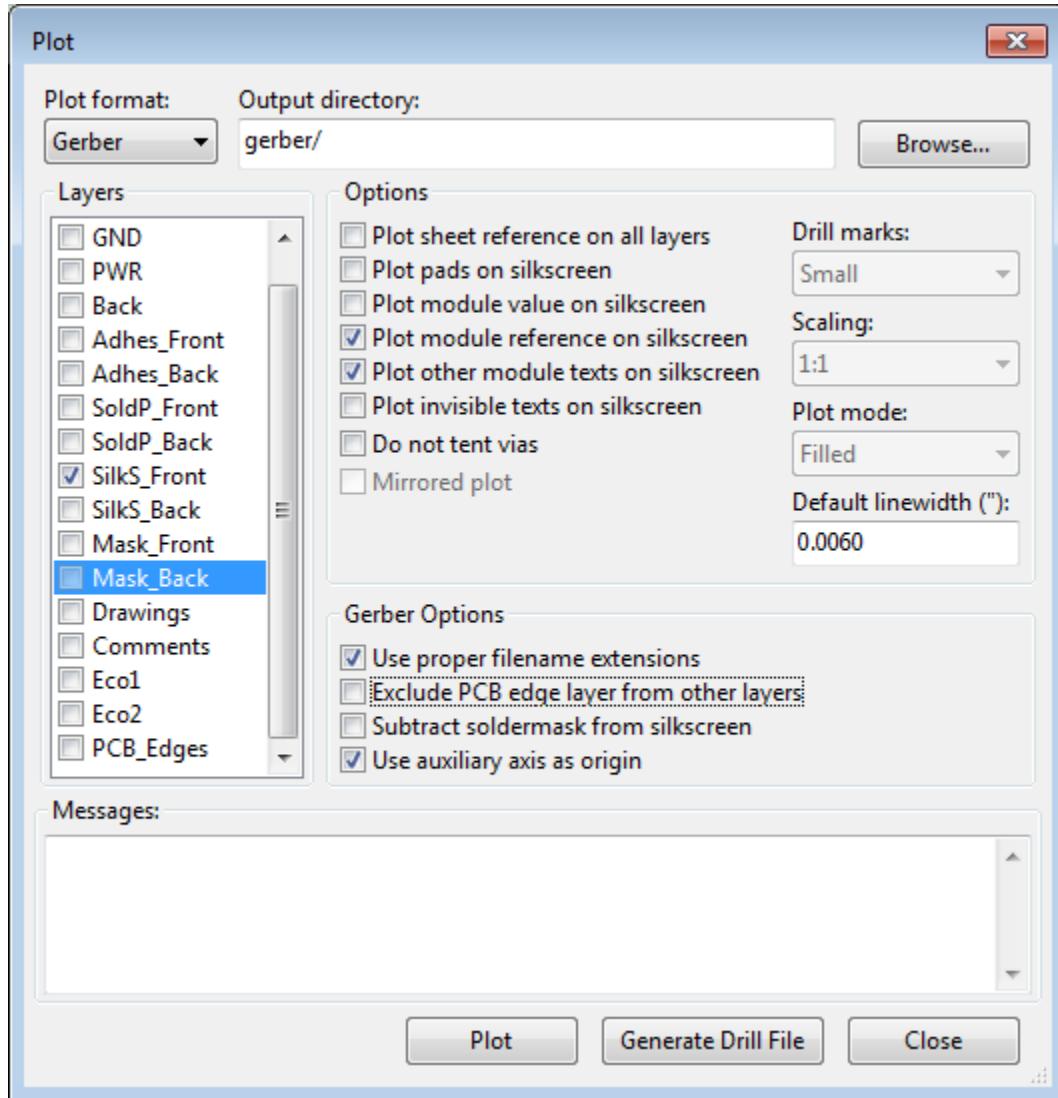


Figure 36: Pcbnew plot dialog

To generate the drill file, while in file->plot, press the "Generate Drill File" button. See Figure 37. Notice the Inches, Suppress trailing zeros, 2:4 precision, Drill Map (gerber), and the auxiliary axis that should have been added to the layout are selected (the auxiliary axis was also selected in Figure 35). It is necessary to have set the auxiliary axis to a corner of the PCB outline in the main drawing window. The Drill Map (gerber) selection will produce the additional "fabrication print showing printed circuit board outline with drill

pattern and sizes in gerber format.”

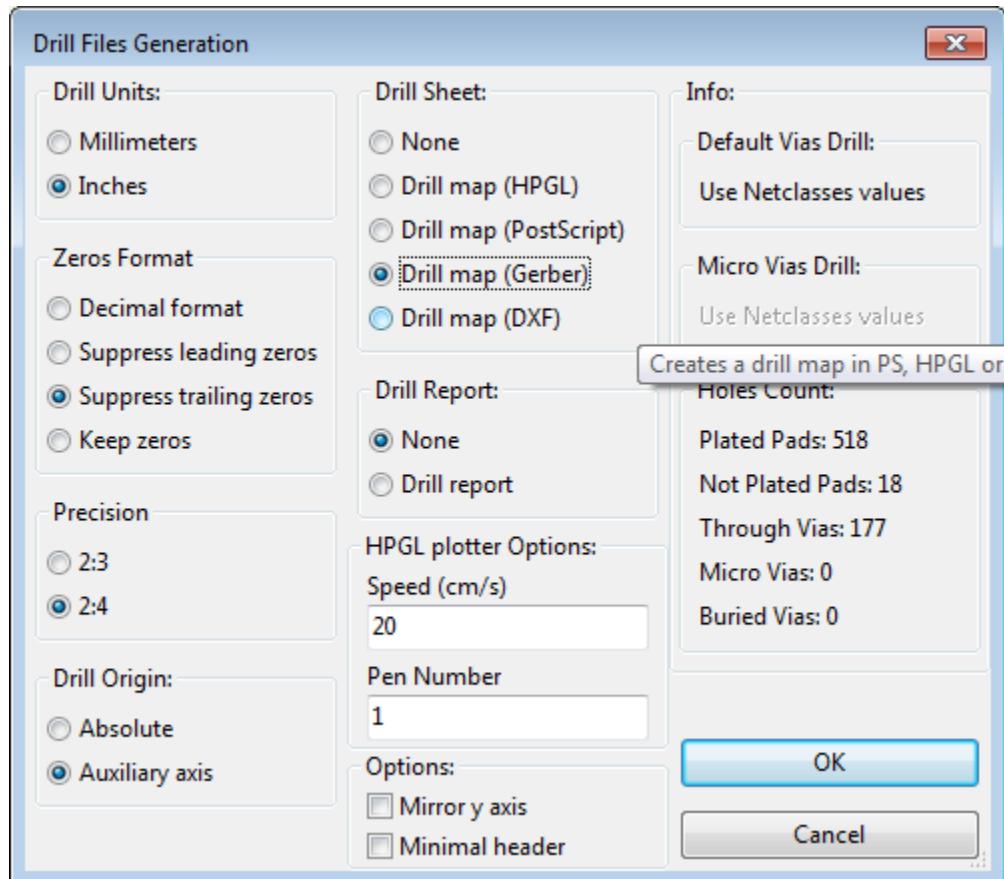


Figure 37: Pcbnew drill dialog

When going through the FreeDFM:

You will have to select what each file is. The program recognizes most files, except for the PCB.Edges which you want to set as "Drawing/Other" in the drop down box and the GND and PWR layers are "Inner Copper" in the dropdown and another drop down will show up in which you tell it that the files are "Positive" (the filled in areas should have copper as opposed to negative in which the filled in areas are not copper) and GND is layer "2" (or "3") while PWR is layer "3" (or "2") (if the .drl file is the Excellon dril file while the .pho file is the fabrication print with drill pattern and sizes in gerber format that should be "Drawing/Other.")

When you are ready to place your order:

1. Add a README.txt with this information:
  - (a) List of every file name with a brief description as to what it is.
  - (b) List all non-gerber specs for this job.
  - (c) Your contact information (include evening phone if you like).
2. Change all of the file names to 8 characters + the 3 character extension
3. Remember that if you place orders later, you will want to have a different zip file name.

## C Bill of Materials

Table 12 in this section shows the list of components used to populate the Electrophysiology Interface board. Information from the KiCAD EDA suite, such as reference designator, footprint name (Package), and component value (Designation), is aligned with data from the part supplier, DigiKey®, such as part number and unit price at the time of purchase.

<b>Id</b>	<b>Designator</b>	<b>Package</b>	<b>Quantity</b>	<b>Designation</b>	<b>DigiKey Part Number</b>	<b>Description</b>	<b>Unit Price</b>	<b>Cost</b>
1	U1	TQFP-64	1	AD7606	AD7606BSTZ-RLCT-ND	IC DAS W/ADC 16BIT 64LQFP	29.32	29.32
2	U10	SSOP16	1	AD5678	AD5678BRUZ-2-ND	IC DAC 12/16BIT SPI/SRL 16TSSOP	21.17	21.17
3	U2	SO8E	1	LT1129-5_SO8	LT1129CS8-5#PBF-ND	IC LDO W/SHTDN 5V 700MA 8SOIC	4.77	4.77
4	U4	SO8E	1	LT1129-3.3_SO8	LT1129CS8-3.3#PBF-ND	IC LDO REG W/SHTDWN 3.3V 8-SOIC	4.77	4.77
5	U5,U6,U9,U8,U7	SO8E	5	LT1124	LT1124CS8-1#PBF-ND	IC OPAMP DUAL PREC HS LN 8SOIC	7.44	37.20
6	R41,R43,R40,[...]	SM0805	85	0	P0.0ACT-ND	RES 0.0 OHM 1/8W 0805 SMD (min 100)	0.0131	1.11
7	R75,R74,R73,[...]	SM0805	16	1k	P1.0KDACT-ND	RES 1.0K OHM 1/8W .1% 0805 SMD (min 50)	0.2494	3.99
8	R70,R69,R63,[...]	SM0805	8	3k	P3.0KDACT-ND	RES 3.0K OHM 1/8W .1% 0805 SMD (min 50)	0.2494	2.00
9	R53,R52,R41,[...]	SM0805	7	10k	P10KACT-ND	RES 10K OHM 1/8W 5% 0805 SMD (min 50)	0.0162	0.11
10	R51,R50,R88,R89	SM0805	4	220	P220ACT-ND	RES 220 OHM 1/8W 5% 0805 SMD (min 50)	0.0162	0.06
11	R49,R48	SM0805	2	560	P560ACT-ND	RES 560 OHM 1/8W 5% 0805 SMD (min 50)	0.0162	0.03
12	R47,R46	SM0805	2	2.7k	P2.7KACT-ND	RES 2.7K OHM 1/8W 5% 0805 SMD (min 50)	0.0162	0.03
13	C15,C14,C13,C9,C8	SM0805	5	1u	445-1419-1-ND	CAP CER 1UF 25V 10% X5R 0805 (min 10)	0.11	0.55
14	C16,C17	SM0805	2	3.3u	445-5970-1-ND	CAP CER 3.3UF 25V 10% X7R 0805	0.49	0.98
15	C18,C19,C20,[...]	SM0805	36	0.1u	445-1351-1-ND	CAP CER 0.1UF 25V 10% X7R 0805 (min 10)	0.072	2.59
16	C26,C7,C6,C35,C37	SM0805	5	10u	445-5984-1-ND	CAP CER 10UF 25V 10% X5R 0805	0.7	3.50
17	C31,C32,C33,C34	SM0805	4	C	N/A	Not populated		
18	F1,F2,F3	SM0805	3	FUSE	MFU0805.50CT-ND	FUSE .50A 0805 VFAST SMD	0.62	1.86
19	J2,J3	PIN_ARRAY_2X1	2	CONN_2	WM8072-ND	CONN HEADER 2POS .100" STR TIN	0.37	0.74
20	J5	PIN_ARRAY_20X2	1	CONN_20X2	WM8134-ND	CONN HEADER 40POS .100" STR TIN	2.71	2.71
21	J7	pin_array_12x1	1	TERM_12	A98075-ND	TERM BLOCK 12POS SIDE ENT 2.54MM	6.54	6.54
22	D9,D8,D7,D6,D5,D10	LED-0805	6	LED	754-1128-1-ND	LED 2X1.2MM 625NM RD WTR CLR SMD	0.16	0.96
23	U3	DIP-6_-300_SMD	1	4N35	516-1730-5-ND	OPTOCOUPLER PHOTOTRANS 6-SMD GW	0.56	0.56
24	D4,D3,D2,D1	D4	4	DIODE	1N4003-E3/54GICT-ND	DIODE GP 200V 1A DO204AL	0.43	1.72
25	C12,C11,C10	C1_3.5mm	3	100u	P5182-ND	CAP ALUM 100UF 50V 20% RADIAL	0.33	0.99
26	P73,P58,P57,[...]	TSTPAD	70	TST	N/A	This is a PCB footprint only		
27	J13,J12,J11,J10,J9	BNA_1	5	CONN_1	J121-ND, J119-ND, J312-ND, J120-ND	CONN JACK TEST VERTICAL BLACKx2, WHITEx1, BLUEx1, REDx1	1.22	6.10
28	U11	VQFP64	1	XCG536XL-VQ64	122-1388-ND	IC CPLD 1.6K 72MCELL 64-VQFP	2.66	2.66
29	J22	SIL-8	1	CONN_8	WM8078-ND	CONN HEADER 8POS .100" STR TIN	0.9	0.90
30	J23,J24,J4	SIL-7	3	CONN_7	WM8077-ND	CONN HEADER 7POS .100" STR TIN	0.85	2.55
31	J6	pin_array_10x1	1	CONN_10	WM8080-ND	CONN HEADER 10POS .100" STR TIN	1.11	1.11
32	J8	pin_array_16x1	1	TERM_16	A98338-ND	TERM BLOCK 8POS SIDE ENT 2.54MM (need 2)	4.56	9.12
33	J1	FX2-100S-1.27	1	HIROSE_FX2-100	H10644-ND	CONN RECEP R/A 100POS 1.27MM	7.63	7.63
34	J19,J18,J20,J17, J21,J16,J15,J14	PCI-E_36	8	PCI-E1X	609-1960-ND	CONN PCI EXPRESS 36POS VERT PCB (min 10)	0.709	5.67
								Total \$164.02

Table 12: Electrophysiology Interface Board Bill of Materials, cost

Id	Designator	Quantity	DigiKey Part Number	Description
1	U1	1	AD7606BSTZ-RLCT-ND	IC DAS W/ADC 16BIT 64LQFP
2	U10	1	AD5678BRUZ-2-ND	IC DAC 12/16BIT SPI/SRL 16TSSOP
3	U2	1	LT1129CS8-5 #PBF-ND	IC LDO W/SHTDN 5V 700MA 8SOIC
4	U4	1	LT1129CS8-3.3 #PBF-ND	IC LDO REG W/SHTDWN 3.3V 8-SOIC
5	U5,U6,U9,U8,U7	5	LT1124CS8-1 #PBF-ND	IC OPAMP DUAL PREC HS LN 8SOIC
6	R41,R43,R40,R39,R38,R44,R42,R37,R36,R35,R34,R33,R32,R31,R30,R29,R28,R27,R26,R25,R24,R23,R22,R21,R20,R19,R18,R17,R16,R15,R14,R72,R65,R59,R58,R57,R56,R55,R54,R45,R86,R13,R12,R11,R10,R9,R8,R7,R6,R5,R79,R116,R117,R111,R110,R105,R104,R141,R140,R135,R134,R129,R128,R123,R122,R99,R98,R93,R92,R91,R90,R94,R95,R96,R97,R100,R101,R102,R103,R106,R108,R109,R112,R113,R114	85	P0.0ACT-ND	RES 0.0 OHM 1/8W 0805 SMD
7	R75,R74,R73,R71,R68,R67,R66,R64,R61,R60,R82,R85,R87,R81,R80,R78	16	P1.0KDACT-ND	RES 1.0K OHM 1/8W .1 % 0805 SMD
8	R70,R69,R63,R83,R84,R76,R77	8	P3.0KDACT-ND	RES 3.0K OHM 1/8W .1 % 0805 SMD
9	R53,R52,R4,R3,R2,R1,R107	7	P10KACT-ND	RES 10K OHM 1/8W 5 % 0805 SMD
10	R51,R50,R88,R89	4	P220ACT-ND	RES 220 OHM 1/8W 5 % 0805 SMD
11	R49,R48	2	P560ACT-ND	RES 560 OHM 1/8W 5 % 0805 SMD
12	R47,R46	2	P2.7KACT-ND	RES 2.7K OHM 1/8W 5 % 0805 SMD
13	C15,C14,C13,C9,C8	5	445-1419-1-ND	CAP CER 1UF 25V 10 % X5R 0805
14	C16,C17	2	445-5970-1-ND	CAP CER 3.3UF 25V 10 % X7R 0805
15	C18,C19,C20,C21,C22,C23,C24,C25,C27,C28,C29,C30,C5,C4,C3,C2,C1,C55,C54,C53,C52,C51,C50,C49,C48,C47,C46,C45,C44,C43,C42,C41,C40,C36,C38,C39	36	445-1351-1-ND	CAP CER 0.1UF 25V 10 % X7R 0805
16	C26,C7,C6,C35,C37	5	445-5984-1-ND	CAP CER 10UF 25V 10 % X5R 0805
17	C31,C32,C33,C34	4	N/A	Not populated
18	F1,F2,F3	3	MFU0805.50CT-ND	FUSE .50A 0805 VFAST SMD
19	J2,J3	2	WM8072-ND	CONN HEADER 2POS .100" STR TIN
20	J5	1	WM8134-ND	CONN HEADER 40POS .100" STR TIN
21	J7	1	A98075-ND	TERM BLOCK 12POS SIDE ENT 2.54MM
22	D9,D8,D7,D6,D5,D10	6	754-1128-1-ND	LED 2X1.2MM 625NM RD WTR CLR SMD
23	U3	1	516-1730-5-ND	OPTOCOUPLER PHOTOTRANS 6-SMD GW
24	D4,D3,D2,D1	4	1N4003-E3/54GICT-ND	DIODE GP 200V 1A DO204AL
25	C12,C11,C10	3	P5182-ND	CAP ALUM 100UF 50V 20 % RADIAL
26	P73,P58,P57,...	70	N/A	This is a PCB footprint only
27	J13,J12,J11,J10,J9	5	J121-ND, J119-ND, J312-ND, J120-ND	CONN JACK TEST VERTICAL BLACKx2, WHITEx1, BLUEx1, REDx1
28	U11	1	122-1388-ND	IC CPLD 1.6K 72MCELL 64-VQFP
29	J22	1	WM8078-ND	CONN HEADER 8POS .100" STR TIN
30	J23,J24,J4	3	WM8077-ND	CONN HEADER 7POS .100" STR TIN
31	J6	1	WM8080-ND	CONN HEADER 10POS .100" STR TIN
32	J8	1	A98338-ND	TERM BLOCK 8POS SIDE ENT 2.54MM
33	J1	1	H10644-ND	CONN RECEPT R/A 100POS 1.27MM
34	J19,J18,J20,J17,J21,J16,J15,J14	8	609-1960-ND	CONN PCI EXPRESS 36POS VERT PCB

Table 13: Electrophysiology Interface Board Bill of Materials, assembly

## D Revision 1.0 Errata

Table 14 is a description of the problems with the first revision of the Electrophysiology Interface Board that require rework of the PCB for it to work as desired or that should be fixed if another board is ordered (Rev1.1)

Affected parts	Problem	Implementation	Solution
D2	D2 is forward bias under normal operation, it shorts AGND and -VA	Immediate	Flip diode around
C13	Reference isn't on silks	Next Rev.	Move reference in Pcb-new
U3/4	No test point on SHDN of U4	Next Rev.	Add test point in Eechema
U4	Output doesn't drop when in shutdown (capacitors stay charged)	Next Rev.	Add load resistor, $220\Omega$ tested, try $10\text{k}\Omega$
P1	Reference isn't on silks	Next Rev.	Move reference in Pcb-new
U11	JTAG TDI and TDO swapped	Immediate	Don't populate R92 and R93, use pads to reroute signal
C1	Reference isn't on silks	Next Rev.	Move reference in Pcb-new
U5/7	Reference is under part	Next Rev.	Move reference in Pcb-new

Table 14: Electrophysiology Interface Board revision 1.0 errata

## E Earthworm Experiment Notes

**Ground Wire** Multiple sources insist that a ground wire is necessary between the stimulating and recording electrodes [9, 12, 13, 14, 18]. In [12], it is suggested that one of the dissecting pins may be connected to ground. In [18], which is an experiment in which the

earthworm is not dissected, a piece of aluminium foil is placed on the earthworm body and connected to ground. [13] implies that a chlorided silver wire is placed under the body of earthworm and connected to ground; this is illustrated in figures 29 and 30, and it is the setup used to achieve the results in section 6.

In some of the first attempts at the experiment, I used a general purpose tin or nickel (I'm not sure which) plated solid copper core hookup wire stripped of its insulation and placed under the earthworm body and connected to ground. With the plated copper wire, I saw 60Hz noise coming out of the Preamp connected to the recording electrodes. Switching to chlorided silver wire for the ground wire under the earthworm eliminated the problem. It was suggested to me by either Dr. Miller or Mr. Mike Ellinger that copper is toxic to cells and should certainly not be used for the recording electrodes, but it seems that plated copper wire should not be used for the ground wire. It may also be that the tin or nickel plating is toxic to the worm (this is only my supposition). [12] and [18] appear to successfully use a steel pin and aluminium foil, respectively, as the ground "wire."

**Response Abnormalities** Another issue that appeared in our attempts at recreating the experiment with earthworm giant axons described in [9, 12, 13, 14] was trying to recreate the shape (biphasic) and amplitude. This issue was unrelated to the DASS hardware, specifically, as much of this behavior was observed with a commercial stimulator and a Preamp board from [10].

The expected biphasic (0V to positive to 0V to negative to 0V) shape of the combined action potentials along the nerve cord, as seen in the lateral response in figure 33, is due to the relative polarization on the nerve cord between the recording electrodes [13, 54]. It is a coincidence that the combined action potential resembles the membrane voltage during a single action potential response. It was somewhat disconcerting to see that the median response in figures 32 and 33 was monophasic (0V to positive to 0V). Although, monophasic median and lateral responses were also observed in figure 32 of [9]. Also, [54] concerns a similar experiment with the sciatic nerve of a frog, and it says that a nerve cord that is crushed at one of the recording electrode will result in a monophasic response measurement.

I hypothesize that a similar phenomenon could occur in the earthworm's nerve cord.

We also experienced inconsistent results in the amplitude of the response waveforms. The position of the recording electrodes will affect the amplitude of the response: recording electrodes placed further apart will result in a lower amplitude, as reported in [13, 54]. Consequently, it is expected that the responses measure with different earthworms will have different amplitudes. But, we experienced varying amplitudes with the same worm. One thing we observed was that when using the commercial Grass SD9 Stimulator set to send stimulation pulses at the same level about 1-5 times per second, the amplitude of the response waveforms were consistent. If the stimulation were turned off for a time and turned back on, the amplitude of the response would be different. This causes inconsistent response amplitudes when using the DASS because stimulation pulses are not happening at a consistent rate: the script run on the DASCC might be set to send one stimulation pulse at some amplitude, the results analyzed by the operator, the stimulation amplitude adjusted, and then another stimulation pulse sent. This means that stimulation pulses are sent at irregular intervals with minutes in between pulses. Moistening the nerve cord also changed the response amplitude.

Large stimulation artifacts that did not settle before the median response occurred (figure 38), abnormal (not mono or bi-phasic) shapes (figure 39), and multiple apparent responses from one stimulus (figure 40) also appeared in the early experiments. As the issues were being investigated, I focused on improving the biological experimental technique. Keeping the nerve cord moist with Ringer's solution (as suggested by [12, 13]) while also keeping the amount of solution collecting around the worm to a minimum (by wicking excess solution away with paper towel) appears to have kept the aforementioned issues from happening again (since the Aug. 10, 2012 experiments).



Figure 38: ALL0002 Aug. 10, 2012; long stimulus artifact settling time

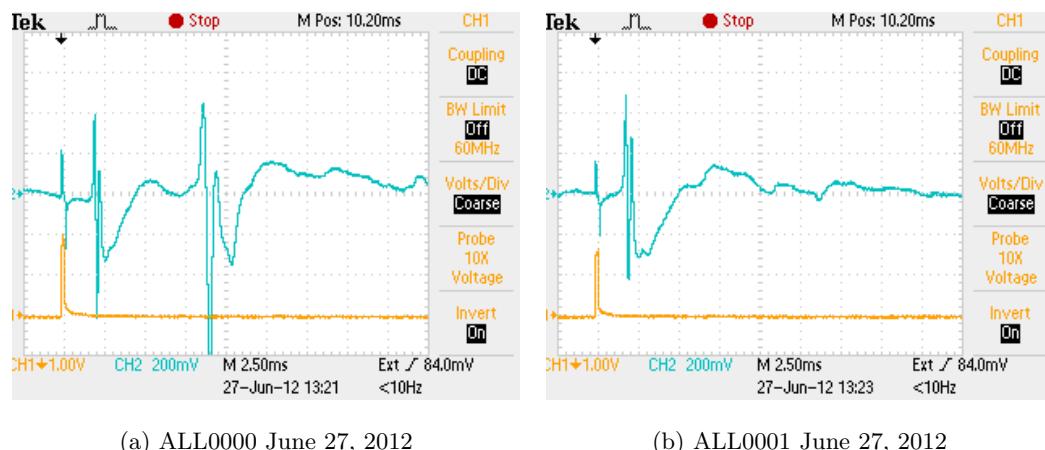
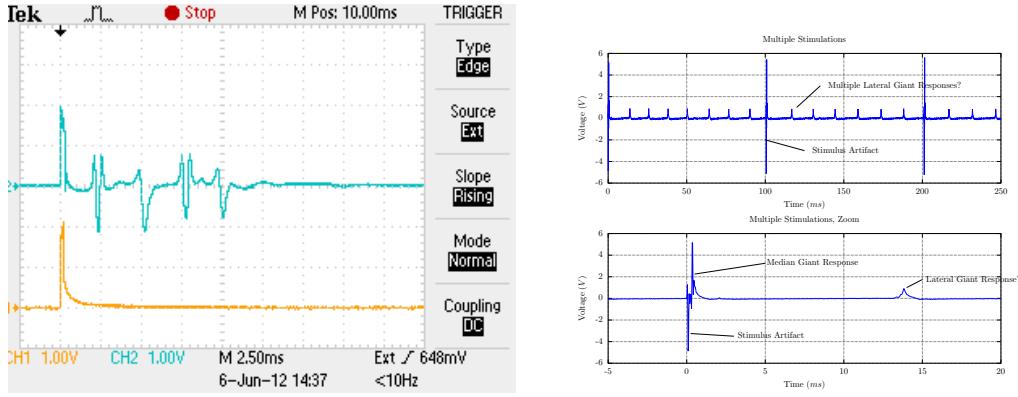


Figure 39: Abnormally shaped earthworm giant axon responses



(a) ALL0003 June 06, 2012

(b) data\_out0-multi1 May 16, 2012

Figure 40: Multiple earthworm giant axon responses per single stimulus

**Silver Wire Size** In an attempt to save money, larger diameter silver wire than is recommended in [13] was used to perform the earthworm experiment. The following is an excerpt from an email composed by me and sent to Dr. Damon A. Miller and Mr. Mike Ellinger on April 22, 2012 summarizing the cost savings:

For the silver wire, [13] says to use 0.25mm diameter wire from Warner Instruments. It looks like it can be bought here: [http://www.warneronline.com/product\\_info.cfm?ID=280&CFID=6793639&CFTOKEN=40541278](http://www.warneronline.com/product_info.cfm?ID=280&CFID=6793639&CFTOKEN=40541278)

Their silver wire is 99.99% pure, and under “pricing and ordering,” 2 meters of 0.25mm diameter wire costs \$24 not including shipping plus there’s a \$10 charge for having an order of less than \$75.

I found another website that sells 99.99% 0.635mm (0.025in) wire at \$3.00/ft. Which means we could get 6ft. for ~\$24 including shipping or ~\$15 for 3ft. Link: <http://www.ccsilver.com/silver/superfines.html>

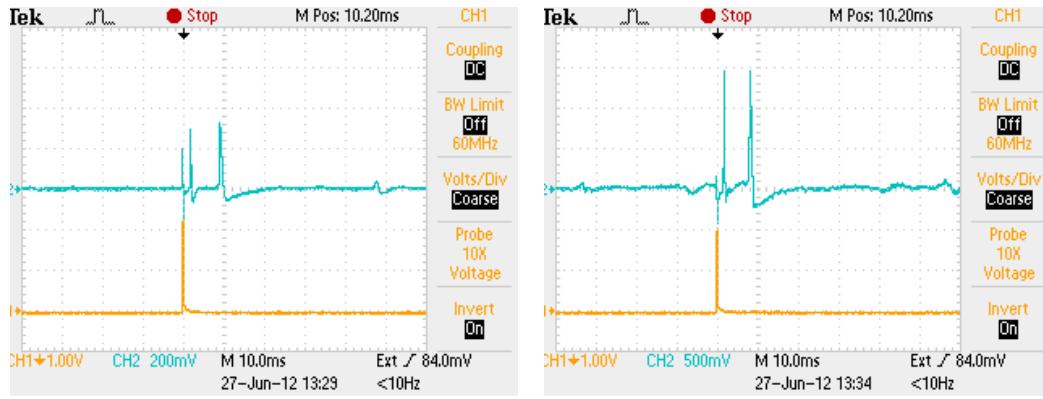
Yet another website sells 6ft. of 99.9% 0.025mm wire for ~\$10 including shipping. Link: <http://www.ottofrei.com/store/product.php?productid=21270&cat=3847&page=1> (dead)

To sum up, we can get the original medical grade, 99.99% purity wire in the

same diameter for >\$35, we can get the same purity wire but with 2.5 times the diameter for \$15, or we can get 99.9% wire in the same diameter as the experiment for \$10.

I'm thinking the 99.99% 0.635mm wire for \$15 would be an acceptable solution.

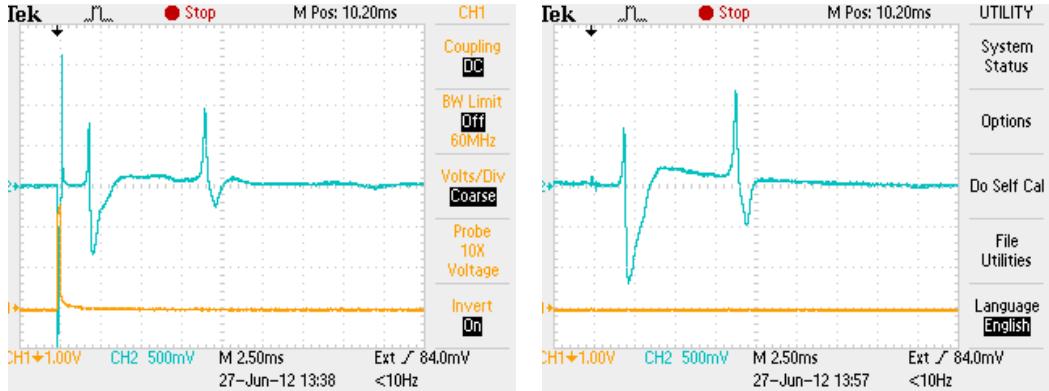
Many of the anomalies in shape and amplitude mentioned in the previous section were observed while using the 0.635mm wire from C.C. Silver for the recording electrodes. To eliminate the wire diameter as a factor in those anomalies, the 0.25mm diameter wire from Warner Instruments specified by [13] was purchased and compared with the 0.635mm wire. Both wire sizes were chlorided and an earthworm was prepared. The commercial stimulator was used along with a Preamp from [10] connected to an oscilloscope. Figure 41 shows a 3.5V stimulation with response recorded first using the 0.25mm wire from Warner Instruments, then using the 0.635mm wire from C.C. Silver. Figure 42 shows a 3.75V stimulation with response recorded first using the 0.635mm wire, then using the 0.25mm wire.



(a) ALL0004 June 27, 2012; 0.25mm wire; 3.5V stimulus

(b) ALL0005 June 27, 2012; 0.635mm wire; 3.5V stimulus

Figure 41: Recording electrode silver wire comparison: 0.25mm to 0.635mm



(a) ALL0006 June 27, 2012; 0.635mm wire;  
3.75V stimulus

(b) ALL0007 June 27, 2012; 0.25mm wire; 3.5V  
stimulus

Figure 42: Recording electrode silver wire comparison: 0.635mm to 0.25mm

Anomalies in shape and amplitude were experienced with both diameter wires, during the experiment. The figures show that similar shapes could be observed with both diameter wires. This led me to the conclusion that wire diameter was not the cause of the difficulties examined in the previous section.

## F GitHub Repository

A GitHub repository [56] has been created that contains the source files and documentation from the companion thesis [15]; experimental data and pictures from work done for section 6.4; KiCAD schematic, layout, and library files for the Electrophysiology Interface board; and the L<sup>A</sup>T<sub>E</sub>Xsource for this thesis.

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