

Next generation platform for implementing fast gates in ion trap quantum computation

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Scalable trapped-ion quantum computation relies on the development of high-fidelity fast entangling gates in a many ion crystal. Conventional geometric phase gates either suffer from scattering errors or off-resonant carrier excitations. A potential route to achieve fast entanglement is creating a standing wave which can suppress the unwanted carrier coupling.

Why Fast Gates?

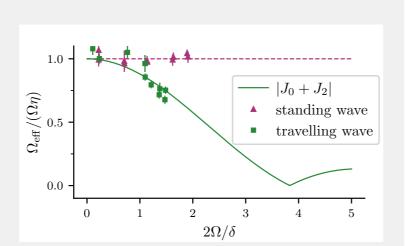
- Two qubit gates are implemented by coupling spin with motion of ions in the trap potential.
- Mølmer Sørenson (MS) interactions achieve this via a bichromatic field incident on the ions. Using travelling waves gives the Hamiltonian

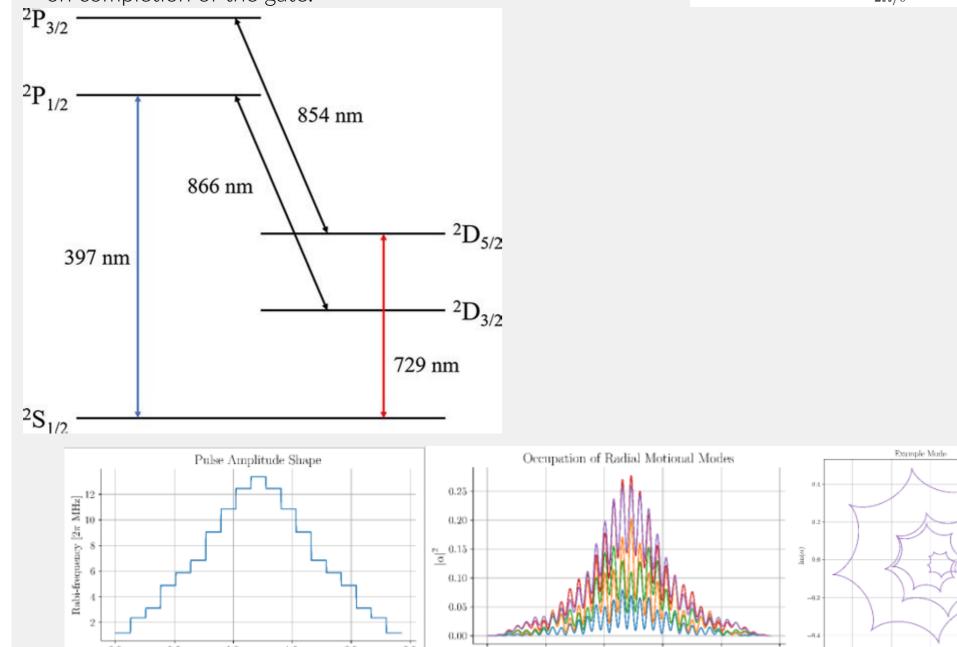
$$\hat{H}_{MS-TW} = \hbar\Omega \hat{S}_{\phi-\pi/2}\cos{(\delta t)} + \hbar\Omega\eta \hat{S}_{\phi}\cos{(\delta t)} (\hat{a}e^{-i\omega_z t} + \hat{a}^{\dagger}e^{i\omega_z t})$$
 with the first term being the carrier whilst the second is the desired coupling.

- Fast entangling gates in ion traps enable the performance of complex quantum computations in reasonable times.
- However going fast requires moving out of the adiabatic regime. With travelling wave MS gates this results in errors due to both the presence of the carrier term and exciting "spectator" modes.
- Moving into the ??interaction picture?? this Hamiltonian may be expressed as [Xref Canzz?X]:

$$\hat{H}_{MS-TW} = \hbar \eta \Omega (J_0(2\Omega/\delta) + J_2(2\Omega/\delta)) \cdot \cos{(\delta t)} \hat{S}_{\phi}(\hat{a}e^{-i\omega_z t} + \hat{a}^{\dagger}e^{i\omega_z t})$$

- Carrier term: Error results in the effective rabi frequency being modulated by (J_0+J_2) . This may be mitigated by supressing the carrier.
- Spectator excitation: Amplitude shaped pulses [ref vera] have been shown to effectively remove this "spectator" error by ensuring all the modes respective phase loops are closed on completion of the gate.



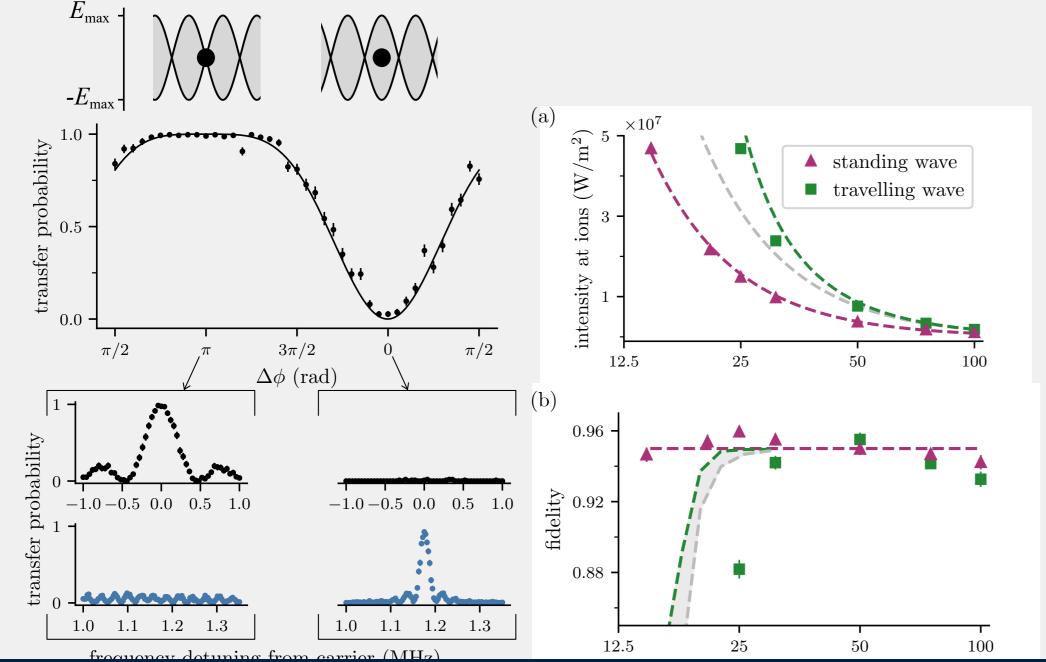


Fast Gates with a Lattice

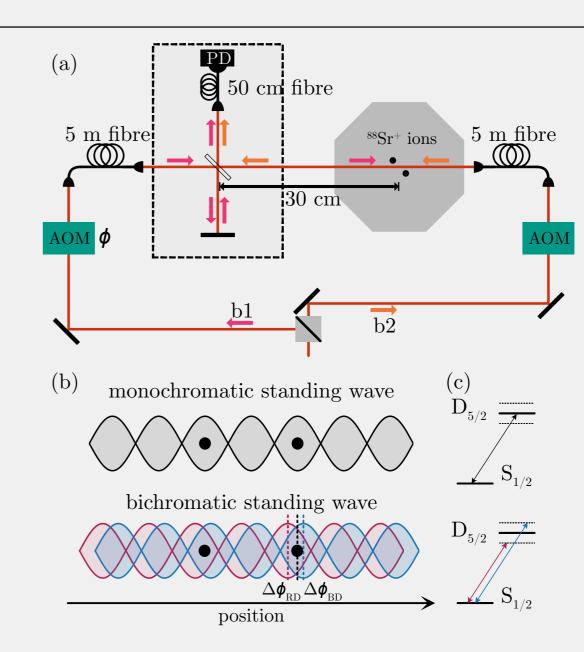
Bichromatic Lattice Hamiltonian where ions are seperated by $n\lambda$:

$$\hat{H}_{MS-SW} = \hbar 2\Omega \hat{S}_{\phi} \cos{(\delta t)} \sin{(\Delta \phi/2)} + \hbar 2\Omega \eta \hat{S}_{\phi} \cos{(\delta t)} (\hat{a}e^{-i\omega_z t} + \hat{a}^{\dagger}e^{i\omega_z t}) \cos{(\Delta \phi/2)}$$

- Setting $\Delta\phi=0$ (ions sitting at antinodes) we entirely null the carrier term and maximise sideband coupling.
- Enables fast gates by preventing the saturation effect seen in the travelling MS.
- Using lattice gives complete control over phase visible to ions.



Phase Stabilization



- Optical lattice requires phase stabilisation to perform coherent interactions.
- Phase stabilised passively using enclosure and actively by two-step process:
- 1) Fast drifts removed utilising interference of light from the two branches on a photodiode (PD). 2) As PD lockpoint is 30 cm away from ions, a second feedback loop using the ion as a sensor is required. We do this by performing a $\pi/2$ -pulse using arm 1 ($\pi/2$, b1) followed immediately by a $\pi/2$ -pulse using arm 2 ($\pi/2$, b2). This is equivalent to a zero-delay Ramsey sequence, which gives a signal sensitive on the difference in phase between the two pulses, hence the relative phase between the branches.
- No detriment using lattice: Standard Randomized Benchmarking gave quality of our single qubit rotations per gate to be $\epsilon = 0.173(3)\%$ for a travelling wave and $\epsilon = 0.144(3)\%$ for the lattice.

New Platform

- whats new: double NA, Ca40, NPL trap (3D heating rates), MuMetal shield, perm magnets.
- quadropole used.
- "In practice, the dominant error source in [quadropole] gates is laser frequency noise resonant with the carrier transition, uncontrolled light shifts arising from the carrier, and laser phase noise at time scales comparable with the gate; all of these are exacerbated by the relatively small Lamb-Dicke parameter (typically 0.05), which also sets a practical limit to the gate speed because it limits gates to the adiabatic regime [Roos 2008]."
- fig: solidworks of new experiment
- fig: array of single addressing SW

