Capacitors are undeterminded. Some could be measured and others are guessed based on size and proximity to measured ones.
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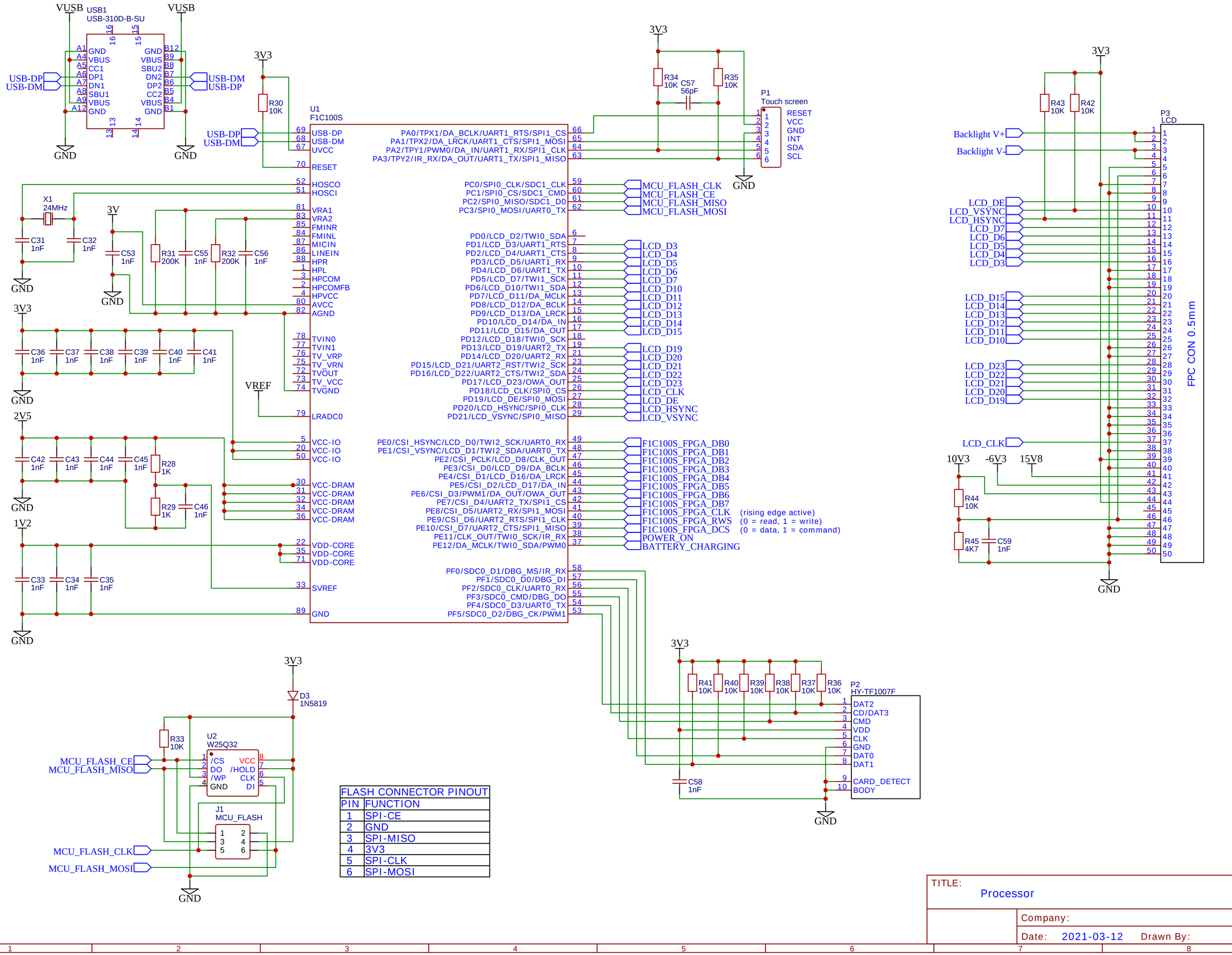

FLASH CONNECTOR PINOUT	
PIN	FUNCTION
1	SPI-CE
2	GND
3	SPI-MISO
4	3V3
5	SPI-CLK
6	SPI-MOSI

TITLE: Processor			REV: 1.0
	Company:		Sheet: 1/4
	Date: 2021-03-12	Drawn By:	

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FPGA Configuration scheme is Active Serial 3V3 (MSEL inputs)

For the ADC's offset binary output is selected (DFS input low)
The data align mode is enabled (S1, S2 inputs high)

U3
EP4CE6E22C8N or AL3-10

JTAG / CONFIGURATION
TDI
TDO
TCK
TMS
MSEL0
MSEL1
MSEL2
nCE
DCLK
CONF_DONE
nCONFIG
nSTATUS

CLOCK INPUTS
CLK1,DIFFCLK_0n
CLK2,DIFFCLK_1p
CLK3,DIFFCLK_1n
CLK4,DIFFCLK_2p
CLK5,DIFFCLK_2n
CLK6,DIFFCLK_3p
CLK7,DIFFCLK_3n

DIGITAL POWER SUPPLY
VCCINT
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
GND
GND (PAD)

ANALOG POWER SUPPLY
VCCA1
VCCD_PLL1
GNDA1
VCCA2
VCCD_PLL2
GNDA2

BANK 1
IO F1C100S_FPGA_CLK
IO F1C100S_FPGA_RWS
IO F1C100S_FPGA_DCS
(DATA1,ASDO),DIFFIO_L1n,IO FPGA_Conf_ASDO
VREFB1N0,IO
(FLASH_nCE,nCSO),DIFFIO_L2p,IO FPGA_Conf_nCE
(DQS0L/CQ1L,DPCLK0),DIFFIO_L4p,IO
DIFFIO_L4n,IO
(DATA0),IO FPGA_Conf_Data

BANK 2
DIFFIO_L6n,IO
(DQS1L/CQ1L#,DPCLK1),DIFFIO_L8p,IO
VREFB2N0,IO
RUP1,IO
RDN1,IO
IO

BANK 3
DIFFIO_B1p,IO FPGA_EEPROM_SDA
DIFFIO_B1n,IO FPGA_EEPROM_SCL
(DQS1B/CQ1B#,DPCLK2),IO FPGA_BACKLIGHT_PWM
PLL1_CLKOUTp,IO
PLL1_CLKOUTn,IO
VREFB3N0,IO
(DQ1B),DIFFIO_B9p,IO
(DQ1B),DIFFIO_B9n,IO
(DQ1B),DIFFIO_B10p,IO
DIFFIO_B11p,IO
DIFFIO_B11n,IO ADC1_ENCB

BANK 4
DIFFIO_B12p,IO ADC1_D7A
DIFFIO_B12n,IO ADC1_D6A
(DQ1B),DIFFIO_B15p,IO ADC1_D5A
(DQ1B),DIFFIO_B16p,IO ADC1_D4A
(DQ1B),DIFFIO_B16n,IO ADC1_D3A
IO ADC1_D2A
VREFB4N0,IO ADC1_D1A
(DQ1B),RUP2,IO ADC1_D0A
(DQ1B),RDN2,IO ADC1_D0B
(DQS0B/CQ1B,DPCLK3),DIFFIO_B20n,IO ADC1_D1B
IO ADC1_D2B
DIFFIO_B21p,IO ADC1_D3B
DIFFIO_B21n,IO ADC1_D4B
DIFFIO_B22p,IO ADC1_D5B

BANK 5
IO ADC1_D6B
IO ADC1_D7B
IO ADC1_ENCA
RUP3,IO
RDN3,IO
VREFB5N0,IO
IO ADC2_ENCB
DIFFIO_R8n,IO ADC2_D7A
(DQS1R/CQ1R#,DPCLK4),DIFFIO_R8p,IO ADC2_D6A
(DEV_OE),DIFFIO_R7n,IO ADC2_D5A
(DEV_CLRn),DIFFIO_R7p,IO ADC2_D4A

BANK 6
(INT DONE),DIFFIO R4n,IO ADC2_D0B
(CRC ERROR),DIFFIO_R4P,IO ADC2_D1B
IO ADC2_D2B
(nCEO),DIFFIO_R3n,IO ADC2_D3B
(CLKUSR),DIFFIO R3p,IO ADC2_D4B
(DQS0R/CQ1R,DPCLK5),IO ADC2_D5B
VERFB6N0,IO ADC2_D6B
DIFFIO_R1n,IO ADC2_D7B

BANK 7
(DQS0T/CQ1T,DPCLK6),DIFFIO_T20p,IO ADC2_ENCA
DIFFIO_T19p,IO ADC2_OFFSET
PLL2_CLKOUTn,IO ADC1_OFFSET
PLL2_CLKOUTp,IO
(DQ1T),RUP4,IO
(DQ1T),RDN4,IO
VREFB7N0,IO
(DQ1T),DIFFIO_T16n,IO
DIFFIO_T16p,IO
DIFFIO_T13p,IO
IO
DIFFIO_T12n,IO
DIFFIO_T12p,IO

BANK 8
DIFFIO_T11n,IO
DIFFIO_T11p,IO
(DQ1T),(DATA2),DIFFIO_T10n,IO
(DQ1T),(DATA3),DIFFIO_T10p,IO
(DQ1T),DIFFIO_T8n,IO F1C100S_FPGA_DB0
VREFB8N0,IO F1C100S_FPGA_DB1
(DQ1T),(DATA5),IO F1C100S_FPGA_DB2
(DATA6),IO F1C100S_FPGA_DB3
DIFFIO_T5p,IO F1C100S_FPGA_DB4
(DQS1T/CQ1T#,DPCLK7),DIFFIO_T2p,IO F1C100S_FPGA_DB5
(DQ1T),DIFFIO_T1n,IO F1C100S_FPGA_DB6
(DM1T),DIFFIO_T1p,IO F1C100S_FPGA_DB7

U7
AD9288BSTZ-100
ADC2_D0A
ADC2_D1A
ADC2_D2A
ADC2_D3A
ADC2_D4A
ADC2_D5A
ADC2_D6A
ADC2_D7A
ADC2_D0B
ADC2_D1B
ADC2_D2B
ADC2_D3B
ADC2_D4B
ADC2_D5B
ADC2_D6B
ADC2_D7B
(rising edge active)
(0 = read, 1 = write)
(0 = data, 1 = command)
AINA
REFINA
REFINB
REFOUT
AINB
ENCA
ENCB
DFS
R22 200 ANALOG2_ADC_INPUT
C23 1nF
ADC2_ENCA
ADC2_ENCB
R25 1K
R24 1K
ADC2_OFFSET
C27 1nF
C26 1nF
C25 1nF

U8
AD9288BSTZ-100
ADC1_D0A
ADC1_D1A
ADC1_D2A
ADC1_D3A
ADC1_D4A
ADC1_D5A
ADC1_D6A
ADC1_D7A
ADC1_D0B
ADC1_D1B
ADC1_D2B
ADC1_D3B
ADC1_D4B
ADC1_D5B
ADC1_D6B
ADC1_D7B
R23 200 ANALOG1_ADC_INPUT
C24 1nF
ADC1_ENCA
ADC1_ENCB
R27 1K
R26 1K
ADC1_OFFSET
C28 1nF
C29 1nF
C30 1nF

R13 1K ANALOG1_RELAIS1
R14 1K ANALOG1_RELAIS2
R15 1K ANALOG2_RELAIS2
R16 1K ANALOG1_RELAIS3
R17 1K ANALOG2_RELAIS3
R18 1K ANALOG2_RELAIS1
R19 1K ANALOG1_AC_DC
R20 1K ANALOG2_AC_DC
R21 1K 1KHZ_CALIB_SIG

U4
W25Q80
/CS
DO
/WP
GND
VCC
/HOLD
CLK
DI
R1 33
FPGA_Conf_nCE
FPGA_Conf_Data
FPGA_Conf_CLK
FPGA_Conf_ASDO
J2
FPGA_FLASH

U5
N24C04
A0
A1
A2
VSS
VCC
WP
SCL
SDA
FPGA_EEPROM_SCL
FPGA_EEPROM_SDA
J3
FPGA_EEPROM

D1 1N5819
D2 1N5819

X2
50MHz
E/D
GND
VDD
OUT

FPGA_Conf_CLK

R8 10K
R11 10K
R12 10K
R10 10K
R9 10K
R7 1K
R6 10K
R5 10K
R4 33
R2 10K
R3 10K

C13 1nF
C14 1nF
C8 1nF
C9 1nF
C11 1nF
C7 1nF
C10 1nF
C12 1nF
C1 1nF
C2 1nF
C5 1nF
C4 1nF
C3 1nF
C6 1nF
L1 2200Ω
L2 2200Ω
L3 2200Ω
L4 2200Ω
C18 1nF
C17 1nF
C16 1nF
C15 1nF
C19 1nF
C20 1nF
C21 1nF
C22 1nF

TITLE:	Data acquisition
REV:	1.0
Company:	
Sheet:	2/4
Date:	2021-03-23
Drawn By:	

Capacitors are undeterminded. Some could be measured and others are guessed based on size and proximity to measured ones.
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ANALOG1_AC_DC
RF1 BNC
C101 100nF
C100 100nF
U18 KAQY214STLD
C99 150nF
R62 150
C102 150nF
R63 3M
C103 150nF
R64 2M7
C104 150nF
C105 150nF
R65 1M2
R68 1M8
C108 1nF
C107 1nF
R66 75K
C106 1nF
C109 1nF
C110 1nF
R67 360K
C111 1nF
K2 HFD4/3-S1R
Q2 SS8550
ANALOG1_RELAIS2
K3 HFD4/3-S1R
Q3 SS8550
ANALOG1_RELAIS3
2V5
U17 RS8751XF
C112 1nF
C113 1nF
R69 3K
C114 1nF
K1 HFD4/3-S1R
R70 3K
C115 1nF
Q1 SS8550
ANALOG1_ADC_INPUT
ANALOG1_RELAIS1
3V3
VRF1
GND

C116 1nF
R71 100
C134 1nF
C135 1nF

R81 200
R82 1
D12 1N5819
D11 1N5819
U21 TL432

ANALOG2_AC_DC
RF2 BNC
C131 100nF
C132 100nF
U19 KAQY214STLD
C133 150nF
R80 150
C130 150nF
R79 3M
C129 150nF
R78 2M7
C128 150nF
C127 150nF
R77 1M2
R74 1M8
C124 1nF
C125 1nF
R76 75K
C126 1nF
C123 1nF
C122 1nF
R75 360K
C121 1nF
K5 HFD4/3-S1R
Q5 SS8550
ANALOG2_RELAIS2
K4 HFD4/3-S1R
Q4 SS8550
ANALOG2_RELAIS3
2V5
U20 RS8751XF
C120 1nF
C119 1nF
R73 3K
C118 1nF
K6 HFD4/3-S1R
R72 3K
C117 1nF
Q6 SS8550
ANALOG2_ADC_INPUT
ANALOG2_RELAIS1
3V3
VRF1
GND

TITLE: Analog Input		REV: 1.0
	Company:	Sheet: 3/4
	Date: 2021-03-23 Drawn By:	

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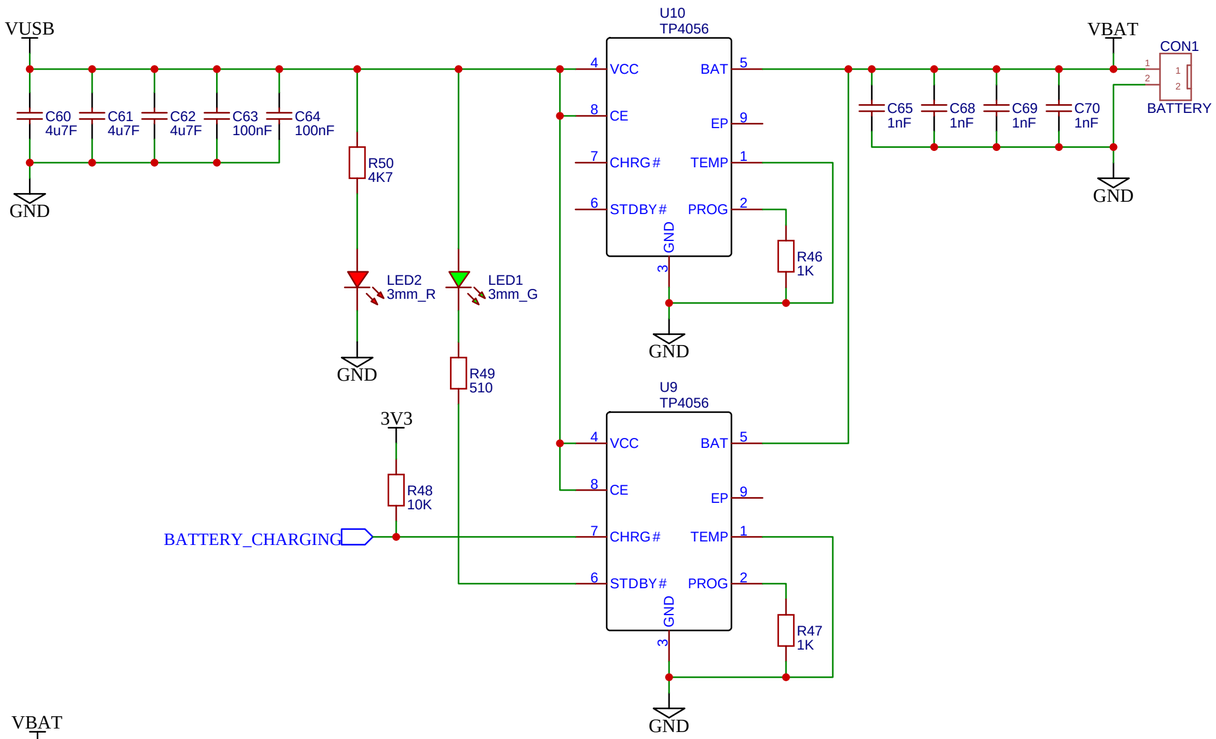

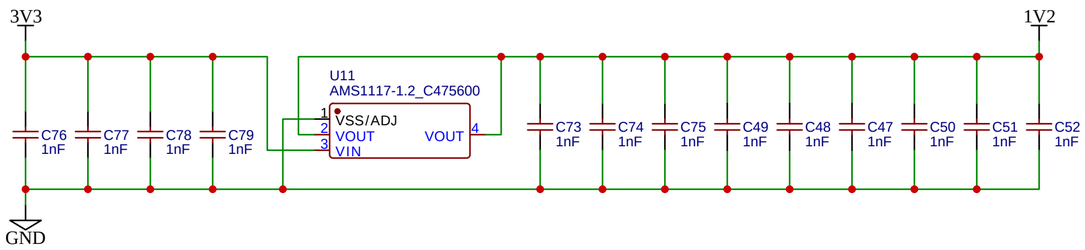

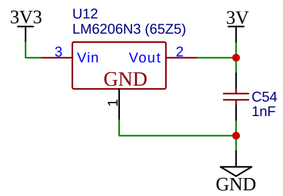

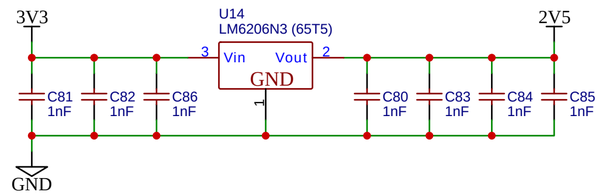

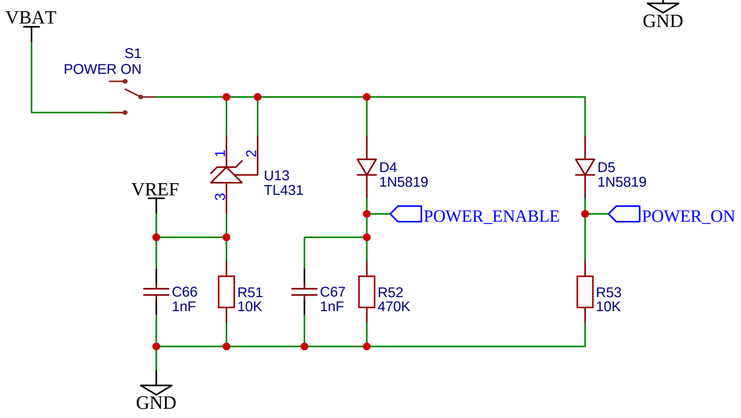

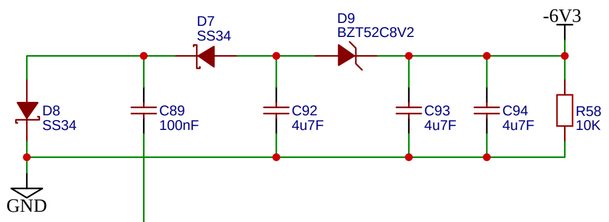

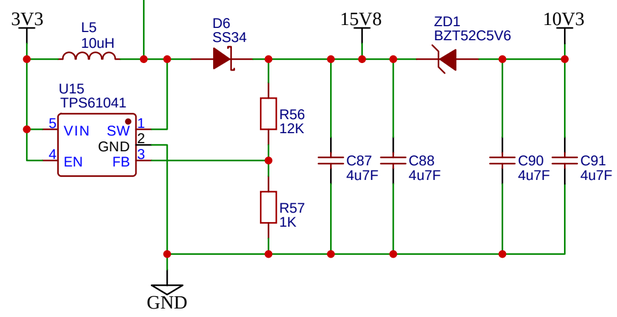

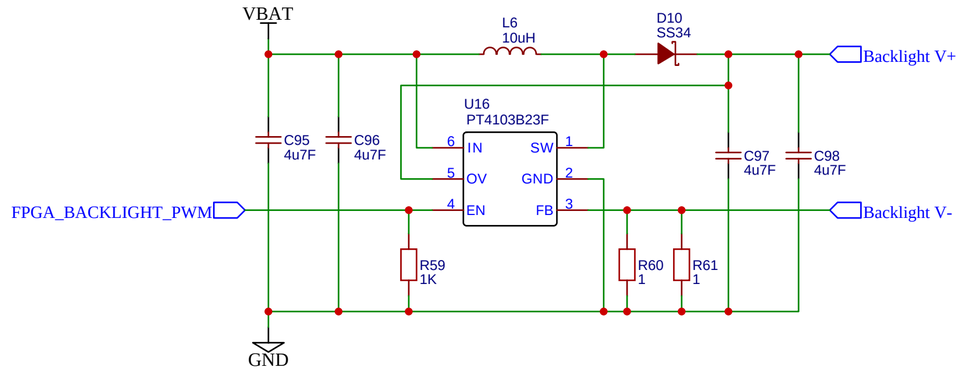

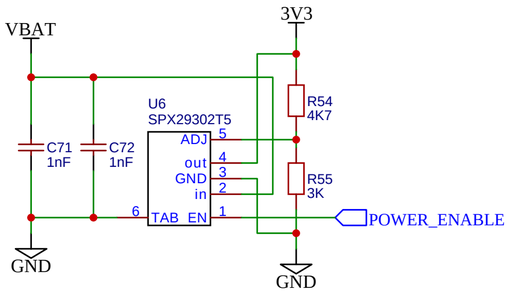

TITLE: Power Supply		REV: 1.0
	Company:	Sheet: 4/4
	Date: 2021-03-23 Drawn By:	