ADS131A0x 2- or 4-Channel, 24-Bit, Analog Front-Ends for Power Monitoring, Control, and Protection

1 Features

- 2 or 4 Simultaneously-Sampling Differential Inputs
- Data Rates Up to 128 kSPS
- Noise Performance:
  - Single-Channel Accuracy: Better Than 0.1% at 10,000:1 Dynamic Range
  - ENOB: 19.1 Bits at 8 kSPS
  - THD: –100 dB at 50 Hz and 60 Hz
- Integrated Negative Charge Pump
- Flexible Analog Power-Supply Operation:
  - Using Negative Charge Pump: 3.0 V to 3.45 V
  - Unipolar Supply: 3.3 V to 5.5 V
  - Bipolar Supply: ±2.5 V
- Digital Supply: 1.65 V to 3.6 V
- Low-Drift Internal Voltage Reference: 4 ppm/°C
- ADC Self Checks
- Cyclic Redundancy Check (CRC) and Hamming Code Error Correction on Communications
- Multiple SPI™ Data Interface Modes:
  - Asynchronous Interrupt
  - Synchronous Master and Slave
- Package: 32-Pin TQFP
- Operating Temperature Range: –40°C to +125°C

2 Applications

- Industrial Power Applications
- Single-Phase and Polyphase Energy Monitoring
- Protection Relays, Circuit Breakers
- Power Quality Meters
- Data Acquisition Systems

3 Description

The ADS131A02 and ADS131A04 are two- and four-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converters (ADCs). The wide dynamic range, scalable data rates, and internal fault monitors make the ADS131A02 and ADS131A04 ideally-suited for energy monitoring, protection, and control applications. The ADC inputs can be independently and directly interfaced to a resistor-divider network, a transformer to measure voltage or current, or a Rogowski coil to measure current. Flexible power-supply options, including an internal negative charge pump, are available to maximize the effective number of bits (ENOB) for high dynamic range applications.

Asynchronous and synchronous master and slave interface options are available, providing ADC configuration flexibility when chaining multiple devices in a single system. Several interface checks, ADC startup checks, and data integrity checks can be enabled on the interface to report errors in the ADC and during data transfer.

The ADS131A02 and ADS131A04 support data rates up to 128 kSPS. The complete analog front-end (AFE) solutions are packaged in a 32-pin TQFP package and are specified over the industrial temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS131A0x	TQFP (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

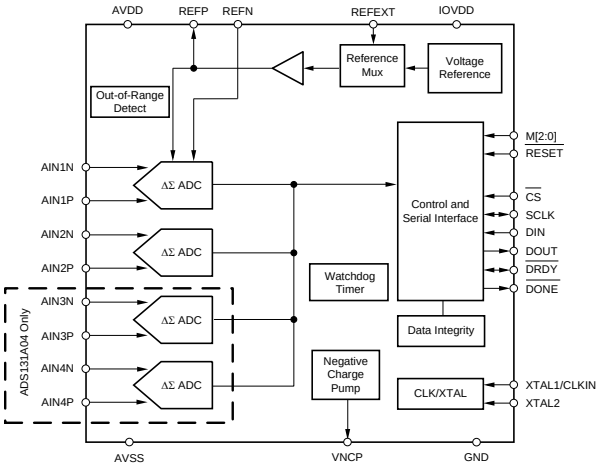


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

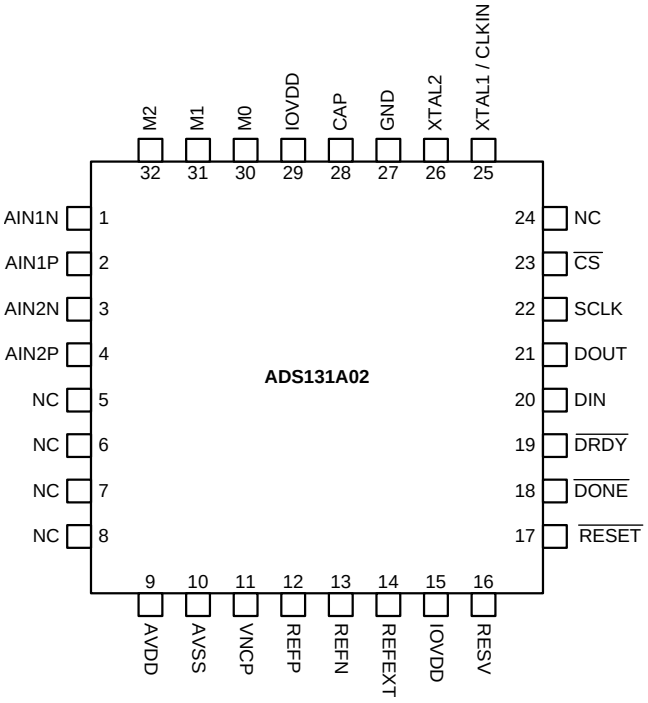
Changes from Original (March 2016) to Revision A	Page
• Released to production	1

5 Device Comparison Table

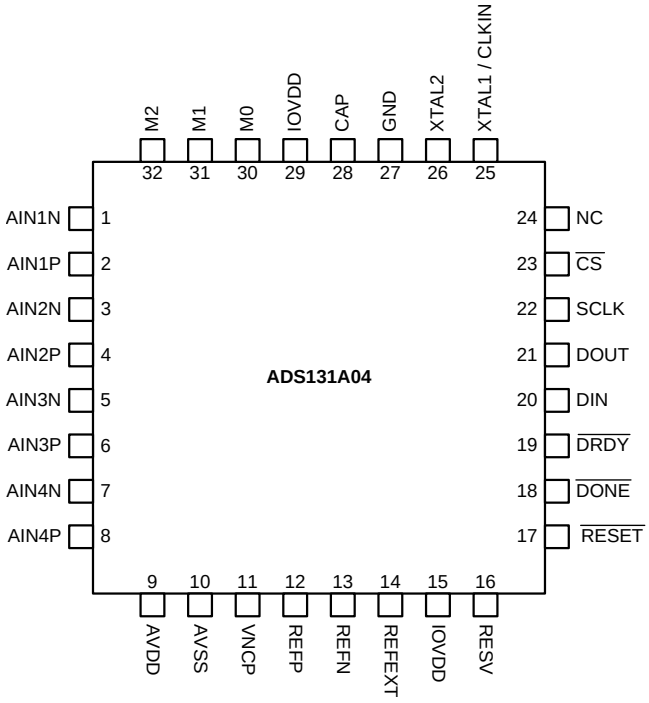
PRODUCT	NO. OF ADC CHANNELS	MAXIMUM SAMPLE RATE (kSPS)
ADS131A02	2	128
ADS131A04	4	128

6 Pin Configuration and Functions

ADS131A02: PBS Package
32-Pin TQFP
Top View



ADS131A04: PBS Package
32-Pin TQFP
Top View



Pin Functions

PIN			I/O	DESCRIPTION[1]
NAME	NO.			
	ADS131A02	ADS131A04		
AIN1N	1	1	Analog input	Negative analog input 1
AIN1P	2	2	Analog input	Positive analog input 1
AIN2N	3	3	Analog input	Negative analog input 2
AIN2P	4	4	Analog input	Positive analog input 2
AIN3N	—	5	Analog input	Negative analog input 3
AIN3P	—	6	Analog input	Positive analog input 3
AIN4N	—	7	Analog input	Negative analog input 4
AIN4P	—	8	Analog input	Positive analog input 4
AVDD	9	9	Supply	Analog supply. Decouple the AVDD pin to AVSS with a 1-µF capacitor.
AVSS	10	10	Supply	Analog ground
CAP	28	28	Analog output	Digital low-dropout (LDO) regulator output. Connect a 1-µF capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.

Pin Functions (continued)

PIN			I/O	DESCRIPTION(1)
NAME	NO.			
	ADS131A02	ADS131A04		
$\overline{CS}$	23	23	Digital input	Chip select; active low
DIN	20	20	Digital input	Serial data input
$\overline{DONE}$	18	18	Digital output	Communication DONE signal; active low
DOUT	21	21	Digital output	Serial data output. Connect a 100-kΩ pullup resistor to IOVDD.
$\overline{DRDY}$	19	19	Digital input/output	Data ready; active low; host interrupt and synchronization for multi-devices
GND	27	27	Supply	Digital ground
IOVDD	15	15	Supply	Digital I/O supply voltage. Connect a 1-µF capacitor to GND.
	29	29		
M0(2)	30	30	Digital input	Serial peripheral interface (SPI) configuration mode. IOVDD: Asynchronous interrupt mode GND: Synchronous master mode No connection(3): Synchronous slave mode; use for multi-device mode
M1(2)	31	31	Digital input	SPI word transfer size. IOVDD: 32 bit GND: 24 bit No connection(3): 16 bit
M2(2)	32	32	Digital input	Hamming code enable. IOVDD: Hamming code word validation on GND: Hamming code word validation off No connection: reserved; do not use
NC	5	—	—	Leave floating or connect directly to AVSS.
	6			
	7			
	8			
NC	24	24	Digital output	No connection
REFEXT	14	14	Analog input	External reference voltage buffered input. Connect a 1-µF capacitor to AVSS when using the internal reference.
REFN	13	13	Analog input	Negative reference voltage. Connect to AVSS.
REFP	12	12	Analog output	Positive reference voltage output. Connect a 1-µF capacitor to REFN.
$\overline{RESET}$	17	17	Digital input	System reset; active low
RESV	16	16	Digital input	Reserved pin; connect to IOVDD
SCLK	22	22	Digital input/output	Serial data clock
VNCP	11	11	Analog output	Negative charge pump voltage output. Connect a 270-nF capacitor to AVSS when enabling the negative charge pump. Connect directly to AVSS if unused.
XTAL1/CLKIN	25	25	Digital input	Master clock input, crystal oscillator buffer input
XTAL2	26	26	Digital output	Crystal oscillator connection. Leave this pin unconnected if unused.

(2) Mode signal states are latched following a power-on-reset (POR). Tie these pins high or low with a < 1-kΩ resistor.
(3) This pin can have a 10-pF capacitor to GND.

7 Specifications

7.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
AVDD to AVSS	Charge pump enabled	–0.3	3.6	V
	Charge pump disabled	–0.3	6.0	
IOVDD to GND		–0.3	3.9	V
AVSS to GND		–3.0	0.3	V
Analog input voltage	Charge pump enabled	AVSS – 1.65	AVDD + 0.3	V
	Charge pump disabled	AVSS – 0.3	AVDD + 0.3	
VNCP to AVSS		–2.5	0.3	V
VNCP to AVDD		–6.0	0.3	V
REFEXT to AVSS		AVSS – 0.3	AVDD + 0.3	V
REFN input to AVSS		AVSS – 0.05	AVSS + 0.05	V
CAP to GND		GND – 0.3	GND + 2.0	V
Digital input voltage		GND – 0.3	IOVDD + 0.3	V
Input current, continuous, any pin except supply pins		–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
Negative Charge Pump Enabled (VNCPEN(1) = 1)						
	Analog supply voltage	V_{AVDD} to V_{AVSS}	3.0	3.3	3.45	V
		V_{AVDD} to V_{GND}	3.0	3.3	3.45	
		V_{AVSS} to V_{GND}	–0.05	0	0.05	
	Digital supply voltage(2)	V_{IOVDD} to V_{GND}	1.65	3.3	3.6	V
Negative Charge Pump Disabled (VNCPEN = 0)						
	Analog supply voltage	V_{AVDD} to V_{AVSS}	3.0	5.0	5.5	V
		V_{AVDD} to V_{GND}	1.5	2.5	5.5	
		V_{AVSS} to V_{GND}	–2.75	–2.5	0.05	
	Digital supply voltage(2)	V_{IOVDD} to V_{GND}	1.65	3.3	3.6	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{AINxP} – V_{AINxN}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
V_{CM}	Common-mode input voltage(3)		V_{AVSS}		V_{AVDD}	V
V_{AINxP}, V_{AINxN}	Absolute input voltage		V_{AVSS}		V_{AVDD}	V
EXTERNAL REFERENCE						
	Reference input voltage	REFEXT – REFN	2.0	2.5	V_{AVDD} – 0.5	V_{REF}
V_{REFN}	Reference negative input			V_{AVSS}		V
V_{REFEXT}	External reference positive input		V_{REFN} + 2.0	V_{REFN} + 2.5	V_{AVDD} – 0.5	V
EXTERNAL CLOCK SOURCE						
f_{CLKIN}	External clock input frequency	IOVDD > 2.7 V	0.4	16.384	25	MHz
		IOVDD ≤ 2.7 V	0.4	8.192	15.6	
	XTAL clock frequency(4)			16.384	16.5	MHz
f_{SCLK}	SCLK input to derive f_{MOD}	CLKSRC bit = 1, $f_{SCLK} = f_{ICLK}$, IOVDD > 2.7 V	0.2	16.384	25	MHz
		CLKSRC bit = 1, $f_{SCLK} = f_{ICLK}$, IOVDD ≤ 2.7 V	0.2	8.192	15.6	
DIGITAL INPUTS						
	Digital input voltage		GND		IOVDD	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		125	°C

(1) VNCPEN is bit 7 of the A_SYS_CFG register.
(2) Tie IOVDD to the CAP pin if IOVDD ≤ 2.0 V.
(3) CMRR is measured with a common-mode signal of (V_{AVSS} + 0.3 V) to (V_{AVDD} – 0.3 V).
(4) Set IOVDD > 3.0 V to use a crystal across the XTAL1/CLKIN and XTAL2 pins.

7.4 Thermal Information

THERMAL METRIC[1]		ADS131A0x PBS (TQFP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_s	Input capacitance			3.5		pF
Z_{in}	Differential input impedance	f_{MOD} = 4.096 MHz		130		kΩ
ADC PERFORMANCE						
	Resolution			24		Bits
	Gain			1, 2, 4, 8, 16		
	Data rate	f_{MOD} = 4.096 MHz	1		128	kSPS
DC PERFORMANCE						
	Dynamic range		105	111		dB
		$V_{AVDD} – V_{AVSS}$ = 5 V, V_{REF} = 4 V, VNCPEN bit = 0		115		
		All other settings	See *Noise Measurements* section			
INL	Integral nonlinearity	Best fit		8	20	ppm
	Offset error			500		µV
	Offset drift			1.2	3	µV/°C
	Gain error	Excluding voltage reference and reference buffer error		±0.03		% of FS
	Gain drift	Excluding voltage reference and reference buffer error		0.25	2	ppm/°C
AC PERFORMANCE						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz or 60 Hz		100		dB
PSRR	Power-supply rejection ratio	AVDD supply, f_{PS} = 50 Hz and 60 Hz		85		dB
		IOVDD supply, f_{PS} = 50 Hz and 60 Hz		105		
	Crosstalk	f_{IN} = 50 Hz and 60 Hz		–125		dB
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz or 60 Hz, V_{REF} = 2.442 V, V_{IN} = –20 dBFS, normalized		111		dB
		f_{IN} = 50 Hz or 60 Hz, V_{REF} = 4.0 V, V_{IN} = –20 dBFS, normalized		115		
THD	Total harmonic distortion	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = –0.5 dBFS		–103.5		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = –0.5 dBFS		101		dB
SFDR	Spurious-free dynamic range	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = –0.5 dBFS		105		dB
EXTERNAL REFERENCE						
	Reference buffer offset	T_A = 25°C		170		µV
	Reference buffer offset drift	–40°C ≤ T_A ≤ +125°C		1.1	4.3	µV/°C
	REFEXT input impedance			50		MΩ

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL REFERENCE VOLTAGE (REFP – REFN)							
V_{REF}	Reference output voltage	VREF_4V bit = 0			2.442		V
		VREF_4V bit = 1, $V_{AVDD} – V_{AVSS}$ > 4.5 V			4.0		
	Accuracy				±0.1%		
	Temperature drift	Including reference buffer drift, –40°C ≤ T_A ≤ +125°C			4	20	ppm/°C
	Start-up time	REFEXT = 1-µF to AVSS, settled to 1%			0.2		ms
		REFEXT = 1-µF to AVSS, settled to 0.1%			1.2		
		REFEXT = 1-µF to AVSS, settled to 0.01%			250		
	REFP source capability				100		µA
EXTERNAL CLOCK SOURCE							
f_{ICLK}	Internal ICLK frequency (SCLK output in master mode)	CLKSRC bit = 0		0.2	8.192	12.5	MHz
f_{MOD}	ADC modulator frequency	High-resolution mode	VNCPEN bit = 0	0.1	4.096	4.25	MHz
			VNCPEN bit = 1	0.512	4.096	4.25	
		Low-power mode	VNCPEN bit = 0	0.1	1.024	1.05	
			VNCPEN bit = 1	0.512	1.024	1.05	
DIGITAL INPUT/OUTPUT							
V_{IH}	High-level input voltage			0.8 IOVDD		IOVDD	V
V_{IL}	Low-level input voltage			GND		0.2 IOVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA		0.8 IOVDD			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA				0.2 IOVDD	V
I_{IN}	Input current	0 V < $V_{Digital\ Input}$ < IOVDD		–10		10	µA
POWER-SUPPLY							
	Power dissipation	Standby mode, f_{CLKIN} = 16.384 MHz			2.6		mW
POWER-SUPPLY (Negative Charge Pump Enabled, VNCPEN = 1)							
VNCP	Negative charge pump output voltage			–2.25	–1.95	–1.65	V
	AVDD current	ADS131A02, high-resolution mode			3.2		mA
		ADS131A02, low-power mode			0.9		
		ADS131A04, high-resolution mode			4.0		
		ADS131A04, low-power mode			1.1		
	IOVDD current	ADS131A02, high-resolution mode			0.6		mA
		ADS131A02, low-power mode			0.5		
		ADS131A04, high-resolution mode			0.8		
		ADS131A04, low-power mode			0.5		
POWER-SUPPLY (ADS131A02, VNCPEN = 1, V_{AVDD} = 3.3 V, V_{AVSS} = 0 V)							
	Power dissipation	High-resolution mode			12.5		mW
		Low-power mode			4.6		
POWER-SUPPLY (ADS131A04, VNCPEN = 1, V_{AVDD} = 3.3 V, V_{AVSS} = 0 V)							
	Power dissipation	High-resolution mode			15.8		mW
		Low-power mode			5.3		

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY (Negative Charge Pump Disabled, VNCPEN = 0, VNCP = AVSS)					
AVDD current	ADS131A02, high-resolution mode		3.0		mA
	ADS131A02, low-power mode		0.9		
	ADS131A04, high-resolution mode		4.0	4.7	
	ADS131A04, low-power mode		1.1		
IOVDD current	ADS131A02, high-resolution mode		0.6		mA
	ADS131A02, low-power mode		0.5		
	ADS131A04, high-resolution mode		0.8	1.0	
	ADS131A04, low-power mode		0.5		
POWER-SUPPLY (ADS131A02, VNCPEN = 0, V_{AVDD} – V_{AVSS} = 5 V, VNCP = AVSS)					
Power dissipation	High-resolution mode		17		mW
	Low-power mode		6.2		
POWER-SUPPLY (ADS131A04, VNCPEN = 0, V_{AVDD} – V_{AVSS} = 5 V, VNCP = AVSS)					
Power dissipation	High-resolution mode		22.7	26.8	mW
	Low-power mode		7.2		

7.6 Timing Requirements: Asynchronous Interrupt Interface Mode

over operating free-air temperature range (unless otherwise noted)

			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(CLKIN)}$	External clock period	Single device	64		40		ns
		Multiple device chaining	88		56		
$t_{w(CP)}$	Pulse duration, CLKIN high or low	Single device	32		20		ns
		Multiple device chaining	44		28		
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge		16		16		ns
$t_{d(SCS)}$	Delay time, SCLK falling edge to $\overline{CS}$ falling edge		5		4		ns
$t_{c(SC)}$	SCLK period	Single device	64		40		ns
		Multiple device chaining	88		64		
$t_{w(SCHL)}$	Pulse duration, SCLK high or low	Single device	32		20		ns
		Multiple device chaining	44		32		
$t_{d(SCCS)}$	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge		5		5		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge		5		5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge		8		8		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high		20		15		ns

7.7 Switching Characteristics: Asynchronous Interrupt Interface Mode

over operating ambient temperature range (unless otherwise noted)

			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{p(SCDOD)}$	Propagation delay time, first SCLK rising edge to DOUT driven			28		15	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT			26		15	ns
$t_{h(LSB)}$	Hold time, last SCLK falling edge to DOUT 3-state	HIZDLY = 00	6	30	6	20	ns
		HIZDLY = 01	8	37	8	27	
		HIZDLY = 10	10	43	10	43	
		HIZDLY = 11	12	47	12	47	
$t_{p(CSDR)}$	Propagation delay time, $\overline{CS}$ rising edge to $\overline{DRDY}$ rising edge			2.0		2.0	t_{ICLK}

7.8 Timing Requirements: Synchronous Master Interface Mode

over operating free-air temperature range (unless otherwise noted)

			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(CLKIN)}$	External clock period	Single device	64		40		ns
		Multiple device chaining	88		56		
$t_{w(CP)}$	Pulse duration, CLKIN high or low	Single device	32		20		ns
		Multiple device chaining	44		28		
$t_{c(SC)}$	SCLK period		$2t_{CLKIN}$		$2t_{CLKIN}$		ns
$t_{w(SCHL)}$	Pulse duration, SCLK high or low		t_{CLKIN}		t_{CLKIN}		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge		5		5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge		8		8		ns

7.9 Switching Characteristics: Synchronous Master Interface Mode

over operating ambient temperature range (unless otherwise noted)

			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{p(SCDOD)}$	Propagation delay time, first SCLK rising edge to DOUT driven			28		15	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT			26		15	ns
$t_{p(SDR)}$	Propagation delay time, SCLK falling edge to $\overline{DRDY}$ falling edge		31		20		ns
$t_{h(LSB)}$	Hold time, last SCLK falling edge to DOUT 3-state	HIZDLY = 00	6	30	6	20	ns
		HIZDLY = 01	8	37	8	27	
		HIZDLY = 10	10	43	10	43	
		HIZDLY = 11	12	47	12	47	
$t_{p(DRS)}$	Delay time, last SCLK rising edge to $\overline{DRDY}$ rising edge			17		15	ns

7.10 Timing Requirements: Synchronous Slave Interface Mode

over operating free-air temperature range (unless otherwise noted)

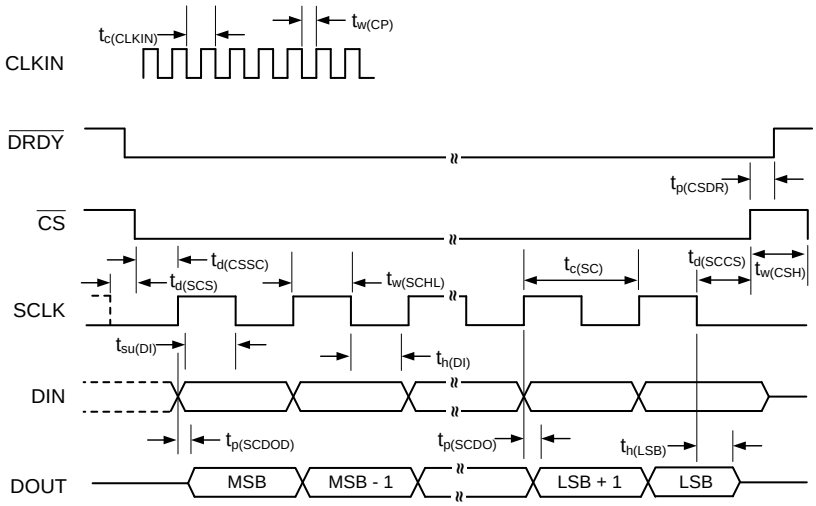
			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(CLKIN)}$	External clock period(1)	Single device	64		40		ns
		Multiple device chaining	88		56		
$t_{w(CP)}$	Pulse duration, CLKIN high or low(1)	Single device	32		20		ns
		Multiple device chaining	44		28		
$t_{d(SCS)}$	Delay time, SCLK falling edge to $\overline{CS}$ falling edge		6		4		ns
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge		16		16		ns
$t_{c(SC)}$	SCLK period	Single device	64		40		ns
		Multiple device chaining	88		64		
$t_{w(SCHL)}$	Pulse duration, SCLK high or low	Single device	32		20		ns
		Multiple device chaining	44		32		
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge		5		5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge		8		6		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge to $\overline{CS}$ rising edge		5		5		ns

(1) Only valid if CLKSRC = 0

7.11 Switching Characteristics: Synchronous Slave Interface Mode

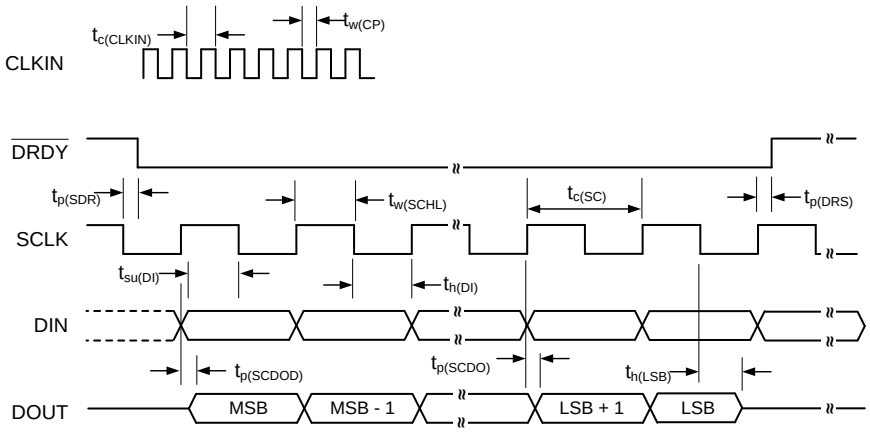
over operating ambient temperature range (unless otherwise noted)

			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{p(SCDOD)}$	Propagation delay time, first SCLK rising edge to DOUT driven			28		15	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT			26		15	ns
$t_{h(LSB)}$	Hold time, last SCLK falling edge to DOUT 3-state	HIZDLY = 00	6	30	6	20	ns
		HIZDLY = 01	8	37	8	27	
		HIZDLY = 10	10	43	10	43	
		HIZDLY = 11	12	47	12	47	



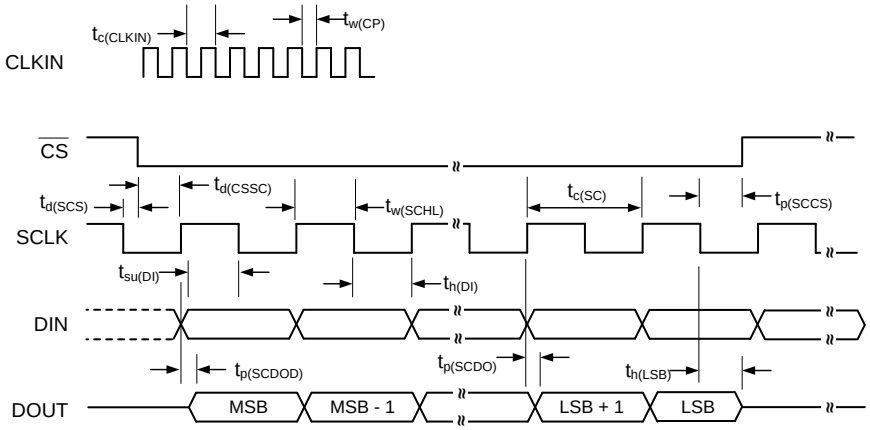
NOTE: SPI settings are CPOL = 0 and CPHA = 1. $\overline{CS}$ transitions must take place when SCLK is low.

Figure 1. Asynchronous Interrupt Mode SPI Timing Diagram



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 2. Synchronous Master Mode SPI Timing Diagram

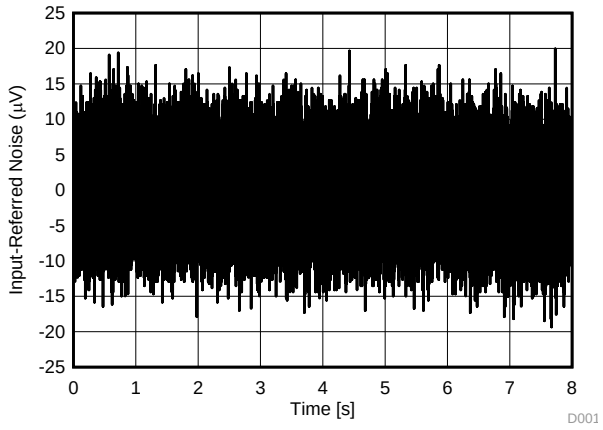


NOTE: SPI settings are CPOL = 0 and CPHA = 1. $\overline{CS}$ can be tied directly to $\overline{DRDY}$.

Figure 3. Synchronous Slave Mode SPI Timing Diagram

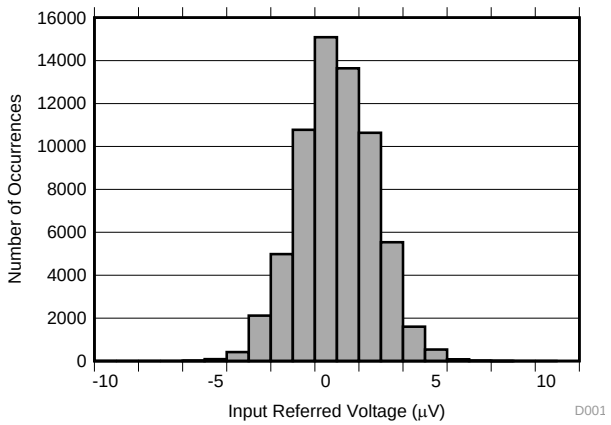
7.12 Typical Characteristics

at T_A = 25°C, V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)



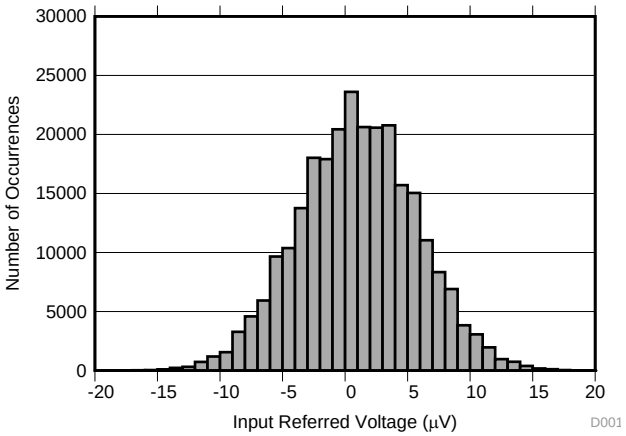
Shorted inputs, 65536 points

Figure 4. Input-Referred Noise vs Time



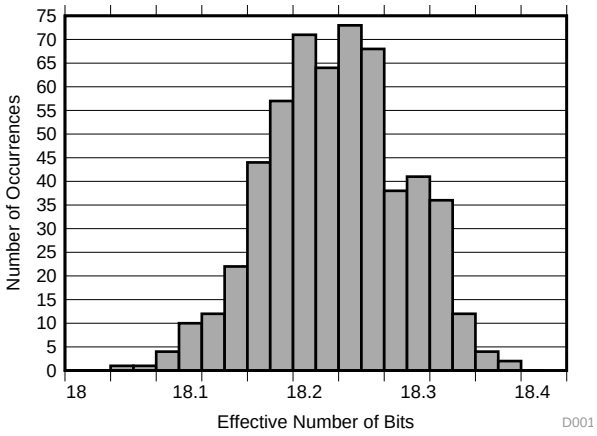
Shorted inputs, 1 kSPS, 65536 points, offset removed

Figure 5. Single Device Noise Histogram



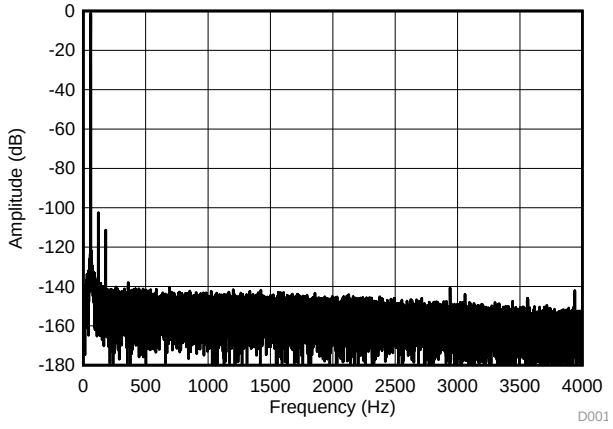
Shorted inputs, 8 kSPS, 262144 points, offset removed

Figure 6. Single Device Noise Histogram



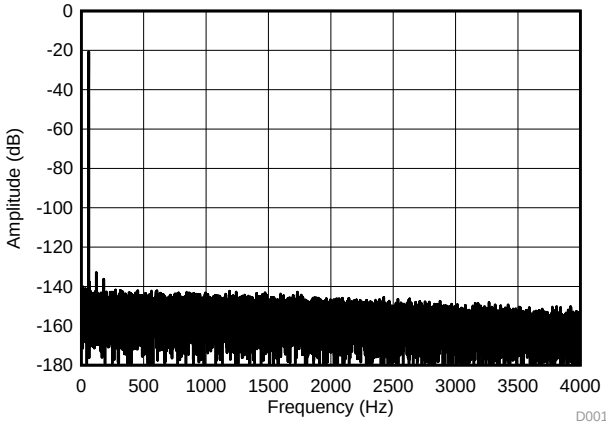
Shorted inputs, 8 kSPS, 560 devices, multiple lots

Figure 7. Multiple Device ENOB Histogram



f_{IN} = 60 Hz, 32768 points

Figure 8. THD FFT Plot at 8 kSPS and –0.5 dBFS

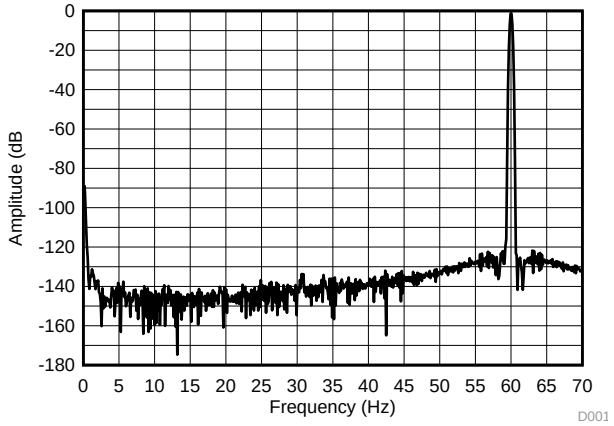


f_{IN} = 60 Hz, 32768 points

Figure 9. THD FFT Plot at 8 kSPS and –20 dBFS

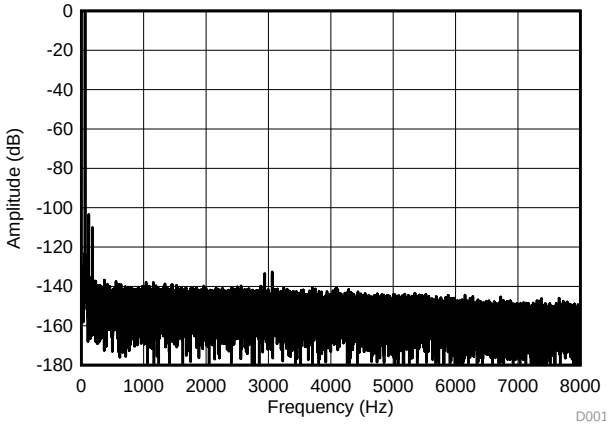
Typical Characteristics (continued)

at T_A = 25°C, V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)



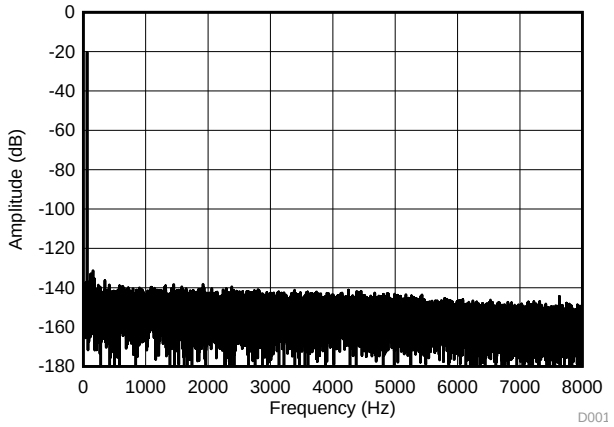
f_{IN} = 60 Hz, 8 kSPS

Figure 10. Low-Frequency FFT Plot



f_{IN} = 60 Hz, 32768 points

Figure 11. THD FFT Plot at 16 kSPS and –0.5 dBFS



f_{IN} = 60 Hz, 32768 points

Figure 12. THD FFT Plot at 16 kSPS and –20 dBFS

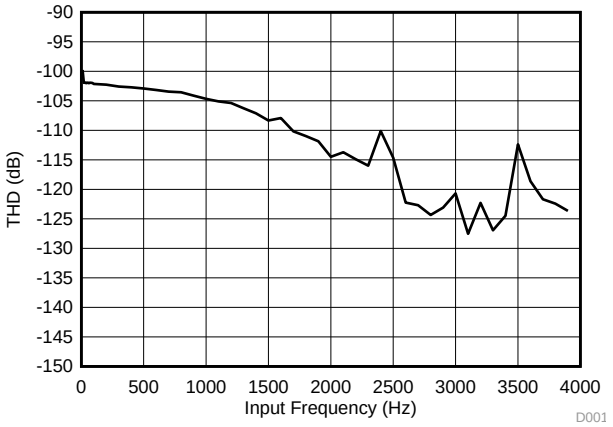


Figure 13. THD vs Input Frequency

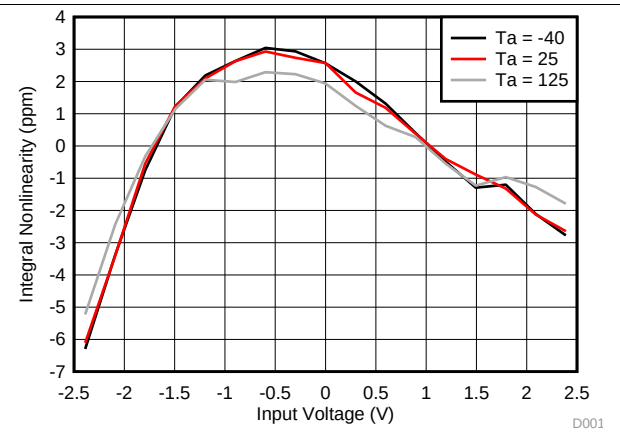


Figure 14. INL vs Temperature

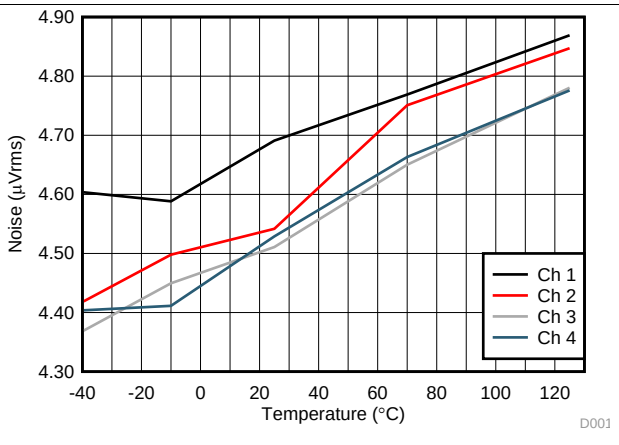


Figure 15. Noise RMS vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)

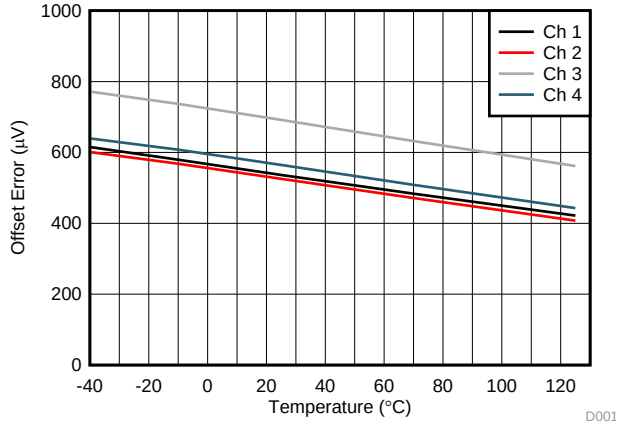


Figure 16. Offset Error vs Temperature

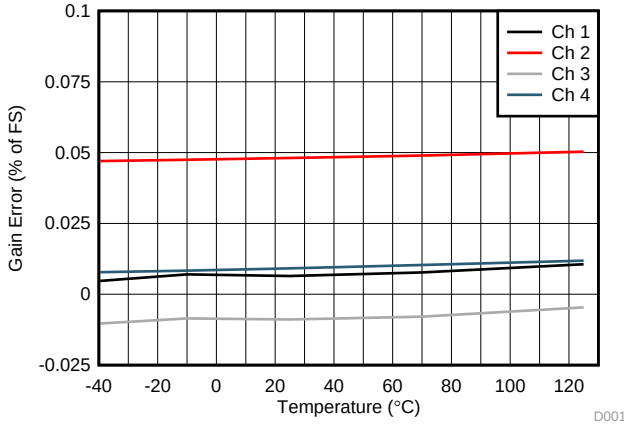
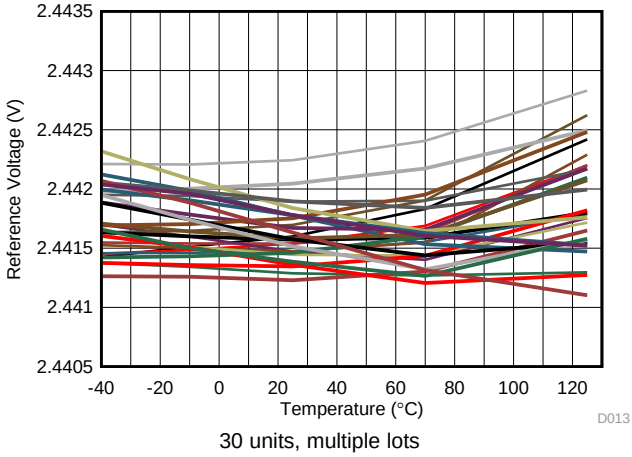


Figure 17. Gain Error vs Temperature



30 units, multiple lots

Figure 18. Internal V_{REF} vs Temperature

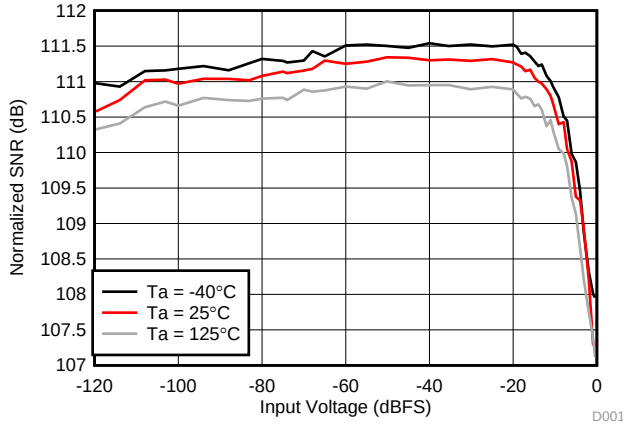


Figure 19. Normalized SNR vs Amplitude

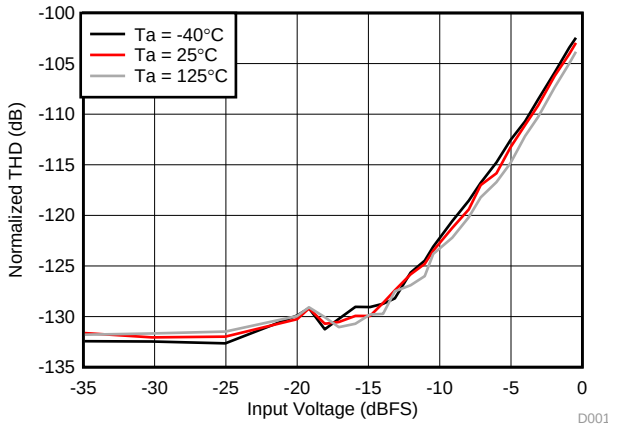


Figure 20. Normalized THD vs Amplitude

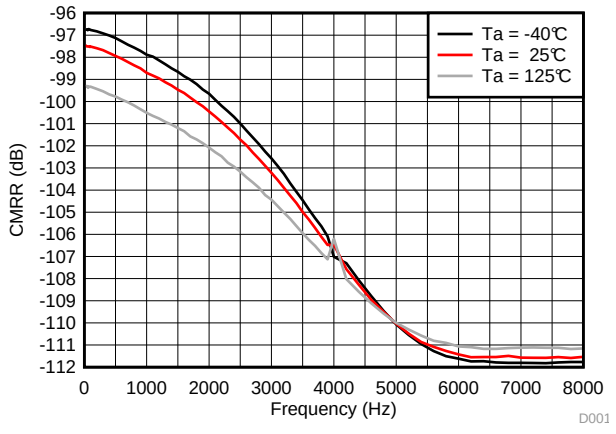


Figure 21. CMRR vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)

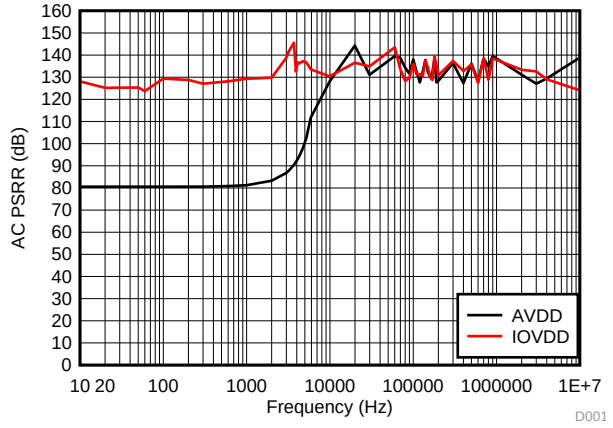


Figure 22. PSRR vs Frequency

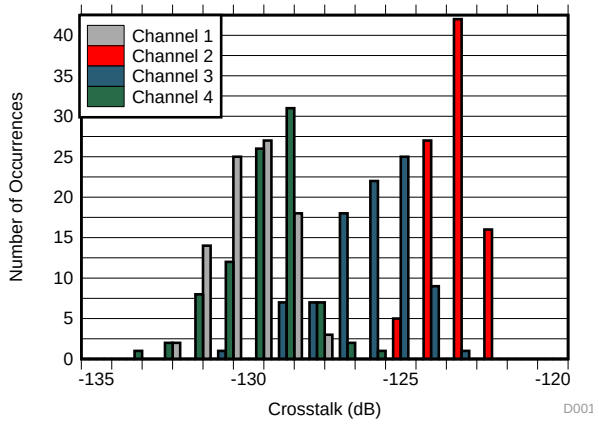


Figure 23. Crosstalk Histogram

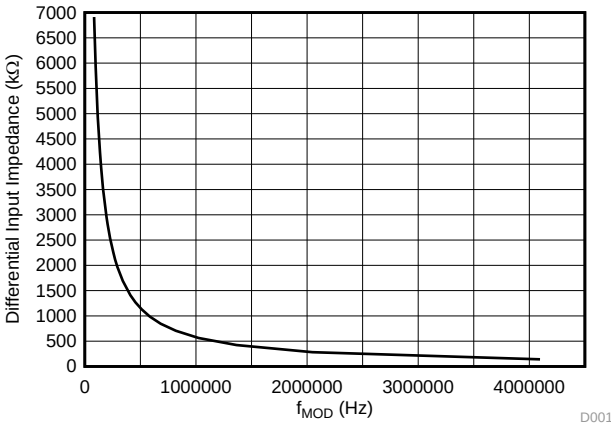


Figure 24. Differential Input Impedance vs Modulator Clock

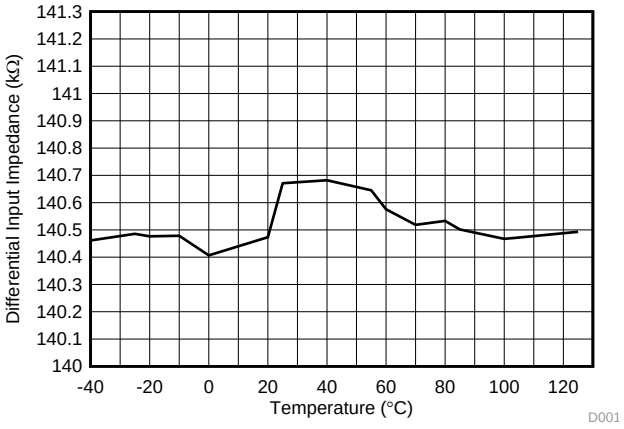


Figure 25. Differential Input Impedance vs Temperature at 4.096-MHz f_{MOD}

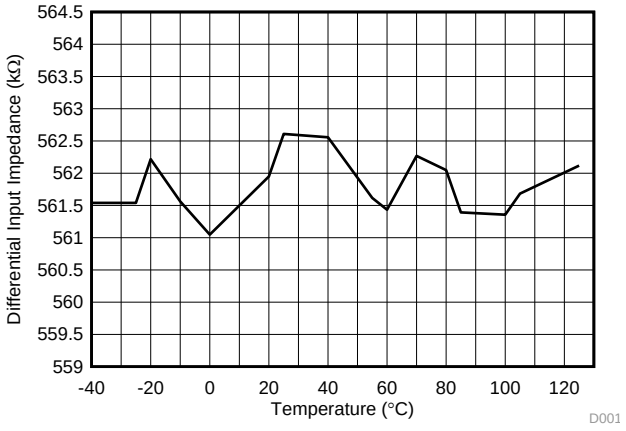
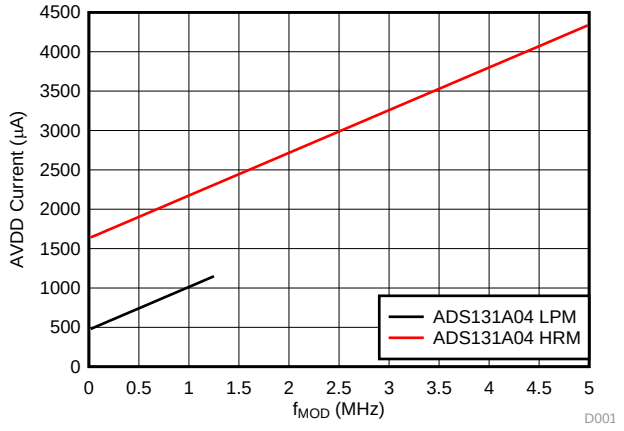


Figure 26. Differential Input Impedance vs Temperature at 1.024-MHz f_{MOD}

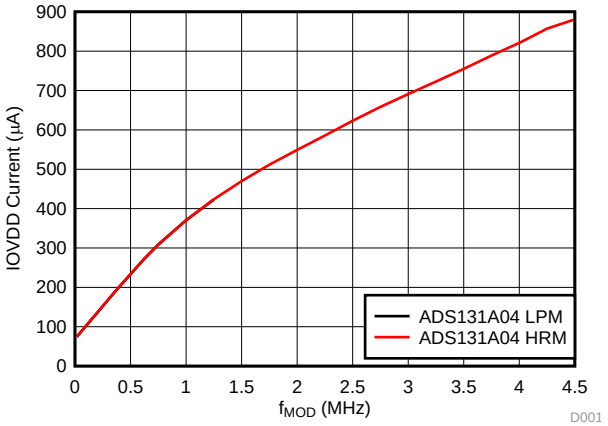


LPM = low-power mode, HRM = high-resolution mode

Figure 27. AVDD Current vs f_{MOD}

Typical Characteristics (continued)

at T_A = 25°C, V_{IOVDD} = 3.3 V, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V, VNCPEN (register 0Bh, bit 7) = 0, internal V_{REF} = 2.442 V, f_{CLKIN} = 16.384 MHz, f_{MOD} = 4.096 MHz, data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)



LPM = low-power mode, HRM = high-resolution mode

Figure 28. IOVDD Current vs f_{MOD}

8 Parameter Measurement Information

8.1 Noise Measurements

Adjust the data rate and gain to optimize the ADS131A02 and ADS131A04 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Table 1 summarizes the ADS131A0x noise performance with a 2.442-V reference and a 3.3-V analog power supply. Table 2 summarizes the ADS131A02 and ADS131A04 noise performance with a 4.0-V reference and a 5-V analog power supply (or using ±2.5-V bipolar analog power supplies). The data are representative of typical noise performance at T_A = 25°C when f_{MOD} = 4.096 MHz. The data shown are typical results with the analog inputs shorted together and taking an average of multiple readings across all channels. A minimum 1 second of consecutive readings are used to calculate the RMS noise for each reading. The data are also representative of the ADS131A0x noise performance when using a low-noise external reference, such as the REF5025 or REF5040. The effective number of bits (ENOB) data in Table 1 and Table 2 are calculated using Equation 1 and the dynamic range data in Table 1 and Table 2 are calculated using Equation 2.

$$\text{ENOB} = \log_2 \left| \frac{0.7071 \times V_{REF}}{V_{RMS\_Noise}} \right| \tag{1}$$

$$\text{Dynamic Range} = 20 \times \log_{10} \left| \frac{0.7071 \times V_{REF}}{V_{RMS\_Noise}} \right| \tag{2}$$

Table 1. Dynamic Range, ENOB, and Noise in μV_{rms} at 3.3-V Analog Supply, and 2.442-V Reference

OSR SETTING	GAIN														
	x1			x2			x4			x8			x16		
	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}
4096	119.49	19.85	1.82	113.49	18.85	3.64	108.08	17.95	6.79	101.72	16.89	14.12	95.45	15.85	29.09
2014	116.47	19.34	2.58	110.97	18.43	4.87	105.22	17.47	9.44	98.88	16.42	19.60	93.07	15.46	38.25
1024	113.85	18.91	3.49	107.91	17.92	6.93	101.77	16.90	14.06	95.97	15.94	27.40	89.82	14.92	55.66
800	112.93	18.76	3.88	106.72	17.72	7.95	101.05	16.78	15.27	95.03	15.78	30.55	88.66	14.72	63.60
768	112.90	18.75	3.90	106.69	17.72	7.98	100.76	16.73	15.79	94.63	15.72	31.98	88.41	14.68	65.43
512	110.73	18.39	5.01	104.83	17.41	9.89	98.75	16.40	19.89	92.75	15.40	39.70	87.00	14.45	76.97
400	109.74	18.23	5.61	103.69	17.22	11.27	97.76	16.23	22.31	91.84	15.25	44.08	85.62	14.22	90.24
384	109.53	18.19	5.75	103.65	17.21	11.32	97.58	16.21	22.76	91.52	15.20	45.74	85.50	14.20	91.56
256	107.74	17.89	7.07	101.67	16.89	14.21	95.72	15.90	28.23	89.57	14.87	57.29	83.58	13.88	114.17
200	106.48	17.68	8.17	100.55	16.70	16.17	94.54	15.70	32.31	88.44	14.69	65.25	82.45	13.69	129.97
192	106.28	17.65	8.36	100.17	16.63	16.90	94.11	15.63	33.97	88.26	14.66	66.58	82.12	13.64	134.98
128	104.05	17.28	10.81	97.98	16.27	21.76	92.00	15.28	43.29	86.02	14.29	86.17	79.80	13.25	176.34
96	101.90	16.92	13.85	95.95	15.93	27.47	89.90	14.93	55.14	83.91	13.93	109.93	77.72	12.91	224.05
64	97.63	16.21	22.64	91.61	15.21	45.28	85.52	14.20	91.33	79.52	13.20	182.23	73.45	12.20	366.66
48	92.58	15.37	40.50	86.62	14.38	80.43	80.59	13.38	161.03	74.60	12.39	321.10	68.47	11.37	650.53
32	85.12	14.12	96.82	78.96	13.11	194.23	73.02	12.11	390.02	66.93	11.11	776.43	60.97	10.11	1561.69

Table 2. Dynamic Range, ENOB, and Noise in μV_{rms} at ±2.5-V Analog Supply, and 4.0-V Reference

OSR SETTING	GAIN														
	x1			x2			x4			x8			x16		
	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}	DYNAMIC RANGE (dB)	ENOB	μV_{rms}
4096	124.55	20.69	1.66	118.69	19.71	3.27	112.32	18.66	6.82	106.35	17.66	13.58	100.66	16.72	26.13
2014	121.47	20.17	2.38	114.98	19.10	5.02	109.58	18.20	9.36	103.40	17.17	19.07	97.37	16.17	38.22
1024	118.44	19.67	3.37	112.48	18.68	6.71	106.31	17.66	13.65	100.46	16.68	26.77	94.59	15.71	52.62
800	117.58	19.53	3.72	111.46	18.51	7.54	105.29	17.49	15.35	99.53	16.53	29.78	93.28	15.49	61.21
768	116.75	19.39	4.10	110.88	18.42	8.06	105.06	17.45	15.76	99.19	16.47	30.99	93.09	15.46	62.51
512	115.16	19.12	4.93	109.23	18.14	9.75	103.10	17.12	19.75	97.31	16.16	38.46	91.08	15.13	78.87
400	114.15	18.96	5.53	108.33	17.99	10.81	102.28	16.99	21.72	96.23	15.98	43.58	90.16	14.97	87.66
384	113.88	18.91	5.71	107.83	17.91	11.46	101.70	16.89	23.21	95.84	15.92	45.59	89.85	14.92	90.88
256	112.09	18.61	7.02	105.76	17.56	14.54	99.83	16.58	28.77	93.87	15.59	57.20	87.73	14.57	115.93
200	110.71	18.39	8.22	104.65	17.38	16.53	98.37	16.34	34.05	92.70	15.39	65.42	86.43	14.35	134.63
192	110.13	18.29	8.79	104.10	17.29	17.60	97.99	16.27	35.59	92.10	15.29	70.14	85.68	14.23	146.74
128	106.93	17.76	12.72	100.76	16.73	25.88	94.59	15.71	52.60	88.58	14.71	105.12	82.42	13.69	213.73
96	104.17	17.30	17.47	98.18	16.30	34.81	92.00	15.28	70.94	86.27	14.33	137.23	80.00	13.29	282.27
64	98.84	16.41	32.27	92.74	15.40	65.15	86.50	14.36	133.58	80.60	13.39	263.36	74.48	12.37	532.93
48	93.30	15.49	61.06	87.45	14.52	119.81	81.31	13.50	242.96	75.29	12.50	485.43	69.10	11.47	990.33
32	85.10	14.13	156.92	78.87	13.10	321.68	73.35	12.16	614.75	67.06	11.14	1252.11	61.17	10.14	2501.17

9 Detailed Description

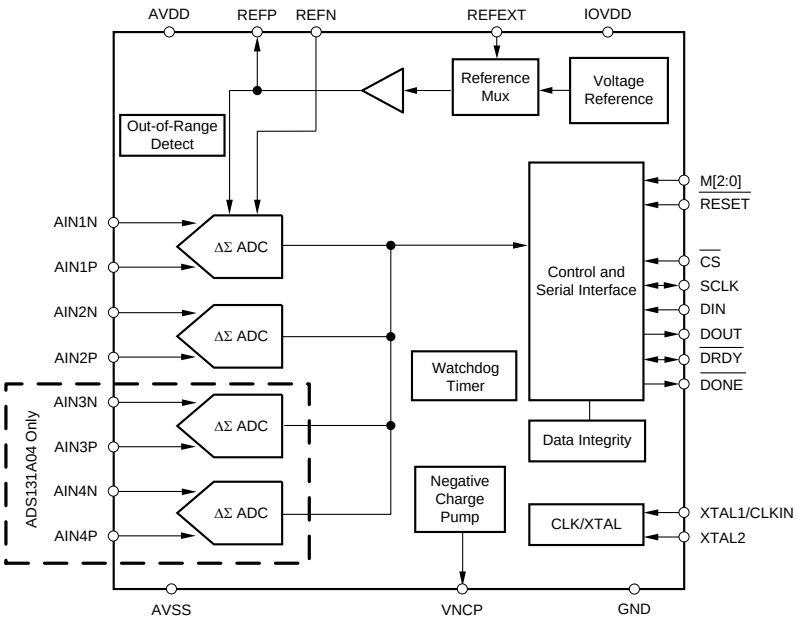
9.1 Overview

The ADS131A02 and ADS131A04 are low-power, two- and four-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converters (ADCs) with an integrated low-drift internal reference voltage. Data rate flexibility, wide dynamic range, and interface options make these devices well-suited for smart-grid and other industrial power monitor, control, and protection applications. The ADC interface checks and data integrity options help with system safety certification specifications. Throughout this document, the ADS131A02 and ADS131A04 are referred to as the ADS131A0x.

The ADS131A0x has very flexible power-supply options. A 5-V single-supply (or ±2.5-V bipolar-supply) operation is available to support up to a 4.5-V external reference to maximize the dynamic range of the converter. Alternatively, a negative charge pump can be enabled to accept input signals down to –1.5 V below ground when powered from a single 3.3-V supply. Five gain options are available to help maximize the ADC code range and 16 selectable oversampling ratio (OSR) options are selectable to optimize the converter for a specific data rate. The low-drift internal reference can be programmed to either 2.442 V or 4 V. Input signal out-of-range detection can be accomplished by using the integrated comparators, with programmable trigger-point settings. A detailed diagram of the ADS131A0x is shown in the *Functional Block Diagram* section.

The device offers multiple serial peripheral interface (SPI) communication options to provide flexibility for interfacing to microprocessors or field-programmable gate arrays (FPGAs). Synchronous real-time and asynchronous interrupt communication modes are available using the SPI-compatible interface. Multiple devices can share a common SPI port and are synchronized by using the $\overline{\text{DRDY}}$ signal. Device communication is specified through configuration of the M0 interface mode pin and chaining of the $\overline{\text{DONE}}$ signal. Optional cyclic redundancy check (CRC) and hamming code correction on the interface enhance communication integrity.

9.2 Functional Block Diagram



9.3 Feature Description

This section contains details of the ADS131A0x internal feature elements. The ADC clocking is discussed first, followed by the analog blocks and the digital filter.

9.3.1 Clock

Multiple clocks are created from one external master clock source in the ADS131A0x to create device configuration flexibility. The ADC operates from the internal system clock, ICLK, which is provided in one of three ways.

- An external master clock, CLKIN, can be applied directly to the XTAL1/CLKIN pin to be divided down to generate ICLK using the CLK_DIV[2:0] bits in the CLK1 register. In this case, leave the XTAL2 pin floating.
- A crystal oscillator can be applied between XTAL1/CLKIN and XTAL2, generating a master clock to be divided down using the CLK_DIV[2:0] bits in the CLK1 register to generate ICLK.
- A free-running SCLK can be internally routed to be set as ICLK. This mode is only available in synchronous slave interface mode. Tie the CLKIN/XTAL1 and XTAL2 pins to GND.

The system ICLK is passed through a second 3-bit clock divider (ICLK_DIV[2:0] in the CLK2 register) to create the modulator clock, MODCLK. MODCLK is used for timing of the delta-sigma (ΔΣ) modulator sampling and digital filter.

The interface operation mode determines the options for sourcing ICLK. When in asynchronous interrupt or synchronous master mode, generate ICLK by a direct external master clock to the XTAL1/CLKIN pin or by using a crystal oscillator across the XTAL1/CLKIN and XTAL2 pins. If directly applying a master clock to the XTAL1/CLKIN pin, leave XTAL2 unconnected or floating. In synchronous slave mode, a free-running SCLK line can be connected directly into the ICLK_DIV block in place of the divided XTAL or CLKIN source. Use the CLKSRC bit in the CLK1 register to select between the XTAL1/CLKIN or SCLK input as the master clock source for the ADC. The CLKSRC bit must be set prior to powering up the ADC channels. Using SCLK as ICLK is useful in isolated applications to limit the digital I/O lines crossing the isolation barrier. The clock dividers and clocking names are shown in Figure 29.

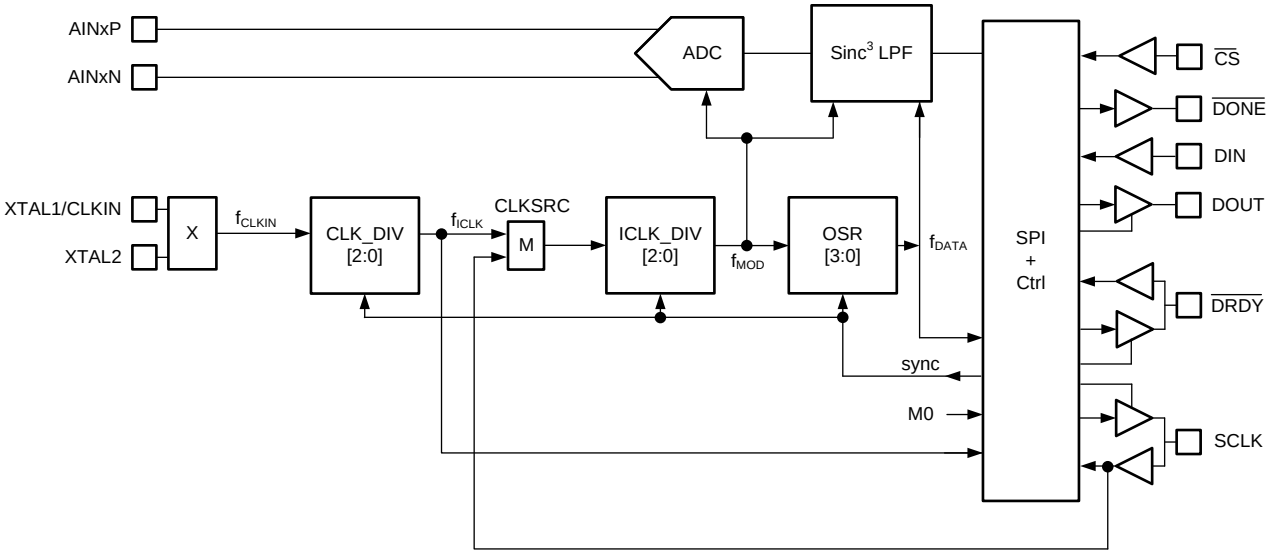


Figure 29. ADC Clock Generation

Feature Description (continued)

9.3.1.1 XTAL1/CLKIN and XTAL2

XTAL1/CLKIN (f_{CLKIN}) is the external clock input to the ADC and can be supplied from a clock source or by using a crystal (along with the XTAL2 pin). Figure 30 shows the configuration for the two clock input options.

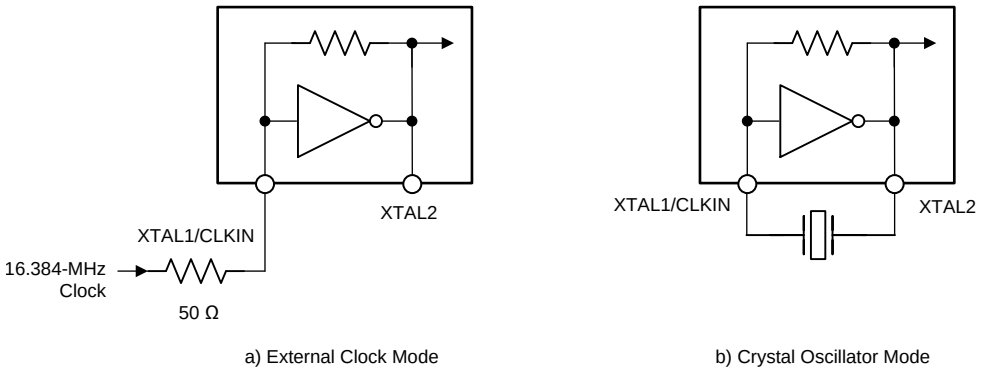


Figure 30. Clock Mode Configurations

Input the clock directly to the XTAL1/CLKIN pin and leave the XTAL2 pin floating when using a direct clock source.

Connect the crystal and load capacitors to the XTAL1/CLKIN and XTAL2 pins, as shown in Figure 30b. Place the crystal and crystal load capacitors close to the ADC pins using short, direct traces. Connect the load capacitors to digital ground. Do not connect any other external circuit to the crystal oscillator. Table 3 lists recommended crystals for use with the ADS131A0x. The crystal oscillator start-up time is typically 5 ms, but can be longer depending on the crystal characteristics.

Table 3. Recommended Crystals

MANUFACTURER	FREQUENCY	OPERATING TEMPERATURE RANGE	PART NUMBER
Abracon	16.384 MHz	–40°C to +125°C	ABLS-16.384MHZ-L4Q-T
Abracon	16.384 MHz	–40°C to +85°C	ABM3C-16.384MHZ-D4Y-T
ECS	16.384 MHz	–40°C to +85°C	ECS-163-18-5PXEN-TR

9.3.1.2 ICLK

ICLK (f_{ICLK}) is the internal system clock to the ADC. ICLK is derived from the CLKIN set through the CLK_DIV[2:0] bits in the CLK1 register or is set as SCLK when operating in synchronous slave mode. Aside from being used for the internal ADC clock timing, ICLK is used as the SCLK output when operating in synchronous master mode. Use the CLKSRC bit to set the source for ICLK.

9.3.1.3 MODCLK

MODCLK (f_{MOD}) is the modulator clock used for the ADC sampling. MODCLK is derived from the ICLK set through the ICLK_DIV[2:0] bits in the CLK2 register. Verify that the f_{MOD} minimum and maximum limits are met in the *Electrical Characteristics* table by adjusting the CLK_DIV[2:0] and ICLK_DIV[2:0] clock dividers.

9.3.1.4 Data Rate

The data rate (f_{DATA}) is the post-decimated data rate clock of the ADC. The OSR[3:0] bits in the CLK2 register set the ADC data rate from the MODCLK.

9.3.2 Analog Input

The ADS131A0x analog inputs are directly connected to the switched-capacitor sampling network of the ΔΣ modulator without a multiplexer or integrated buffer. The device inputs are measured differentially ($V_{IN} = V_{AINxP} – V_{AINxN}$) and can span from $–V_{REF}$ / Gain to V_{REF} / Gain. Figure 31 shows a conceptual diagram of the modulator circuit charging and discharging the sampling capacitor through switches, although the actual implementation is slightly different. The timing for switches S1 and S2 are 180 degrees out-of-phase of one another, as shown in Figure 32.

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 3:

$$V_{AVSS} – 0.3\ V < V_{AINxP} \text{ or } V_{AINxN} < V_{AVDD} + 0.3\ V \quad (3)$$

If the voltages on the input pins have any potential to violate these conditions, external clamp diodes or series resistors may be required to limit the input currents to safe values (see the *Absolute Maximum Ratings* table).

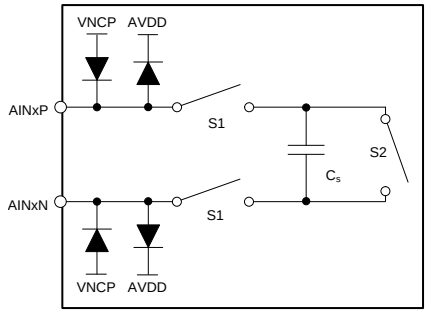


Figure 31. Equivalent Analog Input Circuitry

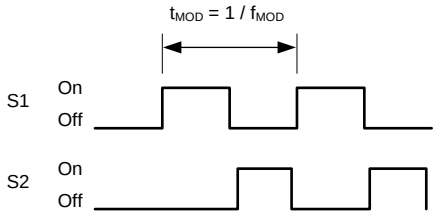


Figure 32. S1 and S2 Switch Timing

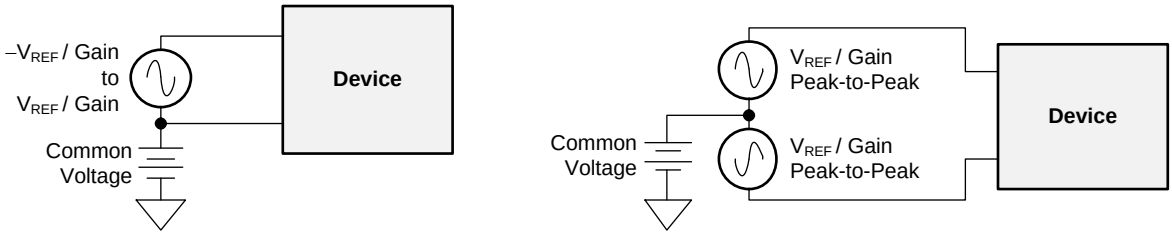
The charging of the input capacitors draws a transient current from the sensor driving the ADS131A0x inputs. The average value of this current can be used to calculate an effective impedance of Z_{IN}, where $Z_{IN} = V_{IN} / I_{AVERAGE}$. This effective input impedance is a function of the modulator sampling frequency and an estimate can be calculated using Equation 4. When using a 4.096-MHz f_{MOD}, the input impedance is approximately 130 kΩ.

$$Z_{in} = \frac{2}{f_{MOD} \times C_s} \quad (4)$$

where

- f_{MOD} = modulator clock and
- C_S = 3.5 pF

There are two general methods of driving the ADS131A0x analog inputs: pseudo-differential or fully-differential, as shown in Figure 33.



a) Psuedo-Differential Input b) Differential Input

Figure 33. Pseudo-Differential and Fully-Differential Inputs

To apply a pseudo-differential signal to the fully-differential inputs, apply a dc voltage to AINxN, preferably analog mid-supply [(AVDD + AVSS) / 2]. Swing the AINxP pin $–V_{REF}$ / Gain to V_{REF} / Gain around the common voltage as shown in Figure 34. The common-mode voltage, V_{CM}, swings with AINxP.

Configure the signals at AINxP and AINxN to be 180° out-of-phase centered around a common-mode voltage to use a fully-differential input method. Both the AINxP and AINxN inputs swing from V_{CM} +½ V_{REF} / Gain to V_{CM} –½ V_{REF} / Gain, as shown in Figure 35. The differential voltage at the maximum and minimum points is equal to V_{REF} / Gain to $–V_{REF}$ / Gain, respectively. The V_{CM} voltage remains fixed when AINxP and AINxN swing. Use the ADS131A0x in a differential configuration to maximize the dynamic range of the data converter. For optimal performance, the V_{CM} is recommended to be set at the midpoint of the analog supplies.

Tie any unused analog input channels directly to AVSS.

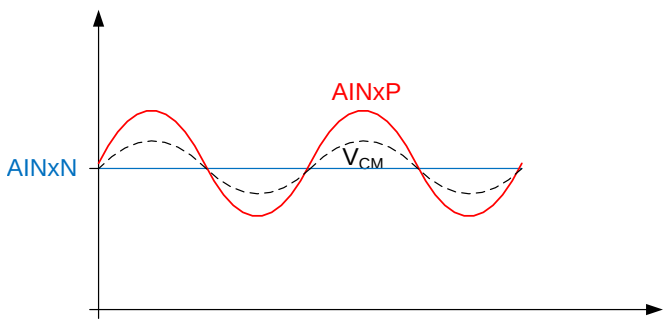


Figure 34. Pseudo-Differential Input Mode

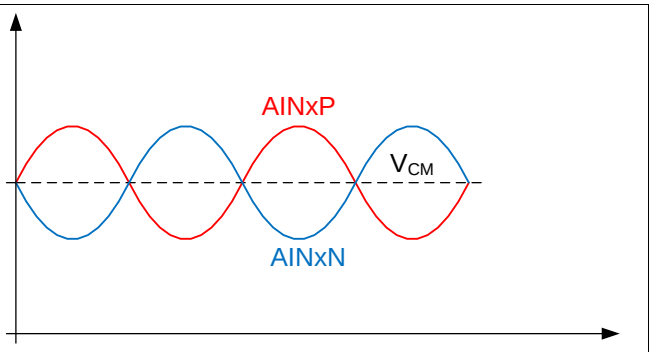


Figure 35. Fully-Differential Input Mode

9.3.3 Input Overrange and Underrange Detection

Each ADS131A0x channel has two integrated comparators to detect overrange and underrange conditions on the input signals. Use the COMP_TH[2:0] bits in the A_SYS_CFG register to set a high and low threshold level using a 3-bit digital-to-analog converter (DAC) to compare to the voltage on the input pins. The voltage monitor triggers an alarm by setting the F_ADCIN bit of the STAT_1 register when the individual voltage on AINxP or AINxN exceeds the threshold set by the COMP_TH[2:0] bits. When the bit is set, indicating an out-of-range event, read the STAT_P register or STAT_N register to determine exactly which input pin exceeded the set threshold. The input overrange and underrange detection block diagram is shown in Figure 36.

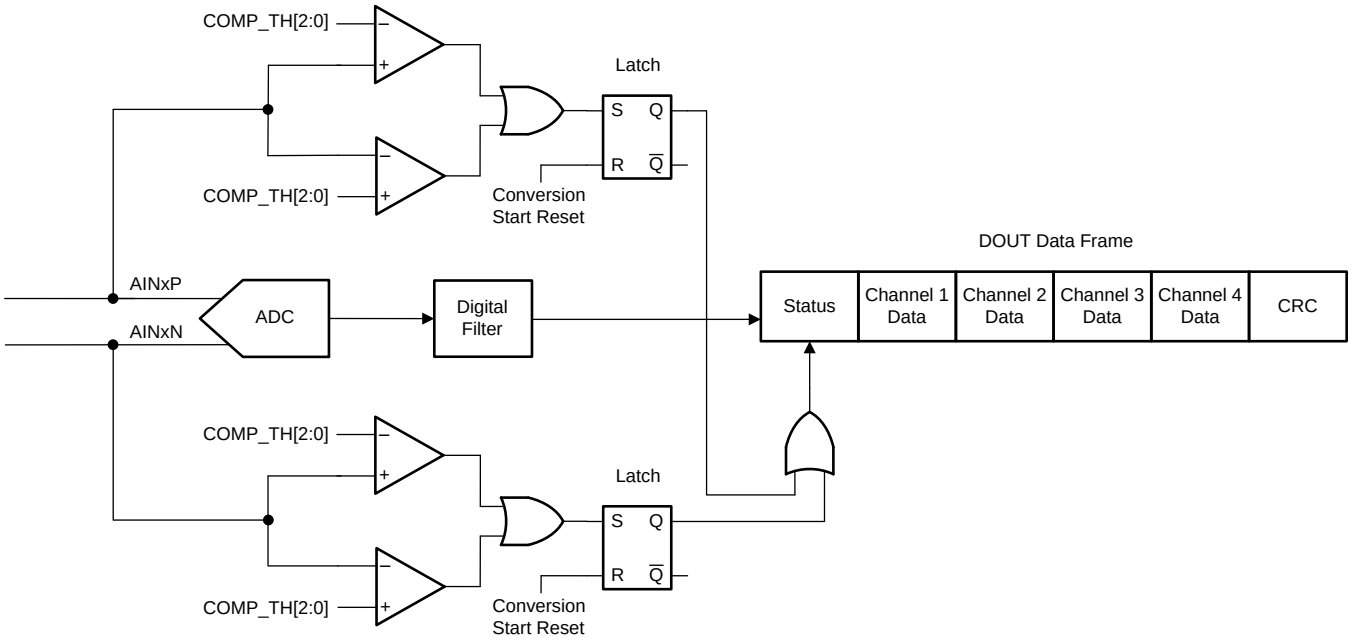


Figure 36. ADC Out-of-Range Detection Monitor

9.3.4 ΔΣ Modulator

The ADS131A0x is a multichannel, simultaneous sampling ΔΣ ADC where each channel has an individual modulator and digital filter. The modulator samples the input signal at the rate of f_{MOD} derived as a function of the ADC operating clock, f_{ICLK}. As in the case of any ΔΣ modulator, the ADS131A0x noise is shaped until f_{MOD} / 2. The modulator converts the analog input voltage into a pulse-code modulated (PCM) data stream. The on-chip digital decimation filters take this bitstream and provide attenuation to the now shaped, higher frequency noise. This ΔΣ sample and conversion process drastically reduces the complexity of the analog antialiasing filters typically required with nyquist ADCs.

9.3.5 Digital Decimation Filter

The digital filter receives the modulator output and decimates the data stream to create the final conversion result. The digital filter on each channel consists of a third-order sinc filter. The decimation ratio determines the number of samples taken to create the output data word, and is set by the modulator rate divided by the data rate (f_{MOD} / f_{DATA}). The decimation ratio of the sinc filters is adjusted by the OSR[3:0] bits in the CLK2 register. The decimation ratio setting is a global setting that affects all channels and, therefore, all channels operate at the same data rate in the device. By adjusting the decimation, tradeoffs can be made between noise and data rate to optimize the signal chain: filter more for lower noise (thus creating lower data rates), filter less for higher data rates. Higher data rates are typically used in grid infrastructure applications that implement software re-sampling techniques to help with channel-to-channel phase adjustment for voltage and current.

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. Equation 5 shows the scaled sinc^3 filter Z-domain transfer function. The integer *N* is the set OSR and the integer *K* is a scaling factor for non-binary OSR values, as shown in Table 4.

$$\left|H(z)\right| = K \times \left| \frac{\left(1 - Z^{-N}\right)}{N \times \left(1 - Z^{-1}\right)} \right|^3 \tag{5}$$

The sinc filter frequency domain transfer function is shown in Equation 6. The integer *N* is the set OSR and the integer *K* is a scaling factor for non-binary OSR values, as shown in Table 4.

$$\left|H(f)\right| = K \times \left| \frac{\sin\left[\frac{N\pi f}{f_{MOD}}\right]}{N \times \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^3 \tag{6}$$

where:

N = decimation ratio

Table 4. K Scaling Factor

OSR (N)	K SCALING VALUE
800, 400, 200	0.9983778
4096, 2048, 1024, 512, 256, 128, 64, 32	1.0
768, 384, 192, 96, 48	1.00195313

The sinc^3 filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 37 and Figure 38 show the digital filter frequency response out to a normalized input frequency (f_{IN} / f_{DATA}) of 5 and 0.5, respectively.

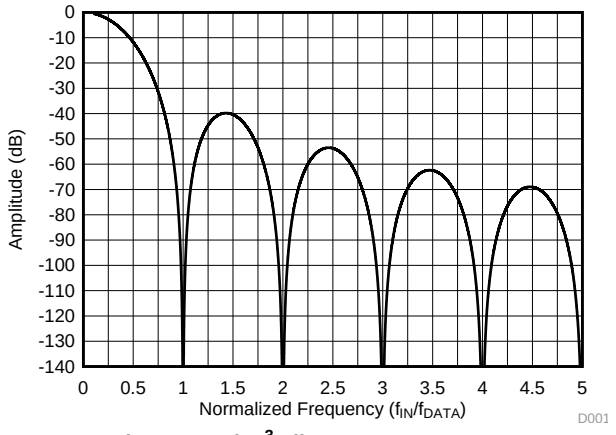


Figure 37. Sinc^3 Filter Frequency Response

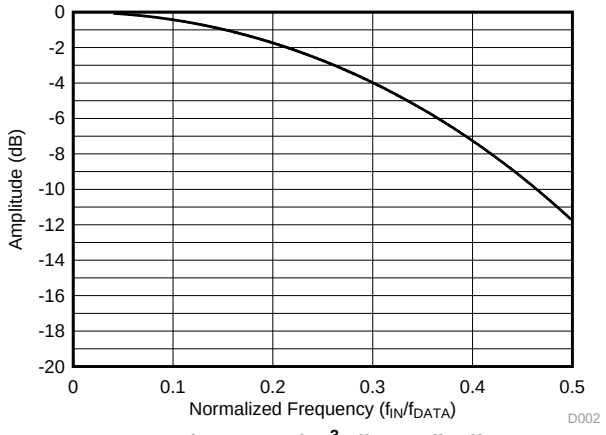


Figure 38. Sinc^3 Filter Roll-Off

Figure 39, Figure 40, and Figure 41 show the frequency response for OSR 32, OSR 512, and OSR 4096 out to the device OSR.

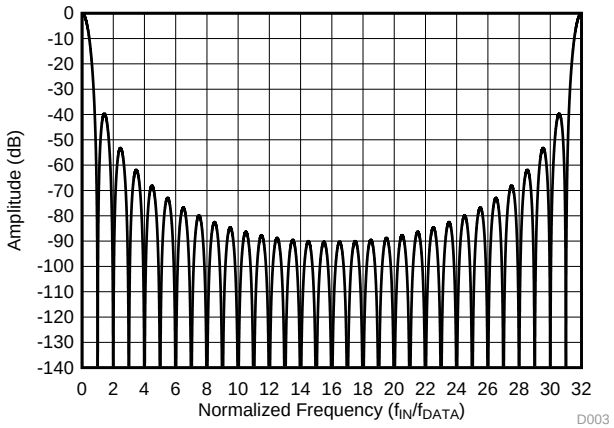


Figure 39. Sinc^3 Filter Frequency Response (OSR 32)

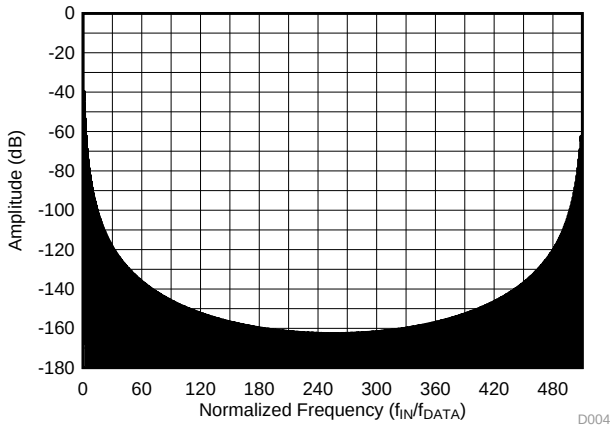


Figure 40. Sinc^3 Filter Frequency Response (OSR 512)

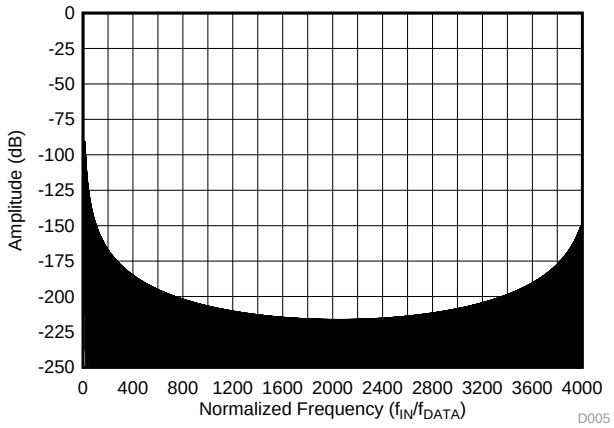


Figure 41. Sinc^3 Filter Frequency Response (OSR 4096)

The K scaling factor for OSR values that are not a power of two adds a non-integer gain factor to the sinc^3 frequency response across all frequencies. Figure 42 overlays the digital filter frequency response for the three K scaling options in Table 4. Note that the graph scaling is set to a narrow limit to show the small gain variation between OSR values.

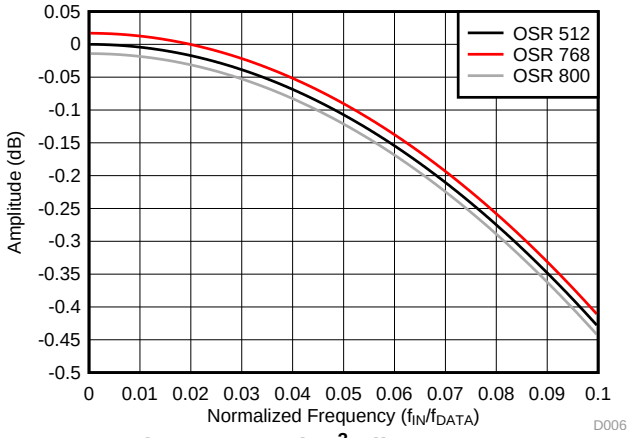


Figure 42. Non-Binary OSR Sinc^3 Filter Frequency Response

The ADS131A0x immediately begins outputting conversion data when powered up and brought out of standby mode using the WAKEUP command. The sinc^3 digital filter requires three conversion cycles to provide a settled conversion result, assuming the analog input has settled to its final value (t_{SETTLE}). The output data are not gated when the digital filter settles, meaning that the first two conversion results show unsettled data from the filter path before settled data are available on the third conversion cycle. The first two unsettled conversion cycles, though unsettled, can be used for diagnostic purposes to ensure the ADC is coming out of standby as expected. Figure 43 shows the new data ready behavior and time needed for the digital filter coming out of standby.

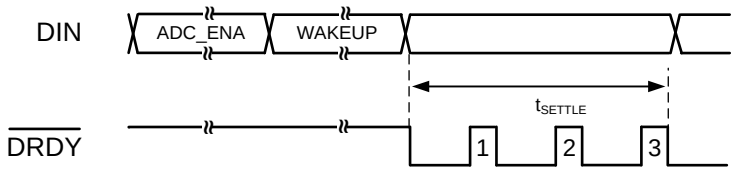


Figure 43. Sinc^3 Filter Settling

The digital filter uses a multiple stage linear-phase digital filter. Linear -phase filters exhibit constant delay time across all input frequencies (also know as *constant group delay*). This behavior results in zero-phase error when measuring multi-tone signals.

9.3.6 Reference

The ADS131A0x offers an integrated low-drift, 2.442-V or 4.0-V reference option. For applications that require a different reference voltage, the device offers a reference input option for use with an external reference voltage.

The reference source is selected by the INT_REFEN bit in the A_SYS_CFG register. By default, the external reference is selected (INT_REFEN = 0). The internal voltage reference requires 0.2 ms to settle to 1% and 250 ms to fully settle to 0.01% when switching from an external reference source to the internal reference (using the recommended bypass capacitor values). The external reference input is internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. Connect the reference voltage to the REFEXT pin when using an external reference.

External band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, choose capacitor values such that the bandwidth is limited to less than 10 Hz so that the reference noise does not dominate the system noise. In systems with strict ADC power-on requirements, using a large capacitor on the reference increases the time for the voltage to meet the desired value, thus increasing system power-on time. Figure 44 illustrates a typical external reference drive circuitry with recommended filtering options.

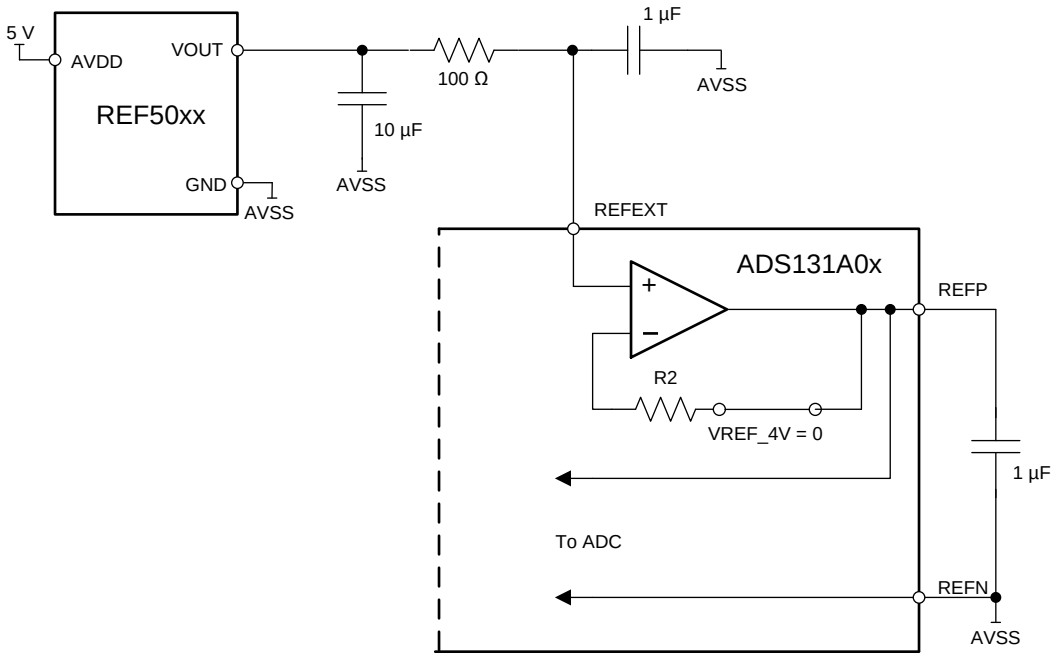
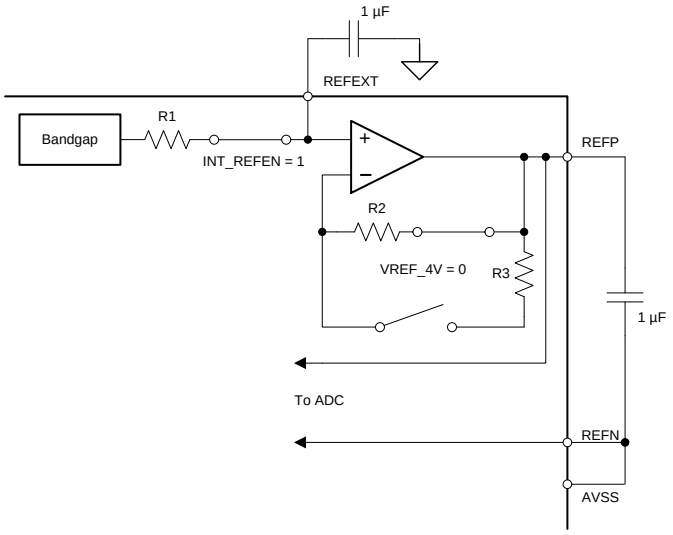


Figure 44. External Reference Driver

Set the INTREF_EN bit to 1 in the A_SYS_CFG register to use the internal reference. When the internal reference is selected, use the VREF_4V bit to select between a 2.442-V or 4.0-V reference. By default, the device is set to use the 2.442-V reference. The VREF_4V bit has no function when set to use the external reference. When enabling the negative charge pump with a 3.0-V to 3.45-V analog supply, the internal reference must be set to 2.442 V. Figure 45 shows a simplified block diagram of the internal ADS131A0x reference. The reference voltage is generated with respect to AVSS requiring a direct connection between REFN and AVSS.



NOTE: R1 = 20 kΩ, R2 = 36 kΩ, and R3 = 62 kΩ.

Figure 45. Internal Reference

9.3.7 Watchdog Timer

The ADS131A0x offers an integrated watchdog timer to protect the device from entering any unresponsive state. The watchdog timer is a 16-bit counter running on an internal 50-kHz clock. The timer resets with each data frame when the $\overline{CS}$ signal transitions from high to low. If a timer reset does not take place and the watchdog timer expires after 500 ms, the device assumes that an unresponsive state has occurred and issues a watchdog timer reset. Following the reset, the device enters the power-up ready state (see the *Power-Up Ready State* section), sets the F_WDT bit in the STAT_1 register, and indicates that a watchdog timer reset has taken place. Enable the watchdog timer by setting the WDT_EN bit in the D_SYS_CFG register.

9.4 Device Functional Modes

9.4.1 Low-Power and High-Resolution Mode

The ADS131A0x offers two modes of operation: high-resolution and low-power mode. High-resolution mode enables a faster modulator clock, f_{MOD} = 4.25 MHz, to maximize performance at higher data rates. Low-power mode scales the analog and digital currents and restricts the maximum f_{MOD} to 1.05 MHz. Select the operating mode using the HRM bit in the A_SYS_CFG register.

9.4.2 Power-Up Ready State

After all supplies are established and the $\overline{RESET}$ pin goes high, an internal power-on-reset (POR) is performed. As part of the POR process, all registers are initialized to the default states, the status of the M0, M1, and M2 pins are latched, the interface is placed in a locked state, and the device enters standby mode. POR can take up to 4.5 ms to initialize. The device outputs a READY status word indicating that the power-on cycle is completed and the device is ready to accept commands. The contents of the STAT_S register indicate if the ADC powered up properly or if any fault occurred during the initialization of the device. Send an UNLOCK command to enable the interface and begin communicating with the device. See Table 16 for more information on the READY status word and the *UNLOCK from POR or RESET* or *RESET: Reset to POR Values* sections for more information on bringing the device out of POR.

9.4.3 Standby and Wake-Up Mode

After being unlocked from POR or after reset, the device enters a low-power standby mode with all ADC channels powered down. After the registers are properly configured, enable all the ADC channels together by writing to the ADC_ENA register and issue a WAKEUP command to start conversions. To enter standby mode again, send the STANDBY command and disable all ADC channels by writing to the ADC_ENA register. The ADS131A0x requires using the WAKEUP and STANDBY commands together with writing to the ADC_ENA register to disable or enable ADC channels to start and stop conversions.

9.4.4 Conversion Mode

The device runs in continuous conversion mode. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion. Data are available at the next data-ready indicator, although data may not be fully settled through the digital filter (see the *Digital Decimation Filter* section for more information on settled data).

Device Functional Modes (continued)

9.4.5 Reset (RESET)

There are two methods to reset the ADS131A0x: pull the RESET pin low for the minimum pulse duration given in Table 5, or send the RESET command. The RESET pin must be tied high if the RESET command is used. The RESET command takes effect at the completion of the command. As part of the reset process, all registers are initialized to the default states, the status of M0, M1, and M2 pins are latched, the interface is placed in a locked state, and the device enters standby mode. Reset can take up to 4.5 ms to complete. The device outputs a READY status word indicating that the reset is completed and the device is ready to accept commands. Send an UNLOCK command to enable the interface and begin communicating with the device. See Table 15 for more information on the READY status word, the UNLOCK from POR, and RESET. Figure 46 shows the critical timing relationship of taking the ADS131A0x into reset and bringing the device out of reset.

There are two methods to reset the ADS131A0x: pull the RESET pin low, or send the RESET command. When using the RESET pin, driving the pin low forces the device into reset. Follow the minimum pulse duration timing specifications before taking the RESET pin back high. The RESET command takes effect at the completion of the command (see the *RESET: Reset to POR Values* section for more information). After the device is reset, 4.5 ms are required to complete initialization of the configuration registers to the default states and to enter the power-up ready state, as shown in Table 5. Figure 46 shows the critical timing relationship of taking the ADS131A0x into reset and bringing the device out of reset. The hardware RESET pin must be tied high if the register format to reset is used.

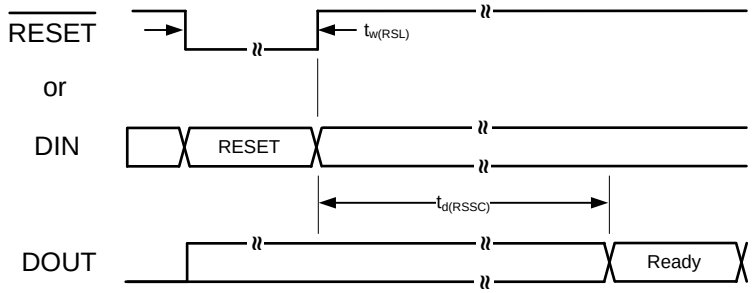


Figure 46. RESET Pin and Command Timing

Table 5. RESET Signal Timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL)}$	Pulse duration, RESET low	800			ns
$t_{d(RSSC)}$	Delay time, RESET rising edge to READY command	4.5			ms

9.5 Programming

9.5.1 Interface Protocol

The ADS131A0x is designed with an interface protocol that expands the capability of outputting more ADC system monitors without disrupting data flow. This protocol communicates through standard serial peripheral interface (SPI) methods, using allocated device words within a single data transmission frame to pass information. A single data frame starts when the interface is enabled, typically done by pulling the $\overline{CS}$ line low. The duration of a data frame is made up of several device words with programmable bit lengths. A visual representation showing how a data frame is made up of multiple device words is shown in Figure 47.

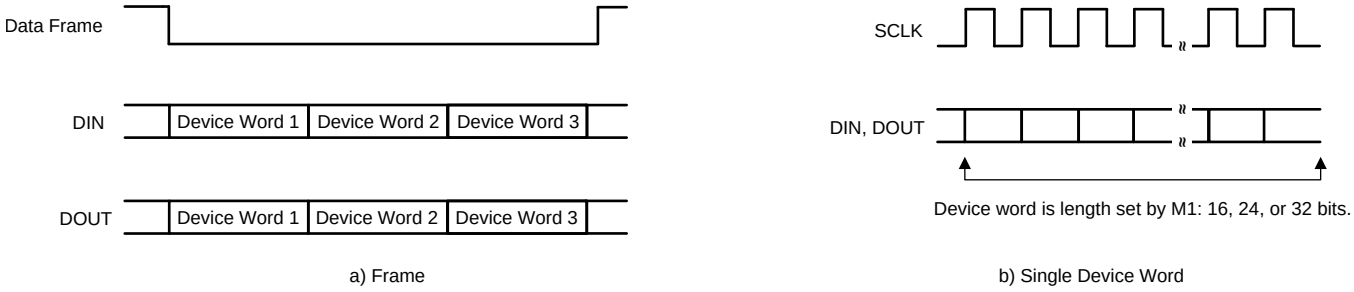


Figure 47. Data Frame versus Device Word

9.5.1.1 Device Word Length

The interface is full duplex, allowing the device to be read to and written from within the same data frame. The length of the individual device words is programmable through the state of the M1 pin. This pin must be set to one of three states at power-up. The pin state is latched at power-up and changing the pin state after power-up has no effect. Table 6 lists the modes associated with the M1 pin state. The M1 pin must be tied high to IOVDD through a < 1-kΩ resistor, low to GND through a < 1-kΩ resistor, or left floating.

Table 6. M1 Pin Setting

M1 STATE	DEVICE WORD LENGTH (Bits)
IOVDD	32
GND	24
Float	16

9.5.1.2 Fixed versus Dynamic Frame Size

The device has two data frame size options to set the number of device words per frame: fixed and dynamic frame size, controlled by the FIXED bit in the D_SYS_CFG register. By default, the ADS131A0x powers up in dynamic frame mode.

In fixed-frame size, there are always six device words for each data frame for the ADS131A04 and four device words for each data frame for the ADS131A02. For the four-channel ADS131A04, the first device word is reserved for the status word, the next four device words are reserved for the conversion data for each of the four channels, and the last word is reserved for the cyclic redundancy check (CRC) data word. For the ADS131A02, the first device word is allocated for the status word, the next two device words are reserved for the conversion data words for each of the two channels, and the last word is reserved for the CRC data word.

In dynamic frame mode, the number of device words per data frame is dependent on if the ADCs are enabled and if CRC data integrity is enabled. When the ADCs are powered down in standby mode, the number of device words per data frame is either one or two depending if CRC data integrity is enabled. In normal operation with the ADC channels powered up, the number of device words per data frame depends on if CRC is enabled. When CRC data integrity is disabled in dynamic frame mode, the sixth device word for the ADS131A04 and the fourth device word for the ADS131A02 are removed from the data frame. If CRC data integrity remains enabled, the device word count remains at six and four, similar to the fixed-frame size option.

An example showing fixed-frame size versus dynamic frame size for the ADS131A04 in standby mode with CRC data integrity enabled and disabled is shown in Figure 48. An example showing fixed-frame size versus dynamic frame size for the ADS131A04 with ADC channels and CRC data integrity enabled and disabled is shown in Figure 49.

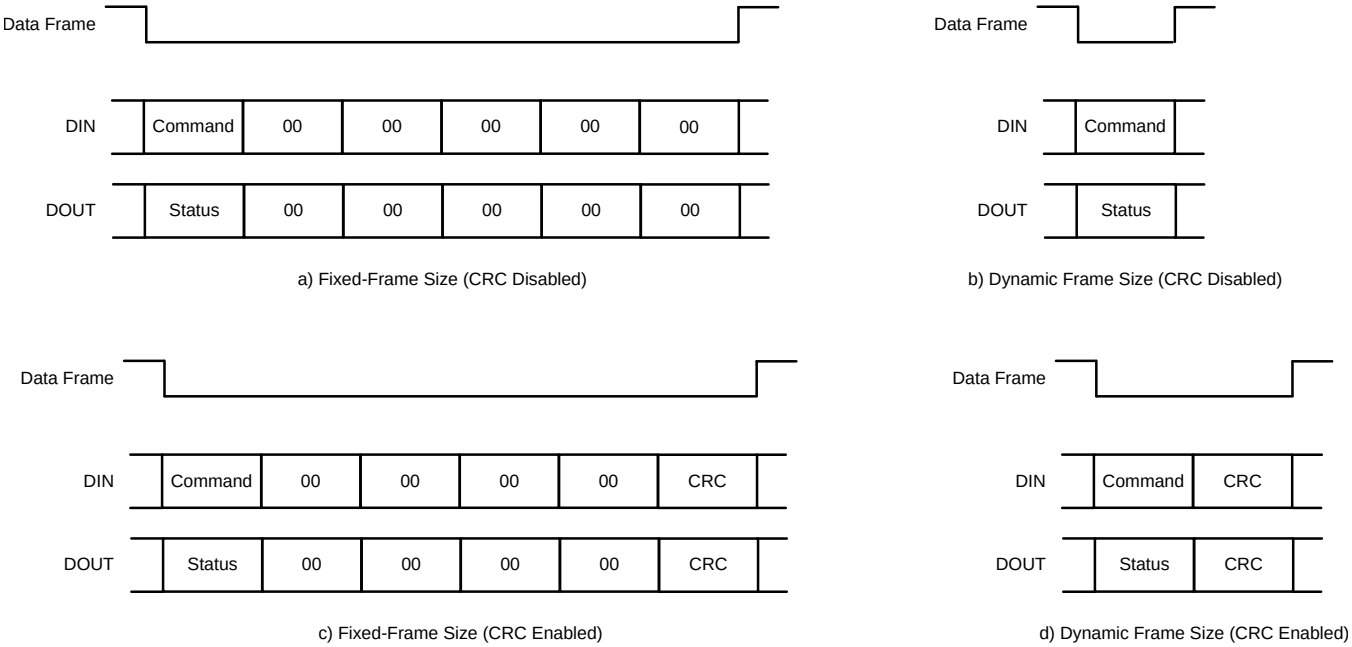
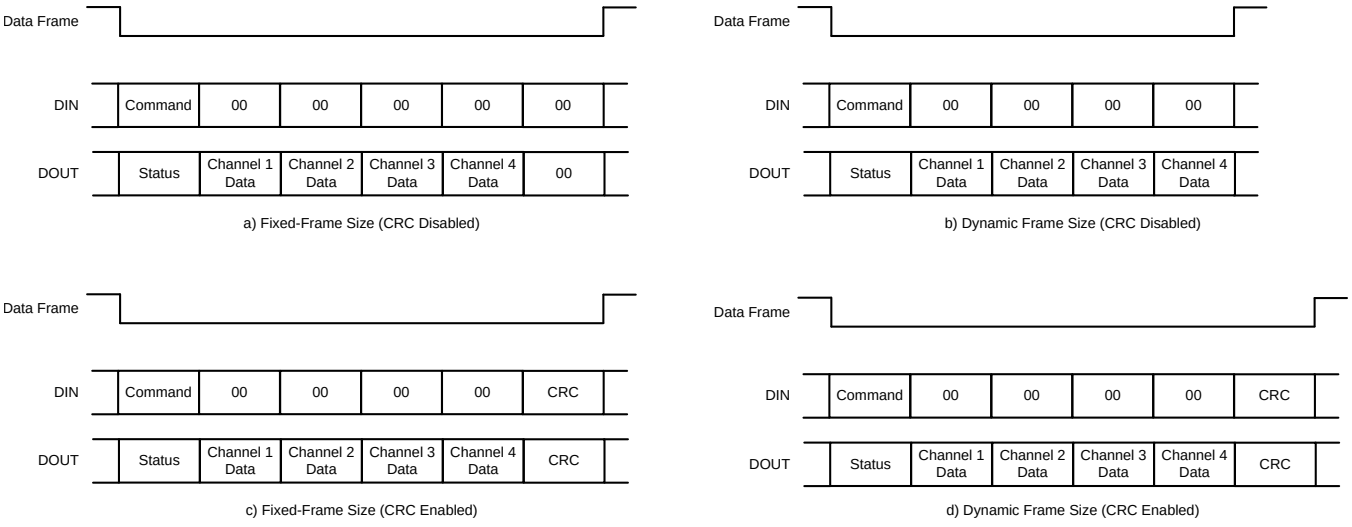


Figure 48. Fixed versus Dynamic Frame Size in Standby Mode



NOTE: CMND = Command.

Figure 49. Fixed versus Dynamic Frame Size with ADCs Enabled

9.5.1.3 Command Word

The command word is the first device word on every DIN data frame. This frame is reserved for sending user commands to write or read from registers (see the *SPI Command Definitions* section). The commands are stand-alone, 16-bit words that appear in the 16 most significant bits (MSBs) of the first device word of the DIN data frame. Write zeroes to the remaining unused least significant bits (LSBs) when operating in either 24-bit or 32-bit word size modes.

9.5.1.4 Status Word

The status word is the first device word in every DOUT data frame. The status word either provides a status update of the ADC internal system monitors or functions as a status response to an input command; see the *SPI Command Definitions* section. The contents of the status word are always 16 bits in length with the remaining LSBs set to zeroes depending on the device word length; see Table 6.

9.5.1.5 Data Words

The data words follow the status word. The device shifts individual channel data in separate data words. The ADS131A0x converter is 24-bit resolution regardless of the device word length; see Table 6. The output data are truncated to 16 bits when using the 16-bit device word length setting (or when enabling hamming code with a 24-bit device word length setting). The output data are extended to 32 bits with eight zeroes (00000000) added to the least significant bits when using the 32-bit device word length setting (when hamming code is disabled).

Use the device word length (see Table 6) to set the output resolution of the ADS131A0x. When placing the hardware M1 pin in a floating state, the interface operates in 16-bit device word length mode by removing the eight least significant bits. The 16 bits of data per channel are sent in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 7:

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{16} = \text{FS} / 2^{15} \quad (7)$$

A positive full-scale input [$V_{IN} \geq (\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

Table 7 summarizes the ideal output codes for different input signals.

Table 7. 16-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} V_{AINxP} - V_{AINxN}	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

Pull the M1 pin to IOVDD (through a < 1-kΩ resistor) or GND (through a < 1-kΩ resistor) to set the device either to a 24-bit or 32-bit device word length. In either setting, the ADS131A0x outputs 24 bits of data per channel in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 8:

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{24} = \text{FS} / 2^{23} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 8 summarizes the ideal output codes for different input signals.

Table 8. 24-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} V_{AINxP} - V_{AINxN}	IDEAL OUTPUT CODE(1)
≥ FS ($2^{23} - 1$) / 2^{23}	7FFFFFh
FS / 2^{23}	000001h
0	000000h
–FS / 2^{23}	FFFFFFh
≤ –FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

9.5.1.6 Cyclic Redundancy Check (CRC)

The CRC word is the last device word in the DIN and DOUT data frame. The CRC device word is optional and is enabled by the CRC_EN control bit in the D_SYS_CFG register. When enabled, a 16-bit CRC data check word is present in the 16 most significant bits of the last device word in the data frame on both DIN and DOUT. Use the CRC to provide detection of single and multiple bit errors during data transmission.

The ADS131A0x implements a standard CRC16-CCITT algorithm using a polynomial of 11021h and an initial remainder of FFFFh.

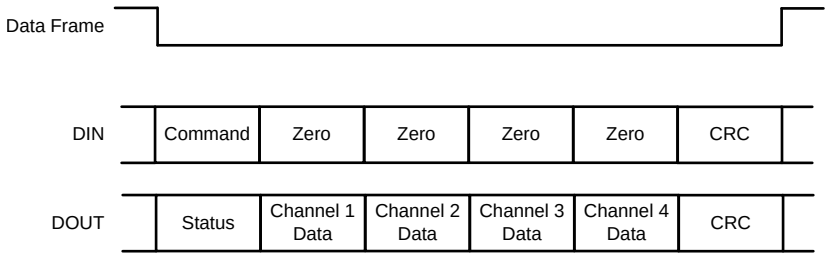
The CRC on all DIN commands is verified by the device prior to command execution except for the WREGS command; see the *WREGS: Write Multiple Registers* section. The WREGS command does not check the CRC prior to writing registers but does indicate if an error occurred. If the CRC on DIN is incorrect, F_CHECK in the STAT_1 register is set to 1 and the input command does not execute. Fill the unused device words on DIN with zeroes, placing the CRC word in the last device word.

The CRC is calculated using specific device words in the data frame determined by the CRC_MODE and FIXED bits in the D_SYS_CFG register. For DIN, when the FIXED bit is 0, all device words are calculated into the CRC. When the FIXED bit is 1 and the CRC_MODE bit is 1, all device words are used for calculating the CRC on DIN. When the FIXED bit is 1 and the CRC_MODE is 0, only the command word and device words are used for the CRC calculation on DIN.

For DOUT, when the FIXED bit is 0, all words in the data frame are included in the CRC calculation. When the FIXED bit is 1 and CRC_MODE is 1, all words in the data frame are included in the DOUT CRC calculation. When the FIXED bit is 1 and CRC_MODE is 0, only the status word and active ADC words are included in the DOUT CRC calculation. When hamming codes are enabled, the hamming byte of each word is omitted in the CRC calculation.

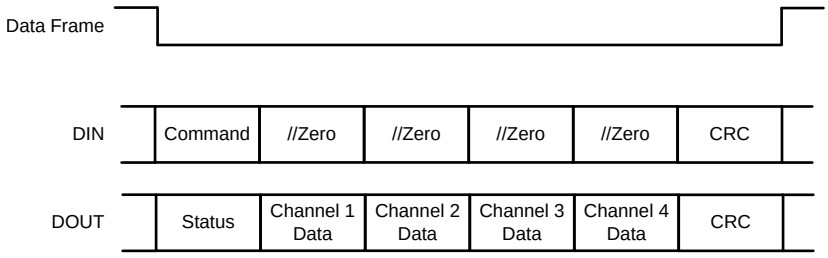
The WREGS command causes the data frame to extend until the last register is written (see the *WREGS: Write Multiple Registers* section for more details), requiring the CRC to be placed on DIN after the data frame extension. The ADS131A0x places the CRC word on DOUT at the end of all ADC data. When sending the WREGS command, the device words following the CRC on DOUT are padded with zeroes and are not included in the CRC calculation; see Figure 52.

Figure 50, Figure 51, and Figure 52 illustrate which device words are included in the CRC calculation on DIN and DOUT under the various CRC settings. In the following examples, the device words that are not checked are listed as //Zero.



NOTE: CRC_MODE = 1.

Figure 50. CRC with CRC_MODE = 1



NOTE: CRC_MODE = 0.

Figure 51. CRC with CRC_MODE = 0

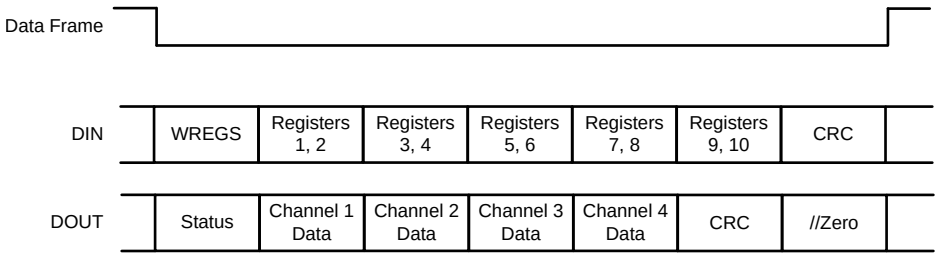


Figure 52. CRC Using the WREGS Command

9.5.1.6.1 Computing the CRC

The CRC byte is the 16-bit remainder of the bitwise exclusive-OR (XOR) operation of the data bytes by a CRC polynomial. The CRC is based on the CRC-CCITT polynomial $X_{16} + X_{12} + X_5 + 1$.

The binary coefficients of the polynomial are: 10001000 00010001. Calculate the CRC by dividing the data bytes (with the XOR operation, thus excluding the CRC) with the polynomial and compare the calculated CRC values to the provided CRC value. If the values do not match, then a data transmission error has occurred. In the event of a data transmission error, read or write the data again.

The following list shows a general procedure to compute the CRC value. Assume the shift register is 16 bits wide:

1. Set the polynomial value to 1021h (see the following note regarding the assumed X16 bit)
2. Set the shift register to FFFFh
3. For each byte in the data stream:
   - Shift the next data byte left by eight bits and XOR the result with the shift register, placing the result into the shift register
   - Do the following eight times:
     (a) If the most significant bit of the shift register is set, shift the register left by one bit and XOR the result with the polynomial, placing the result into the shift register
     (b) If the most significant bit of the shift register is not set, shift the register left by one bit
4. The result in the shift register is the CRC check value

NOTE

The CRC algorithm used here employs an assumed set X16 bit. This bit is divided out by left-shifting it 16 times out of the register prior to XORing with the polynomial register. This process makes the CRC calculable with a 16-bit word size.

9.5.1.7 Hamming Code Error Correction

Hamming code is an optional data integrity feature used to correct for single-bit errors and detect multiple-bit errors in each device word. Enable hamming code with M2 pin settings (see Table 9 for details). Tie the M2 pin to IOVDD through a < 1-kΩ resistor to enable hamming code.

Hamming code is only supported in 24-bit and 32-bit device word sizes. The ADS131A0x outputs 24 bits of conversion data and an 8-bit hamming code per channel when operating in 32-bit word size. The ADS131A0x outputs 16 bits of conversion data and an 8-bit hamming code per channel when operating in 24-bit word size. Table 9 lists the configuration options of the M1 and M2 hardware pins and the associated device word size. The status and command words are always 16 bits in length, reserving the eight least significant bits for hamming code.

Table 9. M2 Pin Setting Options

M2 STATE	M1 STATE	DEVICE WORD SIZE	CONVERSION DATA	HAMMING DATA
IOVDD	IOVDD	32 bits	24 bits	On: 8 bits
	GND	24 bits	16 bits	On: 8 bits
	Float	Not available	Not available	Not available
GND	IOVDD	32 bits	24 bit + 8 zeroes	Off
	GND	24 bits	24 bit	Off
	Float	16 bits	16 bit	Off
Float	N/A	Not available	Not available	Not available

When enabled, the hamming code byte is an additional 8-bits appended to the end of each device word on both the input and output, as shown in Figure 53. This additional eight bits are a combination of five hamming code (Hamming) bits, two checksum (ChS) bits, and one zero bit, as shown in Figure 54.

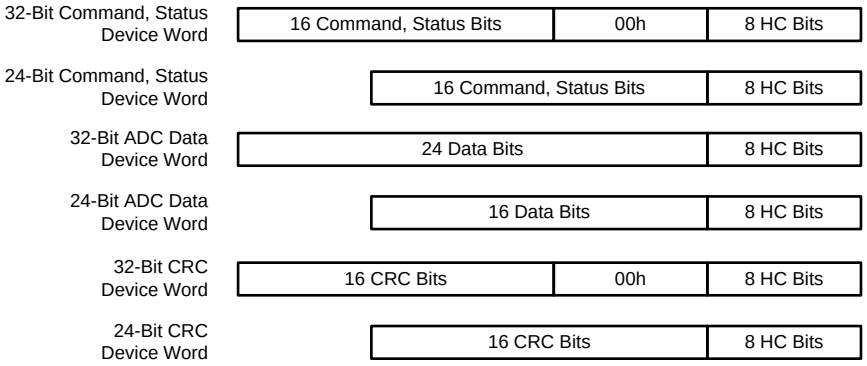


Figure 53. Hamming Code on Each Device Word

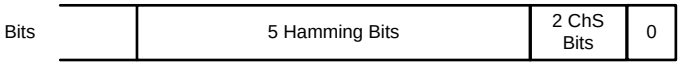


Figure 54. Hamming Code Bit Allocation

CRC can be used with the hamming code error correction enabled. When the hamming code error correction is enabled with CRC, the 8-bit hamming data per device word is not protected by the CRC and is ignored in the calculation. For example, if the 32-bit word size is used with hamming code enabled, the CRC check only uses the most significant 24 bits of each device word and ignores the last eight bits used for the hamming code. The CRC considers each device word as being 24 bits.

Table 10 shows the hamming bit coverage for 24-bit data. The encoded data bit 00 corresponds to the LSB of the data and bit 23 is the MSB of the data. The hamming code bits are interleaved within the data bits. H0 is the least significant bit of the hamming code and H4 is the most significant bit.

Table 10. ADS131A0x Hamming Codes

HAMMING OR DATA		D	D	D	D	D	D	D	D	D	D	D	D	D	H	D	D	D	D	D	D	D	H	D	D	D	H	D	H	H
Encoded data bits		00	01	02	03	04	05	06	07	08	09	10	11	12	04	13	14	15	16	17	18	19	03	20	21	22	02	23	01	00
Parity bit coverage	H0	x		x		x		x		x		x		x		x		x		x		x		x		x		x		x
	H1			x	x			x	x			x	x			x	x			x	x			x	x			x	x	
	H2	x	x					x	x	x	x					x	x	x	x					x	x	x	x			
	H3	x	x	x	x	x	x									x	x	x	x	x	x	x	x							
	H4	x	x	x	x	x	x	x	x	x	x	x	x	x	x															

9.5.2 SPI Interface

The device SPI-compatible serial interface is used to read conversion data, read and write the device configuration registers, and control device operation. Only CPOL = 0 and CPHA = 1 (SPI mode 1) is supported. The interface consists of five control lines ($\overline{CS}$, SCLK, DIN, DOUT, and $\overline{DRDY}$) but can be used with only four signals as well. Three interface configurations are selectable in the ADS131A0x by M0 pin settings, as shown in Table 11: asynchronous interrupt mode, synchronous master mode, and synchronous slave mode.

The M0 pin settings (listed in Table 11) are latched on power-up to set the interface. The same communication lines are used for all three interface modes: SCLK, DIN, DOUT, and $\overline{DRDY}$, with $\overline{CS}$ as an option in 5-wire mode. An optional sixth signal ($\overline{DONE}$) is available for use when chaining multiple devices, as discussed in the *ADC Frame Complete (DONE)* section.

Table 11. M0 Pin Setting

M0 STATE	INTERFACE MODE
IOVDD	Asynchronous interrupt mode
GND	Synchronous master mode
Float	Synchronous slave mode

9.5.2.1 Asynchronous Interrupt Mode

The SPI uses five interface signals: $\overline{CS}$, SCLK, DIN, DOUT, and $\overline{DRDY}$ in asynchronous interrupt mode. Use the four interface lines, $\overline{CS}$, SCLK, DIN, and DOUT to read conversion data, read and write registers, and send commands to the ADS131A0x. Use the $\overline{DRDY}$ output as a status signal to indicate when new conversion data are ready. Figure 55 shows typical device connections for the ADS131A0x to a host microprocessor or digital signal processor (DSP) in asynchronous interrupt mode.

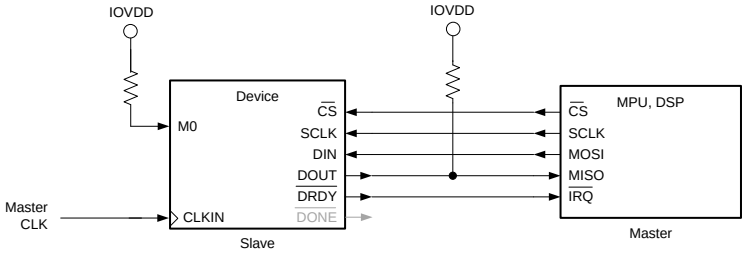


Figure 55. Asynchronous Interrupt Mode Device Connections

9.5.2.1.1 Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) is an active-low input that selects the device for SPI communication and controls the beginning and end of a data frame in asynchronous interrupt mode. $\overline{CS}$ must remain low for the entire duration of the serial communication to complete a command or data readback. When $\overline{CS}$ is taken high, the serial interface (including the data frame) is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ deasserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

9.5.2.1.2 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data into and out of the device on DIN and DOUT, respectively. SCLKs can be sent continuously or in byte increments to the ADC. Even though the input has hysteresis, keeping the SCLK signal as clean as possible is recommended to prevent glitches from accidentally shifting data. When the serial interface is idle, hold SCLK low.

9.5.2.1.3 Data Input (DIN)

Use the data input (DIN) pin and SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write takes effect following completion of the data frame.

9.5.2.1.4 Data Output (DOUT)

Use the data output (DOUT) pin with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high or after the least significant bit is shifted from the output shift register (see the $t_{h(LSB)}$ specification in the *Switching Characteristics: Asynchronous Interrupt Interface Mode* table).

9.5.2.1.5 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ indicates when a new conversion result is ready for retrieval. When $\overline{DRDY}$ transitions from high to low, new conversion data are ready. The $\overline{DRDY}$ signal remains low for the duration of the data frame and returns high either when $\overline{CS}$ returns high (signaling the completion of the frame), or prior to new data being available. The high-to-low $\overline{DRDY}$ transition occurs at the set data rate regardless of the $\overline{CS}$ state. If data are not completely shifted out when new data are ready, the $\overline{DRDY}$ signal toggles high for a duration of 0.5 × t_{MOD} and back low, issuing the F_DRDY bit and indicating that the DOUT output shift register is not updated with the new conversion result. Figure 56 shows an example of new data being ready before previous data are shifted out, causing the new conversion result to be lost. The $\overline{DRDY}$ pin is always actively driven, even when $\overline{CS}$ is high.

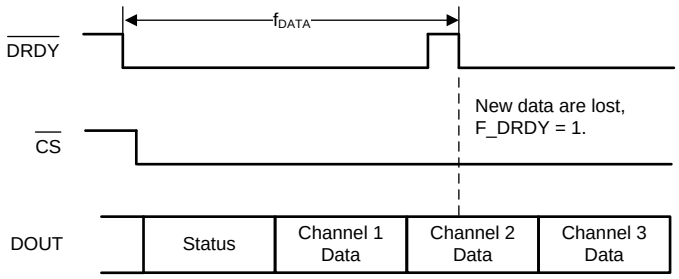


Figure 56. Asynchronous Interrupt Mode Conversion Update During a Read Operation

9.5.2.1.6 Asynchronous Interrupt Mode Data Retrieval

Figure 57 shows the relationship between DRDY, CS, SCLK, DIN, and DOUT during data retrieval. The high-to-low DRDY transition indicates that new data are available. CS transitions from high to low to begin a data frame. At the end of the data frame, CS returns high and brings DRDY high.

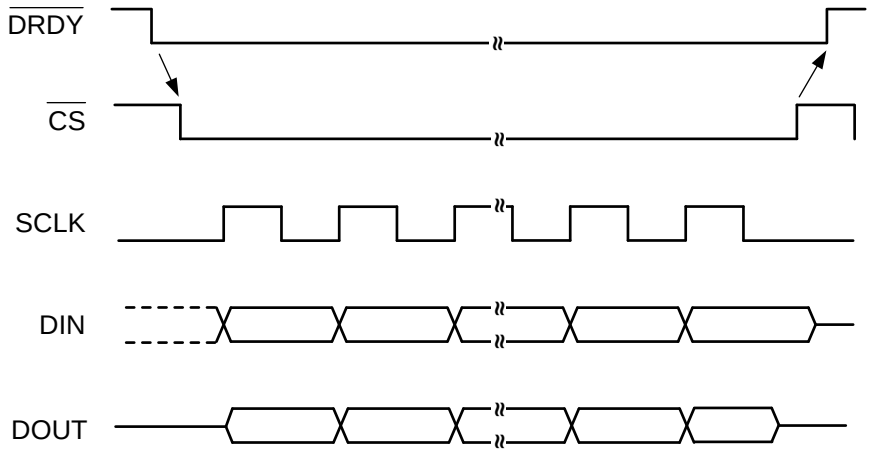


Figure 57. DRDY Behavior with Data Retrieval in Asynchronous Interrupt Mode

9.5.2.2 Synchronous Master Mode

The SPI uses four interface signals: SCLK, DIN, DOUT, and DRDY in synchronous master mode. Connect the CS signal to the DONE signal when using a single device in synchronous master mode. The SCLK, DRDY, and DOUT signals are outputs from the device. Provide DIN from the microprocessor (MPU) or DSP using the SCLK edge timing from the ADS131A0x. Figure 58 shows typical device connections for the ADS131A0x in synchronous master mode to a host microprocessor or DSP.

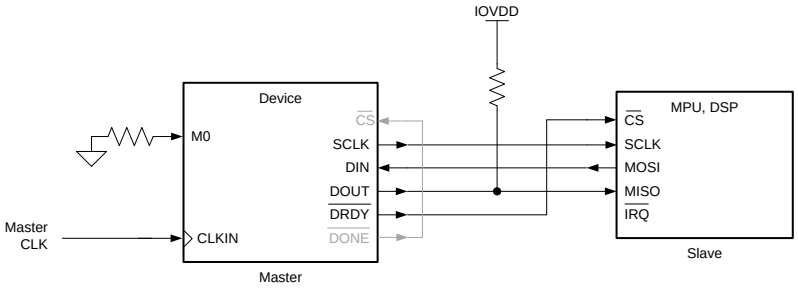


Figure 58. Synchronous Master Mode Device Connections

9.5.2.2.1 Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. Use SCLK to shift in commands and shift out data from the device, similar to the description provided in the *Asynchronous Interrupt Mode* section. The SCLK output equals the ICLK derived from the input clock, CLKIN, using the clock divider control in the CLK1 register. SCLKs continuously output at the ICLK rate with the beginning of a data frame set by a DRDY falling edge.

9.5.2.2.2 Data Input (DIN)

Use the data input (DIN) pin and SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write takes effect following completion of the data frame.

9.5.2.2.3 Data Output (DOUT)

Use the data output pin (DOUT) with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high impedance state when $\overline{CS}$ is high or after the least significant bit is shifted from the output shift register (see the $t_{h(LSB)}$ specification in the *Switching Characteristics: Asynchronous Interrupt Interface Mode* table).

9.5.2.2.4 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ signal is an output that functions as a new data ready indicator and as the control for the start and stop of a data frame. A high-to-low transition of $\overline{DRDY}$ from the ADC indicates that the output shift register is updated with new data and begins a new data frame. Subsequent SCLKs shift out the first device word on DOUT.

9.5.2.2.5 Chip Select ($\overline{CS}$)

For single device operation in synchronous master mode, tie the $\overline{CS}$ line to the $\overline{DONE}$ output signal.

9.5.2.2.6 Synchronous Master Mode Data Retrieval

Figure 59 shows the relationship between $\overline{DRDY}$, DOUT, DIN, and SCLK during data retrieval in synchronous master mode. The high-to-low $\overline{DRDY}$ transition from the ADS131A0x starts a data frame and indicates that new data are available. DIN and DOUT transition on the SCLK rising edge. After the LSB is shifted out $\overline{DRDY}$ returns high, completing the data frame. The ICLK speed must be fast enough to shift out the required bits before new data are available because ICLK determines the SCLK output rate, as described in the *Serial Clock (SCLK)* section. Tie the $\overline{CS}$ signal to the $\overline{DONE}$ signal in single device synchronous master mode.

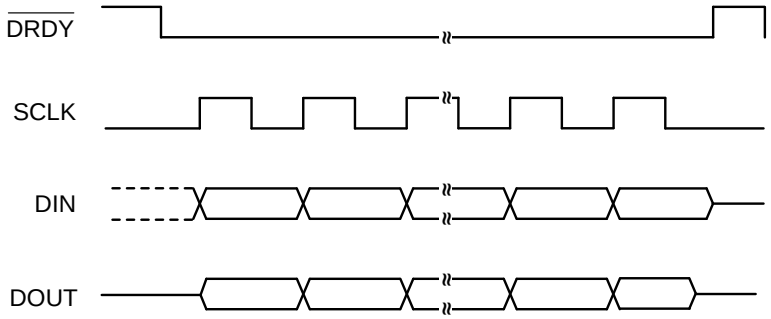


Figure 59. Data Retrieval in Synchronous Master Mode

9.5.2.3 *Synchronous Slave Mode*

The SPI uses five interface signals: $\overline{CS}$, SCLK, DIN, DOUT, and $\overline{DRDY}$ in synchronous slave mode. The $\overline{CS}$, SCLK, DIN, and $\overline{DRDY}$ signals are inputs to the device and the DOUT signal is an output. $\overline{DRDY}$ can be tied directly to $\overline{CS}$ (for a total of four interface lines) or can used independently as a fourth input signal for synchronization to an external event; see the *Data Ready (DRDY)* section for more information on using the $\overline{DRDY}$ line for synchronization. Figure 60 shows typical device connections for the ADS131A0x in synchronous slave mode to a host microprocessor or DSP.

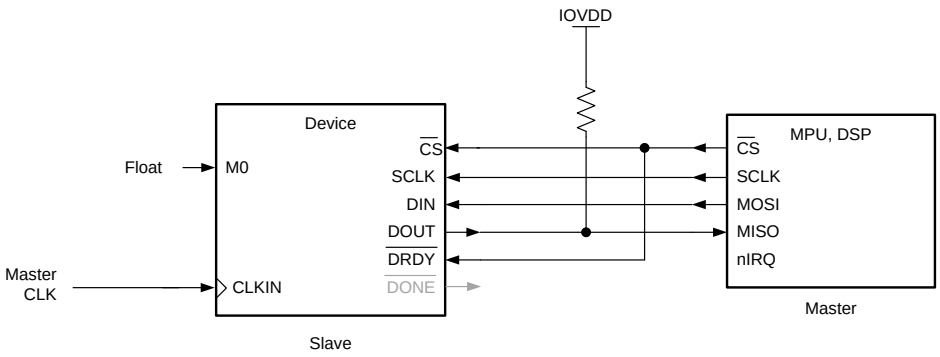


Figure 60. Synchronous Slave Mode Device Connections

9.5.2.3.1 Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) is an active-low input that selects the device for SPI communication and controls the beginning and end of a data frame in synchronous slave mode. $\overline{CS}$ must remain low for the entire duration of the serial communication to complete a command or data readback. When $\overline{CS}$ is taken high, the serial interface (including the data frame) is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. Tie $\overline{CS}$ directly to the $\overline{DRDY}$ input signal to minimize communication lines as long as the synchronization timing in Figure 62 is met. Otherwise, the $\overline{CS}$ line can be used independent of $\overline{DRDY}$.

9.5.2.3.2 Serial Clock (SCLK)

SCLK is the SPI serial clock. Use SCLK to shift in commands on DIN and shift out data from the device on DOUT, similar to the description in the *Asynchronous Interrupt Mode* section.

If the SCLK source is free-running, the SCLK input signal can be set as the ADC ICLK, removing the need of a separate CLKIN. The CLKSRC bit in the CLK1 register controls the source for the ADC ICLK. The modulator clock is derived from the ICLK using the ICLK_DIV[2:0] bits in the CLK2 register; see Figure 29 for a diagram of how SCLK is routed into the device when serving as the ICLK. Setting SCLK as the internal ICLK requires that clocks are sent continuously without any delay or stop periods. Care must be taken to prevent glitches on SCLK at all times.

9.5.2.3.3 Data Input (DIN)

Use the data input pin (DIN) along with SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write will take effect following the completion of the data frame.

9.5.2.3.4 Data Output (DOUT)

Use the data output pin (DOUT) with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high impedance state when $\overline{CS}$ is high or after the least significant bit is shifted from the output shift register (see the $t_{h(LSB)}$ specification in the *Switching Characteristics: Asynchronous Interrupt Interface Mode* table).

9.5.2.3.5 Data Ready ($\overline{DRDY}$)

In synchronous slave mode, $\overline{DRDY}$ is an input signal that must be pulsed at the device set data rate. The $\overline{DRDY}$ input signal is compared to an internally-generated data update signal to verify that these two signals are in sync. A high-to-low $\overline{DRDY}$ transition is expected at the programmed data rate or at multiples thereof. In the event of an unexpected $\overline{DRDY}$ input pulse, the F_RESYNC bit flags in the STAT_1 register and the ADC digital filter resets. Use the $\overline{DRDY}$ input signal as a synchronization method to align new data ready with an external event or with a second ADS131A0x device. In synchronous slave mode, CLKIN or SCLK can be configured as the system clock for the ADC, as explained in Figure 29.

Synchronization timing for the $\overline{\text{DRDY}}$ input signal depends on whether CLKIN or SCLK is used for the system timing. Figure 61 shows the expected behavior of the $\overline{\text{DRDY}}$ input signal with the proper setup and hold timings for $\overline{\text{DRDY}}$ listed in Table 12 when CLKIN is used as the ADC clock (CLKSCR = 0).

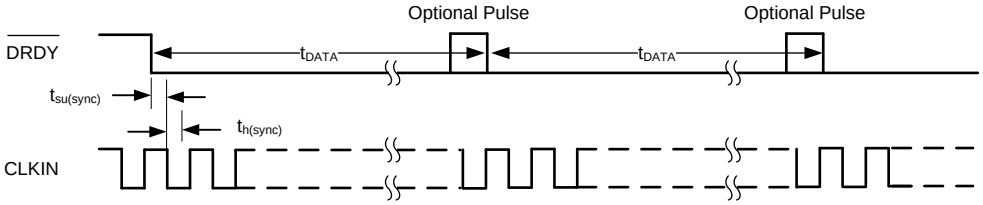


Figure 61. $\overline{\text{DRDY}}$ Synchronization Timing for Synchronous Slave Mode (CLKSRC = 0)

Table 12. $\overline{\text{DRDY}}$ Input Timing (CLKSRC = 0)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(sync)}$	Setup time, $\overline{\text{DRDY}}$ falling edge to CLKIN falling edge (CLKSRC = 0)	10			ns
$t_{h(sync)}$	Hold time, $\overline{\text{DRDY}}$ low after CLKIN falling edge (CLKSRC = 0)	10			ns
t_{DATA}	Data rate period	Set by the CLK1 register and CLK2 register			SPS

Figure 62 shows the expected behavior of the $\overline{\text{DRDY}}$ input signal with proper setup and hold timings for $\overline{\text{DRDY}}$ listed in Table 13 when SCLK is used as the ADC clock (CLKSRC = 1).

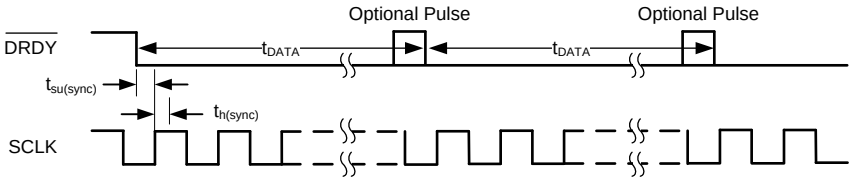


Figure 62. $\overline{\text{DRDY}}$ Synchronization Timing for Synchronous Slave Mode (CLKSRC = 1)

Table 13. $\overline{\text{DRDY}}$ Input Timing (CLKSRC = 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(sync)}$	Setup time, $\overline{\text{DRDY}}$ falling edge to SCLK rising edge (CLKSRC = 1)	10			ns
$t_{h(sync)}$	Hold time, $\overline{\text{DRDY}}$ low after SCLK rising edge (CLKSRC = 1)	10			ns
t_{DATA}	Data rate period	Set by the CLK1 register and CLK2 register			SPS

9.5.2.3.6 Synchronous Slave Mode Data Retrieval

Figure 63 shows the relationship between $\overline{\text{DRDY}}$, $\overline{\text{CS}}$, SCLK, DIN, and DOUT during data retrieval in synchronous slave mode. In synchronous slave mode, the high-to-low $\overline{\text{DRDY}}$ transition sent from the processor must be synchronized with the data rate programmed, or multiples thereof, to avoid a digital filter reset. The data frame begins with a high-to-low $\overline{\text{CS}}$ transition with or after $\overline{\text{DRDY}}$ transitions low. The DIN and DOUT signals transition on the SCLK rising edge. $\overline{\text{DRDY}}$ can return high at any point but must maintain a high-to-low transition at the set data rate to avoid a resynchronization event. To minimize interface lines, the $\overline{\text{CS}}$ signal can be tied directly to the $\overline{\text{DRDY}}$ signal; the timing specifications in the *Timing Requirements: Synchronous Slave Interface Mode* table are still maintained.

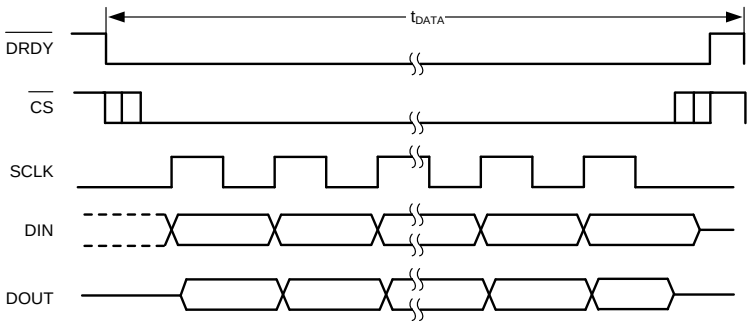


Figure 63. Data Retrieval in Synchronous Slave Mode

9.5.2.4 ADC Frame Complete ($\overline{\text{DONE}}$)

The $\overline{\text{DONE}}$ output signal is an optional interface line that enables chaining multiple devices together to increase channel count. Connect the $\overline{\text{DONE}}$ signal to the $\overline{\text{CS}}$ of the next chained data converter in the system to control the start and stop of the subsequent converter interface. The $\overline{\text{DONE}}$ signal transitions from high to low following the LSB being shifted out. The delay time from the SCLK falling edge shifting out the LSB to the high-to-low $\overline{\text{DONE}}$ transition is configured using the DNDLY[1:0] bits in the D_SYS_CFG register. Figure 64 and Table 14 detail the signals and timings of the $\overline{\text{DONE}}$ signal.

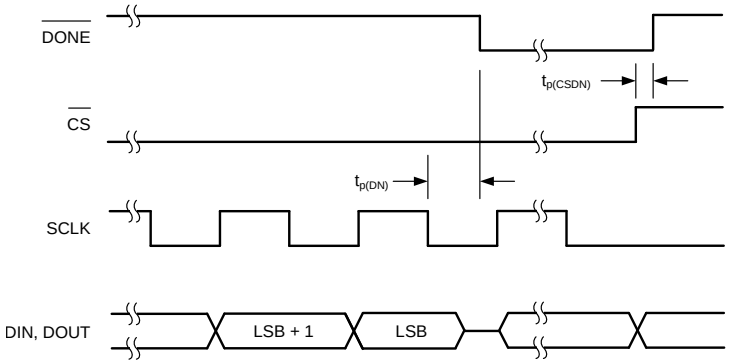


Figure 64. $\overline{\text{DONE}}$ Signal Timing

Table 14. $\overline{\text{DONE}}$ Signal Timing Specifications

PARAMETER			1.65 V ≤ IOVDD ≤ 2.7 V		2.7 V < IOVDD ≤ 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{p(DN)}$	Propagation delay time: SCLK falling edge to $\overline{\text{DONE}}$ falling edge	DNDLY = 00	6	33	6	21	ns
		DNDLY = 01	8	39	8	27	
		DNDLY = 10	10	44	10	32	
		DNDLY = 11	12	48	12	36	
$t_{p(CSDN)}$	Propagation delay time: $\overline{\text{CS}}$ rising edge to $\overline{\text{DONE}}$ rising edge			32		32	ns

For single device operation, configure $\overline{\text{DONE}}$ in the following ways:

- In asynchronous slave mode, either float the $\overline{\text{DONE}}$ output signal or pull the $\overline{\text{DONE}}$ output signal to IOVDD through a 100-kΩ pulldown resistor.
- In synchronous master mode, tie the $\overline{\text{DONE}}$ output signal to the $\overline{\text{CS}}$ input line.
- In synchronous slave mode, either float the $\overline{\text{DONE}}$ output signal float or pull the $\overline{\text{DONE}}$ output signal to IOVDD through a 100-kΩ pulldown resistor.

See the *Chaining for Multiple Device Configuration* section for more information on using the $\overline{\text{DONE}}$ signal for multiple device chaining.

9.5.3 SPI Command Definitions

The ADS131A0x device operation is controlled and configured through ten commands. Table 15 summarizes the available commands. The commands are stand-alone, 16-bit words and reside in the first device word of the data frame. Write zeroes to the remaining LSBs when operating in either 24-bit or 32-bit word sizes because each command is 16-bits in length. The commands are decoded following the completion of a data frame and take effect immediately. Each recognized command is acknowledged with a status output in the first device word of the next data frame.

Table 15. Command Definitions

COMMAND	DESCRIPTION	DEVICE WORD	ADDITIONAL DEVICE WORD	COMMAND STATUS RESPONSE
SYSTEM COMMANDS				
NULL	Null command	0000h		STATUS
RESET	Software reset	0011h		READY
STANDBY	Enter low-power standby mode	0022h		ACK = 0022h
WAKEUP	Wake-up from standby mode	0033h		ACK = 0033h
LOCK	Places the interface in a locked state and ignores all commands except NULL, RREGS, and UNLOCK	0555h		ACK = 0555h
UNLOCK	Brings the device out of an unconfigured POR state or a locked state	0655h		ACK = 0655h
REGISTER WRITE AND READ COMMANDS				
RREG	Read a single register	(001a aaaa nnnn nnnn)b		REG
RREGS	Read *(nnnn nnnn* + 1) registers starting at address *a aaaa*	(001a aaaa nnnn nnnn)b		RREGS
WREG	Write a single register at address *a aaaa* with data *dddd dddd*	(010a aaaa dddd dddd)b		REG (updated register)
WREGS	Write *(nnnn nnnn* + 1) registers beginning at address *a aaaa*. Additional device words are required to send data (*dddd dddd*) to register address (*a*) and data (*eeee eeee*) to register address (*a+1*). Each device word contains data for two registers. The data frame size is extended by (n / 2) device words to allow for command completion.	(011a aaaa nnnn nnnn)b	(dddd dddd eeee eeee)b	ACK = (010a_aaaa_nnnn_nnnn)b

A command status response is 16 bits in length, located in the MSBs of the first device word in the DOUT data frame. The response indicates that the command in the previous data frame is executed. When operating in 24-bit or 32-bit word size modes, the remaining LSBs of the command status response device word read back as zero unless hamming code is used. An example showing the acknowledgment to a user input command is shown in Figure 65.

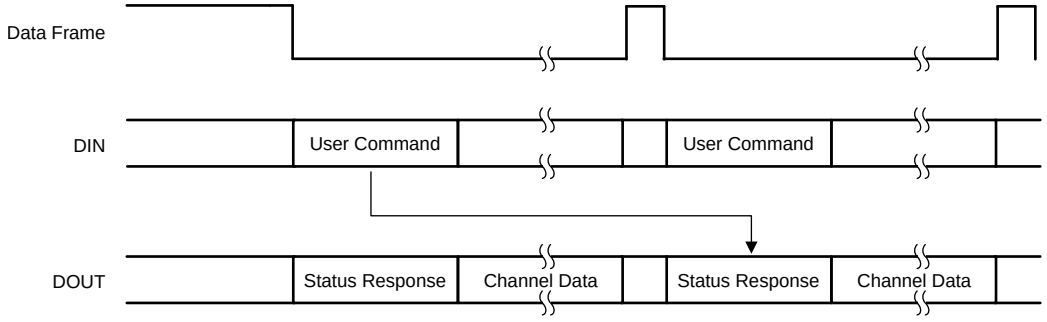


Figure 65. User Command Status Response

Some user commands require multiple data words over multiple device frames. This section describes the commands and details which commands require multiple data words.

The command status responses to the user commands are listed in Table 16. Every data frame begins with one of the listed command status responses on DOUT.

Table 16. Command Status Responses

RESPONSE	DESCRIPTION	DEVICE WORD	ADDITIONAL DEVICE WORD
SYSTEM RESPONSE			
READY	Fixed-status word stating that the device is in a power-up ready state or standby mode and is ready for use. The least significant byte of the device word indicates the address 0 hardware device ID code (*dd*). In the READY state, the device transmits only one word, allowing a 1-word command to be received. An UNLOCK command must be issued before the device responds to other commands.	(FFdd)h	—
ACK	Acknowledgment response. The device has received and executed the command and repeats the received command (*cccc*) as the command status response. (A NULL input does not result in an ACK response).	(cccc)h	—
STATUS/REG	Status byte update. Register address *a aaaa* contains data *dddd dddd*. This command status response is the response to a recognized RREGS or WREG command. An automatic status update of register address (02h) is sent when the NULL command is sent.	(001a aaaa dddd dddd)b	—
RREGS	Response for read (*nnnn nnnn* + 1) registers starting at address *a aaaa*. Data for two registers are output per device word. If the resulting address extends beyond the usable register space, zeroes are returned for remaining non-existent registers. During an RREGS response, any new input commands are ignored until the RREGS status response completes.	(011a aaaa nnnn nnnn)b	(dddd dddd eeee eeee)b

9.5.3.1 NULL: Null Command

The NULL command has no effect on ADC registers or data. Rather than producing an ACK response on DOUT, the command issues a register readback of the STAT_1 register to monitor for general fault updates. An example of the response to a NULL command is shown in Figure 66.

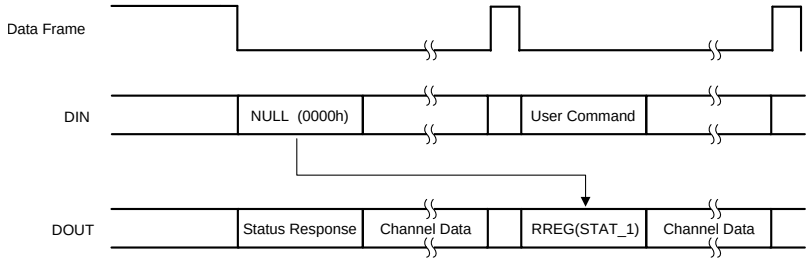


Figure 66. NULL Command Status Response

9.5.3.2 RESET: Reset to POR Values

The RESET command places the ADC into a power-on reset (POR) state, resetting all user registers to the default states. The reset begins following the completion of the frame. When reset completes, the ADC enters a reset locked state and outputs the READY status response on DOUT as the command status response. An example of the response to a RESET command is shown in Figure 67.

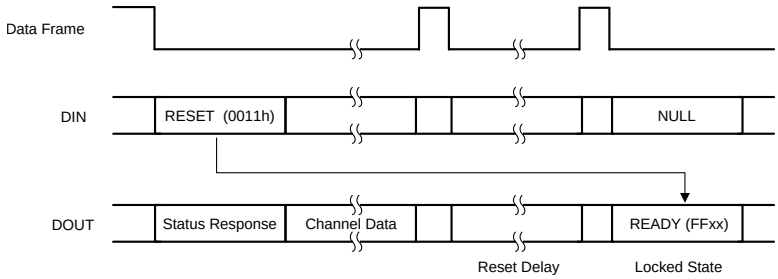


Figure 67. RESET Command Status Response

9.5.3.3 STANDBY: Enter Standby Mode

The STANDBY command places the ADC in a low-power standby mode, halting conversions. The digital interface remains powered, allowing all registers to retain the previous states. When in standby mode, writing and reading from registers is possible and any programmable bits that activate circuitry take effect in the device after the WAKEUP command is issued. The command status response following a STANDBY command is 0022h. In standby mode, the command status response is dependent on the user command that is sent. All ADC channels must be disabled (by writing to the ADCx registers) prior to entering standby mode to reduce current consumption. An example for the response to the STANDBY command and behavior when in standby mode is shown in Figure 68.

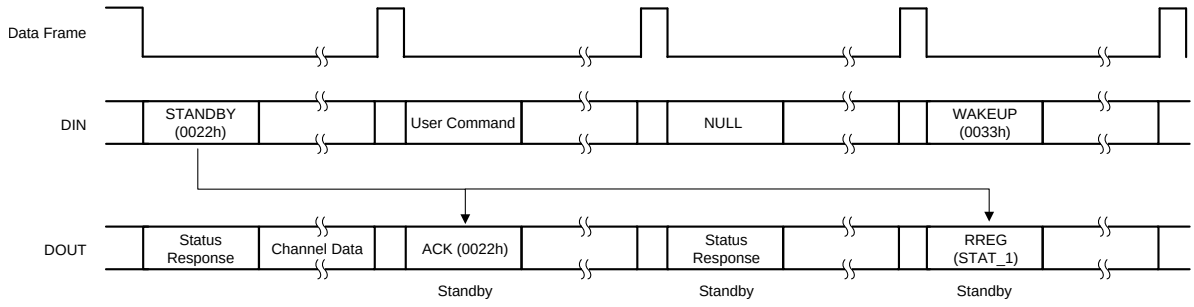


Figure 68. STANDBY Command Status Response

9.5.3.4 WAKEUP: Exit STANDBY Mode

The WAKEUP command brings the ADC out of standby mode. The ADC channels must be enabled (by writing to the ADCx registers) before bringing the device out of standby mode. Allow enough time for all circuits in standby mode to power-up (see the *Electrical Characteristics* table for details). The command status response following a WAKEUP command is 0033h. An example showing the response to exiting standby mode using the WAKEUP command is shown in Figure 69.

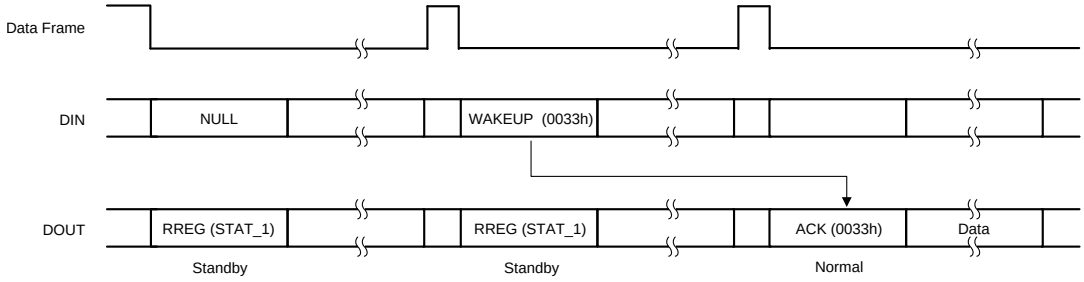


Figure 69. WAKEUP Command Status Response

9.5.3.5 LOCK: Lock ADC Registers

The LOCK command places the converter interface in a locked state where the interface becomes unresponsive to most input commands. The UNLOCK, NULL, RREG, and RREGS commands are the only commands that are recognized when reading back data. Following the LOCK command, the first DOUT status response reads 0555h followed by the command status response of a NULL command (by reading the STAT_1 register). An example showing the response to sending a LOCK command and entering a register locked state is shown in Figure 70.

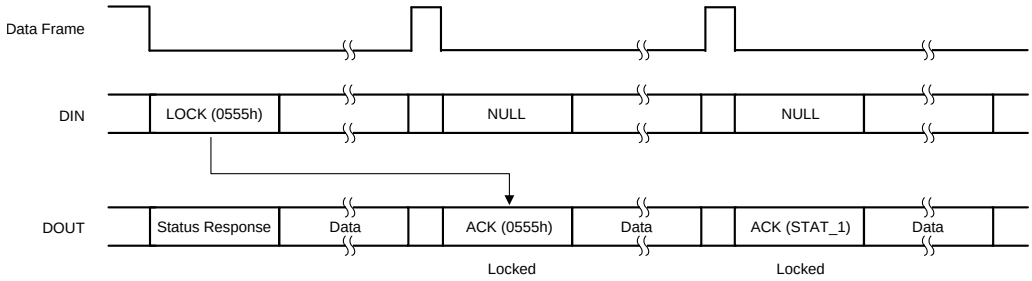


Figure 70. LOCK Command Status Response

9.5.3.6 UNLOCK: Unlock ADC Registers

The UNLOCK command brings the converter out of the locked state, allowing all registers to be accessed in the next data frame. The command status response associated with the UNLOCK command is 0655h. An example of bringing the interface out of the locked state using the UNLOCK command is shown in Figure 71.

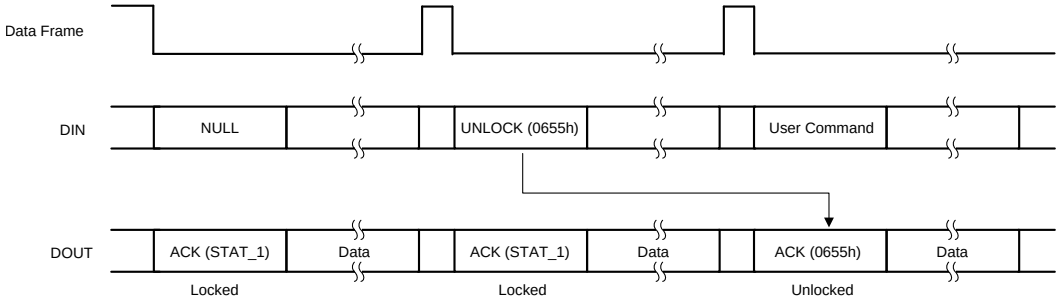


Figure 71. UNLOCK Command Status Response

9.5.3.6.1 UNLOCK from POR or RESET

When powering up the device or coming out of a power-on reset (POR) state, the ADC is in a power-up ready state. In this mode the command status response reads back FFDDh (DD denotes the channel count defined by the NU_CH[3:0] bits in the ID_MSB register), indicating that the ADC power-on cycle is complete and that the ADC is ready to accept commands. Use the UNLOCK command to enable the SPI interface and begin communication with the device. The command status response associated with the UNLOCK command is 0655h. An example of bringing the interface out of power-up ready state using the UNLOCK command is shown in Figure 72.

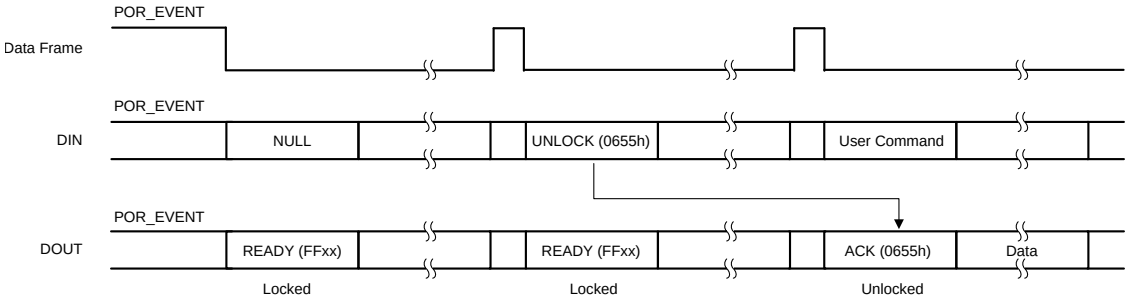


Figure 72. UNLOCK from a POR Command Status Response

9.5.3.7 RREG: Read a Single Register

The RREG command reads register data from the ADC. RREG is a 16-bit command containing the command, the register address, and the number of registers to be to read. The command details are shown below:

First byte: 001*a aaaa*, where *a aaaa* is the starting register address.

Second byte: *nnnn nnnn*, where *nnnn nnnn* is the number of registers to read minus one (n-1).

The ADC executes the command upon completion of the data frame and the register data transmission begins on the first device word of the following data frame. The command status response differs depending on whether a single register or multiple registers are read back. For a single register read, the 16-bit response contains an 8-bit acknowledgment byte with the register address and an 8-bit data byte with the register content. An example showing the command response to a single register read is shown in Figure 73.

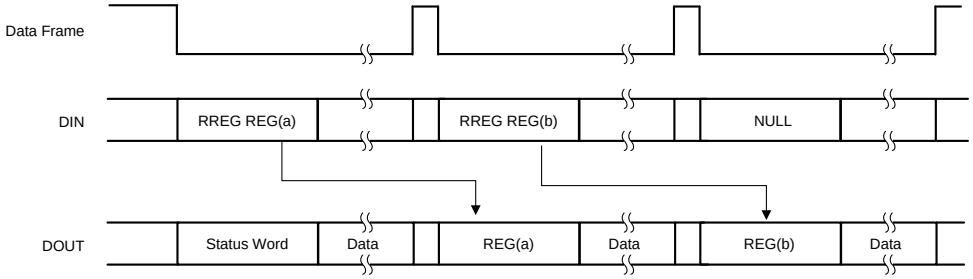


Figure 73. RREGS Command Status Response (Single Register Read)

9.5.3.8 RREGS: Read Multiple Registers

For a multiple register read back, the command status response exceeds the 16-bit reserved device word space, causing an overflow to additional command status words. The first command status response is an acknowledgment of multiple registers to be read back and the additional command status responses shift out register data. The command status response details are shown below:

First command status response: 011*a aaaa nnnn nnnn*, where *a aaaa* is the starting register address and *nnnn nnnn* is the number of registers to read minus one (n-1).

Additional command status responses: *dddd dddd eeee eeee* , where *dddd dddd* is the register data from the first register read back and *eeee eeee* is the register data from the second read back register.

The number of additional command status responses across multiple frames is dependent on the number of registers to be read back. During a RREGS command status response, any new input commands are ignored until the command completes by shifting out all necessary command status responses. If the resulting address extends beyond the usable register space, zeroes are returned for any remaining non-existent registers. An example of the command response to reading four registers using a RREGS command is shown in Figure 74.

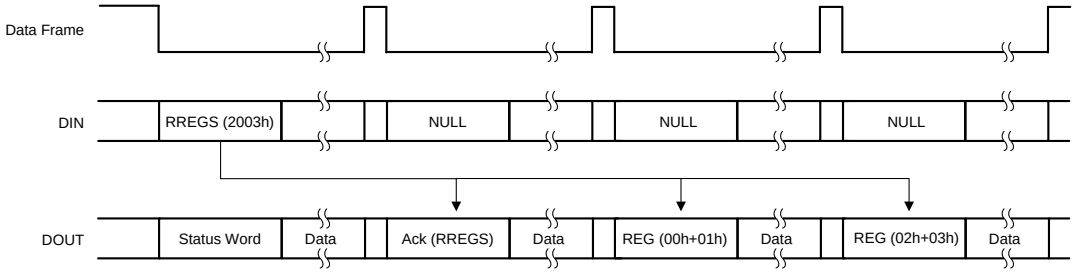


Figure 74. RREGS Command Status Response (Multiple Register Read)

9.5.3.9 WREG: Write Single Register

The WREG command writes data to a single register. The single register write command is a two-byte command containing the address and the data to write to the address. The command details are shown below:

First byte: 010*a aaaa*, where *a aaaa* is the register address.

Second byte: *dddd dddd*, where *dddd dddd* is the data to write to the address.

The resulting command status response is a register read back from the updated register. An example of a single register write and response is shown in Figure 75.

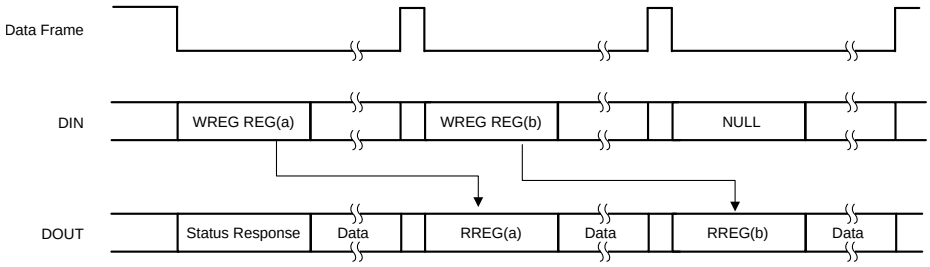


Figure 75. WREG Command Status Response (Single Register Write)

9.5.3.10 WREGS: Write Multiple Registers

The WREGS command writes data to multiple registers. The command steps through each register incrementally, thus allowing the user to incrementally write to each register. This process extends the data frame by (n) device words to complete the command. If the resulting address extends beyond the usable register space, any following data for non-existent registers are ignored. The 16 bits contained in the first device word contain the command, the starting register address, and the number of registers to write, followed by additional device words for the register data. The command details are shown below:

First user command device word: 011*a aaaa nnnn nnnn*, where *a aaaa* is the starting register address and *nnnn nnnn* is the number of registers to write minus one (n-1).

Additional user command device words: *dddd dddd eeee eeee*, where *dddd dddd* is the data to write to the first register and *eeee eeee* is the register data for the second register.

The user command device word uses the 16 MSBs regardless of word length (that is, only the 16 MSBs are used in 16-bit, 24-bit, or 32-bit word lengths). When additional command device words are required, only a maximum of two 8-bit registers can be written per command and any additional LSBs beyond 16 bits are ignored. The command status response for the WREGS command is 010*a aaaa nnnn nnnn*, where *a aaaa* is the starting register address and *nnnn nnnn* is the number of registers written plus one (n+1). An example of a multiple register write and the command status response is shown in Figure 76.

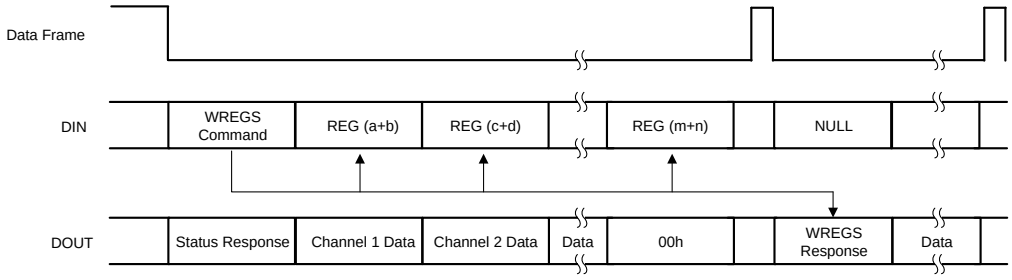


Figure 76. WREGS Command Status Response (Multiple Register Write)

9.6 Register Maps

Table 17. Register Map

ADDRESS (Hex)	REGISTER NAME	DEFAULT SETTING	REGISTER BITS							
			7	6	5	4	3	2	1	0
Read Only ID Registers										
00h	ID_MSB	xxh	DEV_ID[3:0]				NU_CH[3:0]			
01h	ID_LSB	00h	0	0	0	0	0	0	0	0
Status Registers										
02h	STAT_1	00h	0	F_OPC	F_SPI	F_ADCIN	F_WDT	F_RESYNC	F_DRDY	F_CHECK
03h	STAT_P	00h	0	0	0	0	F_IN4P	F_IN3P	F_IN2P	F_IN1P
04h	STAT_N	00h	0	0	0	0	F_IN4N	F_IN3N	F_IN2N	F_IN1N
05h	STAT_S	00h	0	0	0	0	0	F_STARTUP	F_CS	F_FRAME
06h	ERROR_CNT	00h	ER[7:0]							
07h	STAT_M2	xxh	0	0	M2PIN[1:0]		M1PIN[1:0]		M0PIN[1:0]	
08h	Reserved	00h	0	0	0	0	0	0	0	0
09h	Reserved	00h	0	0	0	0	0	0	0	0
User Configuration Registers										
0Ah	Reserved	00h	0	0	0	0	0	0	0	0
0Bh	A_SYS_CFG	60h	VNCPEN	HRM	1	VREF_4V	INT_REFEN	COMP_TH[2:0]		
0Ch	D_SYS_CFG	3Ch	WDT_EN	CRC_MODE	DNDLY[1:0]		HIZDLY[1:0]		FIXED	CRC_EN
0Dh	CLK1	08h	CLKSRC	0	0	0	CLK_DIV[2:0]			0
0Eh	CLK2	86h	ICLK_DIV[2:0]			0	OSR[3:0]			
0Fh	ADC_ENA	00h	0	0	0	0	ENA[3:0]			
10h	Reserved	00h	0	0	0	0	0	0	0	0
11h	ADC1	00h	0	0	0	0	0	GAIN1_2	GAIN1_1	GAIN1_0
12h	ADC2	00h	0	0	0	0	0	GAIN2_2	GAIN2_1	GAIN2_0
13h	ADC3(1)	00h	0	0	0	0	0	GAIN3_2	GAIN3_1	GAIN3_0
14h	ADC4(1)	00h	0	0	0	0	0	GAIN4_2	GAIN4_1	GAIN4_0

(1) This register is for the ADS131A04 only. This register is reserved for the ADS131A02.

9.6.1 User Register Description

9.6.1.1 ID_MSB: ID Control Register MSB (address = 00h) [reset = xxh]

This register is programmed during device manufacture to indicate device characteristics.

Figure 77. ID_MSB Register

7	6	5	4	3	2	1	0
DEV_ID[3:0]				NU_CH[3:0]			
R-Undefined(1)				R-Undefined(1)			

LEGEND: R = Read only; -n = value after reset

(1) Reset values are device dependent.

Table 18. ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DEV_ID[3:0]	R	Undefined(1)	**Device ID.** These bits indicate the revision of the device and are subject to change without notice. 0000: ADS131A02 0001: ADS131A04
3-0	NU_CH[3:0]	R	Undefined(1)	**Channel count identification bits.** These bits indicate the device channel count. 0010: 2-channel device 0100: 4-channel device

(1) Reset values are device dependent.

9.6.1.2 ID_LSB: ID Control Register LSB (address = 01h) [reset = 00h]

This register is reserved for future use.

Figure 78. ID_LSB Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 19. ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	**Reserved**. Always read 0.

9.6.1.3 STAT_1: Status 1 Register (address = 02h) [reset = 00h]

This register contains general fault updates. This register is automatically transferred on the command status response when the NULL command is sent.

Figure 79. STAT_1 Register

7	6	5	4	3	2	1	0
0	F_OPC	F_SPI	F_ADCIN	F_WDT	F_RESYNC	F_DRDY	F_CHECK
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 20. STAT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	**Reserved**. Always read 0.
6	F_OPC	R	0h	**Fault command.** This bit indicates that a received command is not recognized as valid and the command is ignored. This bit auto-clears on a STAT_1 data transfer, unless the condition remains. When in a locked state, this bit is set if any command other than LOCK, UNLOCK, NULL, or RREGS is written to the device. 0: No fault has occurred 1: Possible invalid command is ignored
5	F_SPI	R	0h	**Fault SPI.** This bit indicates that one of the status bits in the STAT_S register is set. Read the STAT_S register to clear the bit. 0: No fault has occurred 1: A bit in the STAT_S register is set high
4	F_ADCIN	R	0h	**Fault ADC input.** This bit indicates that one of the ADC input fault detection bits in the STAT_P or STAT_N register is set. Read the STAT_P and STAT_N registers to clear the bit. 0: No fault has occurred 1: A bit in the STAT_P or STAT_N register is set high
3	F_WDT	R	0h	**Watchdog timer timeout.** This bit indicates if the watchdog timer times out before a new data frame transfer occurs. 0: No fault has occurred 1: Timer has run out (resets following register read back)
2	F_RESYNC	R	0h	**Fault resynchronization.** This bit is set whenever the signal path is momentarily reset resulting from a $\overline{\text{DRDY}}$ synchronization event. 0: Devices are in sync 1: Signal path is momentarily reset to maintain synchronization
1	F_DRDY	R	0h	**Fault data ready.** This bit is set if data shifted out from the previous result are not complete by the time new ADC data are ready. The ADC $\overline{\text{DRDY}}$ line pulses, indicating that new data are available and overwrite the current data. This bit auto-clears on a STAT_1 transfer, unless the condition remains. 0: Data read back complete before new data update 1: New data update during DOUT data transmission
0	F_CHECK	R	0h	**Fault DIN check.** This bit is set if either of the following conditions are detected: • Uncorrectable hamming error correction state is determined for any DIN word transfer when hamming code is enabled. • CRC check word on DIN fails. The input command that triggered this error is ignored. This bit auto-clears on a STAT_S transfer, unless the condition remains. 0: No error in DIN transmission 1: DIN transmission error

9.6.1.4 STAT_P: Positive Input Fault Detect Status Register (address = 03h) [reset = 00h]

This register stores the status of whether the positive input on each channel exceeds the threshold set by the COMP_TH[2:0] bits; see the *Input Overrange and Underrange Detection* section for details.

Figure 80. STAT_P Register

7	6	5	4	3	2	1	0
0	0	0	0	F_IN4P	F_IN3P	F_IN2P	F_IN1P
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 21. STAT_P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	**Reserved**. Always read 0.
3	F_IN4P(1)	R	0h	**AIN4P threshold detect.** 0: The channel 4 positive input pin does not exceed the set threshold 1: The channel 4 positive input pin exceeds the set threshold
2	F_IN3P(1)	R	0h	**AIN3P threshold detect.** 0: The channel 3 positive input pin does not exceed the set threshold 1: The channel 3 positive input pin exceeds the set threshold
1	F_IN2P	R	0h	**AIN2P threshold detect**. 0: The channel 2 positive input pin does not exceed the set threshold 1: The channel 2 positive input pin exceeds the set threshold
0	F_IN1P	R	0h	**AIN1P threshold detect.** 0 =The channel 1 positive input pin does not exceed the set threshold 1: The channel 1 positive input pin exceeds the set threshold

(1) This bit is not available in the ADS131A02 and always read 0.

9.6.1.5 STAT_N: Negative Input Fault Detect Status Register (address = 04h) [reset = 00h]

This register stores the status of whether the negative input on each channel exceeds the threshold set by the COMP_TH[2:0] bits; see the *Input Overrange and Underrange Detection* section for details.

Figure 81. STAT_N Register

7	6	5	4	3	2	1	0
0	0	0	0	F_IN4N	F_IN3N	F_IN2N	F_IN1N
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 22. STAT_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	**Reserved**. Always read 0.
3	F_IN4N(1)	R	0h	**AIN4N threshold detect.** 0: The channel 4 negative input pin does not exceed the set threshold 1: The channel 4 negative input pin exceeds the set threshold
2	F_IN3N(1)	R	0h	**AIN3N threshold detect.** 0: The channel 3 negative input pin does not exceed the set threshold 1: The channel 3 negative input pin exceeds the set threshold
1	F_IN2N	R	0h	**AIN2N threshold detect.** 0: The channel 2 negative input pin does not exceed the set threshold 1: The channel 2 negative input pin exceeds the set threshold
0	F_IN1N	R	0h	**AIN1N threshold detect.** 0: The channel 1 negative input pin does not exceed the set threshold 1: The channel 1 negative input pin exceeds the set threshold

(1) This bit is not available in the ADS131A02 and always read 0.

9.6.1.6 STAT_S: SPI Status Register (address = 05h) [reset = 00h]

This register indicates the detection of SPI fault conditions.

Figure 82. STAT_S Register

7	6	5	4	3	2	1	0
0	0	0	0	0	F_STARTUP	F_CS	F_FRAME
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 23. STAT_S Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	**Reserved**. Always read 0.
2	F_STARTUP	R	0h	**ADC startup fault.** This bit indicates if an error is detected during power-up. This bit clears only when power is recycled. 0: No fault is occurred 1: A fault has occurred
1	F_CS	R	0h	**Chip-select fault.** This bit is set if $\overline{CS}$ transitions when the SCLK pin is high. This bit auto-clears on a STAT_S transfer, unless the condition remains. 0: $\overline{CS}$ is asserted or deasserted when SCLK is low 1: $\overline{CS}$ is asserted or deasserted when SCLK is high
0	F_FRAME	R	0h	**Fame fault.** This bit is set if the device detects that not enough SCLK cycles are sent in a data frame for the existing mode of operation. This bit auto-clears on a STAT_S transfer, unless the condition remains. 0: Enough SCLKs are sent per frame 1: Not enough SCLKs are sent per frame

9.6.1.7 ERROR_CNT: Error Count Register (address = 06h) [reset = 00h]

This register counts the hamming and CRC errors. This register is cleared when read.

Figure 83. ERROR_CNT Register

7	6	5	4	3	2	1	0
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 24. ERROR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ER[7:0]	R	0h	**Error tracking count.** These bits count the number of hamming and CRC errors on the input. The counter saturates if the number of errors exceeds 255, FFh. This register is cleared when read.

9.6.1.8 STAT_M2: Hardware Mode Pin Status Register (address = 07h) [reset = xxh]

This register indicates detection of the captured states of the hardware mode pins.

Figure 84. STAT_M2 Register

7	6	5	4	3	2	1	0
0	0	M2PIN[1:0]		M1PIN[1:0]		M0PIN[1:0]	
R-0h	R-0h	R-Undefined(1)		R-Undefined(1)		R-Undefined(1)	

LEGEND: R = Read only; -n = value after reset

(1) Reset values are dependent on the state of the hardware pin.

Table 25. STAT_M2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	**Reserved**. Always read 0.
5-4	M2PIN[1:0]	R	Undefined(1)	**M2 captured state.** These bits indicate the captured state of the M2 hardware control pins. 00: GND (hamming code word validation off) 01: IOVDD (hamming code word validation on) 10: No connection 11: Reserved
3-2	M1PIN[1:0]	R	Undefined(1)	**M1 captured state.** These bits indicate the captured states of the M1 hardware control pins. 00: GND (24-bit device word) 01: IOVDD (32-bit device word) 10: No connection (16-bit device word) 11: Reserved
1-0	M0PIN[1:0]	R	Undefined(1)	**M0 captured state.** These bits indicate the captured states of the M0 hardware control pins. 00: GND (synchronous master mode) 01: IOVDD (asynchronous slave mode) 10: No connection (synchronous slave mode) 11: Reserved

(1) Reset values are dependent on the state of the hardware pin.

9.6.1.9 Reserved Registers (address = 08h to 0Ah) [reset = 00h]

This register is reserved for future use.

Figure 85. Reserved Registers

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 26. Reserved Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	**Reserved**. Always read 0.

9.6.1.10 A_SYS_CFG: Analog System Configuration Register (address = 0Bh) [reset = 60h]

This register configures the analog features in the ADS131A0x.

Figure 86. A_SYS_CFG Register

7	6	5	4	3	2	1	0
VNCPEN	HRM	1	VREF_4V	INT_REFEN	COMP_TH[2:0]		
R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 27. A_SYS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VNCPEN	R/W	0h	**Negative charge pump enable.** This bit enables the negative charge pump when using a 3.0-V to 3.45-V unipolar power supply. 0: Negative charge pump powered down 1: Negative charge pump enabled
6	HRM	R/W	1h	**High-resolution mode.** This bit selects between high-resolution and low-power mode. 0: Low-power mode 1: High-resolution mode
5	Reserved	R/W	1h	**Reserved**. Always write 1.
4	VREF_4V	R/W	0h	**REFP reference voltage level.** This bit determines the REFP reference voltage level when using the internal reference. 0: REFP is set to 2.442 V 1: REFP is set to 4.0 V
3	INT_REFEN	R/W	0h	**Enable internal reference.** This bit connects the internal reference voltage to the reference buffer to use the internal reference 0: External reference voltage 1: Internal reference voltage enabled
2-0	COMP_TH[2:0]	R/W	0h	**Fault detect comparator threshold.** These bits determine the fault detect comparator threshold level settings; see the *Input Overrange and Underrange Detection* section for details. Table 28 lists the bit settings for the high- and low-side thresholds. Values are approximate and are referenced to the device analog supply range. When VNCPEN = 0, AVDD and AVSS are used for the high and low threshold. When VNCPEN = 1, AVDD is used for the high threshold value. A –1.5-V supply, generated from the negative charge pump, is used for the low threshold value.

Table 28. COMP_TH[2:0] Bit Settings

COMP_TH[2:0]	COMPARATOR HIGH-SIDE THRESHOLD (%)	COMPARATOR LOW-SIDE THRESHOLD (%)
000	95	5
001	92.5	7.5
010	90	10
011	87.5	12.5
100	85	15
101	80	20
110	75	25
111	70	30

9.6.1.11 D_SYS_CFG: Digital System Configuration Register (address = 0Ch) [reset = 3Ch]

This register configures the digital features in the ADS131A0x.

Figure 87. D_SYS_CFG Register

7	6	5	4	3	2	1	0
WDT_EN	CRC_MODE	DNDLY[1:0]		HIZDLY[1:0]		FIXED	CRC_EN
R/W-0h	R/W-0h	R/W-3h		R/W-3h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 29. D_SYS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WDT_EN	R/W	0h	**Watchdog timer enable.** This bit enables the watchdog timeout counter when set. Issue a hardware or software reset when disabling the watchdog timer for internal device synchronization; see the *Watchdog Timer* section. 0: Watchdog disabled 1: Watchdog enabled
6	CRC_MODE	R/W	0h	**CRC mode select.** This bit determines which bits in the frame the CRC is valid for; see the *Cyclic Redundancy Check (CRC)* section. 0: CRC is valid on only the device words being sent and received 1: CRC is valid on all bits received and transmitted
5-4	DNDLY[1:0]	R/W	3h	**$\overline{\text{DONE}}$ delay.** These bits configure the time before the device asserts $\overline{\text{DONE}}$ after the LSB is shifted out. 00: ≥ 6-ns delay 01: ≥ 8-ns delay 10: ≥ 10-ns delay 11: ≥ 12-ns delay
3-2	HIZDLY[1:0]	R/W	3h	**Hi-Z delay.** These bits configure the time that the device asserts Hi-Z on DOUT after the LSB of the data frame is shifted out. 00: ≥ 6-ns delay 01: ≥ 8-ns delay 10: ≥ 10-ns delay 11: ≥ 12-ns delay
1	FIXED	R/W	0h	**Fixed word size enable.** This bit sets the data frame size. 0: Device words per data frame depends on whether the CRC and ADCs are enabled 1: Fixed six device words per frame for the ADS131A04 or fixed four device words per data frame for the ADS131A02
0	CRC_EN	R/W	0h	**Cyclic redundancy check enable.** This bit enables the CRC data word for both the DIN and DOUT data frame transfers. When enabled, DIN commands must pass the CRC checks to be recognized by the device. 0: CRC disabled 1: CRC enabled

9.6.1.12 CLK1: Clock Configuration 1 Register (address = 0Dh) [reset = 08h]

This register configures the ADC clocking and sets the internal clock dividers.

Figure 88. CLK1 Register

7	6	5	4	3	2	1	0
CLKSRC	0	0	0	CLK_DIV[2:0]			0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-4h			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 30. CLK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKSRC	R/W	0h	**ADC clock source.** This bit selects the source for ICLK; see the *Clock* section for more information on ADC clocking. 0: XTAL1/CLKIN pin or XTAL1/CLKIN and XTAL2 pins 1: SCLK pin
6-4	Reserved	R/W	0h	**Reserved**. Always write 0.
3-1	CLK_DIV[2:0]	R/W	4h	**CLKIN divider ratio.** These bits set the CLKIN divider ratio to generate the internal f_{ICLK} frequency. ICLK is used as the f_{SCLK} output when the ADC is operating in an SPI master mode. 000: Reserved 001: $f_{ICLK} = f_{CLKIN} / 2$ 010: $f_{ICLK} = f_{CLKIN} / 4$ 011: $f_{ICLK} = f_{CLKIN} / 6$ 100: $f_{ICLK} = f_{CLKIN} / 8$ 101: $f_{ICLK} = f_{CLKIN} / 10$ 110: $f_{ICLK} = f_{CLKIN} / 12$ 111: $f_{ICLK} = f_{CLKIN} / 14$
0	Reserved	R/W	0h	**Reserved**. Always write 0.

9.6.1.13 CLK2: Clock Configuration 2 Register (address = 0Eh) [reset = 86h]

This register configures the ADC modulator clock and oversampling ratio for the converter.

Figure 89. CLK2 Register

7	6	5	4	3	2	1	0
ICLK_DIV[2:0]			0	OSR[3:0]			
R/W-4h			R/W-0h	R/W-6h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 31. CLK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	ICLK_DIV[2:0]	R/W	4h	**ICLK divide ratio.** These bits set the divider ratio to generate the ADC modulator clock, f_{MOD}, from the f_{ICLK} signal. 000: Reserved 001: $f_{MOD} = f_{ICLK} / 2$ 010: $f_{MOD} = f_{ICLK} / 4$ 011: $f_{MOD} = f_{ICLK} / 6$ 100: $f_{MOD} = f_{ICLK} / 8$ 101: $f_{MOD} = f_{ICLK} / 10$ 110: $f_{MOD} = f_{ICLK} / 12$ 111: $f_{MOD} = f_{ICLK} / 14$
4	Reserved	R/W	0h	**Reserved**. Always write 0.
3:0	OSR[3:0]	R/W	6h	**Oversampling ratio.** These bits set the OSR to create the ADC output data rate, f_{DATA}; see Table 32 for more details. 0000: $f_{DATA} = f_{MOD} / 4096$ 0001: $f_{DATA} = f_{MOD} / 2048$ 0010: $f_{DATA} = f_{MOD} / 1024$ 0011: $f_{DATA} = f_{MOD} / 800$ 0100: $f_{DATA} = f_{MOD} / 768$ 0101: $f_{DATA} = f_{MOD} / 512$ 0110: $f_{DATA} = f_{MOD} / 400$ 0111: $f_{DATA} = f_{MOD} / 384$ 1000: $f_{DATA} = f_{MOD} / 256$ 1001: $f_{DATA} = f_{MOD} / 200$ 1010: $f_{DATA} = f_{MOD} / 192$ 1011: $f_{DATA} = f_{MOD} / 128$ 1100: $f_{DATA} = f_{MOD} / 96$ 1101: $f_{DATA} = f_{MOD} / 64$ 1110: $f_{DATA} = f_{MOD} / 48$ 1111: $f_{DATA} = f_{MOD} / 32$

Table 32. Data Rate Settings

OSR[3:0]	OSR	f_{DATA} AT 2.048-MHz f_{MOD} (kHz)	f_{DATA} AT 4.096-MHz f_{MOD} (kHz)	f_{DATA} AT 4-MHz f_{MOD} (kHz)
0000	4096	0.500	1.000	0.977
0001	2048	1.000	2.000	1.953
0010	1024	2.000	4.000	3.906
0011	800	2.560	5.120	5.000
0100	768	2.667	5.333	5.208
0101	512	4.000	8.000	7.813
0110	400	5.120	10.240	10.000
0111	384	5.333	10.667	10.417
1000	256	8.000	16.000	15.625
1001	200	10.240	20.480	20.000
1010	192	10.667	21.333	20.833
1011	128	16.000	32.000	31.250
1100	96	21.333	42.667	41.667
1101	64	32.000	64.000	62.500
1110	48	42.667	85.333	83.333
1111	32	64.000	128.000	125.000

9.6.1.14 ADC_ENA: ADC Channel Enable Register (address = 0Fh) [reset = 00h]

This register controls the enabling of ADC channels.

Figure 90. ADC_ENA Register

7	6	5	4	3	2	1	0
0	0	0	0	ENA[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 33. ADC_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0h	**Reserved**. Always write 0.
3-0	ENA[3:0]	R/W	0h	**Enable ADC channels.** These bits power-up or power-down the ADC channels. Note that this setting is global for all channels. 0000: All ADC channels powered down 1111: All ADC channels powered up

9.6.1.15 Reserved Register (address = 10h) [reset = 00h]

This register is reserved for future use.

Figure 91. Reserved Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read only; -n = value after reset

Table 34. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0h	**Reserved**. Always write 0.

9.6.2 ADCx: ADC Channel Digital Gain Configuration Registers (address = 11h to 14h) [reset = 00h]

These registers control the digital gain setting for the individual ADC channel (x denotes the ADC channel). For the ADS131A02, these registers are reserved.

Figure 92. ADC1 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	GAIN1_2	GAIN1_1	GAIN1_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 93. ADC2 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	GAIN2_2	GAIN2_1	GAIN2_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 94. ADC3 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	GAIN3_2	GAIN3_1	GAIN3_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 95. ADC4 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	GAIN4_2	GAIN4_1	GAIN4_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 35. ADCx Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0h	**Reserved**. Always write 0.
2-0	GAINx_[2:0]	R/W	0h	**Gain control (digital scaling).** These bits determine the digital gain of the ADC output. 000: Gain = 1 001: Gain = 2 010: Gain = 4 011: Gain = 8 100: Gain = 16 101, 110, 111: Reserved

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave any unused analog inputs floating or connected to AVSS. For the ADS131A02, the NC pins (pins 5-8) can be left floating or tied directly to AVSS.

Pin 24 is a digital output NC pin. Leave pin 24 floating or tied to GND through a 10-kΩ pulldown resistor.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, IOVDD or DGND, even when in power-down mode. If the DONE or DRDY outputs are not used, leave these pins (pins 18 and 19, respectively) unconnected or tie these pins to IOVDD using a weak pullup resistor.

10.1.2 Power Monitoring Specific Applications

Each channel of the ADS131A0x is identical, giving designers the flexibility to sense voltage or current with any channel. Simultaneous sampling allows the application to calculate instantaneous power for any simultaneous voltage and current measurement. Figure 96 shows an example system that measures voltage and current simultaneously.

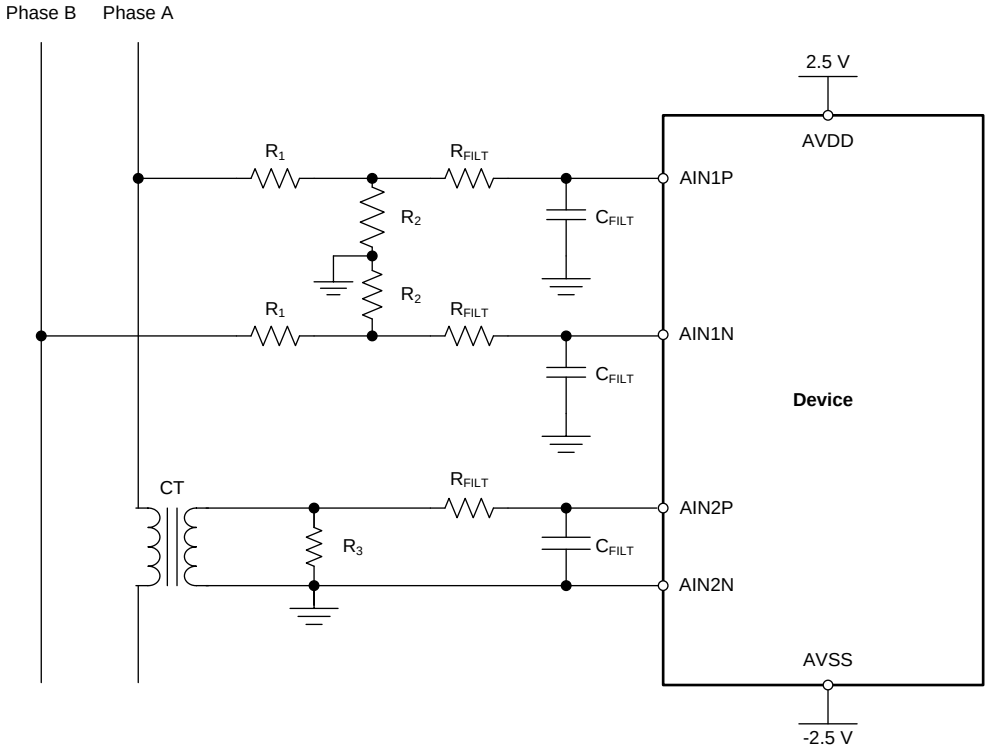


Figure 96. Example Power-Monitoring System

Application Information (continued)

In Figure 96, channel 1 is dedicated to measuring the voltage between phase A and phase B and channel 2 is dedicated to measuring the current on phase A.

The resistors R_1 and R_2 form a voltage divider that steps the line voltage down to within the measurement range of the ADC. R_1 can actually be formed by multiple resistors in series to dissipate power across several components. Note that this configuration is also valid in case the voltage is measured with respect to neutral instead of between phases.

Channel 2 is dedicated to measuring current that flows on phase A. The resistor R_3 serves as a burden resistor that is used to shunt the current that flows across the secondary coil of the current transformer (CT). Current can also be measured using a Rogowski coil and an analog integrator or by performing integration digitally after a conversion.

The RC filters formed by R_{FILT} and C_{FILT} serve as antialiasing filters for the converter. If an application requires a steeper roll-off, a second-order RC filter can be used.

10.1.3 Chaining for Multiple Device Configuration

The ADS131A0x allows the designer to add channels by adding an additional device to the bus. The first device in the chain can be configured using any of the interface modes. All subsequent devices must be configured in synchronous slave mode. In all cases, however, the chain of ADS131A0x devices appear as a single device with extra channels with the exception that each device sends individual status and data integrity words. In this manner, no additional pins on the host are required for an additional device on the chain. There are no special provisions that must be made in the interface except for extending the frame to the appropriate length.

10.1.3.1 First Device Configured in Asynchronous Interrupt Mode

Figure 97 illustrates a multiple device configuration where the first device is configured in asynchronous interrupt mode as noted by the state of the M0 pin. Note that the second ADS131A0x device and any additional devices are configured in synchronous slave mode. Figure 98 illustrates an example interface timing diagram for this configuration.

Application Information (continued)

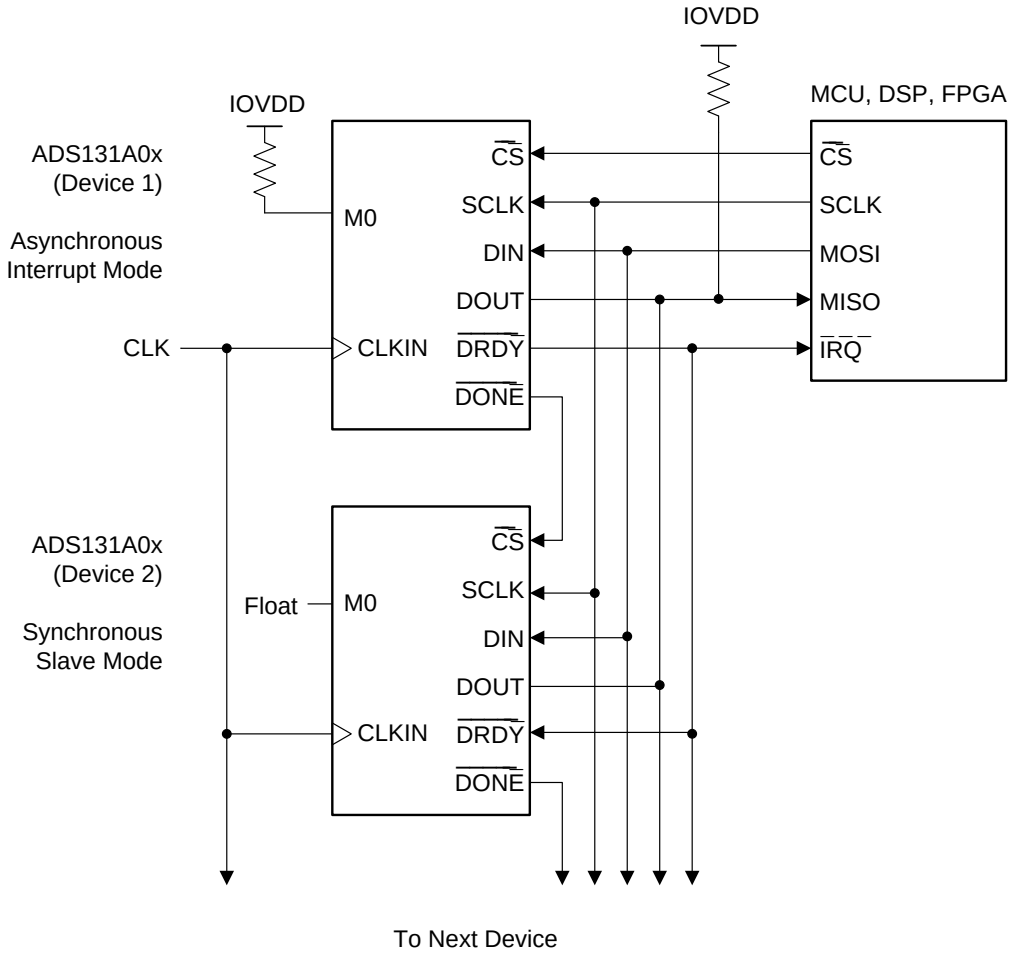
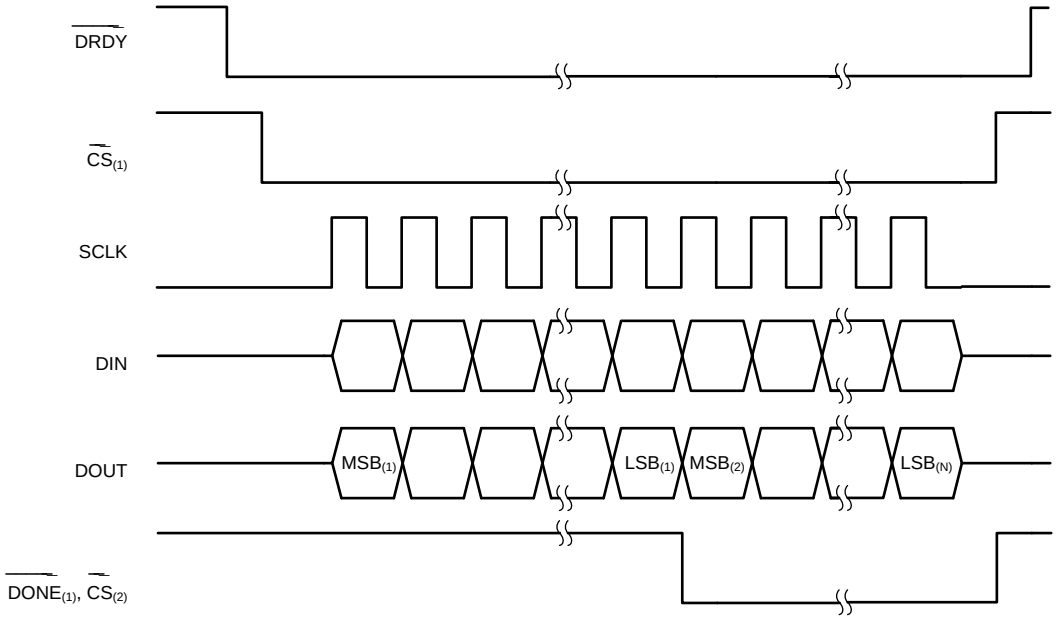


Figure 97. Multiple Device Configuration Using Asynchronous Interrupt Mode

Application Information (continued)



NOTE: (1) denotes device 1, (2) denotes device 2, and (N) denotes device N.

Figure 98. Multiple Device Configuration Timing Diagram when Using Asynchronous Interrupt Mode

The $\overline{\text{DONE}}$ pin of each device connects to the $\overline{\text{CS}}$ pin of the subsequent device. In each case, after a device shifts out the contents of the output shift register, the device deasserts $\overline{\text{DONE}}$, causing the subsequent device to be selected for communication. The DOUT of a device whose contents are already shifted out assumes a high-impedance state, allowing the DOUT pins of all devices to be tied together.

To send commands to specific devices, send the respective command of the device when that device is selected for communication.

The $\overline{\text{DRDY}}$ output of the first device serves as an input to all other devices to synchronize conversions.

10.1.3.2 First Device Configured in Synchronous Master Mode

Figure 99 illustrates a multiple device configuration where the first device is configured in synchronous master mode as noted by the state of the M0 pin. Note that the second ADS131A0x device and any additional devices are configured in synchronous slave mode. Figure 100 illustrates an example interface timing diagram for this configuration.

Application Information (continued)

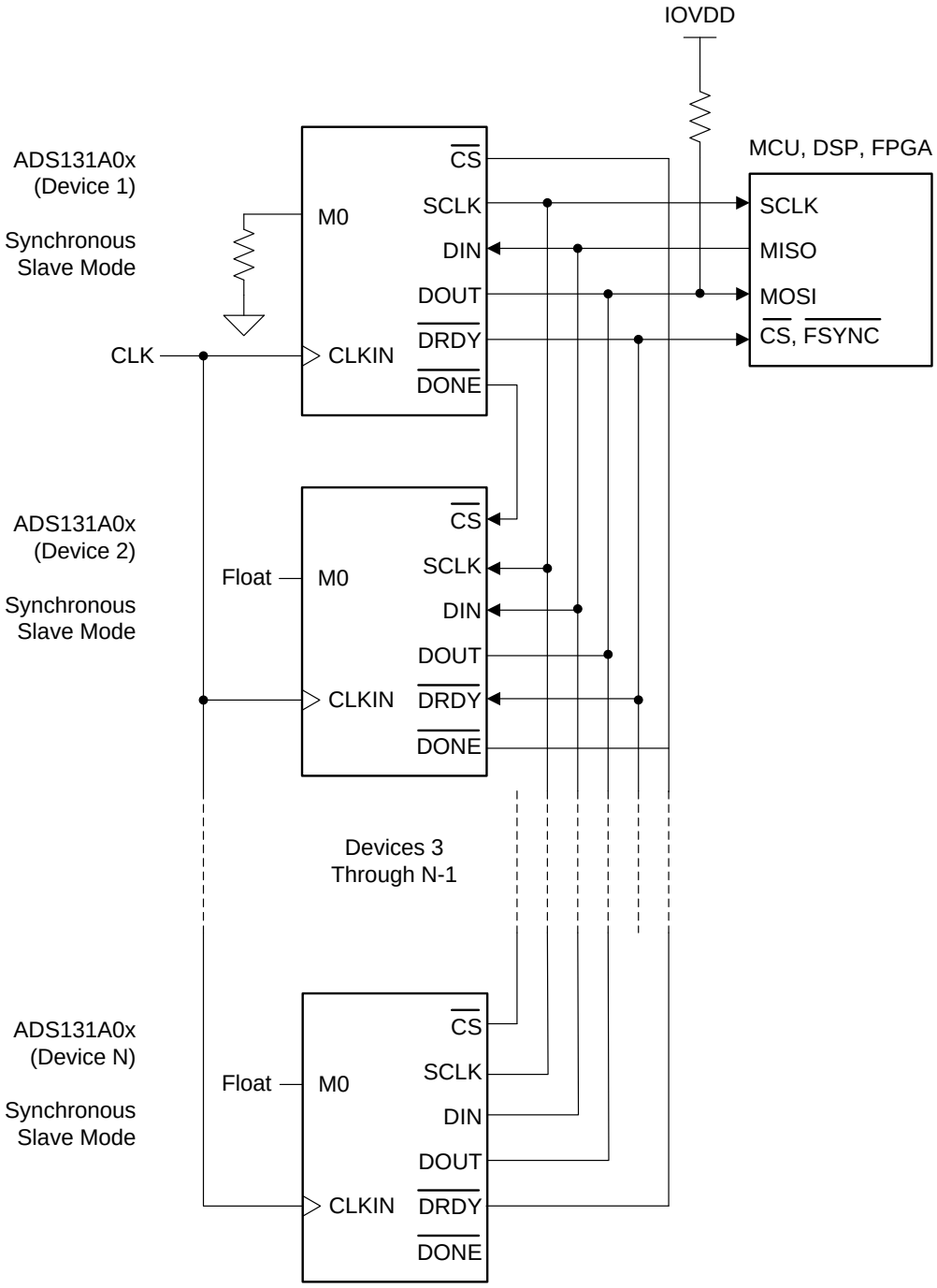
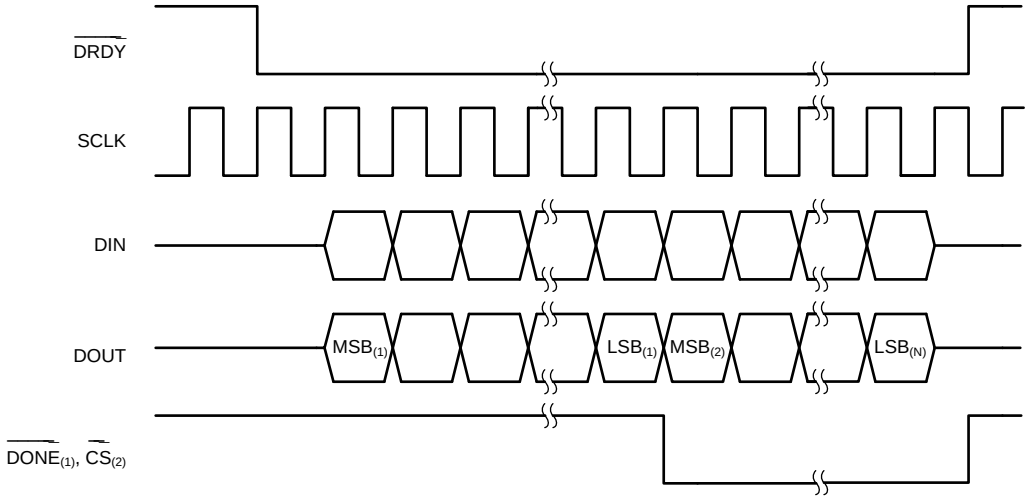


Figure 99. Multiple Device Configuration Using Synchronous Master Mode

Application Information (continued)



NOTE: (1) denotes device 1, (2) denotes device 2, and (N) denotes device N.

Figure 100. Multiple Device Configuration Timing Diagram When Using Synchronous Master Mode

The $\overline{\text{DONE}}$ pin of each device connects to the $\overline{\text{CS}}$ pin of the subsequent device. In each case, after a device shifts out the contents of the shift register, the device deasserts $\overline{\text{DONE}}$, causing the subsequent device to be selected for communication. The DOUT of a device whose contents are already shifted out assumes a high-impedance state, allowing the DOUT pins of all devices to be tied together.

Note that the $\overline{\text{DONE}}$ pin of the last device is tied to the $\overline{\text{CS}}$ pin of the first device to allow for a second read back if a data integrity test failed.

To send commands to specific devices, send the respective command of the device when that device is selected for communication.

The $\overline{\text{DRDY}}$ output of the first device serves as an input to all other devices to synchronize conversions. The $\overline{\text{DRDY}}$ output also serves as the chip-select or frame sync for the host.

In this configuration, the serial clock is free-running with the same frequency as ICLK.

10.1.3.3 All Devices Configured in Synchronous Slave Mode

Figure 101 illustrates a multiple device configuration where all devices are configured in synchronous slave mode. Figure 102 illustrates an example interface timing diagram for this configuration. Note that if the modulator clock is derived from the serial clock by configuring bits 2-0 in the CLK2 register, then SCLK must be free-running.

Application Information (continued)

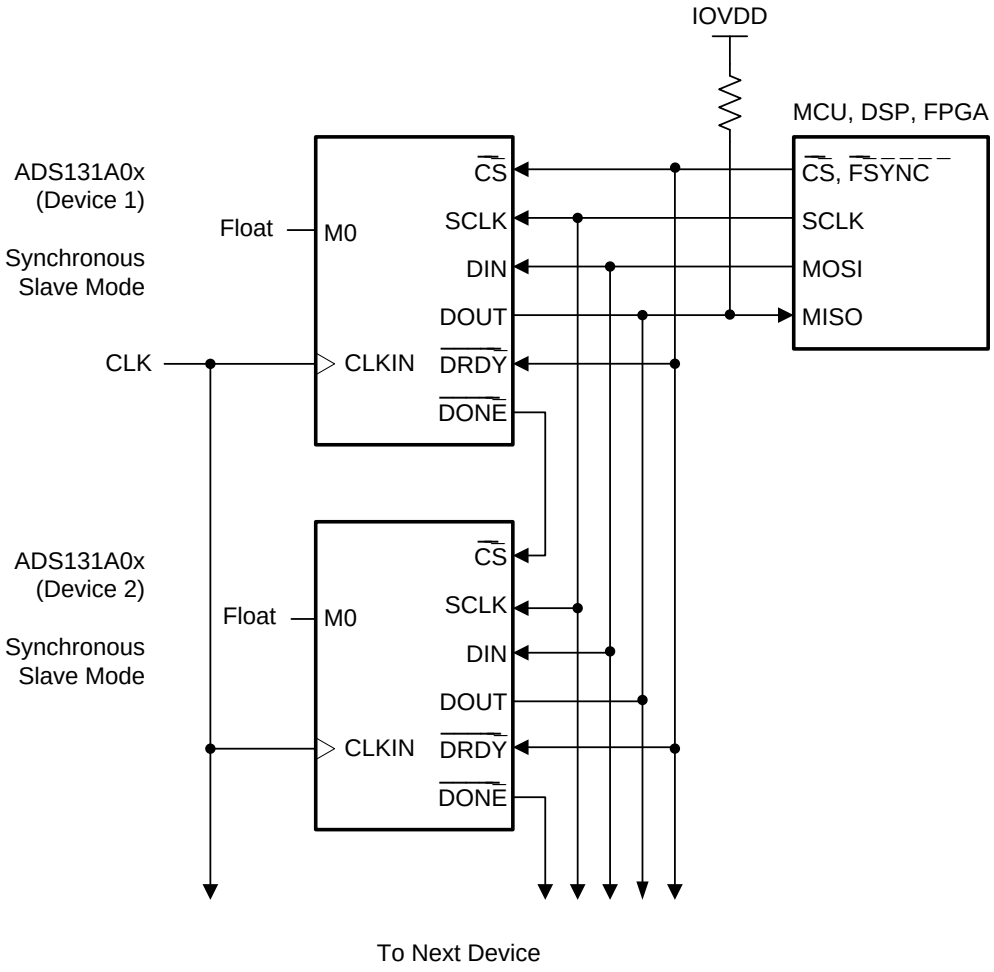
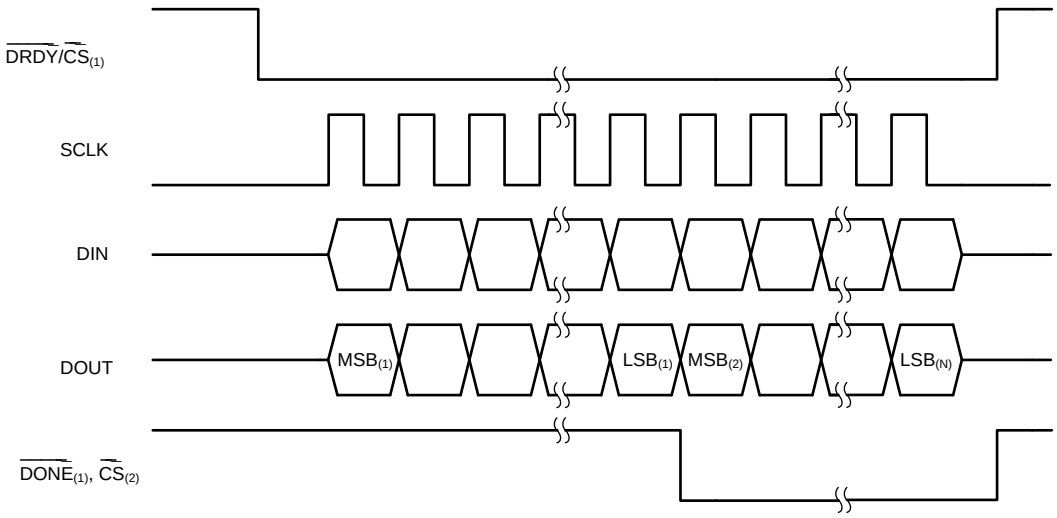


Figure 101. Multiple Device Configuration using Synchronous Slave Mode



NOTE: (1) denotes device 1, (2) denotes device 2, and (N) denotes device N.

Figure 102. Multiple Device Configuration Timing Diagram When Using Synchronous Slave Mode

Application Information (continued)

The $\overline{\text{DONE}}$ pin of each device connects to the $\overline{\text{CS}}$ pin of the subsequent device. In each case, after a device shifts out the contents of the output shift register, the device deasserts $\overline{\text{DONE}}$, causing the subsequent device to be selected for communication. The DOUT of a device whose contents are already shifted out assumes a high-impedance state, allowing the DOUT pins of all devices to be tied together.

To send commands to specific devices, send the respective command of the device when that device is selected for communication.

In this configuration, conversions must be synchronized by the master. This synchronization is accomplished by tying the chip-select or frame sync output of the host to the $\overline{\text{DRDY}}$ input of each device.

Figure 101 illustrates an external clock at the CLKIN pin, but a free-running SCLK can also be used as the conversion clock in this mode. Note that if the modulator clock is derived from the serial clock by configuring bits 2-0 in the CLK2 register, SCLK must be free-running.

10.2 Typical Application

Figure 103 shows an ADS131A0x device used as part of a power-metering application. The ADS131A0x device is ideal because this device allows for simultaneous sampling of voltage and current. The upper channel is used to measure voltage, accomplished by stepping down the line voltage with a voltage divider. The lower channel measures current directly from the line by measuring voltage across the burden resistors R_4.

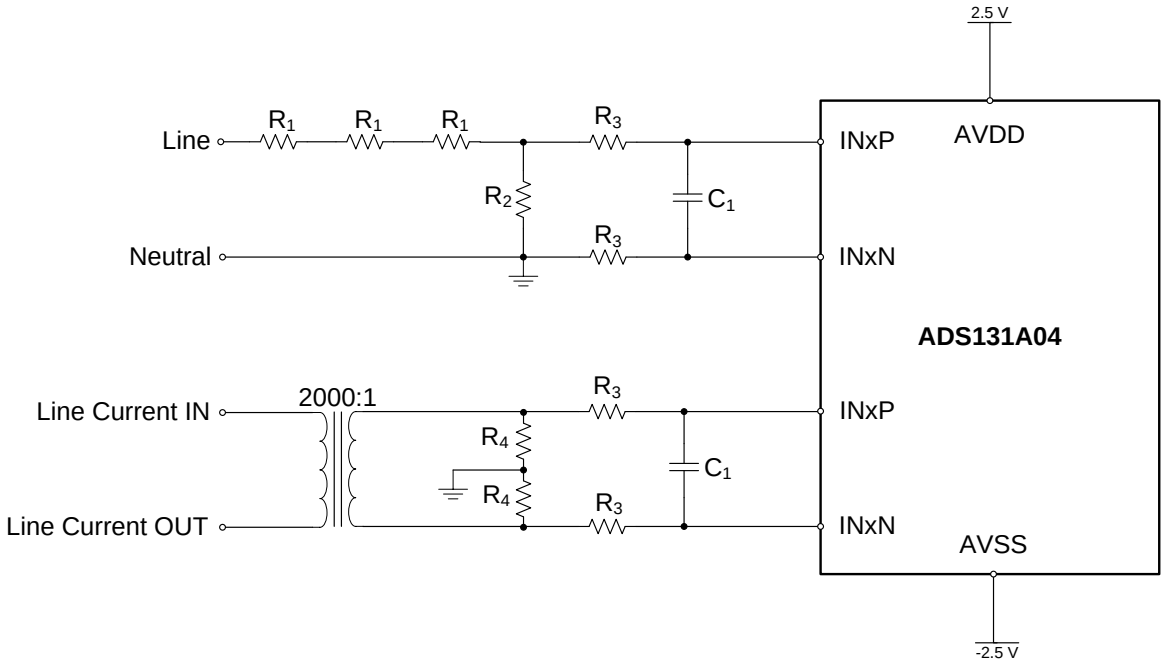


Figure 103. Typical Power Metering Connections

10.2.1 Design Requirements

Table 36. Power Metering Design Requirements

DESIGN PARAMETER	VALUE
Voltage input	230 V_{RMS} at 50 Hz
Current input range	0.05 A_{RMS} to 100 A_{RMS}
Active power measurement error	< 0.2%

10.2.2 Detailed Design Procedure

In this configuration, line voltage is measured as a single-ended input. The 230-V_{RMS} signal must be stepped down such that the signal peaks fall within the measurement range of the ADS131A04 when using the internal 2.442-V reference. A voltage divider using the series combination of multiple R_1 resistors and the R_2 resistor steps the input to within an acceptable range. Using multiple R_1 resistors along with proper spacing disperses energy among several components and provides a line of defense against short-circuits caused when one resistor fails. The output of this voltage divider can be calculated using Equation 9:

$$V_{IN} = V_{LINE}\left(\frac{R_2}{3 \times R_1 + R_2}\right) \tag{9}$$

If R_1 and R_2 are chosen as 330 kΩ and 3.9 kΩ, respectively, the voltage at the input of the ADS131A0x is 0.9025 V_{RMS}, corresponding to a 1.276 V_{peak} that is within the measurement range of the ADC.

Line current is measured by stepping the input current down through a current transformer (CT) then shunting the current on the secondary side through burden resistors. Then, the voltage is measured across the resistors and current is back calculated in the processor. The voltage across the burden resistors R_4 is measured differentially by grounding the node between the two resistors. Equation 10 relates the voltage at the input to the ADS131A0x to the line current.

$$V_{IN} = \left(\frac{2 \times I_{LINE} \times R_4}{N}\right) \tag{10}$$

If a CT with a 2000:1 turns ratio is used and R_4 is chosen to be 8.2 Ω, then 100 A_{RMS} of line current corresponds to 0.82 V_{RMS} (1.16 V_{peak}) at the input to the ADS131A0x. The design minimum line current of 50 mA_{RMS} corresponds to 0.41 mV_{RMS} (0.58 mV_{peak}).

The combination of R_3 and C_1 on each line serves as an antialiasing filter. Having C_1 populated differentially between the inputs helps improve common-mode rejection because the tolerance of the capacitor is shared between the inputs. The half-power frequency of this filter can be calculated according to Equation 11:

$$f_{-3dB} = \left(\frac{1}{4 \times \pi \times R_3 \times C_1}\right) \tag{11}$$

A filter with R_3 populated as 100 Ω and C1 as 2.7 nF gives a cutoff frequency of approximately 295 kHz. This filter provides nearly 17 dB of attenuation at the modulator frequency when the ADS131A04 modulator frequency is set to 2.048 MHz. R_3 must be kept relatively low because large series resistance degrades THD.

To get an accurate picture of instantaneous power, the phase delay of the current transformer must be taken into account. Many kinds of digital filters can be implemented in the application processor to delay the current measurement to better align with the input voltage.

10.2.3 Application Curve

Figure 104 shows the active power measurement accuracy for the ADS131A0x across varying currents. Data was taken for a 0.5 lead, 0.5 lag, and unity power factors. For this test, the external 16.384-MHz crystal frequency was divided to give a modulator frequency of 2.048 MHz. Finally, an OSR of 256 was chosen to give the ADS131A04 an output data rate of 8 kSPS.

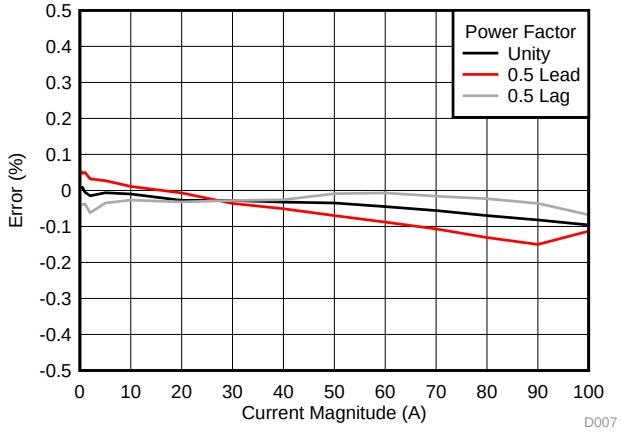


Figure 104. Active Power Measurement Error

10.3 Do's and Don'ts

- Do partition the analog, digital, and power-supply circuitry into separate sections on the printed circuit board (PCB).
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified voltage range under all input conditions.
- Do tie unused analog input pins to GND.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout (LDO) regulator to reduce ripple voltage generated by switch-mode power supplies. This reduction is especially true for AVDD where the supply noise can affect performance.
- Do keep the input series resistance low to maximize THD performance.
- Do not cross analog and digital signals.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 3.6 V under any conditions, including during power-up and power-down when the negative charge pump is enabled.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 6 V under any conditions, including during power-up and power-down when the negative charge pump is disabled.
- Do not allow the digital supply voltage to exceed 3.9 V under any conditions, including during power-up and power-down.

Figure 105 and Figure 106 illustrate correct and incorrect ADC circuit connections.

Do's and Don'ts (continued)

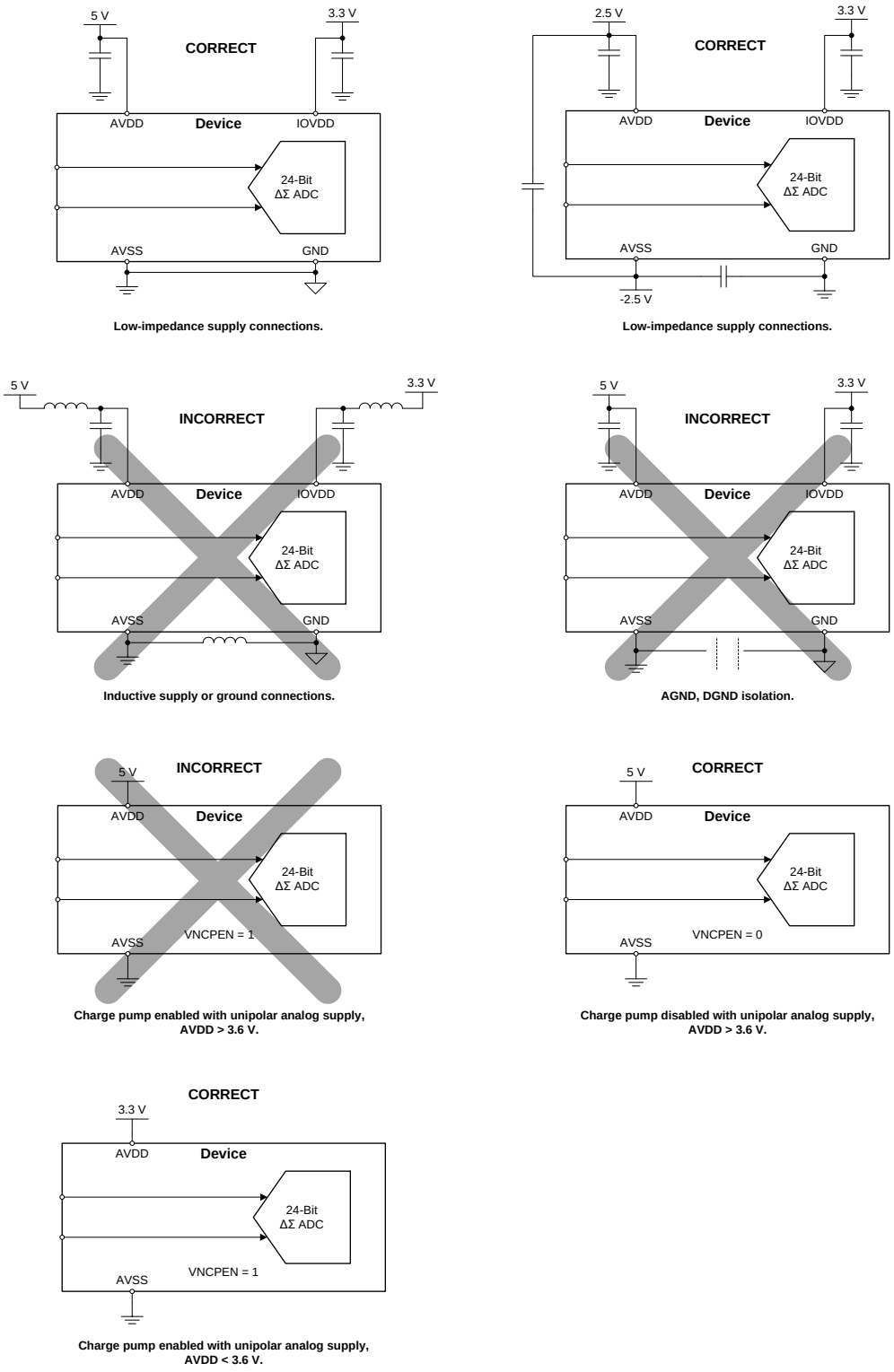


Figure 105. Correct and Incorrect Circuit Connections

Do's and Don'ts (continued)

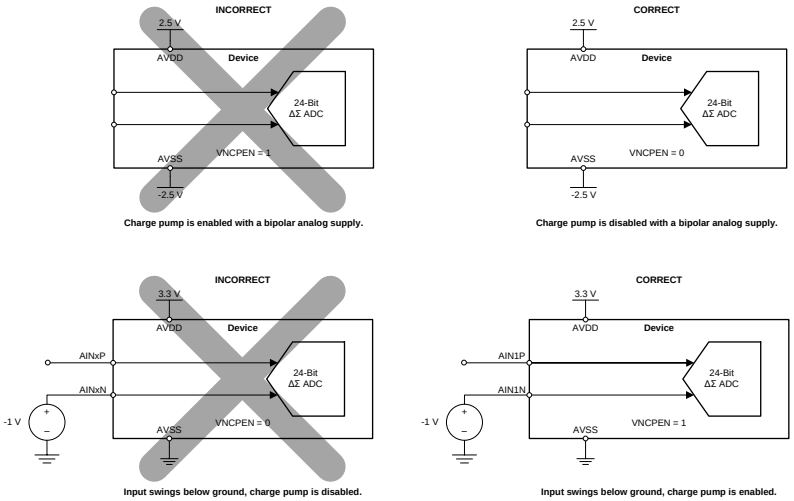


Figure 106. Correct and Incorrect Circuit Connections, Continued

10.4 Initialization Set Up

Figure 107 illustrates a general procedure to configure the ADS131A0x to collect data.

Initialization Set Up (continued)

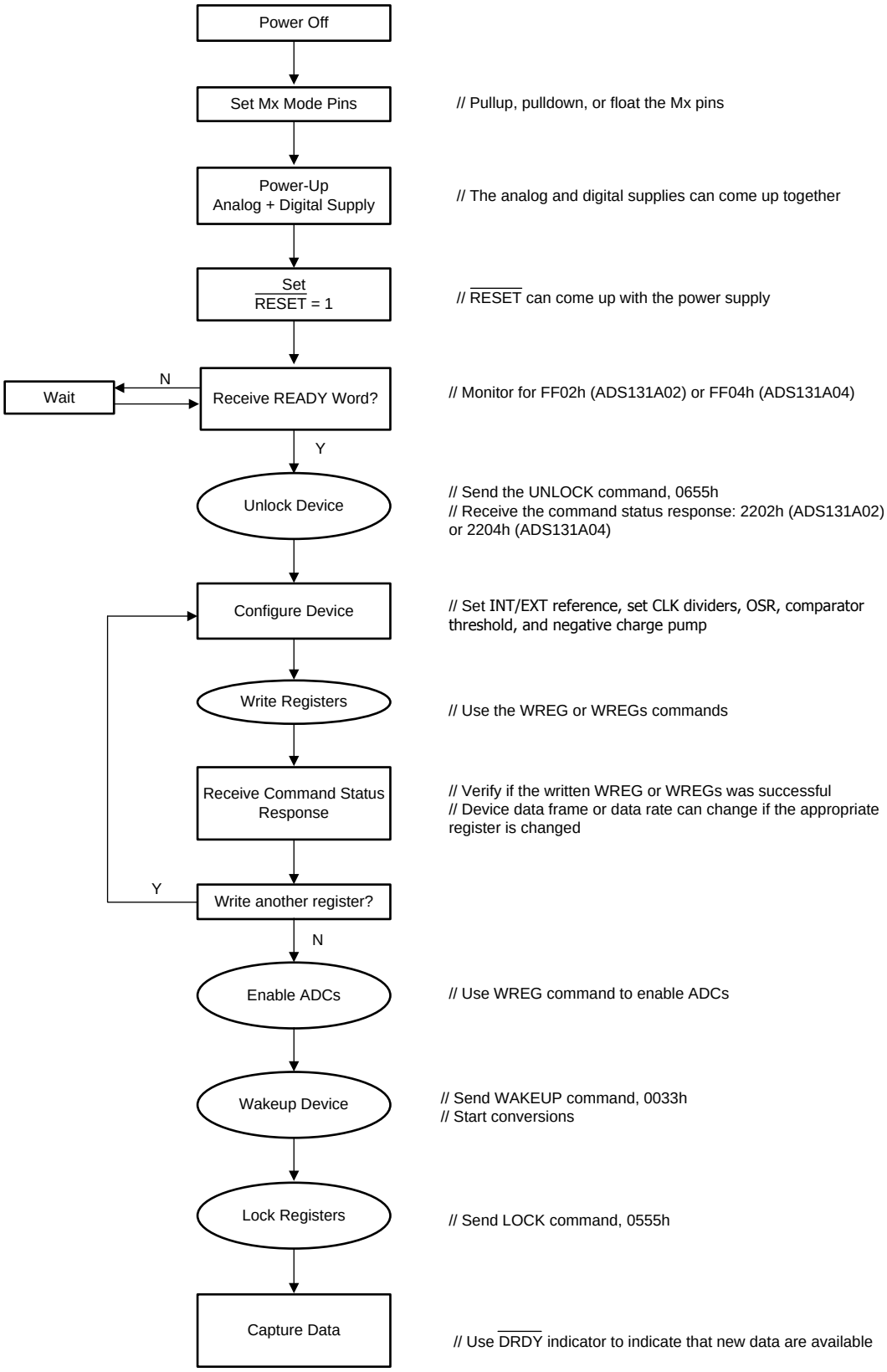


Figure 107. ADS131A0x Configuration Sequence

11 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (IOVDD, GND). The analog power supply can be bipolar (for example, V_{AVDD} = 2.5 V, V_{AVSS} = –2.5 V), unipolar (for example, V_{AVDD} = 5 V, V_{AVSS} = 0 V), or unipolar using the negative charge pump (for example, V_{AVDD} = 3.3 V, V_{AVSS} = V_{VNCP}), and is independent of the digital power supply. The digital supply range sets the digital I/O levels.

11.1 Negative Charge Pump

An optional negative charge pump is available to power V_{AVSS} with an operating voltage of –1.95 V. Enabling the negative charge pump allows for input signals below analog ground when using a unipolar analog supply (for example, V_{AVDD} = 3.3 V, V_{AVSS} = 0 V). The VNCPEN bit in the A_SYS_CFG register must be set high by the user to enable the negative charge pump. The VNCP pin outputs the nominal –1.95-V negative charge pump output and requires a capacitor to GND in the range of 220 pF to 470 pF. The charge pump operates at a switching frequency of $2f_{MOD}$. The minimum ADC absolute input voltage range is –1.5 V with the negative charge pump enabled. The maximum analog supply limit (AVDD – AVSS) is restricted to 3.6 V maximum. Exceeding this limit can lead to permanent damage of the device.

The negative charge pump is internally activated when the VNCPEN bit is set to 1 and the device is in wake-up mode with all ADC channels enabled (ADC_ENA = 0Fh).

Connect VNCP directly to AVSS when not using the negative charge pump.

11.2 CAP Pin

The ADS131A0x core digital voltage operates from 1.8 V, created from an internal LDO from IOVDD. The CAP pin outputs the LDO voltage created from the IOVDD supply and requires an external bypass capacitor. When operating from V_{IOVDD} > 2 V, place a 1-µF capacitor on the CAP pin to GND. If V_{IOVDD} ≤ 2 V, tie the CAP pin directly to the IOVDD pin and decouple both pins using a 1-µF capacitor to GND.

11.3 Power-Supply Sequencing

The power supplies can be sequenced in any order but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage limits. Wait approximately 50 µs after all power supplies are stabilized before communicating with the device to allow the power-up reset process to complete.

11.4 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply), and IOVDD must be decoupled with at least a 1-µF capacitor, as shown in Figure 108, Figure 109, and Figure 110. A 270-nF capacitor is required on the VNCP pin when using the negative charge pump. Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. The analog and digital ground are recommended to be connected together as close to the device as possible.

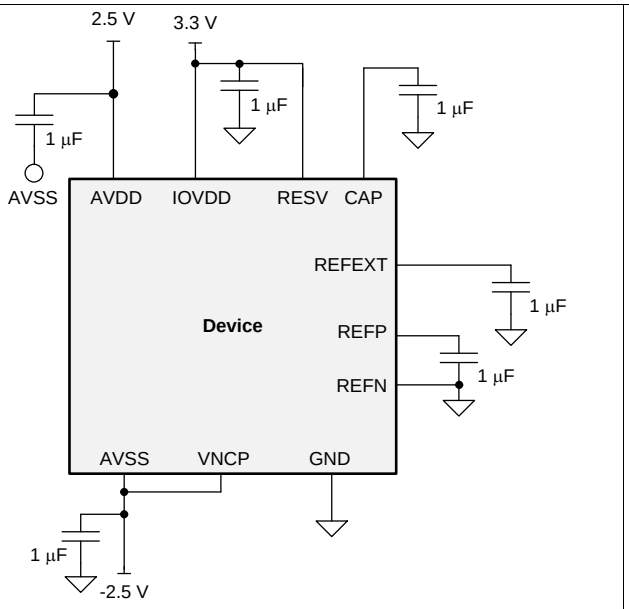


Figure 108. Bipolar Analog Power Supply

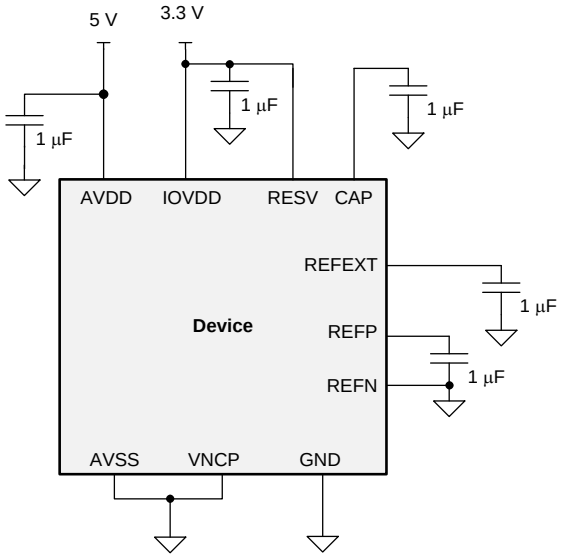


Figure 109. Unipolar Analog Power Supply

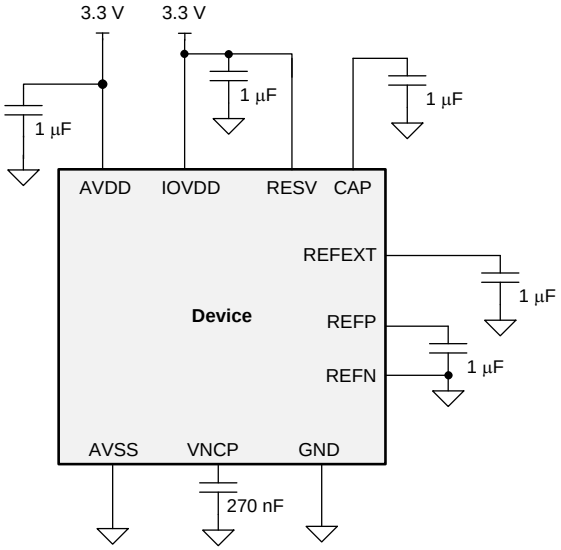


Figure 110. Unipolar Analog Power Supply with Negative Charge Pump Enabled

12 Layout

12.1 Layout Guidelines

Use a low-impedance connection for ground so that return currents flow undisturbed back to the respective sources. For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. Keep connections to the ground plane as short and direct as possible. When using vias to connect to the ground layer, use multiple vias in parallel to reduce impedance to ground. Figure 111 shows the proper component placement for the system.

A mixed-signal layout sometimes incorporates separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital, and power-supply components are properly placed. Proper placement of components partitions the analog, digital, and power-supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. If ground plane separation is necessary, then make the connection at the ADC. Connecting individual ground planes at multiple locations creates ground loops, and is not recommended. A single ground plane for the analog and digital grounds avoids ground loops.

Bypass the supply pins with a low-ESR ceramic capacitor. The placement of the bypass capacitors must be as close as possible to the supply pins using short, direct traces. For optimum performance, the ground-side connections of the bypass capacitors must also be made with low-impedance connections. The supply current flows through the bypass capacitor pin first and then to the supply pin to make the bypassing most effective (also known as a Kelvin connection). If multiple ADCs are on the same PCB, use wide power-supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs.

If external filtering is used for the analog inputs, use C0G-type ceramic capacitors when possible. C0G capacitors have stable properties and low-noise characteristics. Ideally, route differential signals as pairs to minimize the loop area between the traces. Route digital circuit traces (such as clock signals) away from all analog pins. Note that the internal reference output return shares the same pin as the AVSS power supply. To minimize coupling between the power-supply trace and reference return trace, route the two traces separately; ideally, as a star connection at the AVSS pin.

Treat the AVSS pin as a sensitive analog signal and connect directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS131A0x if shielding is not implemented. Keep digital signals as far as possible from the analog input signals on the PCB.

The SCLK input of the serial interface must be free from noise and glitches when this device is configured in a slave mode. This configuration is especially true when SCLK is used as the master clock for this device. Even with relatively slow SCLK frequencies, short digital signal rise and fall times can cause excessive ringing and noise. For best performance, keep the digital signal traces short, using termination resistors as needed, and make sure all digital signals are routed directly above the ground plane with minimal use of vias.

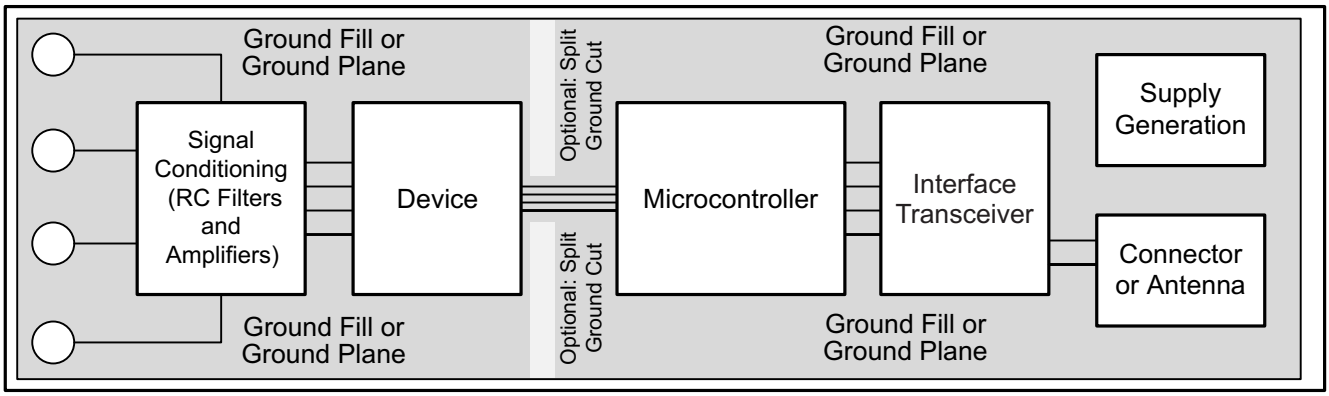


Figure 111. System Component Placement

12.2 Layout Example

Figure 112 is an example layout of the ADS131A0x requiring a minimum of three PCB layers. This example shows the device supplied with a bipolar supply, though the layout can be replicated for a unipolar case. In general, analog signals and planes are partitioned to the left and digital signals and planes to the right.

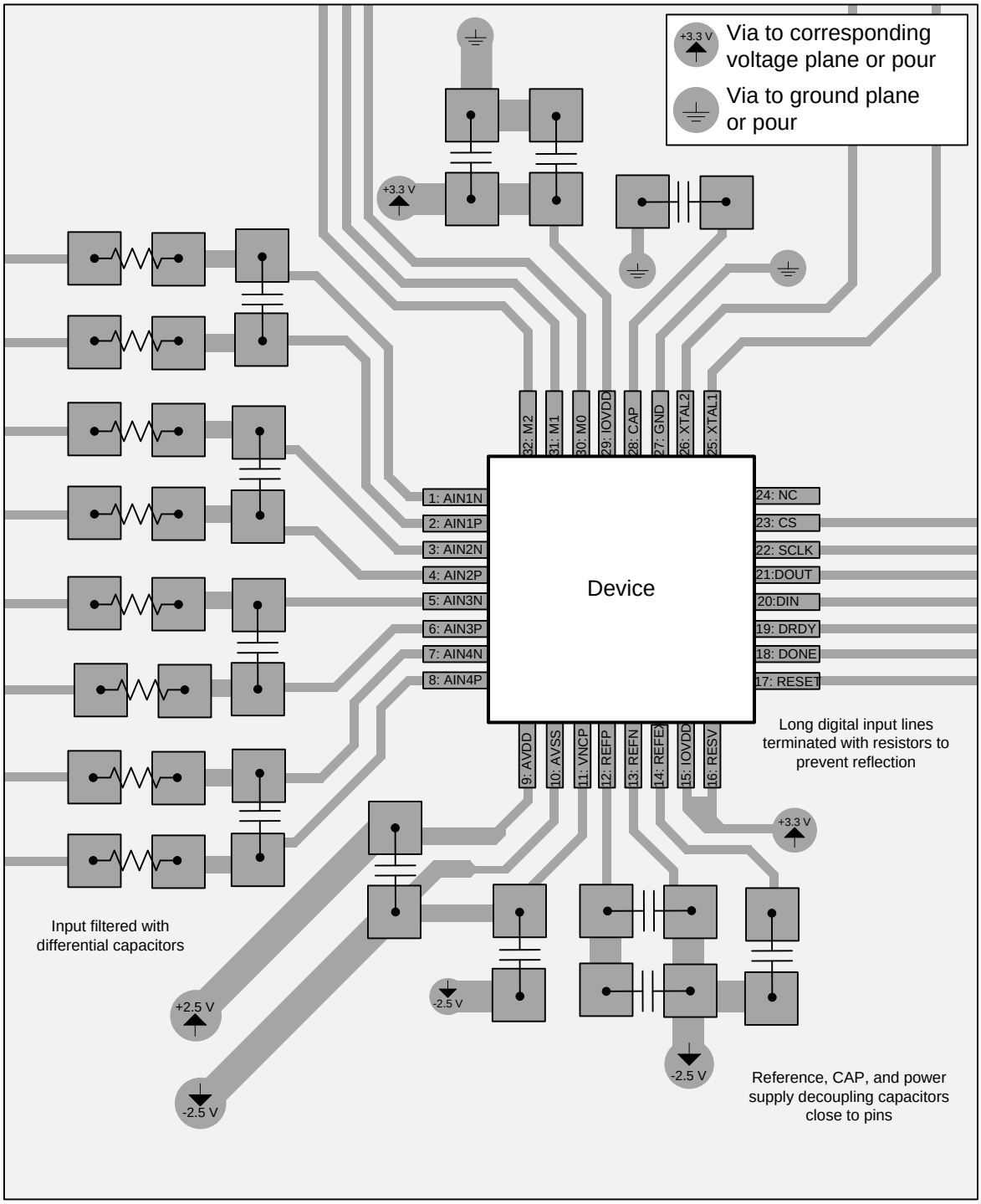


Figure 112. ADS131A0x Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

REF5025, REF5040 Data Sheet, SBOS410

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 37. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS131A02	Click here	Click here	Click here	Click here	Click here
ADS131A04	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
Multiple SPI is a trademark of Motorola Mobility LLC.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS131A04IPBS	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	131A04	Samples
ADS131A04IPBSR	ACTIVE	TQFP	PBS	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	131A04	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

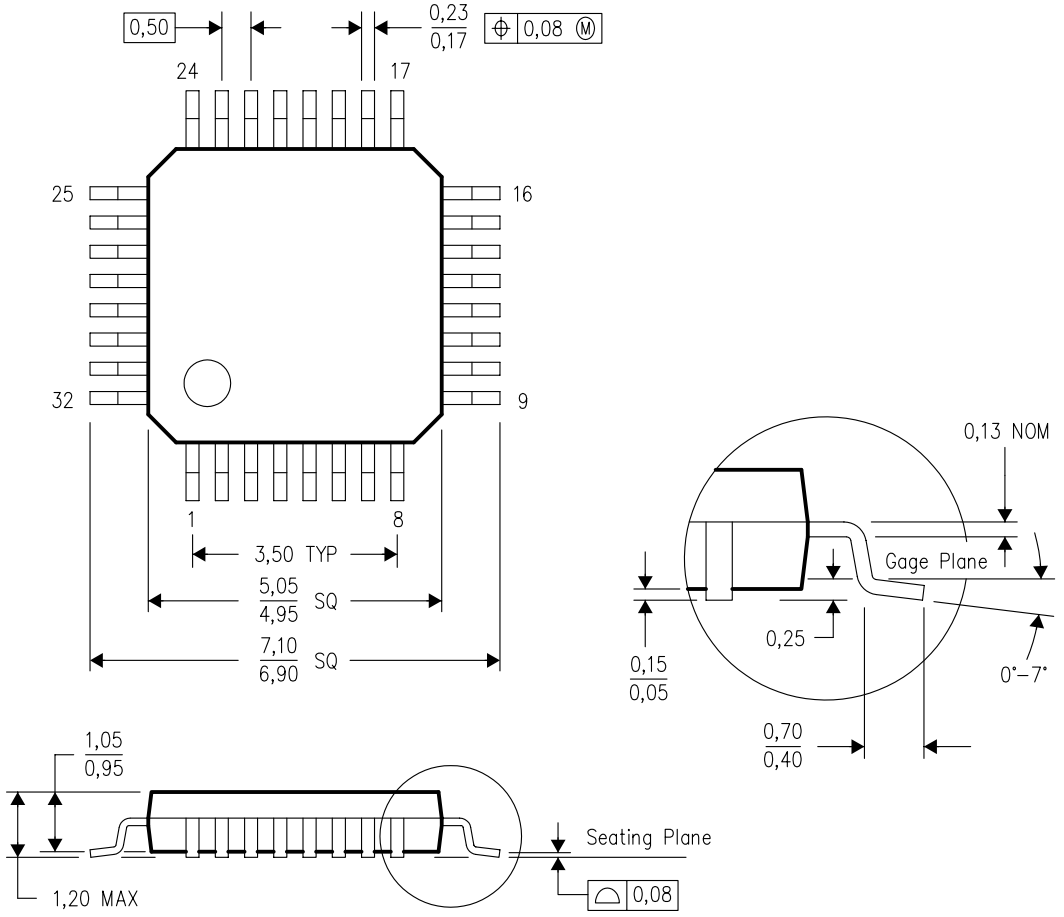
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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