AT40KEL-DK Design Kit

User Guide

Section 7

Section 8

Section 1
Introduction

1.1 Features

- Prototyping for Atmel AT40KEL [(1)] Series of SRAM-based FPGA Devices
- Up and Running with Power Supply, Reset, Clock Source and Configuration Memory
- Modular Docking Platform for ATDH40D160 and ATDHD256 FPGA Daughterboards
- Designed to Work with Atmel Integrated Design System (IDS) Software
- Downloading for AT17LV010 Devices Direct from PC Parallel Port
- Supports ISP (In-System Programming) for Atmel AT17LV010 Series Configuration EEPROMs

1.2 Kit Contents

- Prototyping Motherboard (ATDH40M) with AT17LV010 Configuration EEPROM
- Daughterboard for MQFPF160 (ATDH40D160) or MQFPF256 (ATDH40D256) with associated AT40KEL040 Engineering Sample
- Standard Parallel Cable with Male/Female DB25 Connectors
- ISP Download Cable (ATDH2225) for AT17LV010 Configuration EEPROM in Customer Final Application
- FPSLIC® System Designer CD-ROM (contains IDS software)
- AT40KEL040 CD-ROM with related documents, software patches, etc.

1.3 Description

The Atmel AT40KEL-DK design kit allows designers to quickly evaluate and prototype their application using AT40KEL Rad Hard FPGA devices and AT17LV010 configuration EEPROM devices.

The ATDH40M board connects to any x86 PC via parallel port through a standard parallel cable to program the AT17LV010 configuration memory. The motherboard interfaces with daughterboards in order to program different package footprints.

The AT40KEL-DK Design Kit is delivered with a daugtherboard for 160-pin or for 256-pin MQFPF (Multi-layer Ceramic Quad Flat Pack with Flat Leads).

1.All features and characteristics described for AT40KEL040 in this document also apply to the AT40KFL040, unless specified otherwise.

The AT17LV010 configuration EEPROM can be programmed in customer's final application using the ATDH2225 ISP cable included in the kit.

1.4 Software Setup

On the Atmel FPSLIC® System Designer CD-ROM, users will find the IDS (Integrated Development System).

The IDS software allows for place and route, and for back-annotation. In case you are already licensed with the Mentor ModelSim HDL simulator (for either the logic synthesis from a VHDL model entry, or the direct gate level entry) and the LeonardoSpectrum (for final simulation), the tool encompasses the relevant libraries.

A specific software patch is available on AT40KEL CD-ROM to support AT40KEL040 devices in IDS.

1.5 Technical Support

North America Hot Line: radhard-fpga@atmel.com

Rest of the World Hot Line: radhard-fpga@nto.atmel.com

Section 2

Installing System Designer

2.1 System Requirements

For a single-user system, System Designer requires the following:

Hard Disk	350-Mbyte Minimum
Operating System	Windows 2000/XP
RAM	128-Mbyte
Peripherals	Parallel Interface Port
Network	Network Interface Card (needed for the software license)
Browser	Internet Explorer 5 or above
Privileges	Administrative Privileges

Before starting SystemDesigner installation, please make sure the network card on your PC is connected to an active network, since the power-save option for the network cards may cause the MAC address (which the software license HostID relies on) not to be visible after the network card was disconnected from the network.

2.2 System Designer Installation

1. Insert the supplied System Designer CD-ROM into the computer. If the CD does not automatically start, execute `SETUP.EXE` from the CD.
2. From the CD Browser, select *Install Products* and select *System Designer*, see Figure 2-1.

Figure 2-1. Install Products

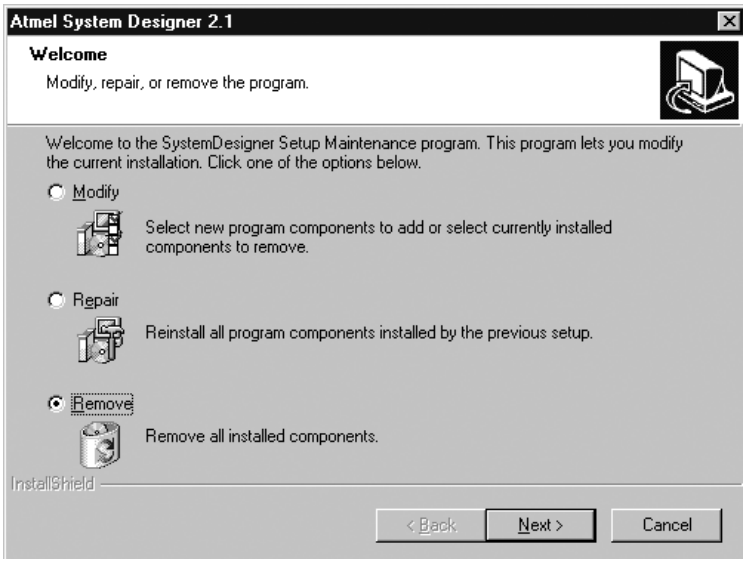
If you have a previous version of System Designer installed on your machine, the installation wizard will detect it, see Figure 2-2.

Figure 2-2. Detection of a Previous Version of System Designer

3. Press *Yes* to remove the previous version of System Designer and continue with the installation. *No* will cancel the installation.

   InstallShield® will guide you through the setup. The *Modify, repair or remove the program* dialog box appears, see Figure 2-3.

Figure 2-3. Modify, Repair or Remove the Program Dialog Box

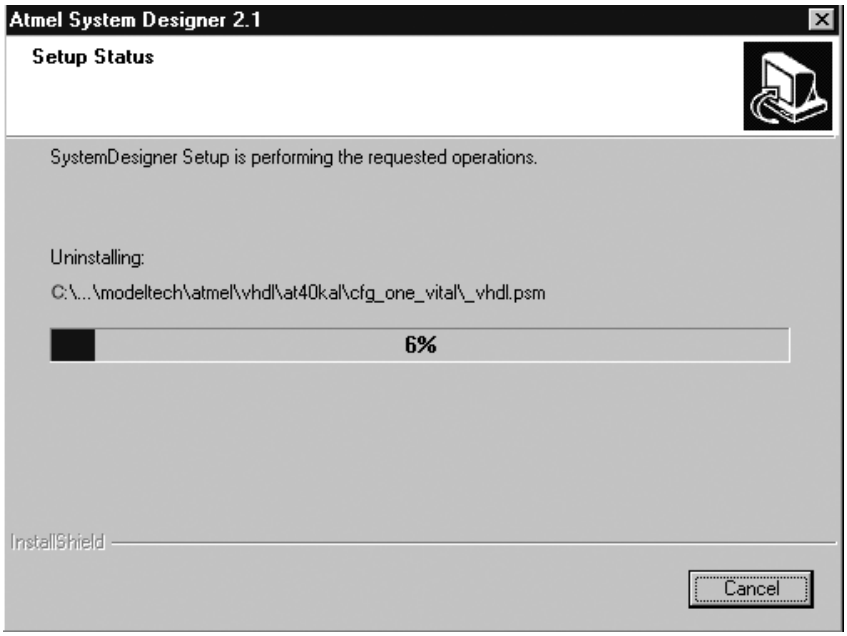


4. Select *Remove* and press *Next* >. The *Confirm File Deletion* dialog box appears, see Figure 2-4.

Figure 2-4. Confirm File Deletion Dialog Box

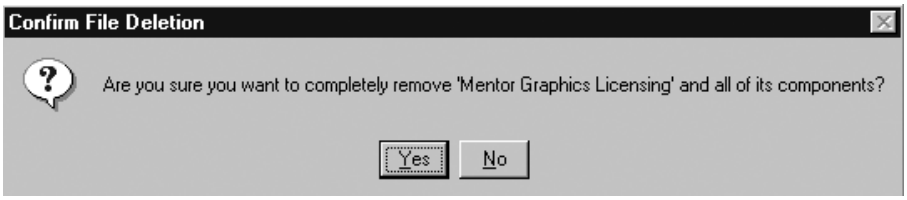
5. Press *OK*. The System Designer setup will remove the current version, see Figure 2-5.

Figure 2-5. Setup Status



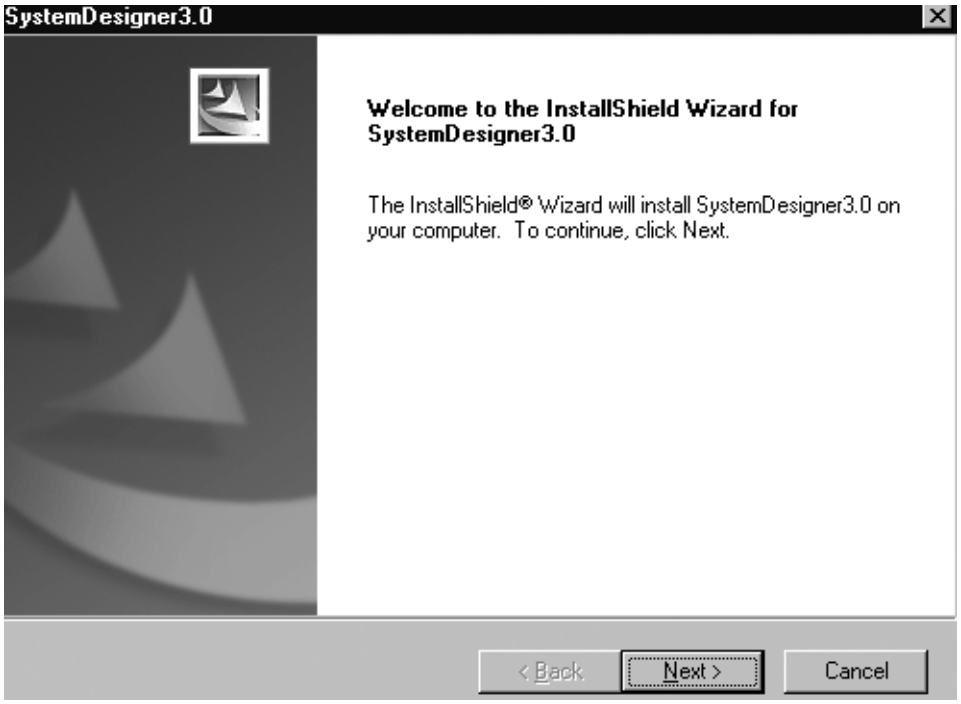
InstallShield will then remove Mentor Graphics Licensing. The *Confirm File Deletion* dialog box appears, see Figure 2-6.

Figure 2-6. Confirm File Deletion Dialog Box



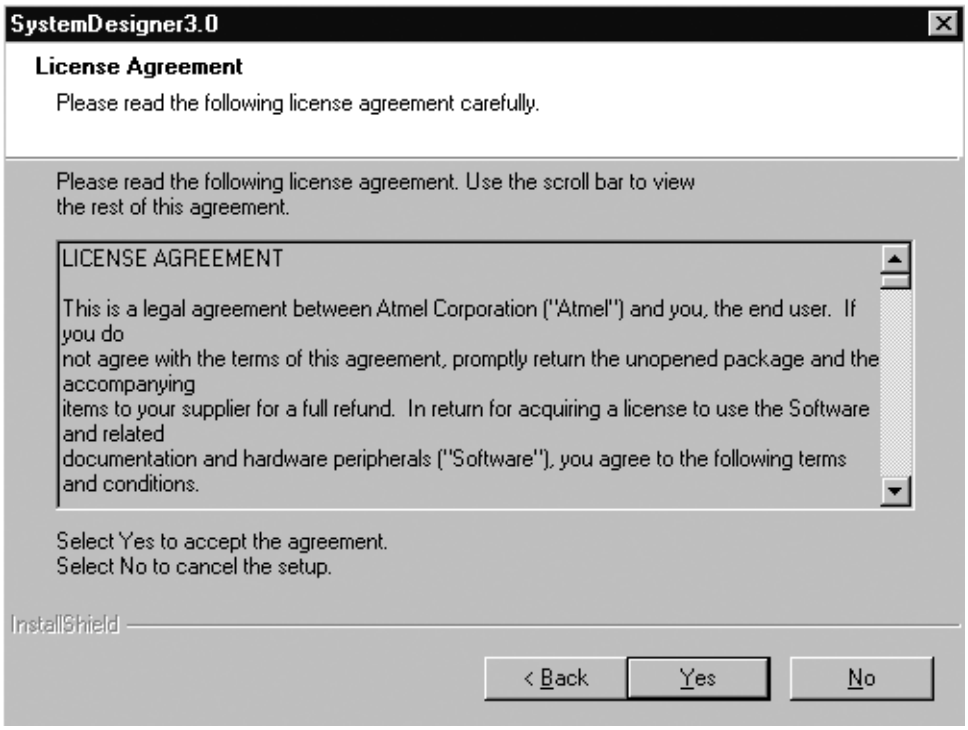
6. Press *Yes*. The System Designer 3.0 installation dialog box appears, see Figure 2-7.

Figure 2-7. .System Designer 3.0 Installation Dialog Box



7. Press *Next* >. The License Agreement dialog appears, see Figure 2-8.

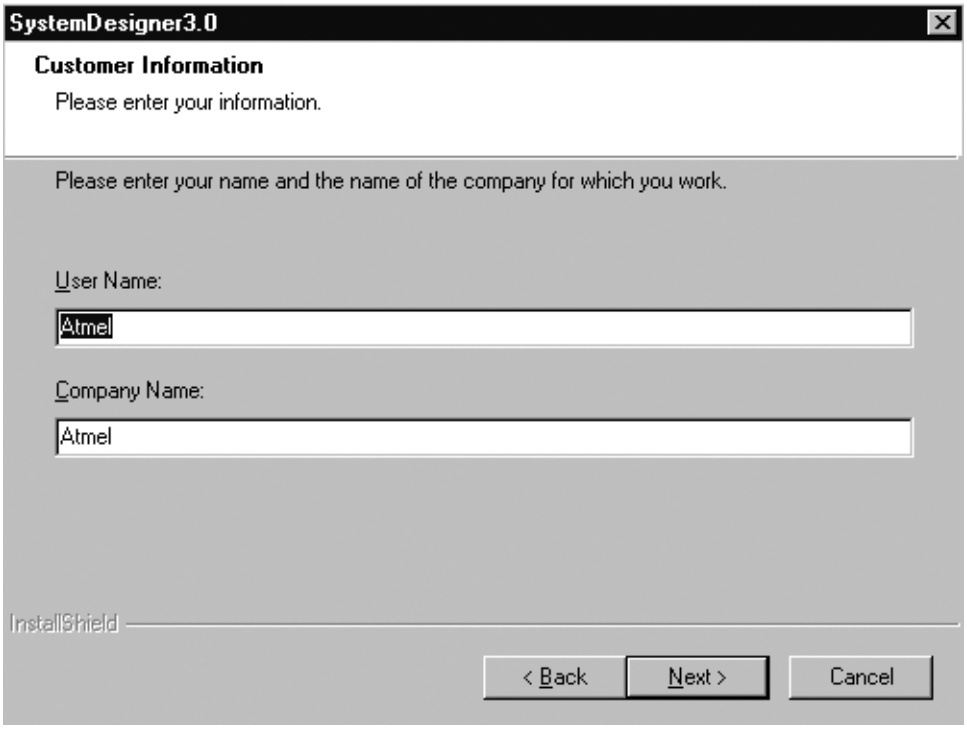
Figure 2-8. License Agreement Dialog



8. Read the License Agreement and press *Yes*. You must accept this agreement if you want to install System Designer. If you choose *No*, the setup will close.

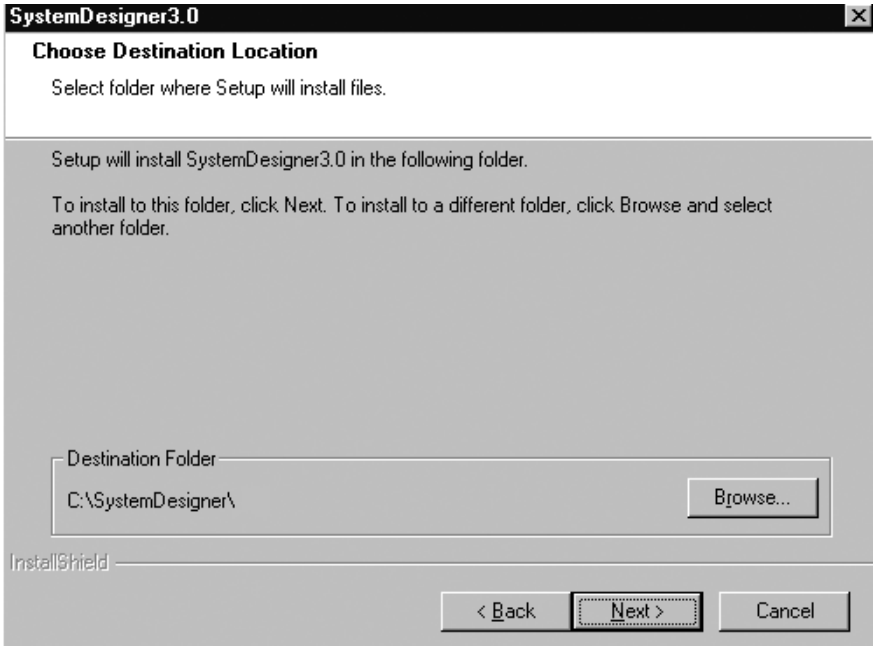
   The *Customer Information* dialog box appears, see Figure 2-9.

Figure 2-9. Customer Information Dialog Box



9. Enter the requested information and press *Next* >. The *Choose Destination Location* dialog box appears, see Figure 2-10.

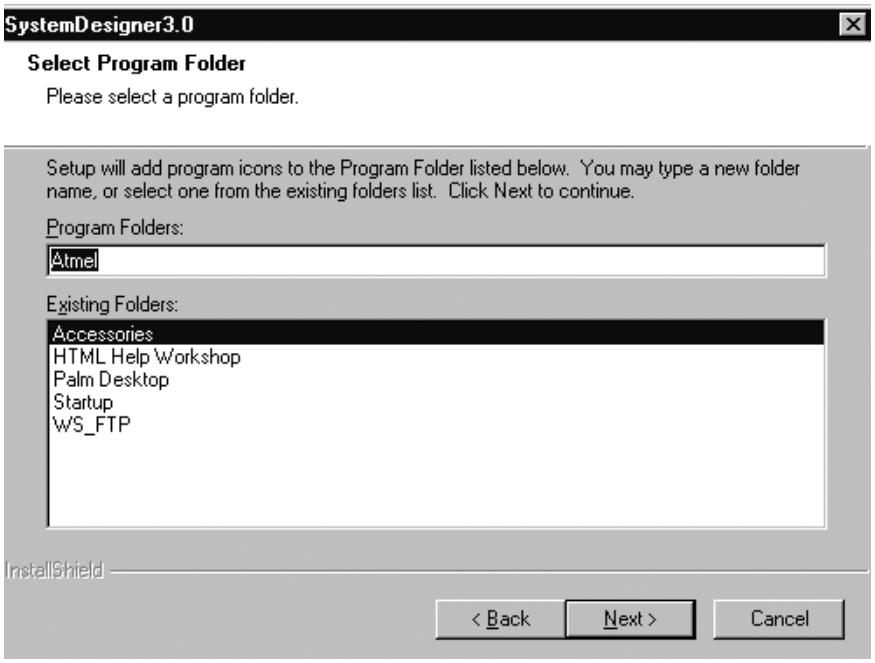
Figure 2-10. Choose Destination Location Dialog Box



System Designer's default installation path is `C:\SystemDesigner`. If you prefer to use another path, press the *Browse* button to navigate to the destination folder. Do not use spaces between words.

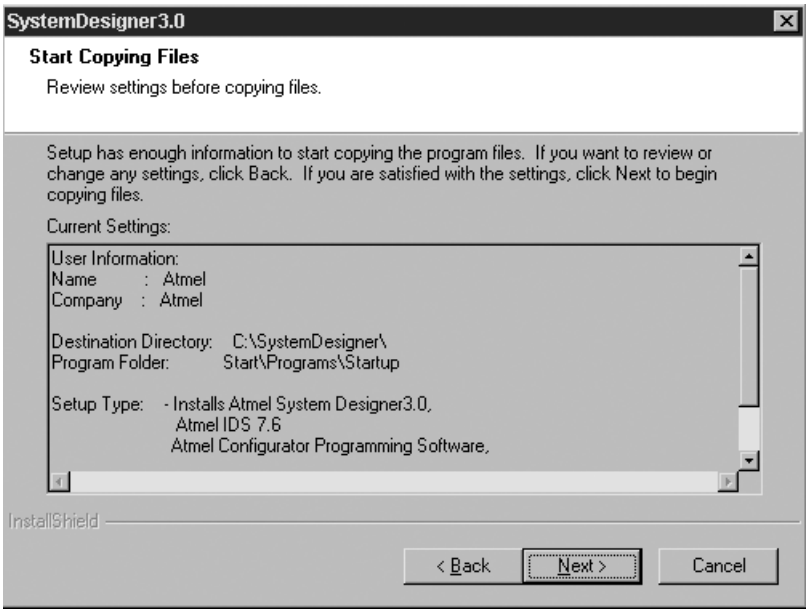
10. Press *Next* >. The *Select Program Folder* dialog box appears, see Figure 2-11.

Figure 2-11. Select Program Folder Dialog Box



11. Take the default and press *Next* >. The *Start Copying Files* dialog box appears, see Figure 2-12.

Figure 2-12. Start Copying Files Dialog Box

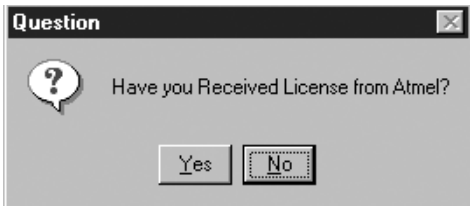


12. Review the current settings and press *Next* > to proceed with the installation.
13. The installation will require to restart your computer, see Figure 2-13. Press OK.

Figure 2-13. Restart Window

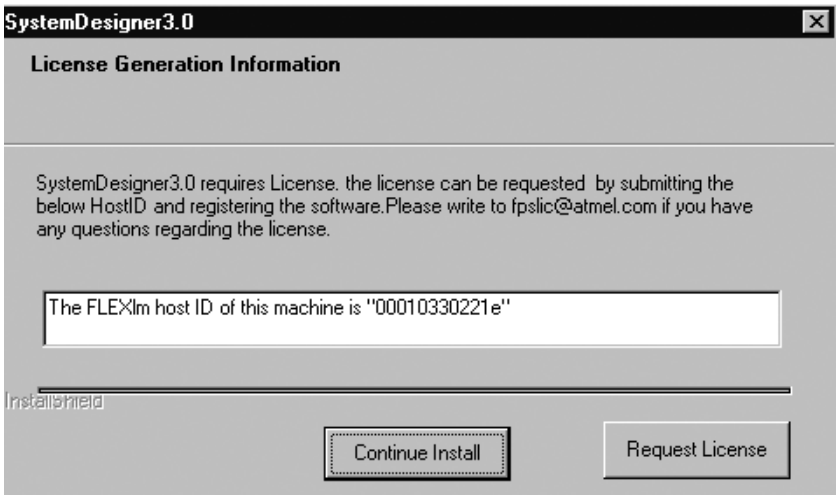
Once your computer has been restarted, a dialog box asking if you have received a license from Atmel appears, see Figure 2-14.

Figure 2-14. Information Dialog Box - Atmel's License



– Press *Yes* if you have received a license.
– Press *No* if you don't have one. A dialog box with your Host ID appears, see Figure 2-15.

Figure 2-15. License Generation Information

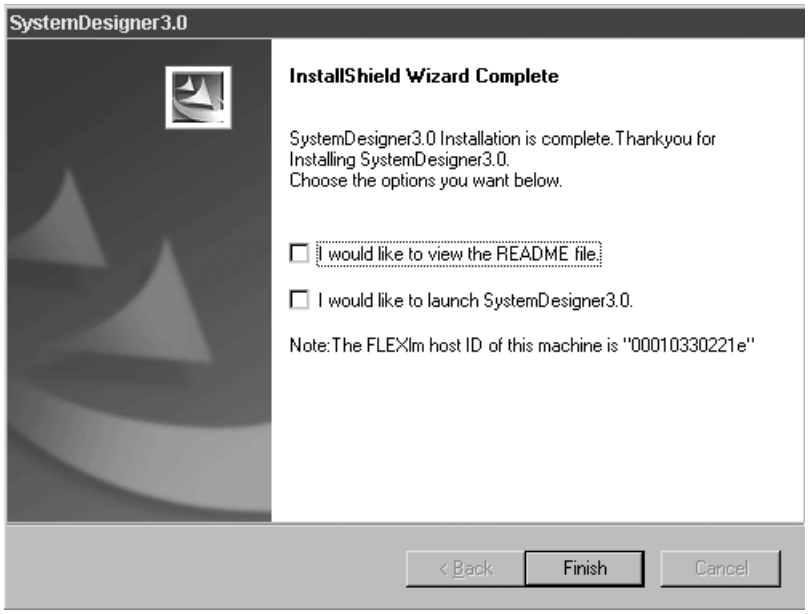


– To request a license, please contact your hotline (See “Technical Support” on page 2.) and give your FLEXlm HostID (please note “000000000000” and “ffffffffffff” are not valid HostIDs).

– Press *Continue Install*.

14. A dialog box asking you view the README file or to launch System Designer appears, see Figure 2-16.

Figure 2-16. InstallShield Wizard Complete Dialog



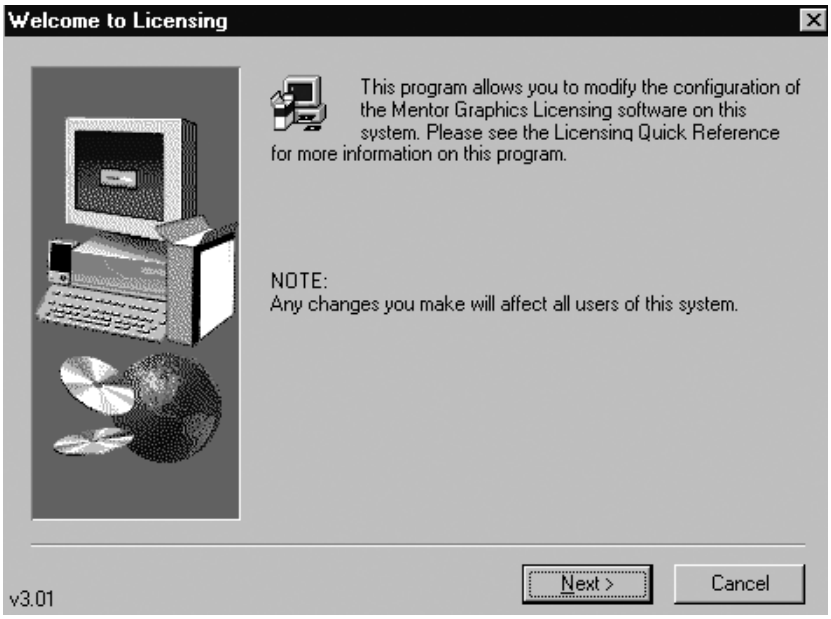
15. Select your option and press *Finish*.

2.3 Configuring the Product License

You must have a valid license in order to proceed.

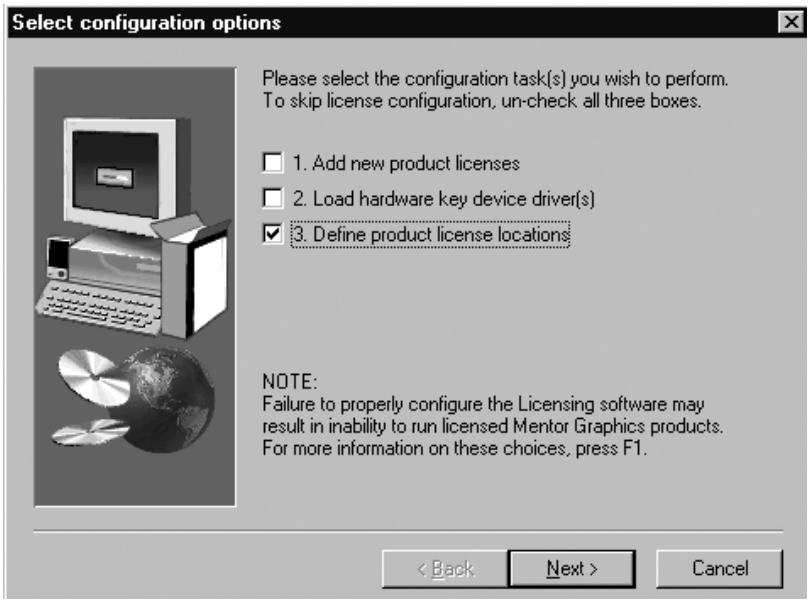
1. Save your license under `C:\SystemDesigner\fpslic.dat`.
2. Go to the *Start* menu and choose *Programs* > *Atmel* > *Mentor Graphics Licensing* > *Configure Licensing*. The *Welcome to Licensing* dialog box appears, see Figure 2-17.

Figure 2-17. Welcome to Licensing Dialog Box



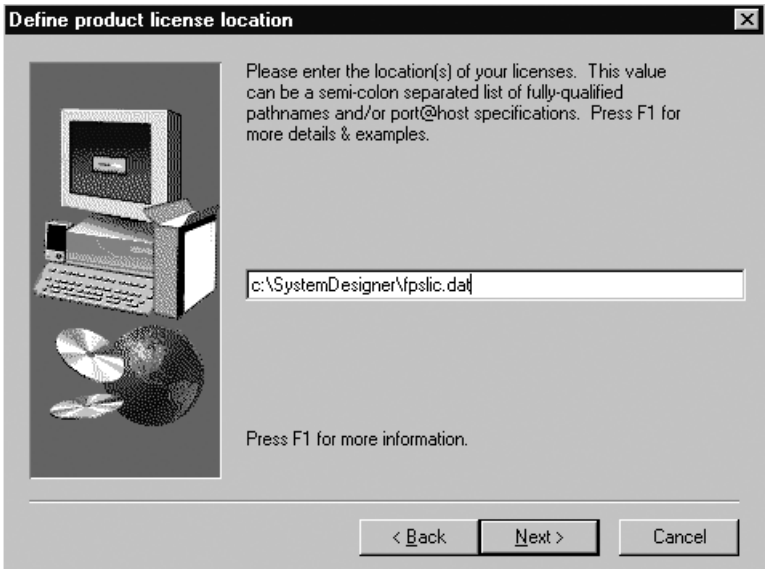
3. Press *Next* >. The *Select Configuration Options* dialog appears, see Figure 2-18.

Figure 2-18. Select Configuration Options Dialog Box



4. Select *Define Product License Locations* and press *Next* >. The *Define Product License Locations* dialog box appears, see Figure 2-19.

Figure 2-19. Define Product License Location Dialog Box



5. Specify the path `C:\SystemDesigner\fpslic.dat`. Press *Next*. An *Information* dialog box appears, see Figure 2-20.

Figure 2-20. Information Dialog Box – License Setup Complete

6. The license setup is now complete, press *OK*.

2.4 License Troubleshooting

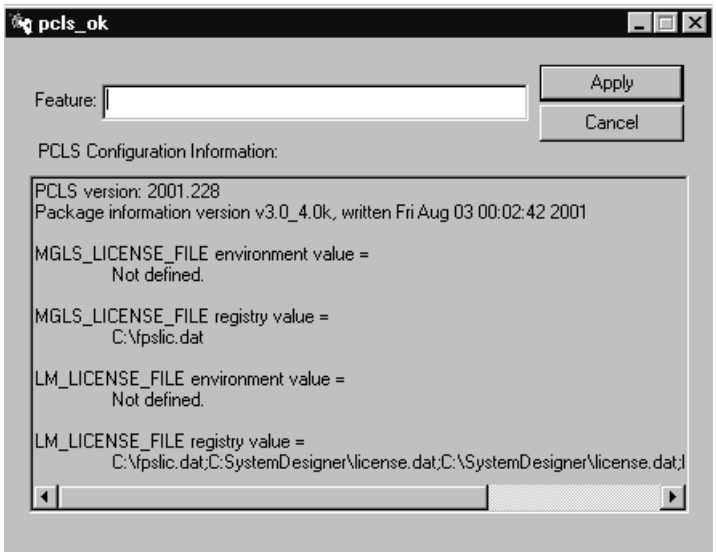
In order to check if all the licenses work, follow the procedure below:

1. Open your `fpslic.dat` file, the file should contain the 4 product names as shown below:

```
INCREMENT cveatmel1...
INCREMENT atmelmti...
INCREMENT leospecls1...
INCREMENT leospecls1atmel...
```

2. Go to the *Start* menu and choose *Programs* > *Atmel* > *Mentor Graphics Licensing* > *pcls_ok*. The *pcls_ok* dialog box appears, see Figure 2-21.

Figure 2-21. pcls_ok Dialog Box



3. Type the first *Feature* name (`cveatmel1`) and press *Apply*. If the license was installed successfully, the *PCLS_OK* dialog box appears, see Figure 2-22.

Figure 2-22. PCLS_OK Dialog Box

4. Repeat the same procedure with the rest of the products (`atmelmti, leospecls1,leospecls1atmel`).

If after checking all the licenses, you still have problems launching Leonardo, check for an expired FPSLIC license file that may be located in `c:\flexlm` directory. If found, remove the expired license and try launching Leonardo again.

If both ModelSim and Leonardo fail to launch, check if the host ID matches with your license file.

5. Go to the *Start* menu and choose *Programs* > *Atmel* > *Mentor Graphics Licensing* > *Lmtools*. The *Lmtools* window appears.
6. Click on *Hostid* and write down the number, see Figure 2-23.

Figure 2-23. Lmtools Window

7. Open the `fpslic.dat` file and compare the host ID. If it is the same host id, check one of the other options below. If it is different, See “Technical Support” on page 2.
8. Check for the expiration date on the license file.
9. Check if the path in your `autoexec.bat` file matches as shown below:

```
SET
PATH%PATH%;c:\SystemDesigner\bin;c:\SystemDesigner\Mentorgraphics\cve_home.i
xn\bin;c:\SystemDesigner\Mentorgraphics\cve_home.ixn\lib
SET ATMELDIR=c:\SystemDesigner\etc
SET FIGARO_HOME=c:\SystemDesigner
SET CVE_HOME=c:\SystemDesigner\MentorGraphics\CVE_HOME.IXN
SET MGLS_HOME=c:\SystemDesigner\MentorGraphics\CVE_HOME.IXN\MGLS
SET MGC_CVE_MAX_SHMEM_SIZE=3
SET PCLS_DIR=c:\Mentor~1\Licens~1
SET PATH=%PATH%;%PCLS_DIR%
```

Section 3

Updating Software For AT40KEL Support

3.1 Description

In order to have System Designer and associated tools integrate the latest features, Atmel releases updates on the web (http://www.atmel.com) on a regular basis. As of today, updating System Designer for AT40KEL support requires:

- Updating System Designer with the latest patch (`sysdesupdate.pat`)
- Updating Figaro IDS with an AT40KEL-specific patch (`figaro.im`)

These patch files can be found on the accompanying *AT40KEL040 Design Kit* CDROM in the "`Update`" directory.

3.2 System Designer Update

AT40KEL040 Design Kit CDROM contains System Designer 3.0 Patch Level 2 Update (3 MB, updated 04/21/04).

To apply the patch, follow these instructions:

- Launch System Designer
- In System Designer, select "Update via File" under the "Help" menu
- In the file browser dialog box, starting from the top-level of the CDROM, browse to the "`Update\System_Designer_3.0_Patch_Level_2`" directory and select the "`sysdesupdate.pat`" file: System Designer will then update itself from the file

A message will then be displayed asking for Figaro IDS update (patch 2b4). This operation can be safely ignored as Figaro IDS will be updated as described in the next section.

- Click "`OK`" to save the newly updated image file.

3.3 Figaro IDS Update

AT40KEL040 Design Kit CDROM contains Figaro IDS 7.6.7 Patch Level 3a2 Update (29.2 MB, updated 05/15/04).

To apply the patch, follow these instructions.

- Remove or rename file "`C:\SystemDesigner\bin\figaro.im`"
- In Windows Explorer, starting from the top-level of the CDROM, browse to the

"`Update\IDS_7.6.7_Patch_Level_3a2`" directory and copy the "`figaro.im`" file to the location of the removed/renamed file "`C:\SystemDesigner\bin`"

To check Figaro IDS has been properly updated:

- Launch Figaro IDS 7.6 from the start menu
- Select "`About Figaro...`" under the "`Help`" menu: a popup window will appear saying "`Atmel Figaro version ids7.6.7 (patch level 3a2 applied)`"

Section 4

Integrated Development System (IDS)

4.1 Features

- Support for Industry-standard PC and Workstation Tools
- Schematic, PLD, Verilog® and VHDL Design Entry Supported
- Macro Libraries for AT40K FPGA Families
- Automatic Macro Generators for AT40K
- HDL Planner for VHDL and Verilog Entry
- Hierarchy Browser
- User Library Management
- Technology Mapping
- Multi-chip Partitioning
- Floor Planning Capability
- Graphical Constraint Entry
- Incremental Design Change
- Timing Driven Design with Advanced Static Timing Analysis
- Automatic Place and Route
- Interactive Layout Editing
- Power Calculation
- Full Back-annotation for Functional and Post-layout Simulation
- Online Tutorials for New and Advanced Users
- Applications Support

4.2 Description

Atmel's Integrated Development System (IDS) lets designers create fast, predictable designs with AT40KEL Series FPGAs.

Available for use with Windows® 2000/XP based computers, IDS combines industry-standard software for design entry, synthesis and simulation with Atmel's proprietary software for component generation, automatic and interactive placement and routing, timing analysis and bitstream generation.

The IDS Desktop is shown in Figure 4-1. The Design Flow Bar provides push-button access to all the steps in the design flow. This includes opening schematic entry and synthesis tools and generating files for simulations automatically.

Figure 4-2 shows the HDL Planner tool which is used for VHDL and Verilog Design Entry.

Figure 4-3 shows the Macro Generator used to generate standard components with optimal layout and performance.

For further details about working with IDS, please read the "Integrated Development System - Figaro, User Guide, September 2002" found in file `C:\SystemDesigner\doc\User Guide.pdf`

Figure 4-1. Integrated Development System

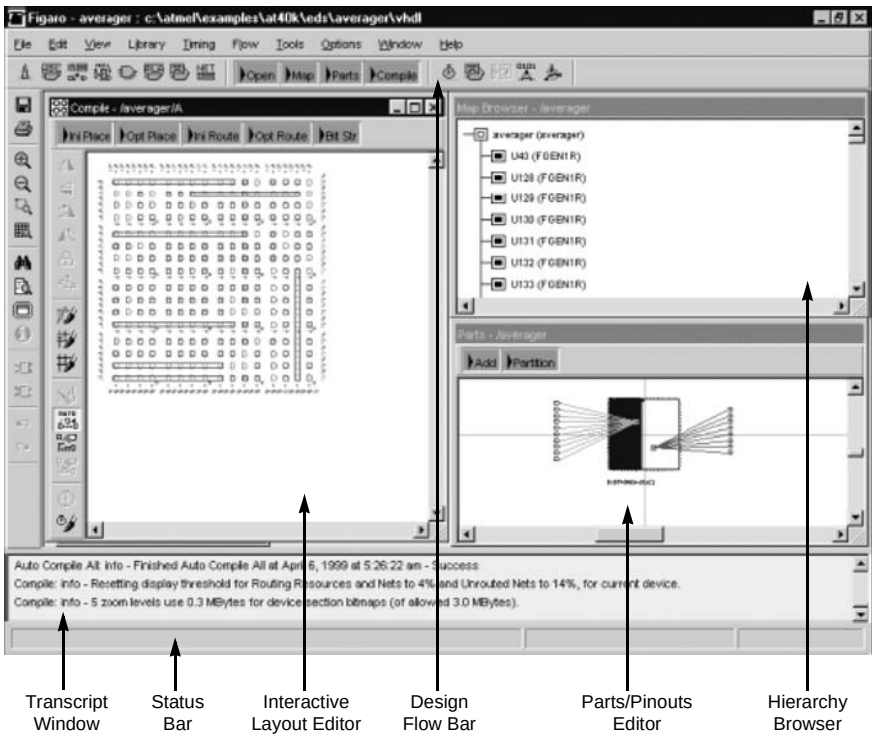


Figure 4-2. HDL Planner Tool

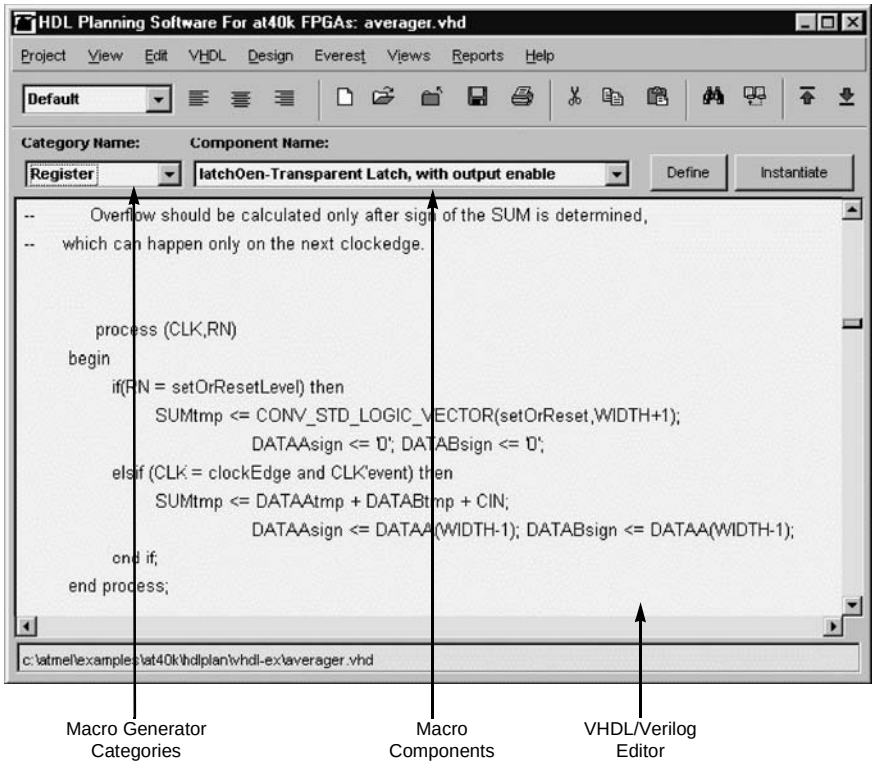
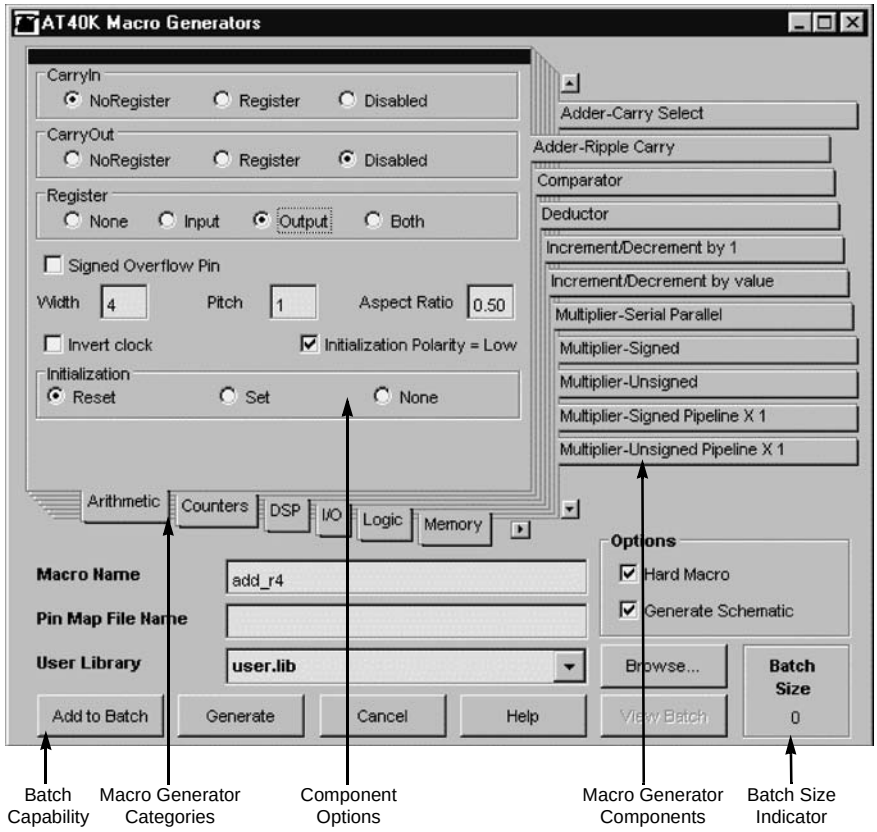


Figure 4-3. Macro Generator



4.3 Selecting Devices

To select a part in IDS, always set “Application” menu to “Aerospace” to limit the list of available devices. Then select IDS part name according to product part number (written on device):

Product Part Number	IDS Part Name
AT40KEL040KW1-E	AT40KEL040KW1S
5962-0325001QXC	
5962-0325001VXC	
930400801	
AT40KFL040KW1-E	
5962-0325002QXC	
5962-0325002VXC	
AT40KFL040KW1-SCC	
AT40KEL040KZ1-E	AT40KEL040KZ1S
5962-0325001QYC	
5962-0325001VYC	
930400802	
AT40KFL040KZ1-E	
5962-0325002QYC	
5962-0325002VYC	
AT40KFL040KZ1-SCC	

4.4 Known Problems and Limitations

- Flip-flops embedded in pads cannot be used yet.
- The “clear ram” feature that shall initialize Free RAM at reset does not work yet, so memory contents after power-on/reset shall be considered unknown.
- Always generate an 8-bit bitstream for programming an AT17LV010 configurator (never generate a 16-bit bitstream: although this is still possible, such a bitstream cannot properly be loaded by an FPGA).
- AT40KAL synthesis library in LEONARDO synthesis tool were characterized at 5V worst case while AT40KEL product operates at 3.3V. Synthesis constraints shall be scaled accordingly to drive synthesis process. Nevertheless, timings in IDS are based on a 3.3V characterization and no scaling is required.

Section 5

Configurator Programming System (CPS)

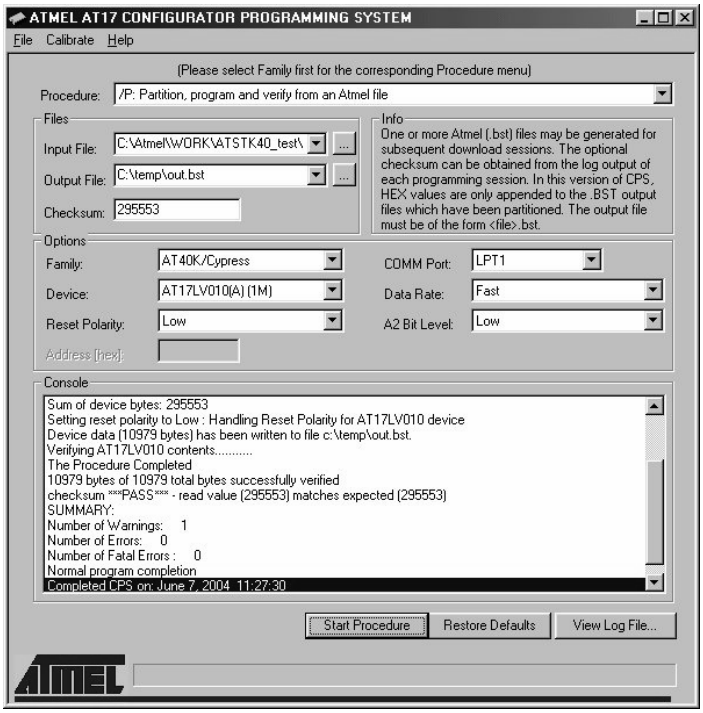
5.1 Description

The CPS software programs, verifies, and reads back AT17 Configuration EEPROM on:

- ATDH40M prototyping board using a standard DB25 M/F parallel cable
- Customer's final application board using Atmel's ATDH2225 ISP dongle

It also converts and partitions from several file formats to support Atmel FPGA applications.

Figure 5-1. CPS Main Window



CPS is installed as part of the SystemDesigner software.

5.2 Programming the Contents of a *.bst File to AT17 Devices

- *Procedure*: Select "/P: Partition, program and verify from an Atmel file"
- *Files*: Default or previous settings are given. You may need to modify the following:
  - *Input File*: <design>.bst
  - *Output File*: Defaults to *CPS_INSTALL_DIRECTORY*\out.bst or the most recently used output filename
  - *Checksum*: Clear area if not automatically done
- *Options*: Default or previous settings are given. You may need to modify the following:
  - *Family*: Select "AT40K/Cypress"
  - *Device*: Select "AT17LV010(A) (1M)"
  - *Reset Polarity*: Select the reset polarity
  - *COMM PORT*: Select the port the cable is connected to (usually LPT1)
  - *Data Rate*: Select "Fast"
  - *A2 Bit Level*: Select "Low"
- Press "Start Procedure" (1)

5.3 Reading the Contents of the Configurator to a *.bst File

- *Procedure*: Select "/R: Read data from device and save to an Atmel file"
- *Files*: Default or previous settings are given. You may need to modify the following:
  - *Output File*: Defaults to <CPS_INSTALL_DIRECTORY>\out.bst or the most recently used output filename
- *Options*: Default or previous settings are given. You may need to modify the following:
  - *Family*: Select "AT40K/Cypress"
  - *Device*: Select "AT17LV010(A) (1M)"
  - *COMM PORT*: Select the port the cable is connected to (usually LPT1)
  - *A2 Bit Level*: Select "Low"
- Press "Start Procedure" (1)

5.4 Verifying the Device against a *.bst File

- *Procedure*: Select "/V: Verify device against an Atmel file"
- *Files*: Default or previous settings are given. You may need to modify the following:
  - *Input File*: <design>.bst
  - *Checksum*: Provide checksum if known, otherwise clear area
- *Options*: Default or previous settings are given. You may need to modify the following:
  - *Family*: Select "AT40K/Cypress"
  - *Device*: Select "AT17LV010(A) (1M)"
  - *COMM PORT*: Select the port the cable is connected to (usually LPT1)
  - *A2 Bit Level*: Select "Low"
- Press "Start Procedure" (1)

1. When starting for the first time, CPS will open a popup asking to launch clock-calibration. Please safely accept, normal operation will resume once clock is calibrated.

5.5 Other Procedures

All other procedures available in CPS are not supported on ATDH40M nor on customer's final application.

Section 6

Board Configuration

6.1 Programming Setup

Figure 6-1 is the board layout of the ATDH40M motherboard.

Figure 6-1. Motherboard Layout – ATDH40M

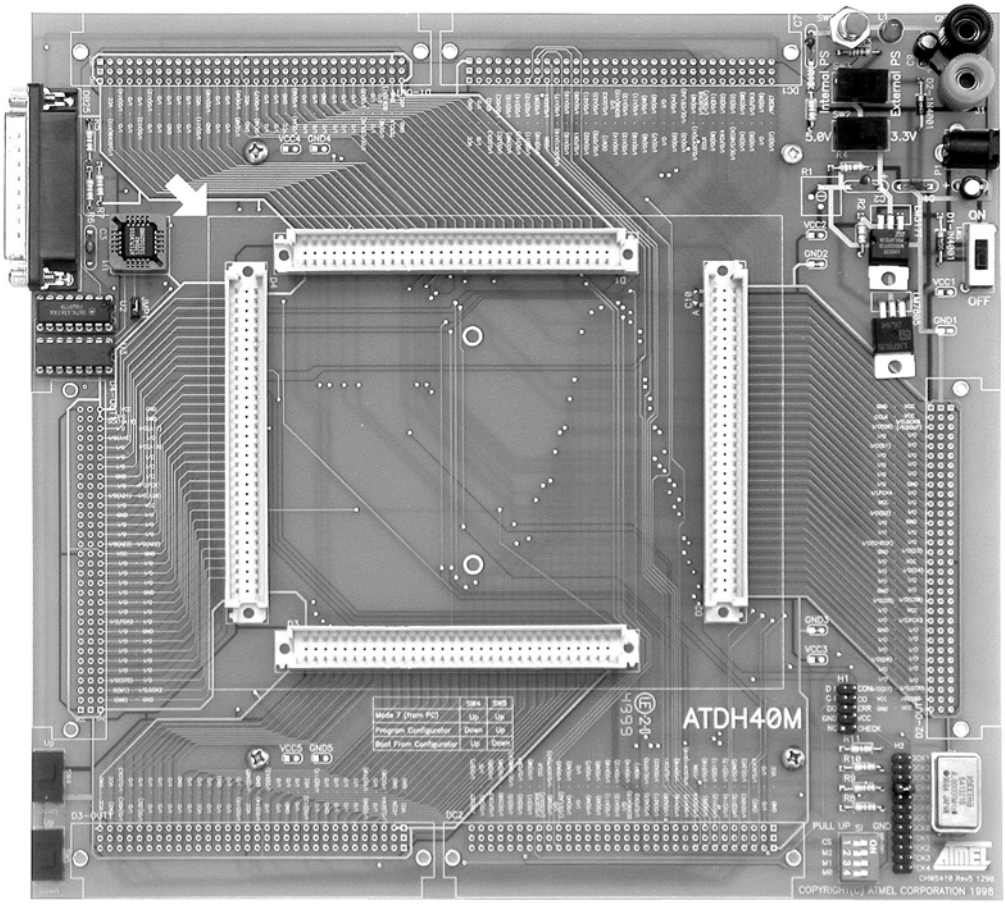


Figure 6-2 & Figure 6-3 show the compatible daughterboards (only one included in the kit). To connect a daughterboard to the motherboard, fit the daughterboard on top of the motherboard by aligning the two arrows together. The two boards will only fit one way.

Figure 6-2. Daughterboard Layout - MQFP160

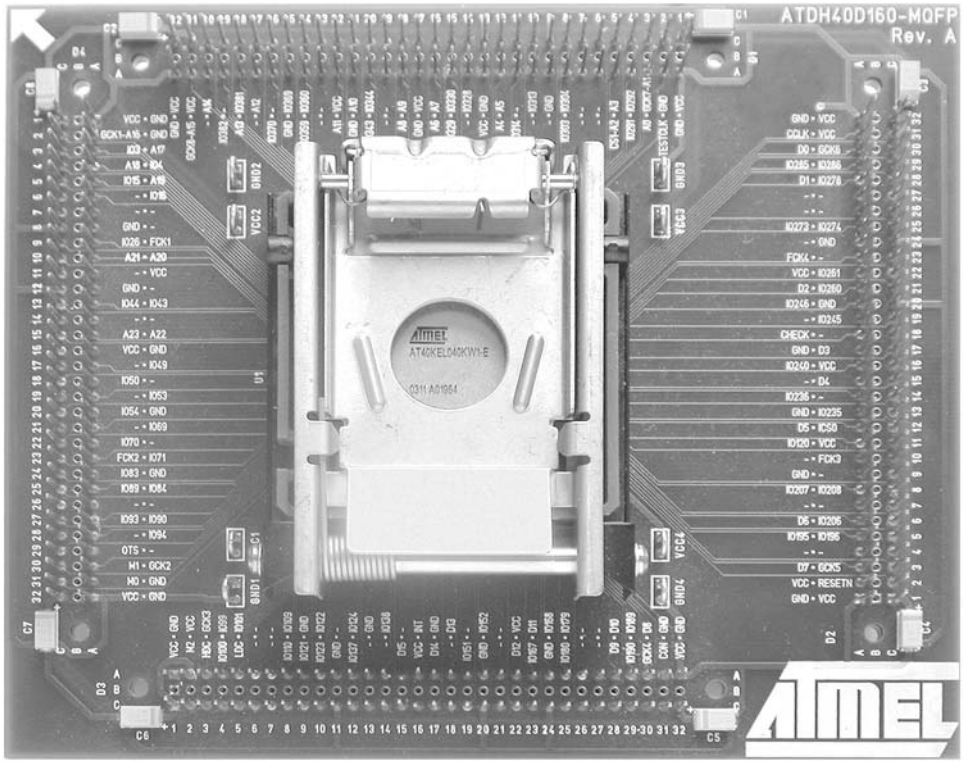
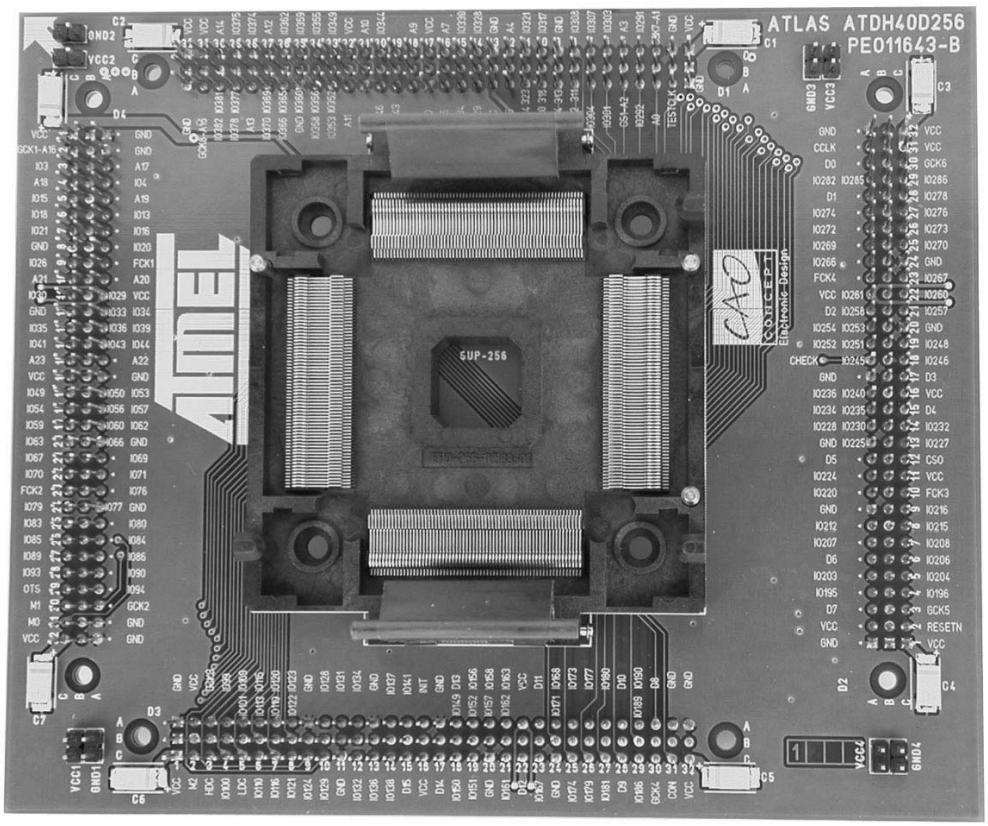


Figure 6-3. Daughterboard Layout - MQFP256



6.2 Power Configuration

Power for the motherboard can come from one of two sources located in the upper right corner. It can be supplied by either the jack inputs J1 and J2, or by a 9V power input P1. The source that will drive the motherboard is determined by switch SW3. Power supplied by the jacks uses the *external* setting. Power supplied by the 9V source uses the *internal* setting. Voltage on the motherboard for the latter setting is regulated by switch SW2. AT40KEL parts use the 3.3V setting. The LED L1 will light up only when power is correctly supplied to VCC. Table 1 details the configuration.

Table 1. Motherboard Power Distribution

SW1	SW2	SW3	Voltage
Off	X	X	0.0V (no power)
On	X	External	Variable (beware of a diode voltage drop on the internal supply since a diode protection is present on the motherboard)
On	3.3V	Internal	3.3V (for use with 3.3V devices only)
On	5.0V	Internal	5.0V (for use with 5V devices only)

6.3 FPGA Configuration Mode Settings

Switch DIP-SW1 determines the AT40KEL040 FPGA configuration mode settings. It is located in the bottom right corner. When *On*, corresponding FPGA signal is pulled-up by a 4.7K Ohm resistor. When *Off*, corresponding FPGA signal is connected directly to ground. Table 3 lists the switch combinations and their effects. .

Table 2. Configuration Modes

CS	M2	M1	M0	Effect
Off	-	-	-	Pull CS signal to a (weak) ‘1’, used when CS is a User I/O or for direct control from the DCx and Dx-OUT prototyping connectors all around motherboard
On	-	-	-	Pull CS signal to ground, used when cascading FPGAs
-	On	On	On	Mode 0: Master Serial
-	On	On	Off	Mode 1: Slave Serial
-	On	Off	On	Mode 2: Slave Parallel
-	Off	On	On	Mode 4: Synchronous RAM
-	Off	Off	On	Mode 6: Slave Parallel UP
-	Off	Off	Off	Mode 7: Slave Serial Also leaves Mx pins for direct control from the DCx and Dx-OUT prototyping connectors all around motherboard

6.4 EEPROM Program/Boot Settings

Switches SW4 and SW5 determine the *program* and *boot* settings for the ATDH40M. They are located in the bottom left corner. Table 3 lists the switch combinations and their effects. SW4 controls the $\overline{\text{SER\_EN}}$ signal line of the motherboard to the 2:1 multiplexer (device U3) and the AT17 (device U1). SW5 connects signal D0 from the FPGA

device to the AT17 configuration memory device only (*down*) or leaves it unconnected (*up*).

Table 3. Programming Modes

SW4	SW5	Effect
Up	Up	Disconnect on-board AT17 memory
Down	Up	Program AT17 Configuration Memory
Up	Down	Program FPGA in Master Serial mode from AT17
Down	Down	Not allowed

6.5 Programming the AT17 Configuration Memory Device

When SW4 is set to *Down* and SW5 is set to *Up*, the AT17 FPGA configuration memory can be programmed by the parallel port interface located on the top left corner. Please connect the motherboard to the PC using the DB25 parallel cable. Programming the AT17 FPGA configuration memory from the PC can be achieved using the Configurator Programming System (CPS) software installed together with SystemDesigner. This software accepts the ASCII bitstream files (.bst) generated by IDS.

6.6 Programming the FPGA Device Using the AT17 Configuration Memory

When SW4 is set to *Up* and SW5 is set to *Down*, the AT17 configuration memory can program the FPGA in Master Serial mode. Please configure AT40KEL040 FPGA in Master Serial mode at switch DIP-SW1. To ensure reliable system power-up, set jumper JMP1 (located below the AT17 configuration memory socket). The AT17 configuration memory must be programmed prior to this setup.

6.7 Troubleshooting

1. Check that the motherboard is connected to the PC through the parallel port.
2. Check that the motherboard power switch SW1 is *ON* and the power configuration switches SW2 and SW3 are correct.
3. Make sure programming configuration switches SW4 and SW5 are correct.
4. Verify that the daughterboard is inserted correctly and that it receives power.

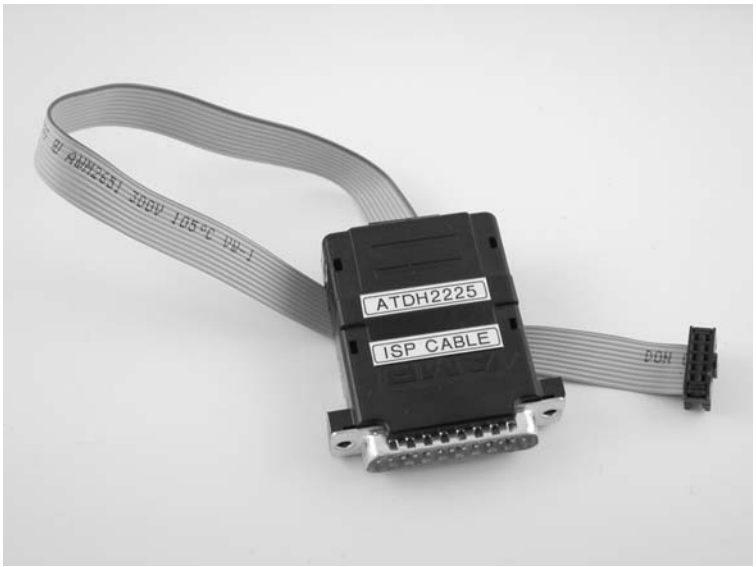
Section 7

In-System Programming AT17LV010 Configuration EEPROM

7.1 Description

The ATDH2225 in-system programming (ISP) cable is a PC-only based cable that attaches to the parallel port of a computer. This cable allows designers to quickly and economically program Atmel's family of AT17 configuration memories into their application. This cable can also be used to download and verify configuration data cascading up to 8 devices. Therefore, it is a truly portable solution that allows engineers to work from their lab bench or office.

Figure 7-1. ATDH2225 ISP dongle



7.2 Software Support

Make sure to use the latest CPS software (http://www.atmel.com/dyn/products/tools_card.asp?tool_id=3191). CPS is used to program configurators and supports the ISP cable. The software, in conjunction with Atmel ISP cable, can be used to download programming files directly to Atmel's configurator(s).

- CPS – Configurator Programming System
- GUI Based Interface
- Supports Windows® 95/98/2000 and Windows NT®

- Supports up to 8 devices
- Supports programming reset polarity
- Verification routines to validate programming
- Accepts HEX, MCS, POF, RBF, HXU and BST file formats
- Online help
- Ability to enable or disable internal oscillator

7.3 Connecting Cable to Target System

The cable draws its power from the target system through VCC and GND. Therefore, power to the cable, as well as to the target FPGA, must be stable. Do not connect any signals before connecting VCC and GND. Connect the programming dongle to the parallel port of your PC. Connect the other end with 10-pin header to your target system (Figure 7-2). Your target system should have the 10-pin header pin layout as follow in order to match the download cable (Figure 7-3). The pin 9 of the 10-pin header on the target system is not connected, so it can be made a key pin when cut off. The control signals generated by the software are fed to the header. The programming algorithms written by Atmel can be used to program an AT17 device in-system.

Figure 7-2. In-System Programming Application

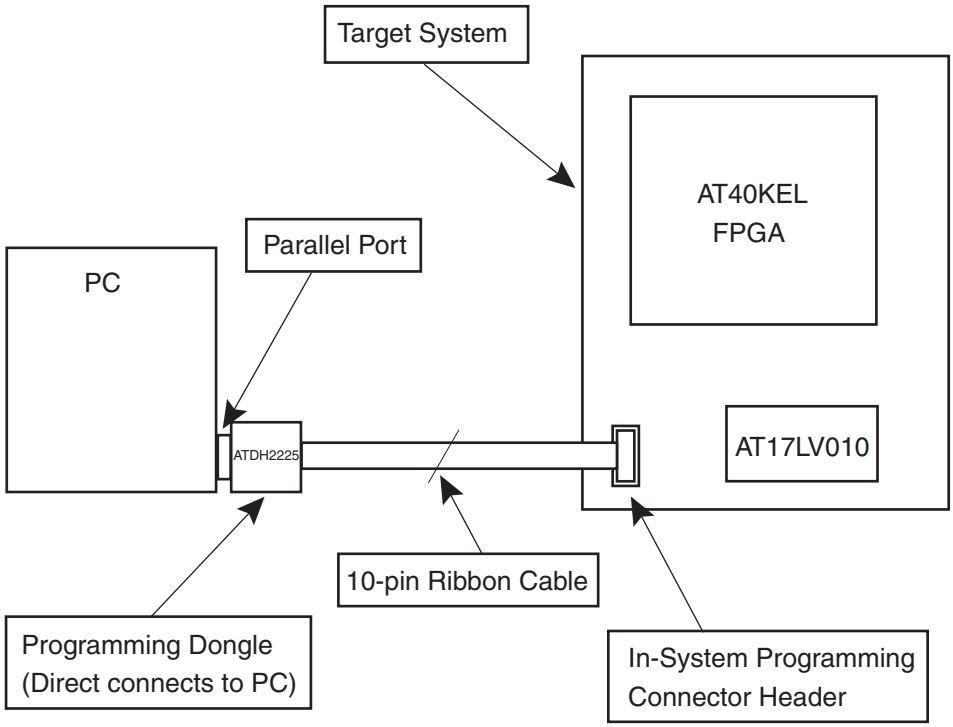


Figure 7-3. In-System Programming Connector Header (shown from above)

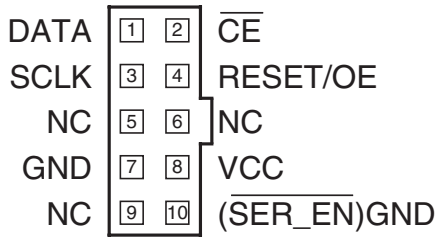


Table 4. 10-pin Header Pin Location on Target Board

1 - DATA	2 - $\overline{CE}$ *(unused)*
3 - SCLK	4 -RESET/OE (*unused*)
5 - SW1 *(optional)*	6 - SW2 *(optional)*
7 - GND	8 - VCC
9 - NC	10 - $\overline{SER\_EN}$

Notes:
1. The 10-pin header is 0.1' spacing.
2. Pin 9 is the key pin (can be cut off).
3. Pin 5 and Pin 6 of the 10-pin header are the two signals used for selecting the appropriate device when cascading up to 8 devices. The latest CPS software has the ability to control the two signals SW1 and SW2, and by using the A2 pin of the device, you can select up to 8 devices. Therefore, you could use a 2-to-4 decoder to cascade 8 devices using our existing ISP circuit (see Figure 7-5).

7.4 ISP Hardware Interface

Supporting In System Programming (ISP) in your final application is very simple and requires only four additional components (a 10-pin connector, a diode and 2 resistors), as shown in Figure 7.4.

Figure 7-4. In-System Programming of AT17LV010 for AT40KEL

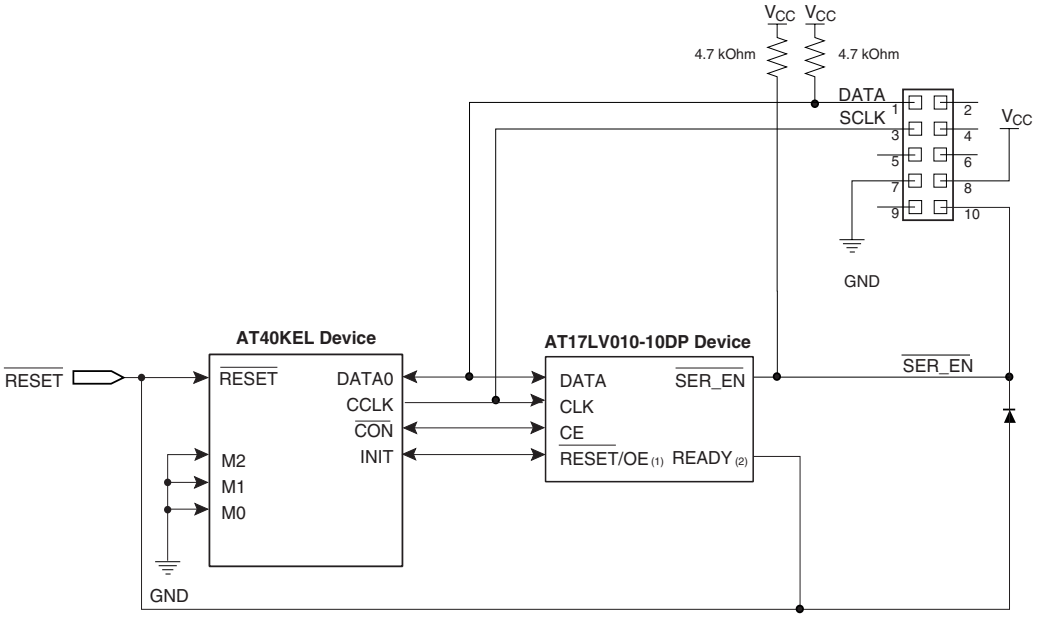


Figure 7-5. ISP of Cascaded AT17LV010 in AT40KEL FPGA Applications

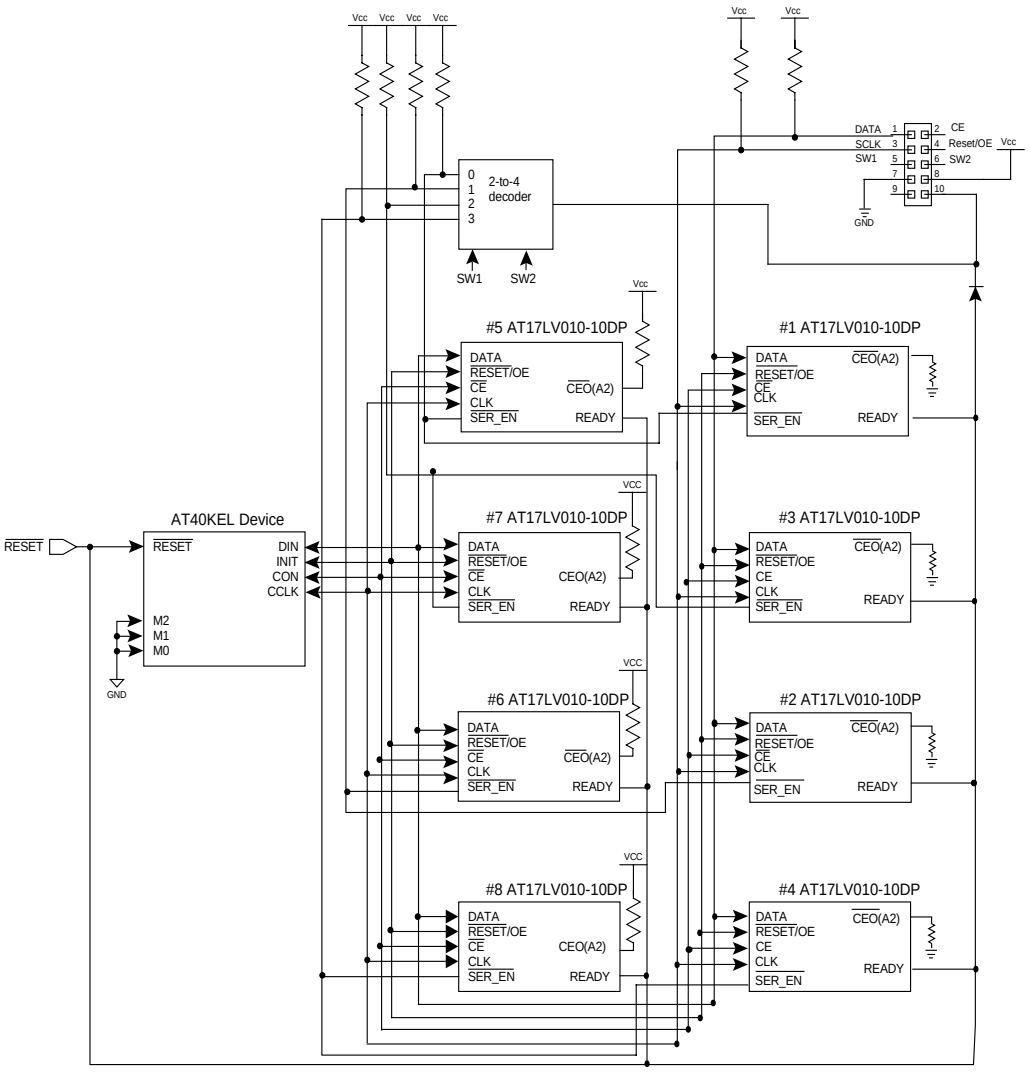


Table 5. 2 Devices

Device	A2
Device #1	pull down
Device #2	pull up

Note: No additional logic required, SW1 and SW2 not used.

Table 6. 4 Devices

Device	SW1	A2
Device #1	0	pull down
Device #2	1	pull down
Device #3	0	pull up
Device #4	1	pull up

Note: SW1 and some additional logic required for selecting up to 4 devices.

Table 7. 8 Devices

Device	SW1	SW2	A2
Device #1	0	0	pull down
Device #2	0	1	pull down
Device #3	1	0	pull down
Device #4	1	1	pull down
Device #5	0	0	pull up
Device #6	0	1	pull up
Device #7	1	0	pull up
Device #8	1	1	pull up

Note: SW1, SW2 and some additional logic required for selecting up to 8 devices.

Related Documents

AT17LV010-10DP Datasheet

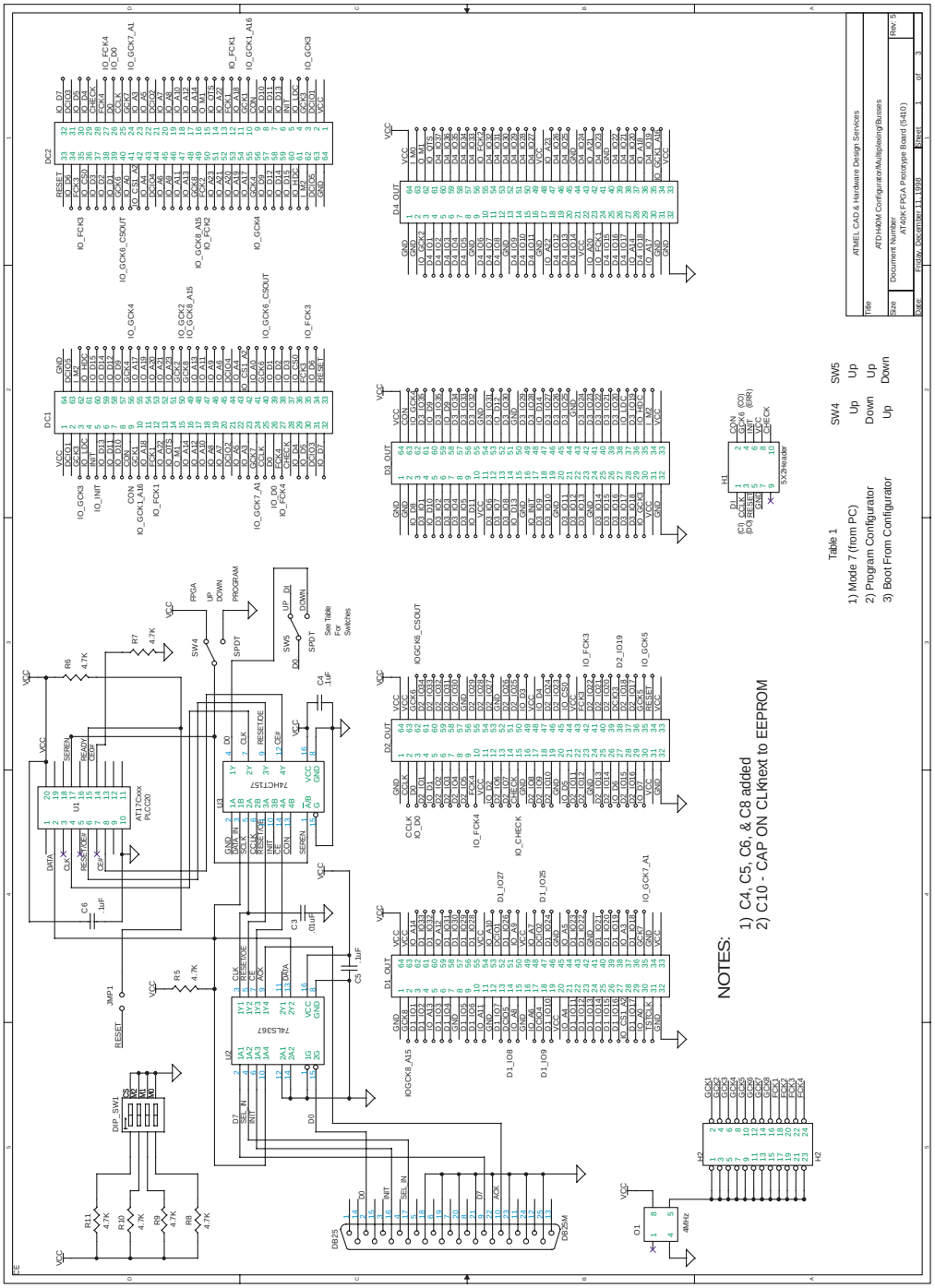
Programming Specification for Atmel's FPGA Serial Configuration Memories

Section 8

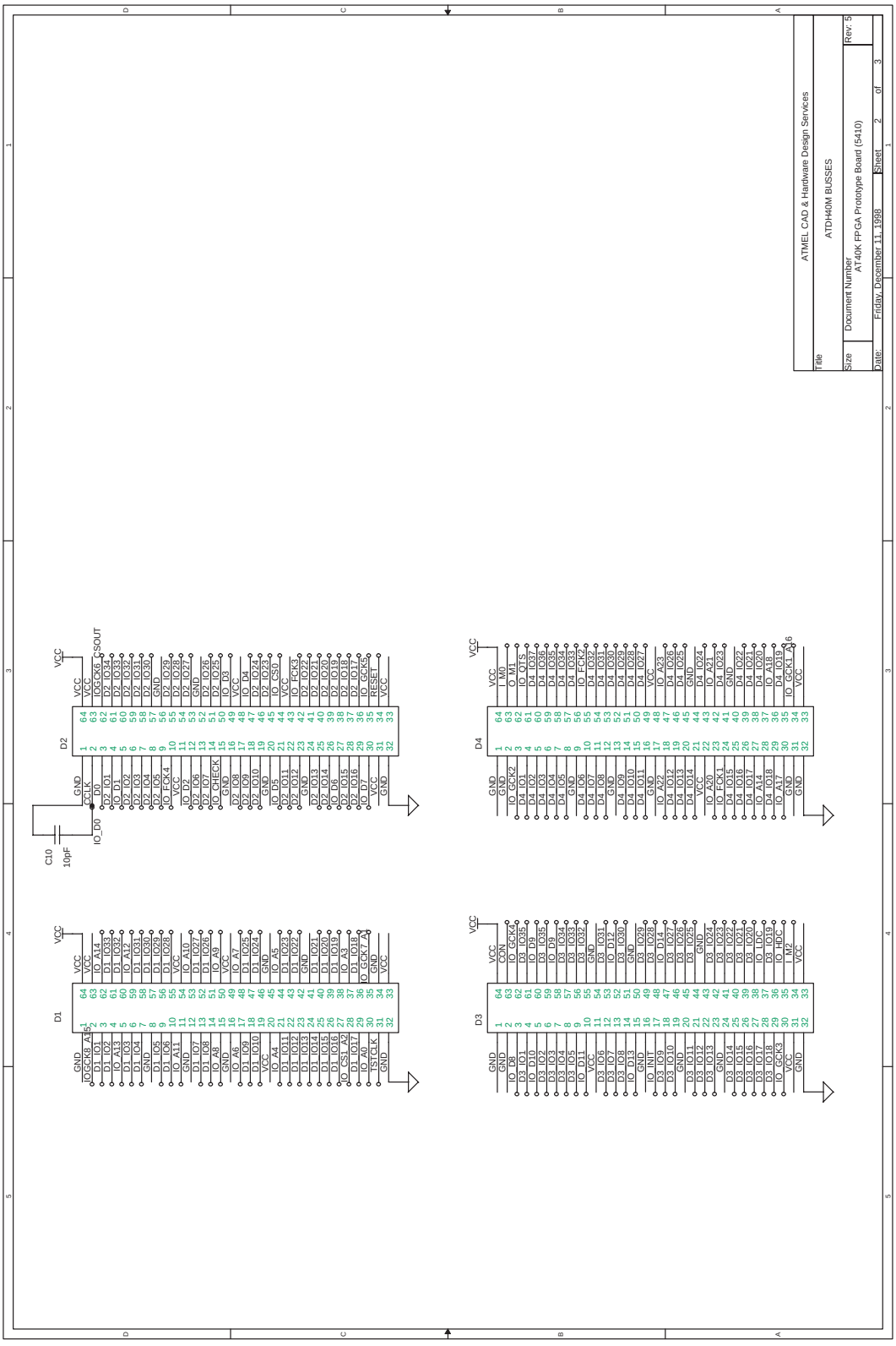
Appendix A

8.1 ATDH40M Layout Schematics

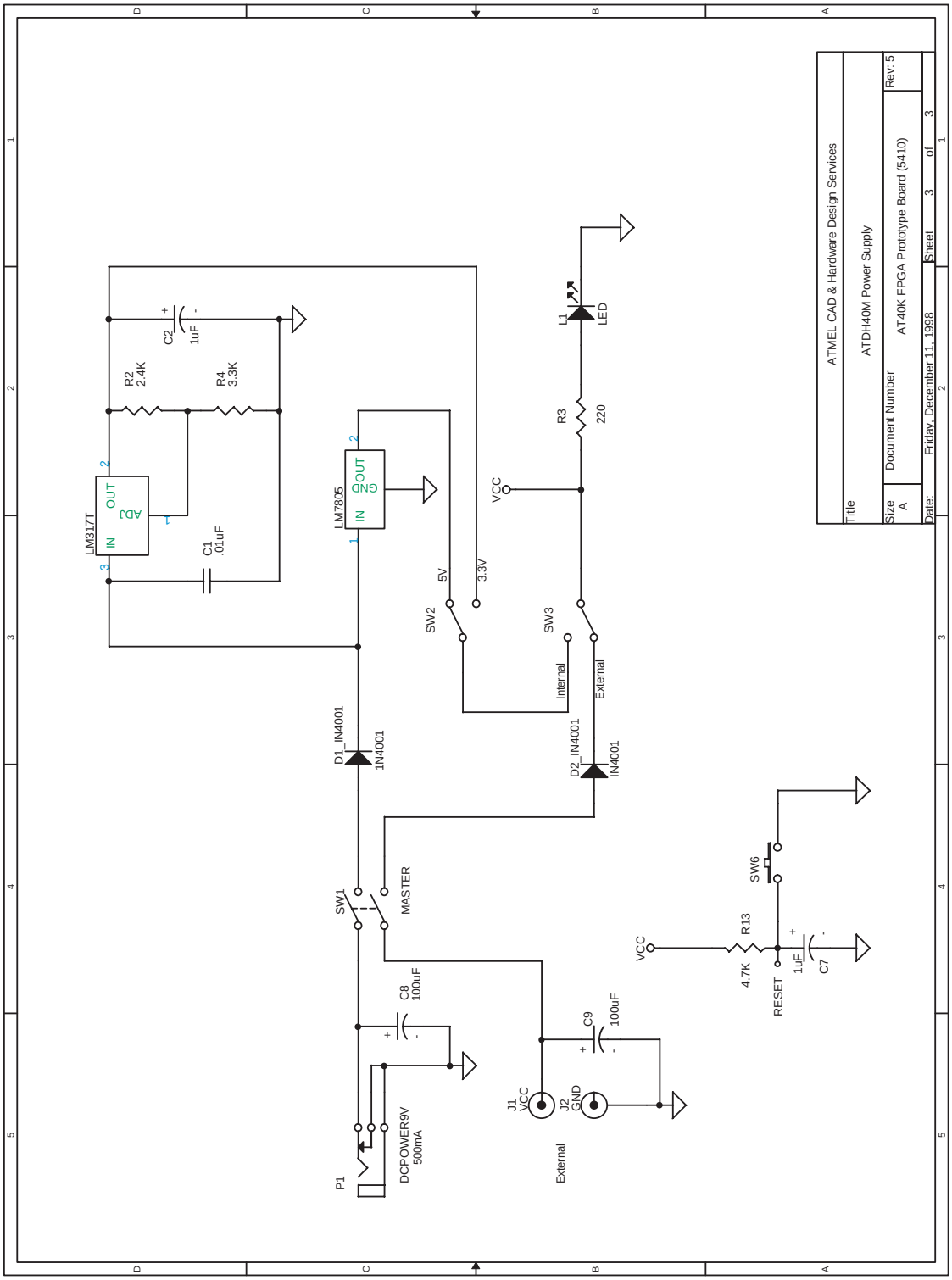
8.1.1 Configurator/Multiplexing /Buses



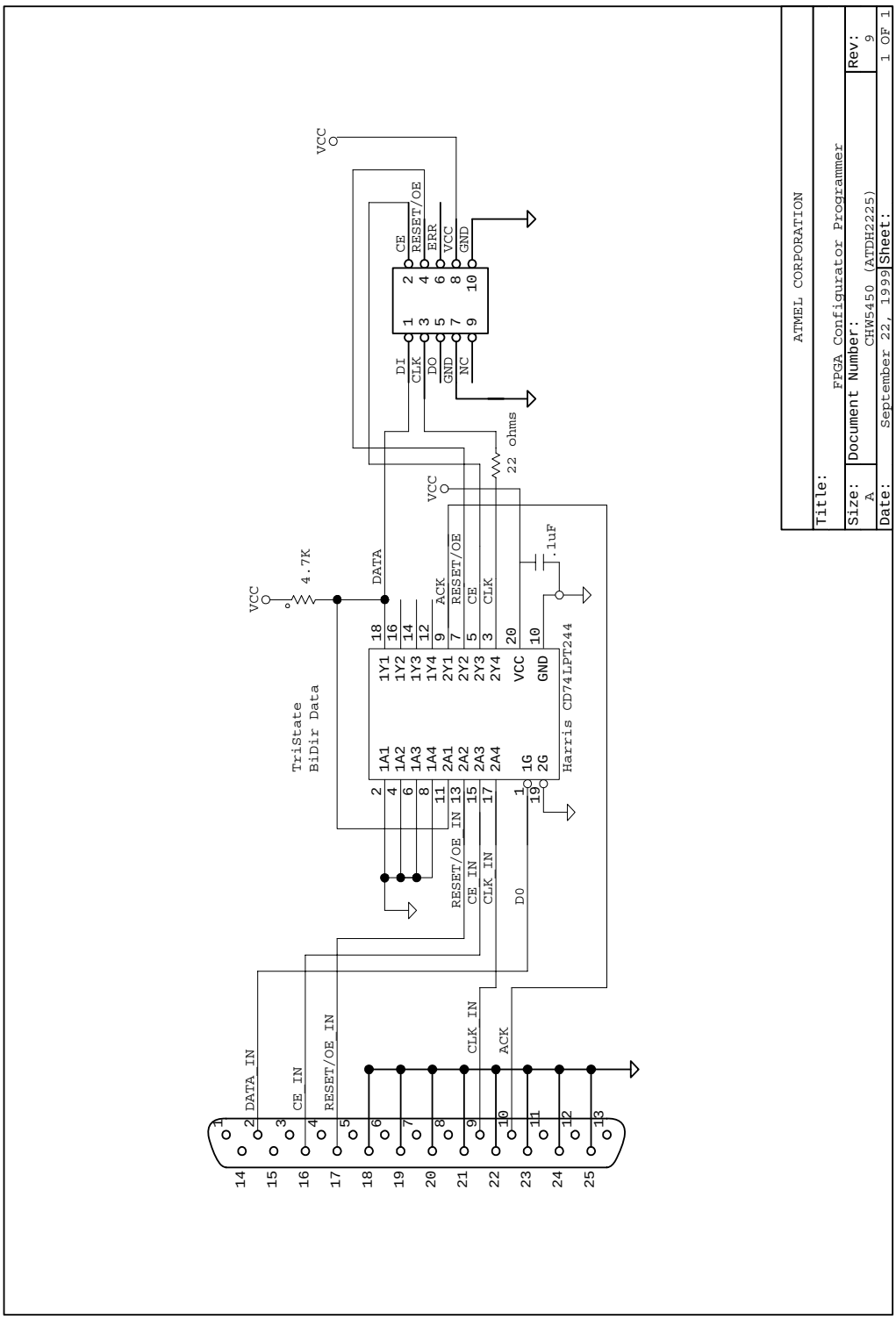
8.1.2 Buses


ATMEL CAD & Hardware Design Services
Title
ATDH40M BUSSES
Size
Document Number
AT40K FPGA Prototype Board (5410)
Rev: 5
Date: Friday, December 11, 1998
Sheet 2 of 3
D1
D2
D3
D4
C10
10pF
IO_D0
VCC
GND

8.1.3 Power Supply



8.2 ATDH2225 Schematics



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