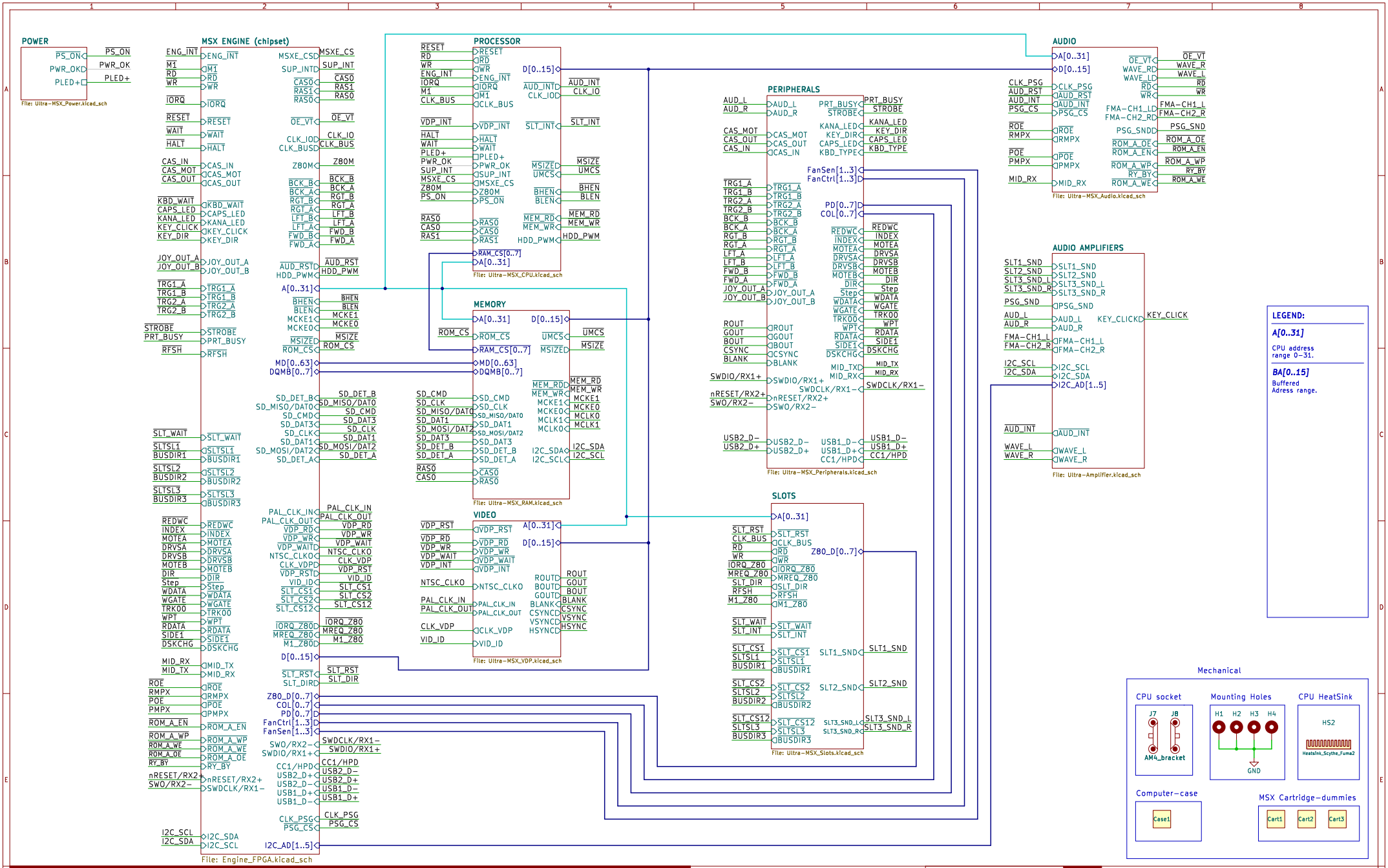
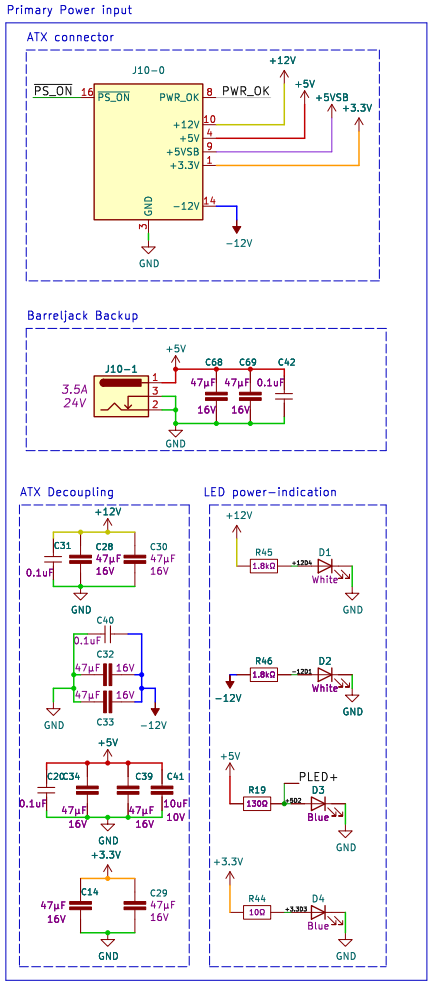
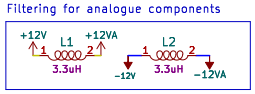
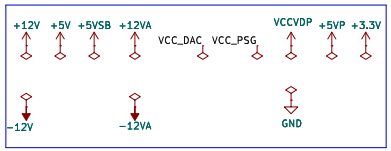
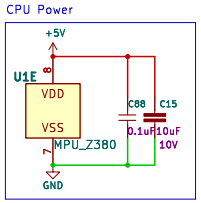
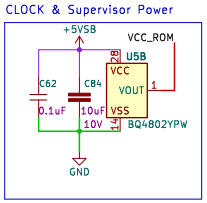

POWER
PS_ON
PWR_OK
PLED+
File: Ultra-MSX_Power.kicad_sch
MSX ENGINE (chipset)
File: Engine_FPGA.kicad_sch
PROCESSOR
File: Ultra-MSX_CPU.kicad_sch
MEMORY
File: Ultra-MSX_RAM.kicad_sch
VIDEO
File: Ultra-MSX_VDP.kicad_sch
PERIPHERALS
File: Ultra-MSX_Peripherals.kicad_sch
SLOTS
File: Ultra-MSX_Slots.kicad_sch
AUDIO
File: Ultra-MSX_Audio.kicad_sch
AUDIO AMPLIFIERS
File: Ultra-Amplifier.kicad_sch
LEGEND:
A[0..31]
CPU address range 0-31.
BA[0..15]
Buffered Adress range.
Mechanical
CPU socket
Mounting Holes
CPU HeatSink
Computer-case
MSX Cartridge-dummies
ULTRA-MSX
Rev A-A
Size A3
Date 2022-06-05
Sheet 1/10
File Ultra-MSX.kicad_sch
KiCad E.D.A. kicad 7.0.5

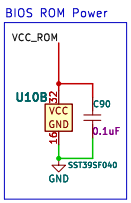


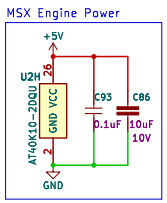


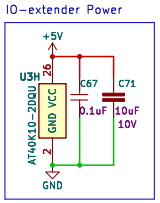


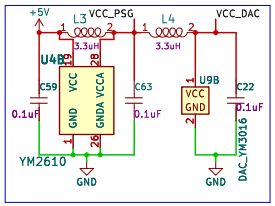


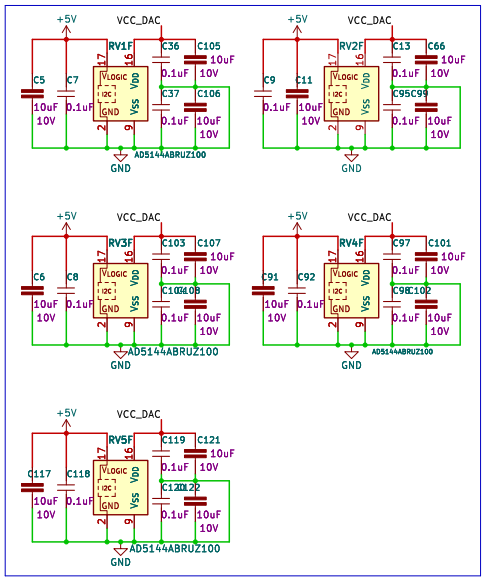


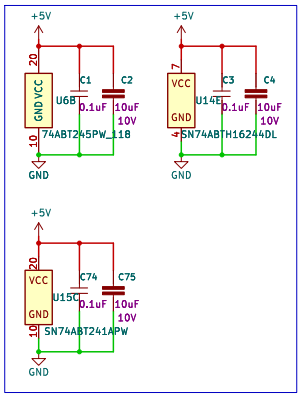


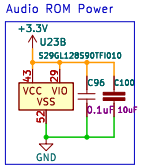


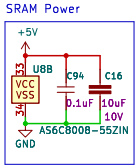












Power-use Calculation:

12V:

Wave:
MIDI:
A_AMP(x7):

5V:

CPU: 20 mA
MSXE: 40 mA
IOE:
RAM:
BUF(x3):
WD:
ROM:
CAS_AMP:
CAS_RY:

AUD:

2610:
VT(x4):
Sample:
RV(x4):
A_DAC:

Power-management:
---
https://www.embedded.com/adding-a-power-management-mcu-to-your-system-reduces-standby-energy-use/
--

LEGEND:

/PS_ON = from Motherboard - when PSU is on, this line will be grounded by a device on the Motheboard.

PWR_OK = output from PSU, indicating that power-out has stabilized.

+5VSB = Standby-signal - supplies power when other lines are off. can be used to power the device sending PS_ON.

GNDA = Analog ground.

GNDPWR1,2 = the incoming Ground from the PSU(s) connected to the board.

+5VP = External five volts from the FPGA-programmer.

VCT = VCC Target (device to be programmed by JTAG)

EXTERNAL NETS

PWR_OK ▷PWR_OK
PS_ON ▷PS_ON
PLED+ ▷PLED+

ULTRA-MSX

ULTRA-MSX

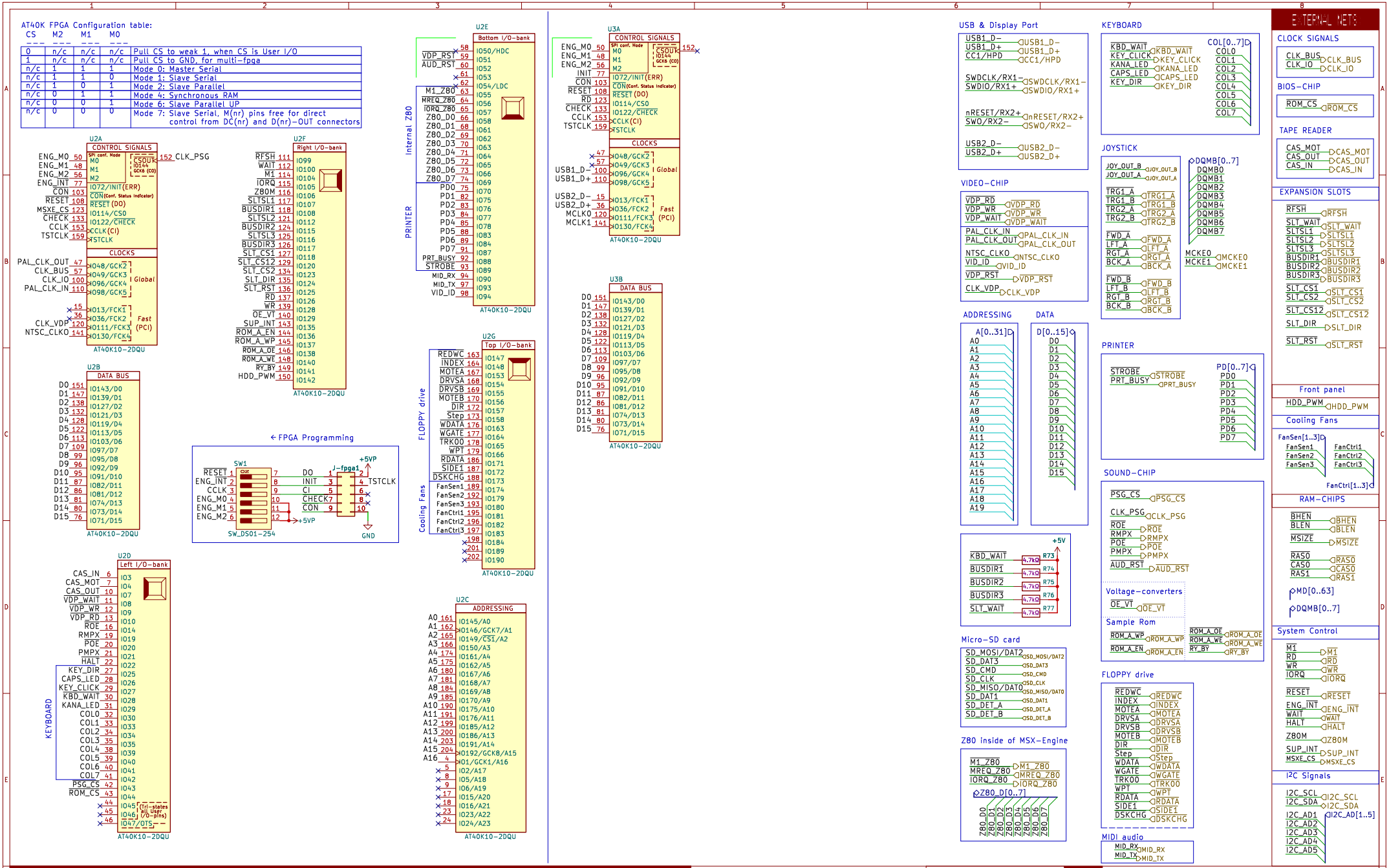
POWER

Size: A3 | Date: 2022-06-05 | Rev: 2/10 | Rev: A-A | File: Ultra-MSX_Power.kicad_sch

KiCad E.D.A. kicad 7.0.5

AT40K FPGA Configuration table:

CS	M2	M1	M0	
0	n/c	n/c	n/c	Pull CS to weak 1, when CS is User I/O
1	n/c	n/c	n/c	Pull CS to GND, for multi-fpga
n/c	1	1	1	Mode 0: Master Serial
n/c	1	1	0	Mode 1: Slave Serial
n/c	1	0	1	Mode 2: Slave Parallel
n/c	0	1	1	Mode 4: Synchronous RAM
n/c	0	0	1	Mode 6: Slave Parallel UP
n/c	0	0	0	Mode 7: Slave Serial, M(nr) pins free for direct control from DC(nr) and D(nr)-OUT connectors

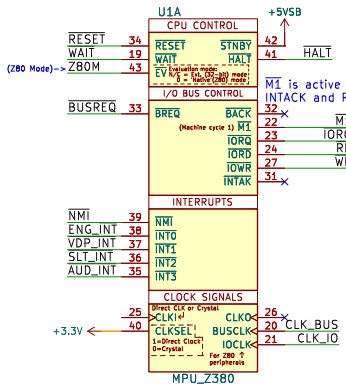


ULTRA-MSX

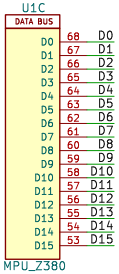
ULTRA-MSX

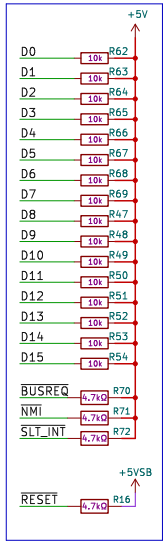
MSX ENGINE (chipset)

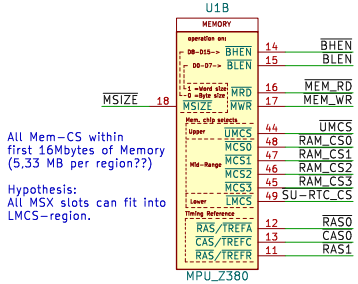
Size: A3	Date: 2022-06-05	Rev: 3/10	Sheet: A-A
KiCad E.D.A. kicad 7.0.5			File: Engine_FPGA.kicad_sch



M1 is active during INTACK and RETI.

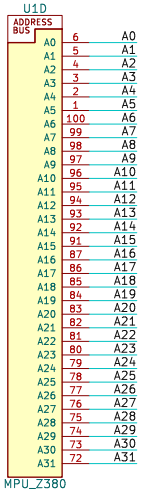


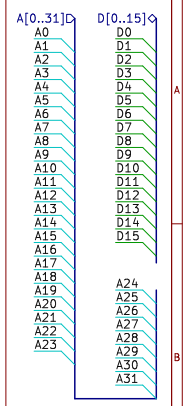


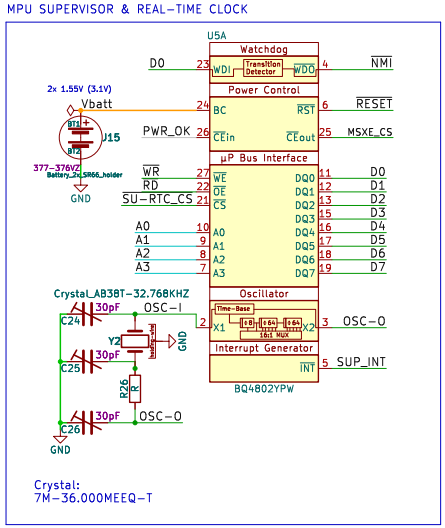


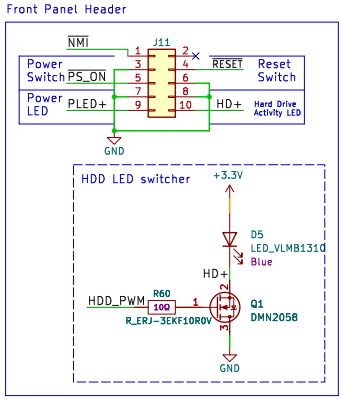
All Mem-CS within first 16Mbytes of Memory (5.33 MB per region??)

Hypothesis:
All MSX slots can fit into LMCS-region.









NMI address in MSX Bios:
0066h

You need a way to return the /NMI signal to normal after the interrupt is accepted by the Z80, otherwise you'd be having NMI's over & over again. Probably would need some logic (a few 74xx IC's or something).

IIRC, address 0066h is used for a File Control Block or something like that under DOS, so that might be a problem. In BASIC a hook is called.

Chip-Select chain:
SU-RTC_CS -> MSXE_CS -> ROM_CS

Omega chip-select chain:
[Z80]WR/IORQ/M1 ->[SPLD]RTC_CS ->[WD]RTC_CS_B ->[RTC]Alarm??

Socket CPU:
--
M3 industries - 8468-21A1-RK-TP

https://www.digikey.se/en/products/detail/8468-21A1-RK-TP/3M6821A1-ND/1026489?utm_campaign=buynow&utm_medium=aggregator&curr=usd&utm_source=octopart

Reference design RTC:
https://e2e.ti.com/support/clock-timing-group/clock-and-timing/f/clock-timing-forum/792830/bq4802y-bq4802y-don-t-keep-clocking-in-vbc-mode

Front panel

Control signals

Memory Signals

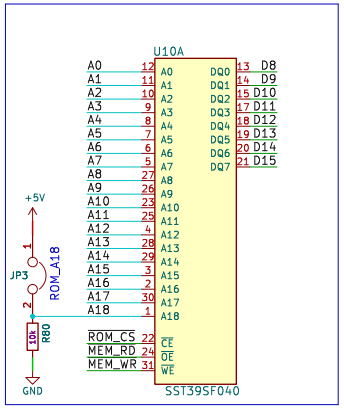
WATCHDOG signals

ULTRA-MSX

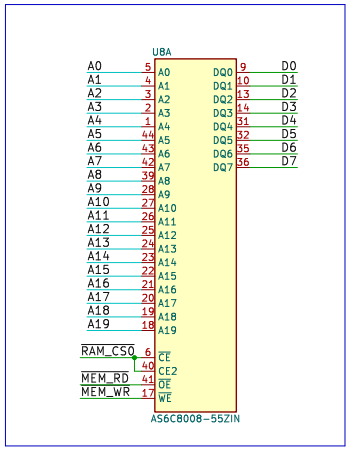
PROCESSOR

Size: A3	Date: 2022-06-05	Rev: 4/10	Sheet: A-A
KiCad E.D.A. kicad 7.0.5			File: Ultra-MSX_CPU.kicad_sch

ROM/BIOS chip



RAM Chip

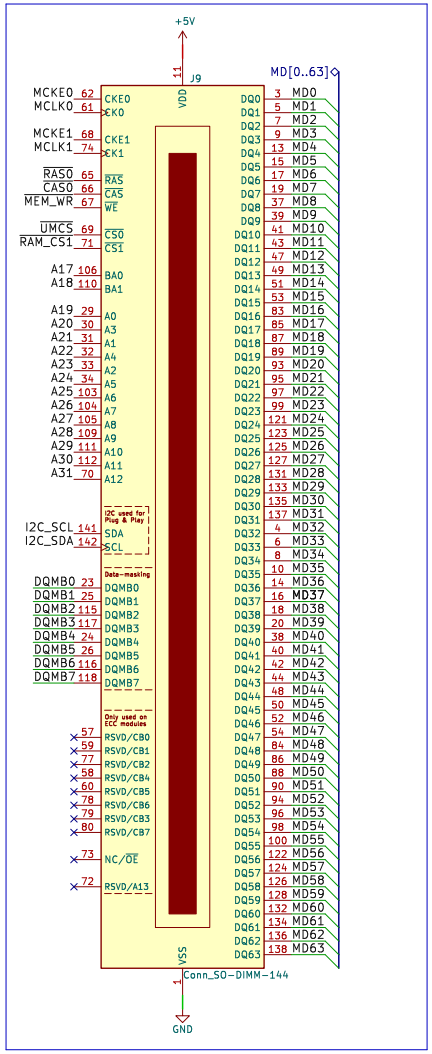


MSX Memory-links:
---
https://hansotten.file-hunter.com/do-it-yourself/memory-mappers-slots/

Example of good Memory mapper
https://www.msx.org/wiki/Padial_LPE-4FMB-V8SKP

Talk to Jurjen Kranenborg
about the Z380 and system
design:
---
https://www.kranenborg.org/

RAM module



3.3V SDRAM module, 100-133 MHz

DDR2?

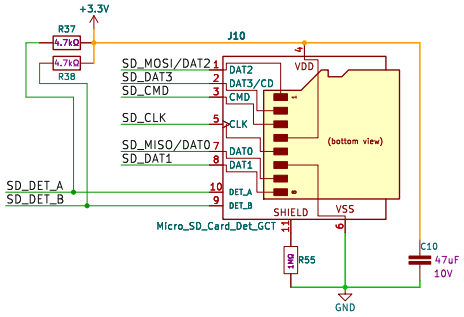
EDO 5V, 32MB

Open source memory controllers:
---
https://web.archive.org/web/20191020220315/http://hamsterworks.co.nz/mediawiki/index.php/SDRAM_Memory_Controller

https://web.archive.org/web/20191020145937/http://hamsterworks.co.nz/mediawiki/index.php/Simple_SDRAM_Controller

https://github.com/alvieboy/ZPUino-HDL/blob/dcache/zpu/hdl/zpuino/boards/papilio-pro/S6LX9/sdram_hamster.vhd

https://github.com/stffrdhrn/sdram-controller



MSX2SD
https://github.com/fbelavenuto/msxsdmapperv2

IDEtoSD:
https://goughlui.com/2019/02/03/tested-generic-sintechi-fc1307a-based-sd-to-ide-adapter-sd35vc0/

My own memory-module:
32 Address
16 Data
MHEN
LHEN
CS1
CS2
CS3
CS4
MEMRD
MEMWR

56 pins

SO-DIMM-144-modules:
64+4+8 = 76 I/O

Look into an address-decoder for interfacing
smaller address-bus memory chips with the CPU.

Priority Encoder is the name of one such.

Note:
The i80386SX uses 72-pin sims for memory-modules.

An example of an encoder/controller for a 386DX:
http://www.s100computers.com/My%20System%20Pages/80386%20Board/80386%20CPU%20Board.htm

Ram-chip suggestion:
CY62167ELL-45ZXIT (2 MB, 20 Address, 16 Data)

IS42S16320D-7BLI (512 MB, 14 Address, 16 Data)

Suggestion for memory controller,
instead of FPGA:
MKE14F512VLL16
(mcu)

Z80380 Evaluation Board

+CMOS 80380 MPU
*18.432 MHz Oscillator
+1 Socketed 48KB EPROM

1 Socketed 128KB (128x8) SRAM

2 Unsocketed 128KB (1 Mb) DRAM Slots

Reset Switch
NMI Switch

Memory-slot suggestions:
G42V12352HR
HSEC8-137-01-L-DV-A

Memory-suggestions:

Modern

IS42S16100H
IS45S16100H

Legacy

MEMORY MAPPING:

- have 512K available for direct addressing in combination with the standard FC/FD/FE/FF ports
- make another port available(which can accept 8bit,16bit, 32bit or even larger page numbers..fed sequentially)
for some sub-switching to a larger memory.
- to unload the processor with moving/clearing/copying one can add something as simple
as a microcontroller to move the memory around.

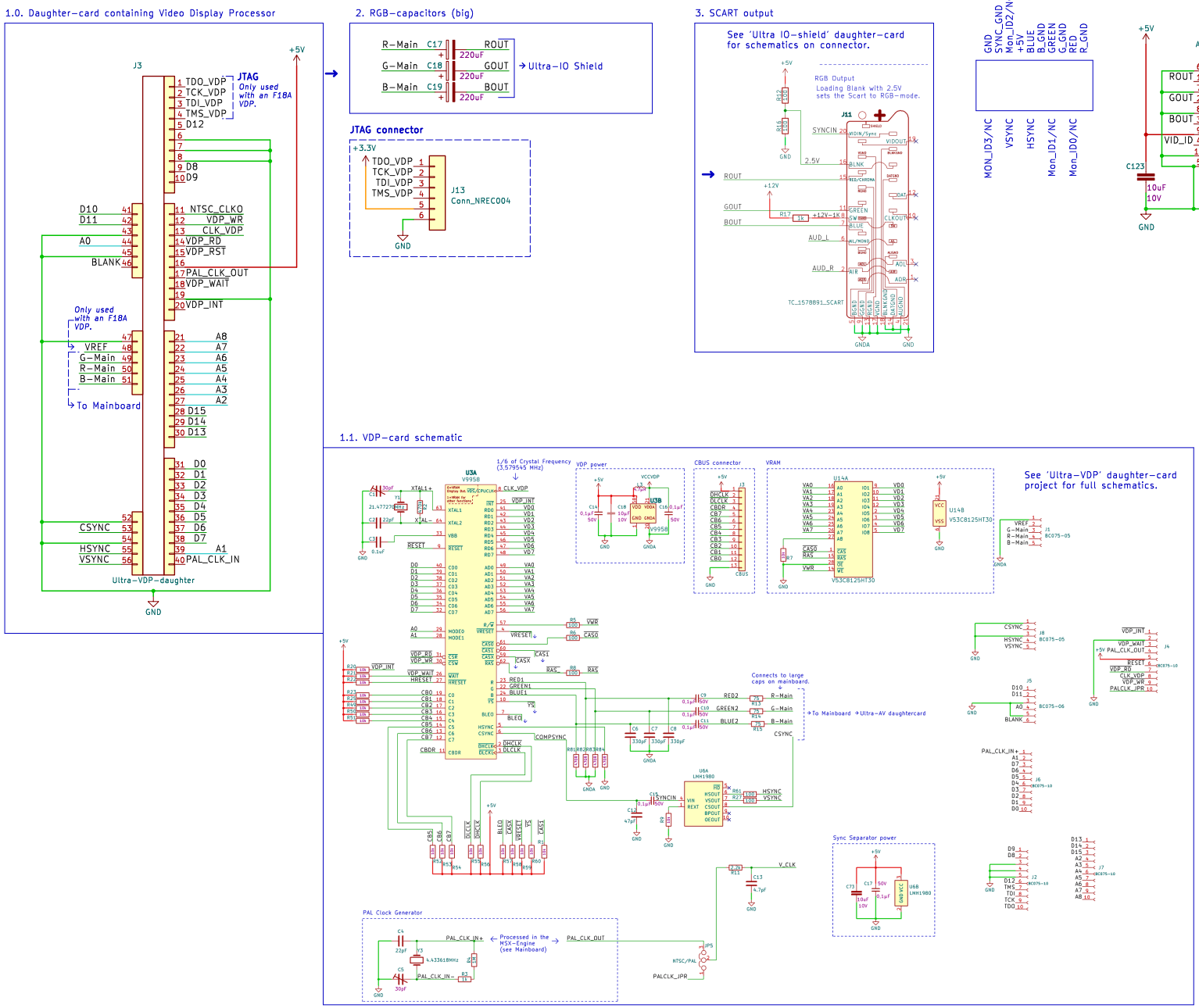
EXTERNAL NETS

A[0..31]
D[0..15]
RAS0 CAS0
DQMB[0..7]
MCLK0 MCLK1
MCKE0 MCKE1
I2C_SCL I2C_SDA
MEM_RD MEM_WR
ROM_CS
MSIZE
UMCS
RAM_CS[0..7]
SD_MOSI/DAT2 SD_DAT3 SD_CMD SD_CLK SD_MISO/DAT0 SD_DAT1 SD_DET_A SD_DET_B

ULTRA-MSX

MEMORY

Size: A3	Date: 2022-06-05	Rev: 5/10	Sheet: A-A
KiCad E.D.A. kicad 7.0.5			File: Ultra-MSX_RAM.kicad_sch



DisplayPort has a mode where it sends raw RGB down the wire, meaning a DP to VGA converter is "just" a DAC and maybe a presence detection EEPROM.

Example-chip:
PTN3356R1BSMP

VGA clocks:

640x400 (70Hz) - 25.175 MHz
640x480 (60Hz) - 25.175 MHz

Pal clocks:

704x576 (50Hz) - 4.43361875 MHz

NTSC clocks:

704x480 (60Hz) - 3.579545 MHz

https://www.msx.org/wiki/SCART_connector#Pinout_.28RGB_and_Composite_Video.29

EXTERNAL NETS

VDP_INT
VDP_WAIT
VDP_RD
VDP_WR
NTSC_CLKO
VDP_RST

Clocks VDP

CLK_VDP
PAL_CLK_IN
PAL_CLK_OUT

Addressing

A[0..31]
A0
A1
A2
A3
A4
A5
A6
A7
A8

Data Bus

D[0..15]
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

Video Signals

ROUT
GOUT
BOUT
CSYNC
HSYNC
VSYNC
BLANK
VID_ID

ULTRA-MSX

ULTRA-MSX

VIDEO

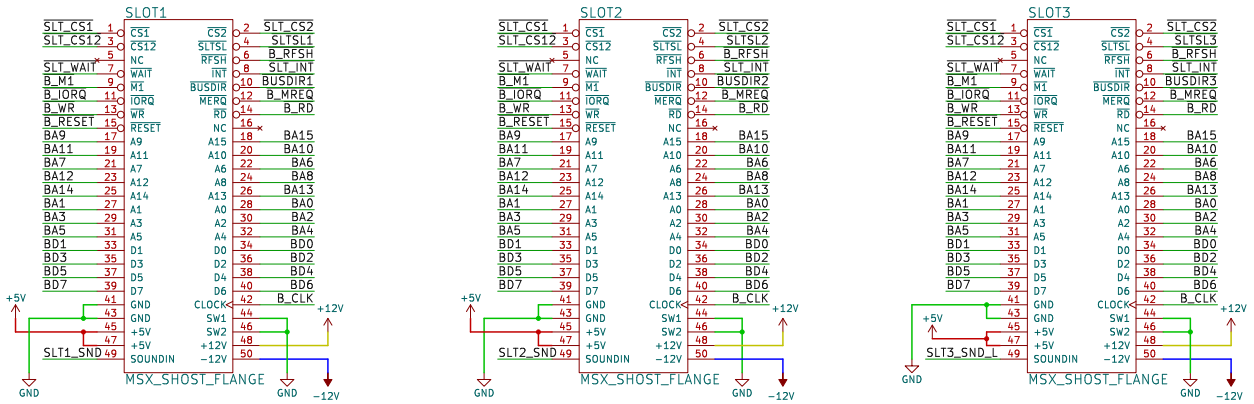
Size: A3	Date: 2022-06-05	Rev: 6/10	Sheet: A-A
KiCad E.D.A. kicad 7.0.5			File: Ultra-MSX_VDP.kicad_sch

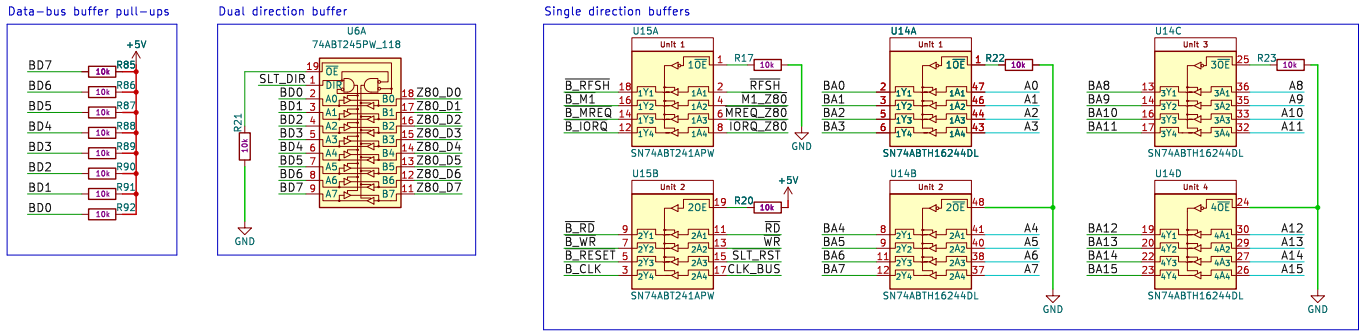
JUMPER

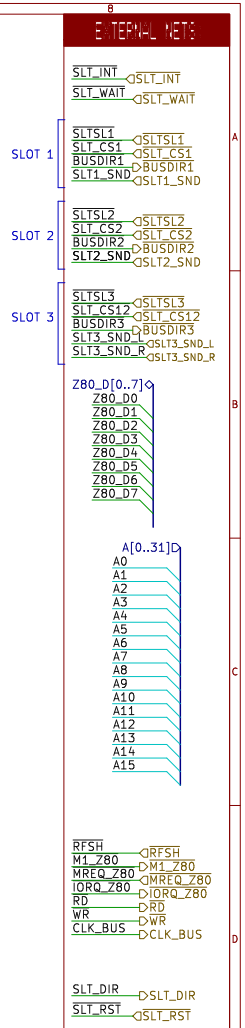
JP3, JP4: 1-2: V9938; 2-3: V9958 (Use a wire link)
JP4, JP5: 1-2: NTSC; 2-3: PAL (Use a wire link)

PAL: R9 - 16k, C91 - 18pF
R9 - Tolerance 1%

PCB Layout Notes:
Keep trace length between AD723 and 75 ohm resistors to minimum
AD723 bypass capacitors: VCC1(12), VREF(14) -> GND1(1), VCC2(19) -> GND2(24)





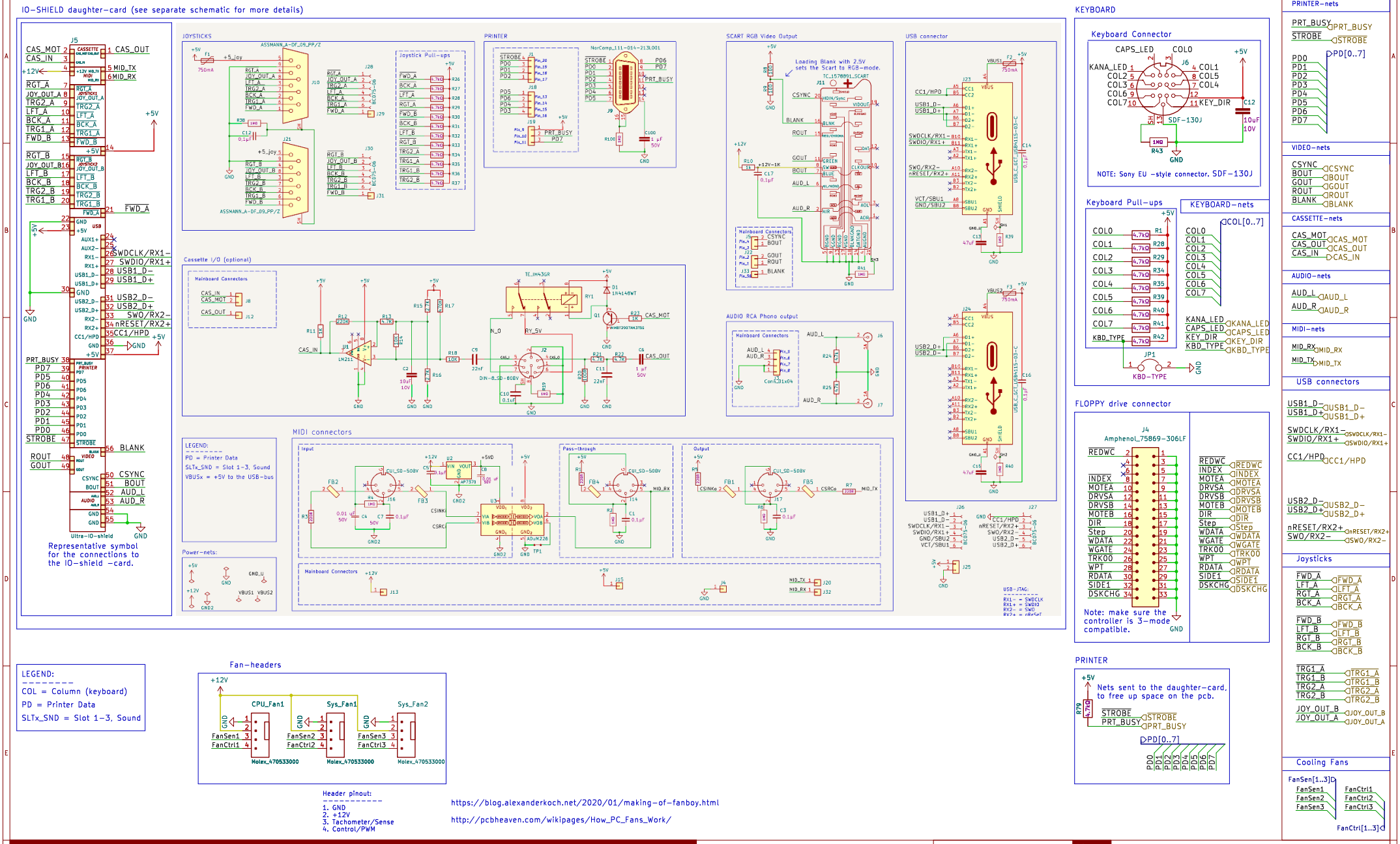


ULTRA-MSX

ULTRA-MSX

SLOTS

Size: A3	Date: 2022-06-05	Rev: 7/10	Rev: A-A
KiCad E.D.A. kicad 7.0.5			File: Ultra-MSX_Slots.kicad_sch



EXTERNAL NETS

PRINTER-nets

PRT_BUSY, STROBE, PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7, PD[0..7]

VIDEO-nets

CSYNC, BOUT, GOUT, ROUT, BLANK

CASSETTE-nets

CAS_MOT, CAS_OUT, CAS_IN

AUDIO-nets

AUD_L, AUD_R

MIDI-nets

MID_RX, MID_TX

USB connectors

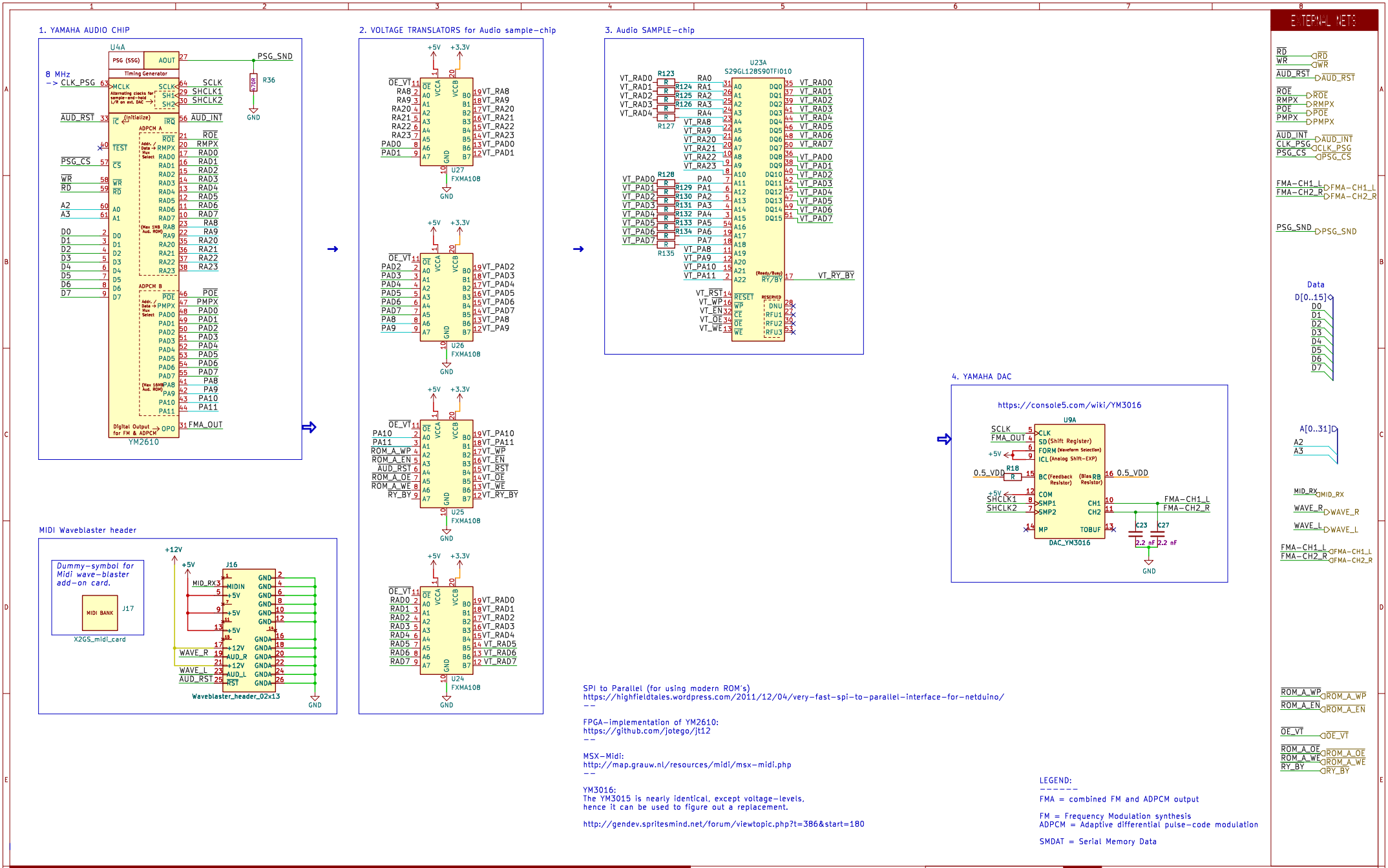
USB1_D-, USB1_D+, SWDCLK/RX1-, SWDIO/RX1+, CC1/HPD, USB2_D-, USB2_D+, nRESET/RX2+, SWO/RX2-

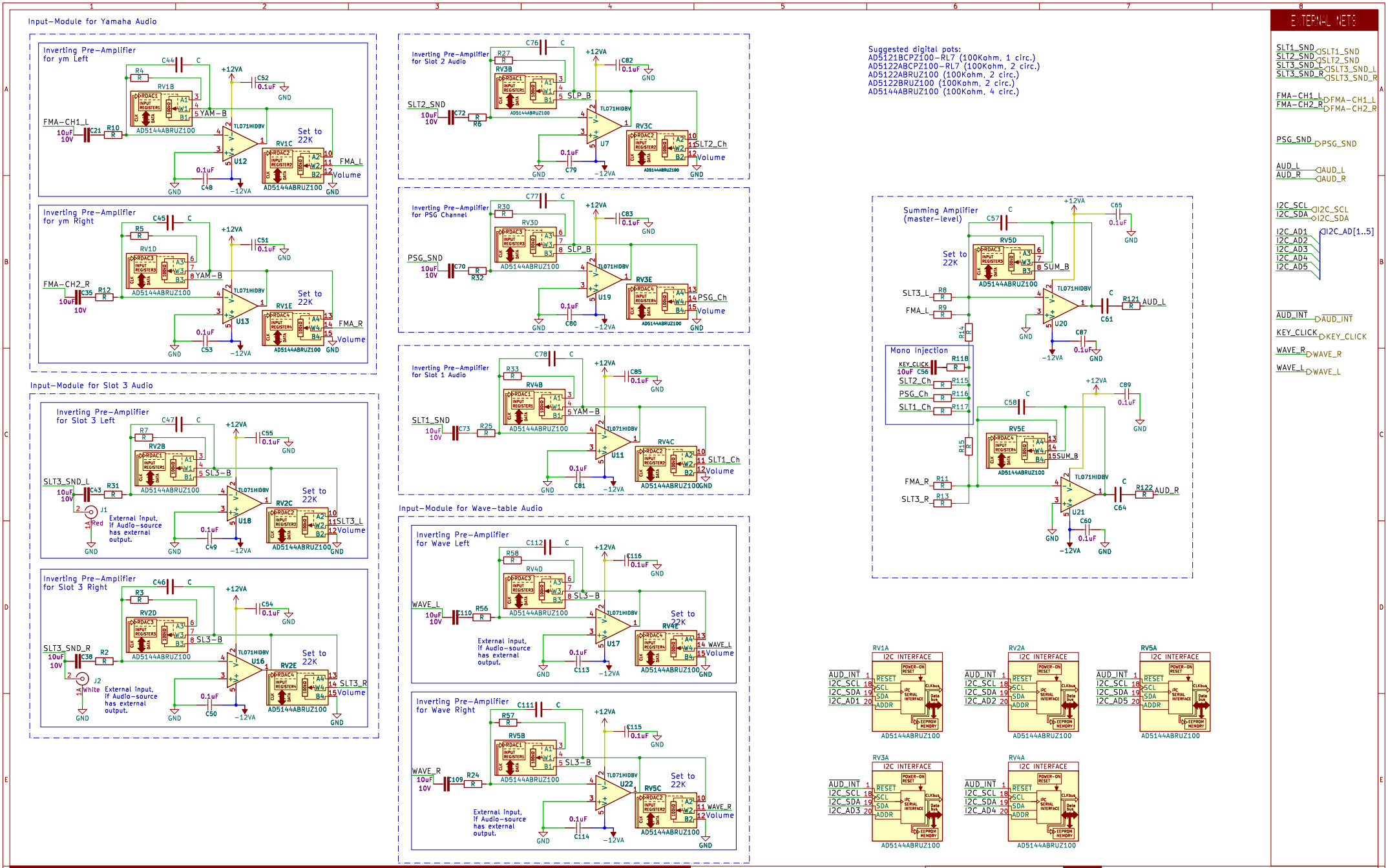
Joysticks

FWD_A, LFT_A, RGT_A, BCK_A, FWD_B, LFT_B, RGT_B, BCK_B, TRG1_A, TRG1_B, TRG2_A, TRG2_B, JOY_OUT_B, JOY_OUT_A

Cooling Fans

FanSen[1..3], FanSen1, FanSen2, FanSen3, FanCtrl1, FanCtrl2, FanCtrl3, FanCtrl[1..3]


1. YAMAHA AUDIO CHIP
U4A
YM2610
8 MHz
CLK_PSG
PSG (SSG)
AOUT
PSG_SND
R36
Timing Generator
ADPCM A
ADPCM B
AUD_RST
PSG_CS
WR
RD
A2
A3
D0
D1
D2
D3
D4
D5
D6
D7
SCLK
SHCLK1
SHCLK2
AUD_INT
ROE
RMPX
RAD0
RAD1
RAD2
RAD3
RAD4
RAD5
RAD6
RAD7
RA8
RA9
RA20
RA21
RA22
RA23
POE
PMPX
PAD0
PAD1
PAD2
PAD3
PAD4
PAD5
PAD6
PAD7
PA8
PA9
PA10
PA11
FMA_OUT
GND
2. VOLTAGE TRANSLATORS for Audio sample-chip
U27
U26
U25
U24
FXMA108
+5V
+3.3V
3. Audio SAMPLE-chip
U23A
S29GL128S90TFI010
VT_RAD0
VT_RAD1
VT_RAD2
VT_RAD3
VT_RAD4
VT_PAD0
VT_PAD1
VT_PAD2
VT_PAD3
VT_PAD4
VT_PAD5
VT_PAD6
VT_PAD7
VT_RY_BY
VT_RST
VT_WP
VT_EN
VT_OE
VT_WE
4. YAMAHA DAC
https://console5.com/wiki/YM3016
U9A
DAC_YM3016
SCLK
FMA_OUT
0.5_VDD
SHCLK1
SHCLK2
FMA-CH1_L
FMA-CH2_R
MID_RX
WAVE_R
WAVE_L
MIDI Waveblaster header
Dummy-symbol for Midi wave-blaster add-on card.
MIDI BANK
J17
X2GS_midi_card
J16
Waveblaster_header_02x13
+12V
AUD_R
AUD_L
RST
SPI to Parallel (for using modern ROM's)
https://highfieldtales.wordpress.com/2011/12/04/very-fast-spi-to-parallel-interface-for-netduino/
FPGA-implementation of YM2610:
https://github.com/jotego/jt12
MSX-Midi:
http://map.grauw.nl/resources/midi/msx-midi.php
YM3016:
The YM3015 is nearly identical, except voltage-levels,
hence it can be used to figure out a replacement.
http://gendev.spritesmind.net/forum/viewtopic.php?t=386&start=180
LEGEND:
FMA = combined FM and ADPCM output
FM = Frequency Modulation synthesis
ADPCM = Adaptive differential pulse-code modulation
SMDAT = Serial Memory Data
EXTERNAL NETS
Data
D[0..15]
A[0..31]
ROM_A_WP
ROM_A_EN
OE_VT
ROM_A_OE
ROM_A_WE
RY_BY
ULTRA-MSX
AUDIO
A-A
A3
2022-06-05
9/10
Ultra-MSX_Audio.kicad_sch
KiCad E.D.A. kicad 7.0.5
Slew Rate = 2* Pi * Freq_max * Vpeak
2* 3.14159 * 25000 * 48 = 7539822.368616 V/s
=> 7.54 V/uS


Input-Module for Yamaha Audio
Inverting Pre-Amplifier for ym Left
Inverting Pre-Amplifier for ym Right
Input-Module for Slot 3 Audio
Inverting Pre-Amplifier for Slot 3 Left
Inverting Pre-Amplifier for Slot 3 Right
Inverting Pre-Amplifier for Slot 2 Audio
Inverting Pre-Amplifier for PSG Channel
Inverting Pre-Amplifier for Slot 1 Audio
Input-Module for Wave-table Audio
Inverting Pre-Amplifier for Wave Left
Inverting Pre-Amplifier for Wave Right
External input, if Audio-source has external output.
Set to 22K
Suggested digital pots:
AD5121BCPZ100-RL7 (100Kohm, 1 circ.)
AD5122ABCPZ100-RL7 (100Kohm, 2 circ.)
AD5122ABRUZ100 (100Kohm, 2 circ.)
AD5122BRUZ100 (100Kohm, 2 circ.)
AD5144ABRUZ100 (100Kohm, 4 circ.)
Summing Amplifier (master-level)
Mono Injection
EXTERNAL NETS
ULTRA-MSX
AUDIO AMPLIFIERS
Ultra-MSX
A-A
A3
2022-06-05
10/10
Ultra-Amplifier.kicad_sch
KiCad E.D.A. kicad 7.0.5