AT40K05, AT40K10, AT40K20, AT40K40

5K – 50K Gates Coprocessor FPGA with FreeRAM™

DATASHEET

Features

- Ultra high performance
  - System speeds to 100MHz
  - Array multipliers > 50MHz
  - 10ns flexible SRAM
  - Internal tri-state capability in each cell
- FreeRAM™
  - Flexible, single/dual port, synchronous/asynchronous 10ns SRAM
  - 2,048 – 18,432 bits of distributed SRAM independent of logic cells
- 128 – 384 PCI compliant I/Os
  - 5V capability
  - Programmable output drive
  - Fast, flexible array access facilitates pin locking
  - Pin-compatible with XC4000 and XC5200 FPGAs
- Eight global clocks
  - Fast, low skew clock distribution
  - Programmable rising/falling edge transitions
  - Distributed clock shutdown capability for low power management
  - Global reset/asynchronous reset options
  - 4 additional dedicated PCI clocks
- Cache Logic® dynamic full/partial re-configurability in-system
  - Unlimited re-programmability via serial or parallel modes
  - Enables adaptive designs
  - Enables fast vector multiplier updates
- Pin-compatible package options
  - Thin, Plastic Quad Flat Packs (LQFP and PQFP)
- User-friendly design tools
  - Timing driven placement and routing
  - Automatic/Interactive multi-chip partitioning
  - Fast, efficient synthesis
  - Over 75 automatic component generators create 1000s of reusable, Fully Deterministic Logic and RAM functions
- Intellectual property cores
  - Fir Filters, UARTs, PCI, FFT, and other system level functions
- Supply voltage 5V for AT40K

Table 1. AT40K Series Family[1]

Device	AT40K05	AT40K10	AT40K20	AT40K40
Usable Gates	5K – 10K	10K – 20K	20K – 30K	40K – 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256[1]	576[1]	1,024[1]	2,304[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have eight less registers.

1. Description

The AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual-port/single-port SRAM, eight global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 5V designs for AT40K.

The AT40K is designed to quickly implement high-performance, large gate count designs through the use of synthesis, and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic.

The AT40K can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution, and other multimedia applications.

1.1 Fast, Flexible and Efficient SRAM

The AT40K FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

1.2 Fast, Efficient Array, and Vector Multipliers

The AT40K's patented 8-sided core cell with direct horizontal, vertical, and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K/AT40KLV's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

1.3 Cache Logic Design

The AT40K, AT6000, and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K can act as a reconfigurable coprocessor.

1.4 Automatic Component Generators

The AT40K FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs, speed, and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40K series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 2,304 registers. Pin locations are consistent throughout the AT40K series for easy design migration in the same package footprint. The AT40K series FPGAs utilize a reliable 0.6µ single-poly, CMOS process, and are 100% factory-tested. Atmel's PC-based Integrated Development System (IDS) is used to create AT40K series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

2. The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 2-1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2-2. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM(1), with either synchronous or asynchronous operation.

Note: 1. The right-most column can only be used as single-port RAM.

Figure 2-1. Symmetrical Array Surrounded by I/O (AT40K20)

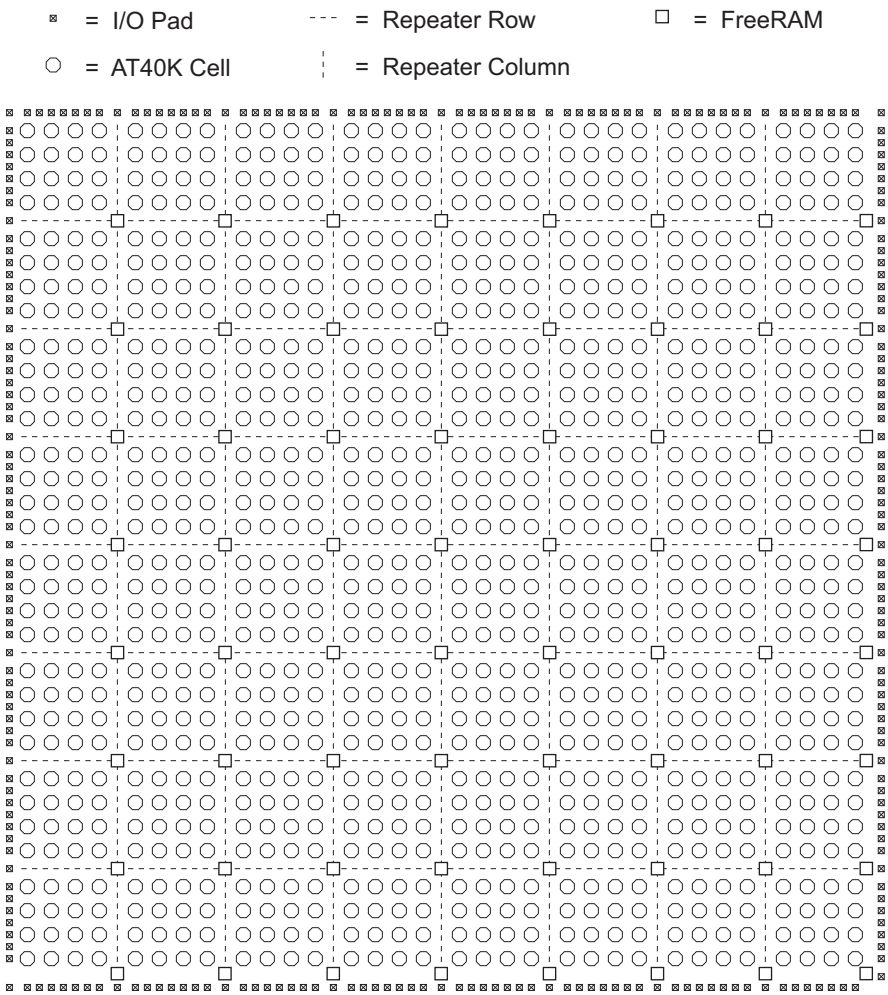
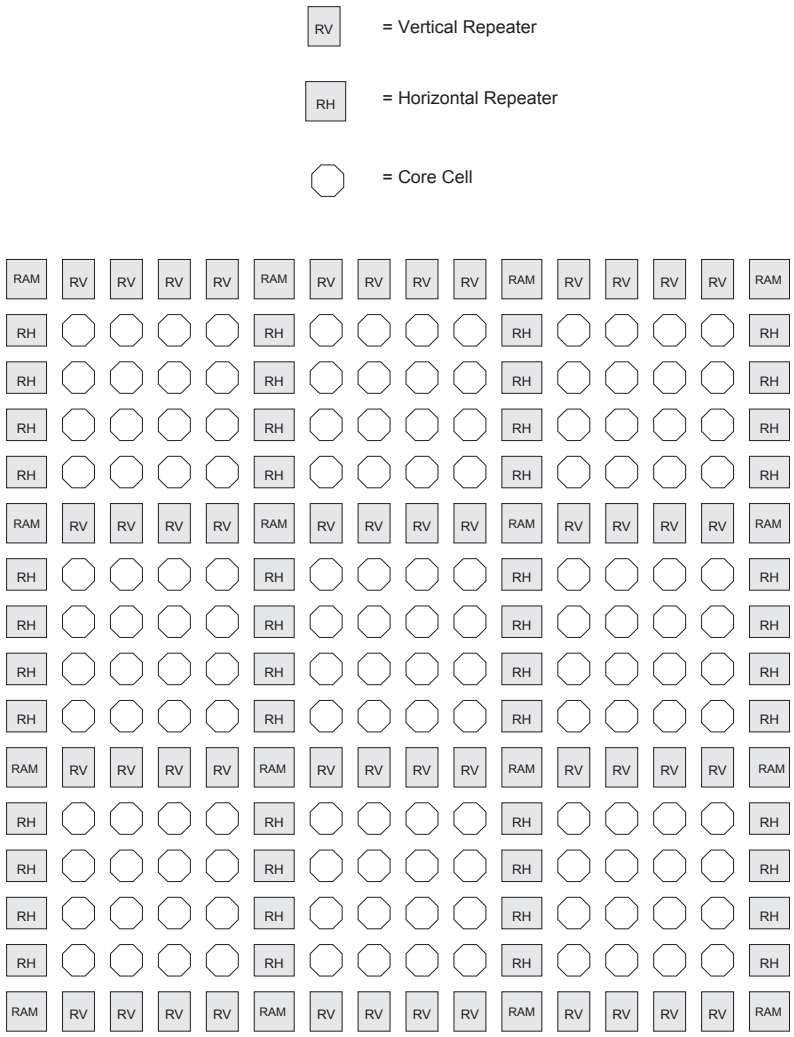


Figure 2-2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the Integrated Development System (IDS) tool.

3. The Busing Network

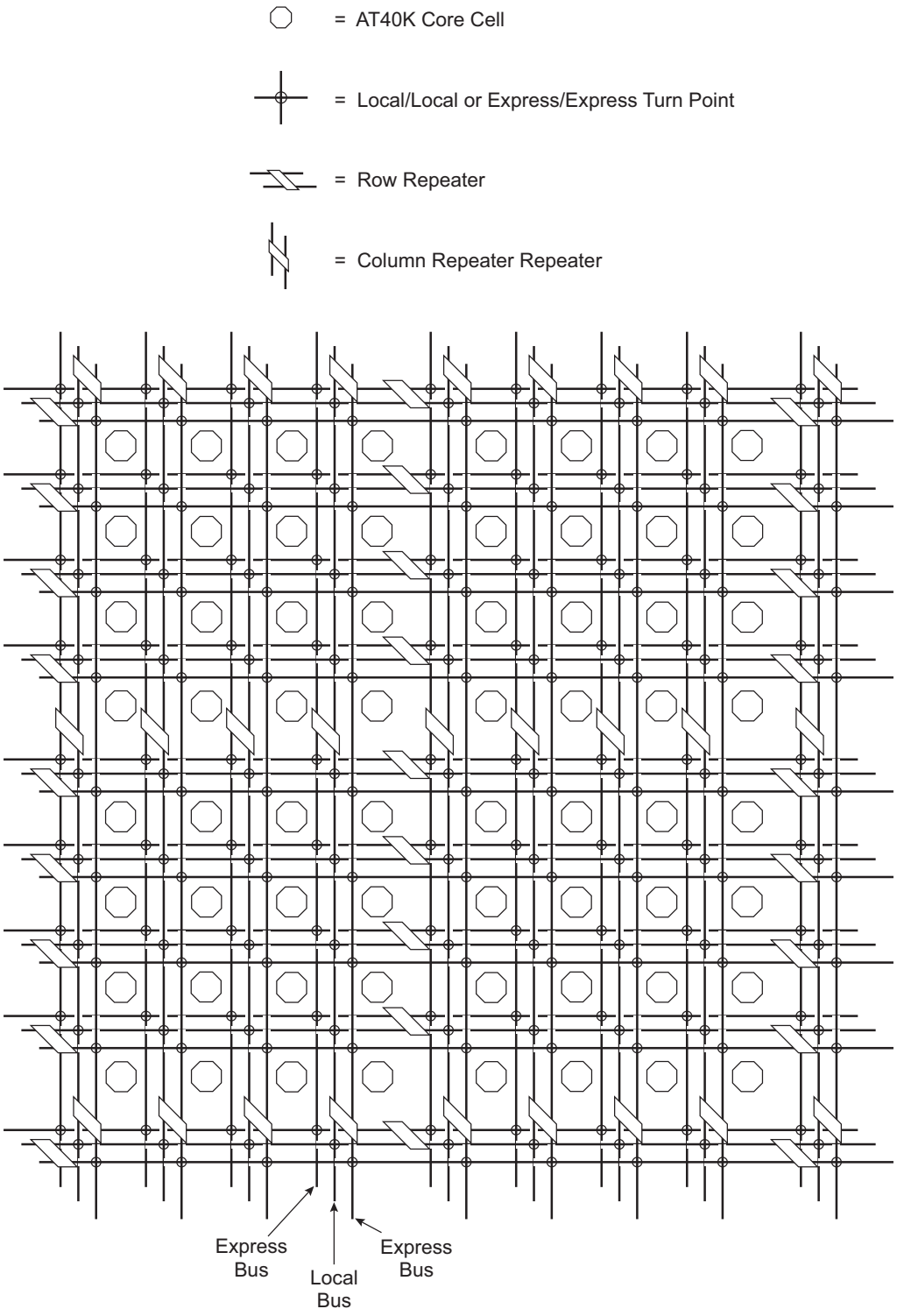
Figure 3-1 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40K are used as a dual-function resources. Table 3-1 shows which buses are used in a dual-function mode and which bus plane is used. The AT40K software tools are designed to accommodate dual-function buses in an efficient manner.

Table 3-1. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge. Bus in first column to left of RAM block.
RAM Write Enable	Express	1	Vertical	Bus full length at array edge. Bus in first column to left of RAM block.
RAM Address	Express	1 – 5	Vertical	Buses full length at array edge. Buses in second column to left of RAM block.
RAM Data In	Local	1	Horizontal	Data In connects to local. Bus Plane 1.
RAM Data Out	Local	2	Horizontal	Data out connects to local. Bus Plane 2.
Clocking	Express	4	Vertical	Bus half length at array edge.
Set/Reset	Express	5	Vertical	Bus half length at array edge.

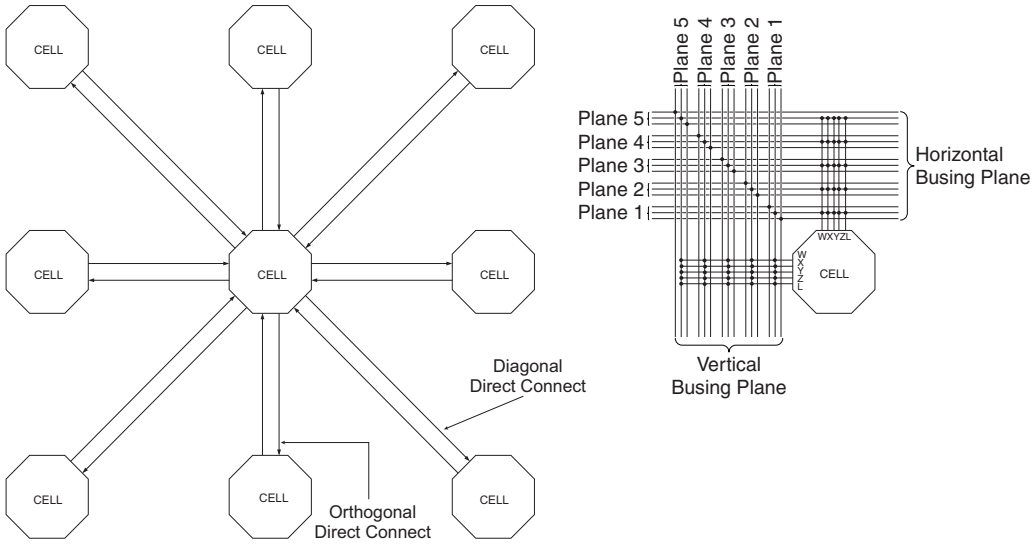
Figure 3-1. Busing Plane (One of Five)



4. Cell Connections

Figure 4-1(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4-1(b) shows the connections between a cell and five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4-1. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

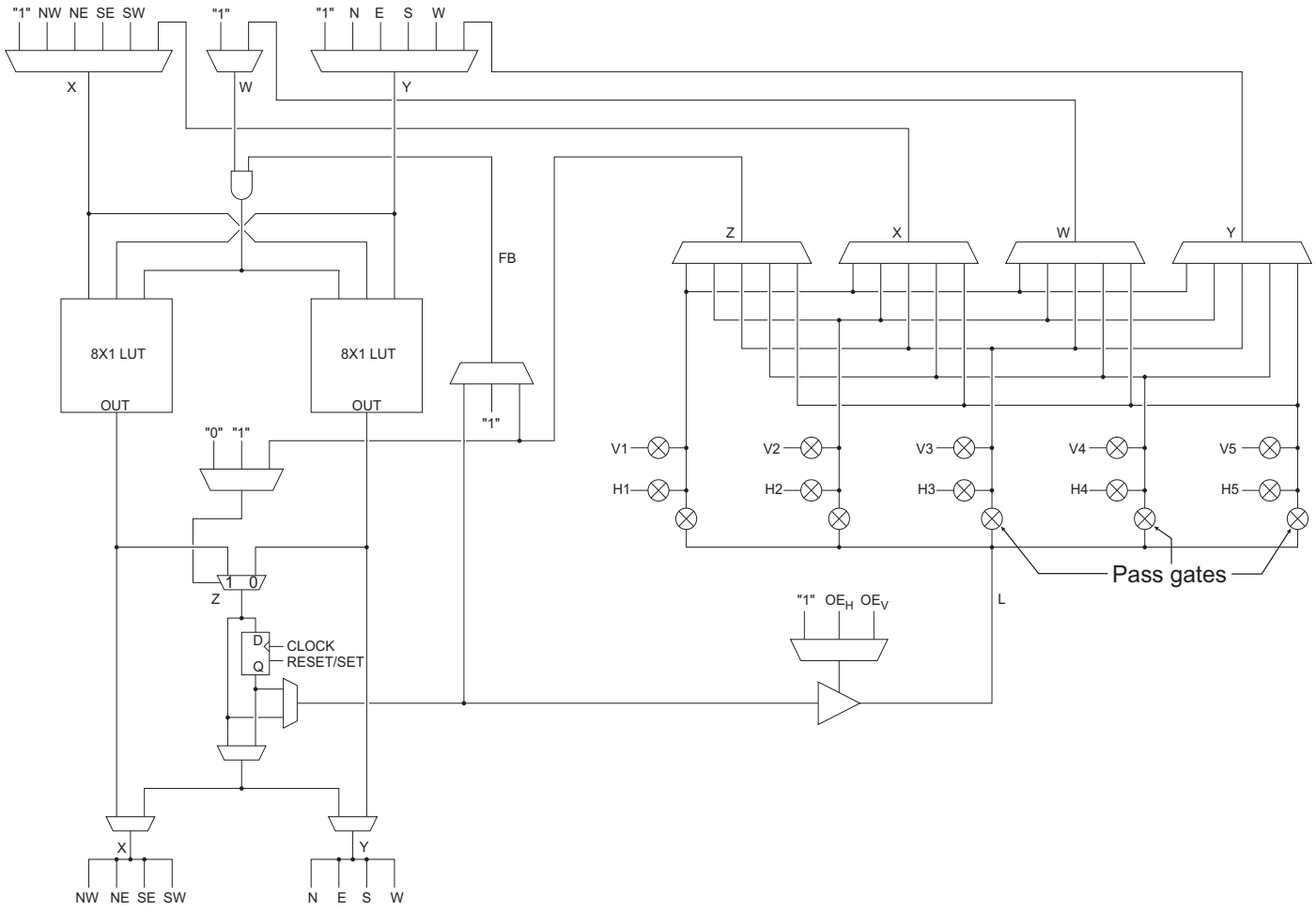
5. The Cell

Figure 5-1 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 – V_5) is connected to the vertical local bus in plane n. H_n (H_1 – H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40K FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of three inputs or one function of four inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

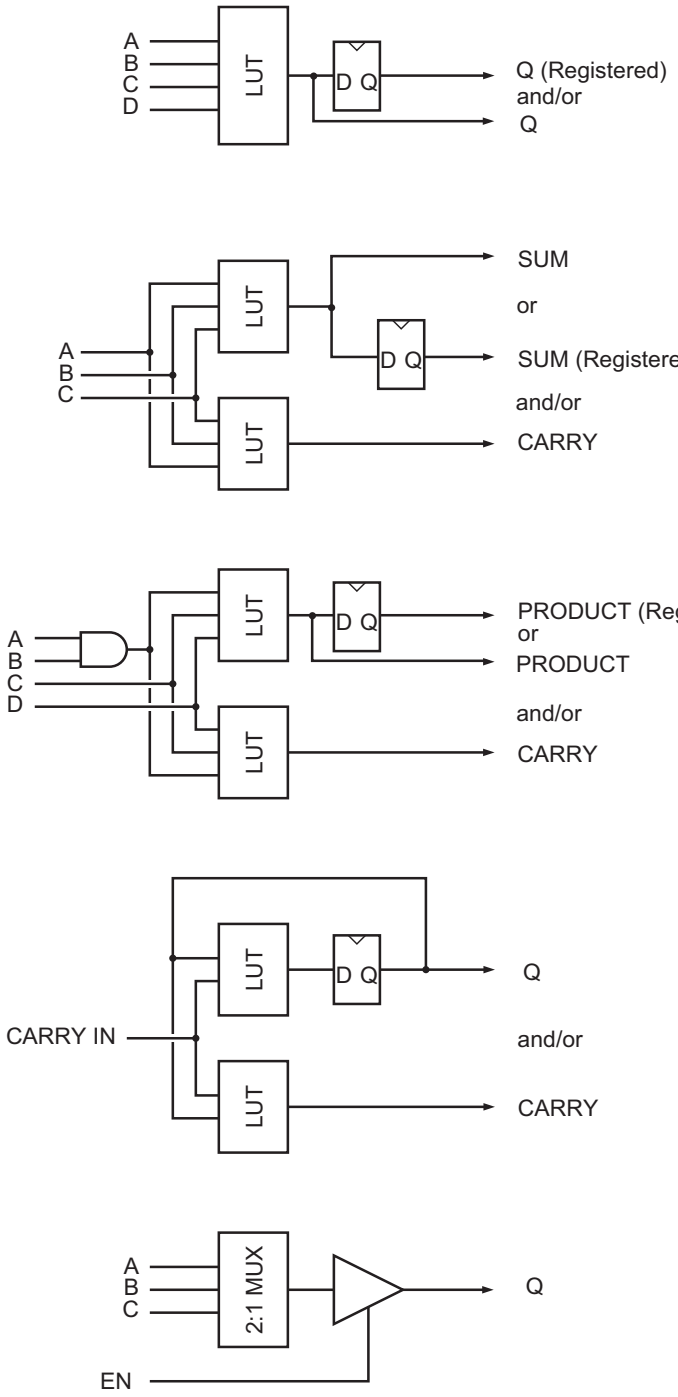
With this functionality in each core cell, the core cell can be configured in several modes. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas, see Figure 5-2.

Figure 5-1. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 5-2. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40K core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K architecture.

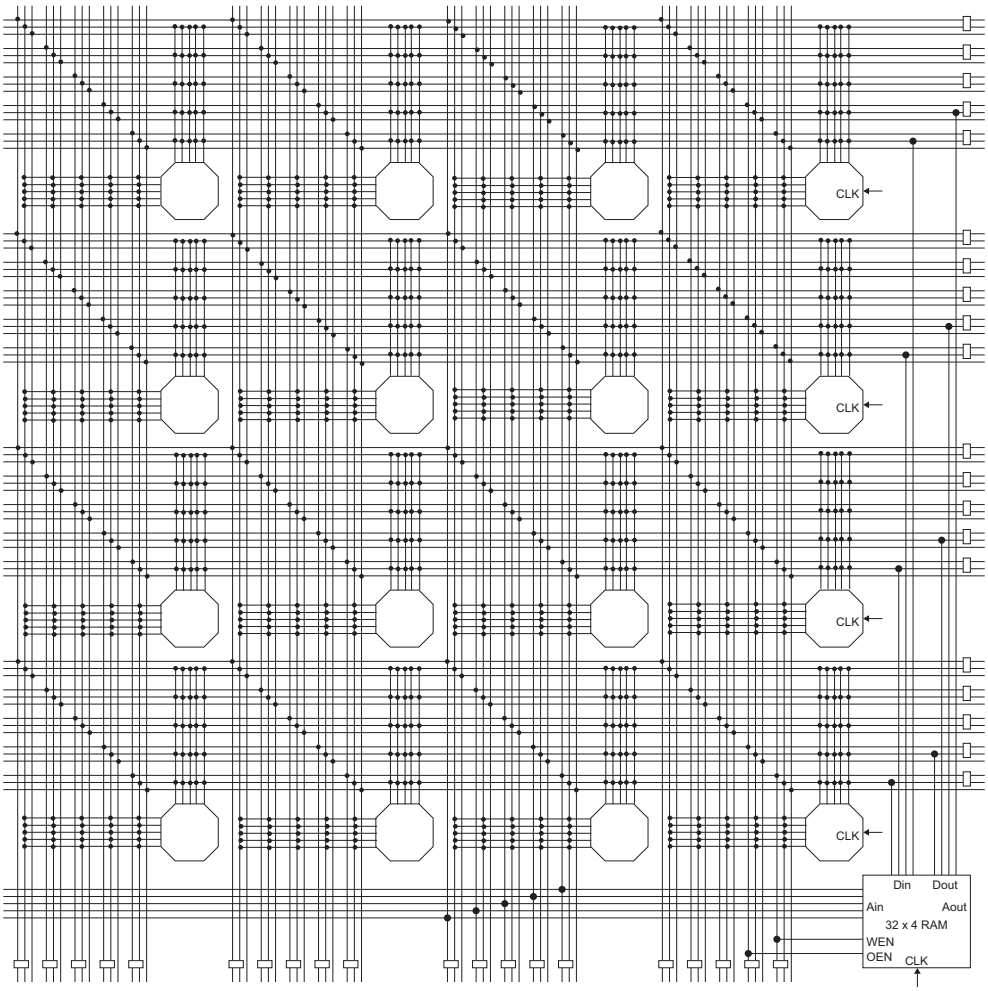
Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

6. RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 6-1. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (Plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sectors in the same column. A 5-bit Output Address Bus connects to five vertical express buses in the same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 6-1. RAM Connections (One Ram Block)



Reading and writing of the 10ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is Logic 1, data flows through; when Load is Logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is Logic 1 and $\overline{\text{WE}}$ is Logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is Logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select “1” (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the “*AT40K Configuration Series”* application note at www.atmel.com).

Figure 6-2. RAM Logic

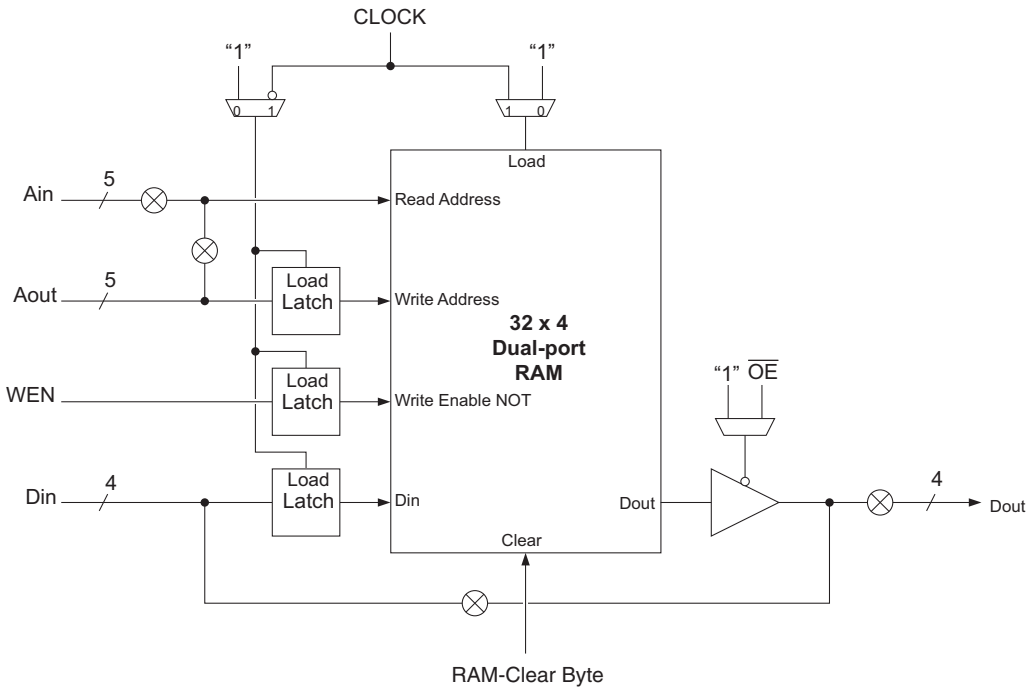
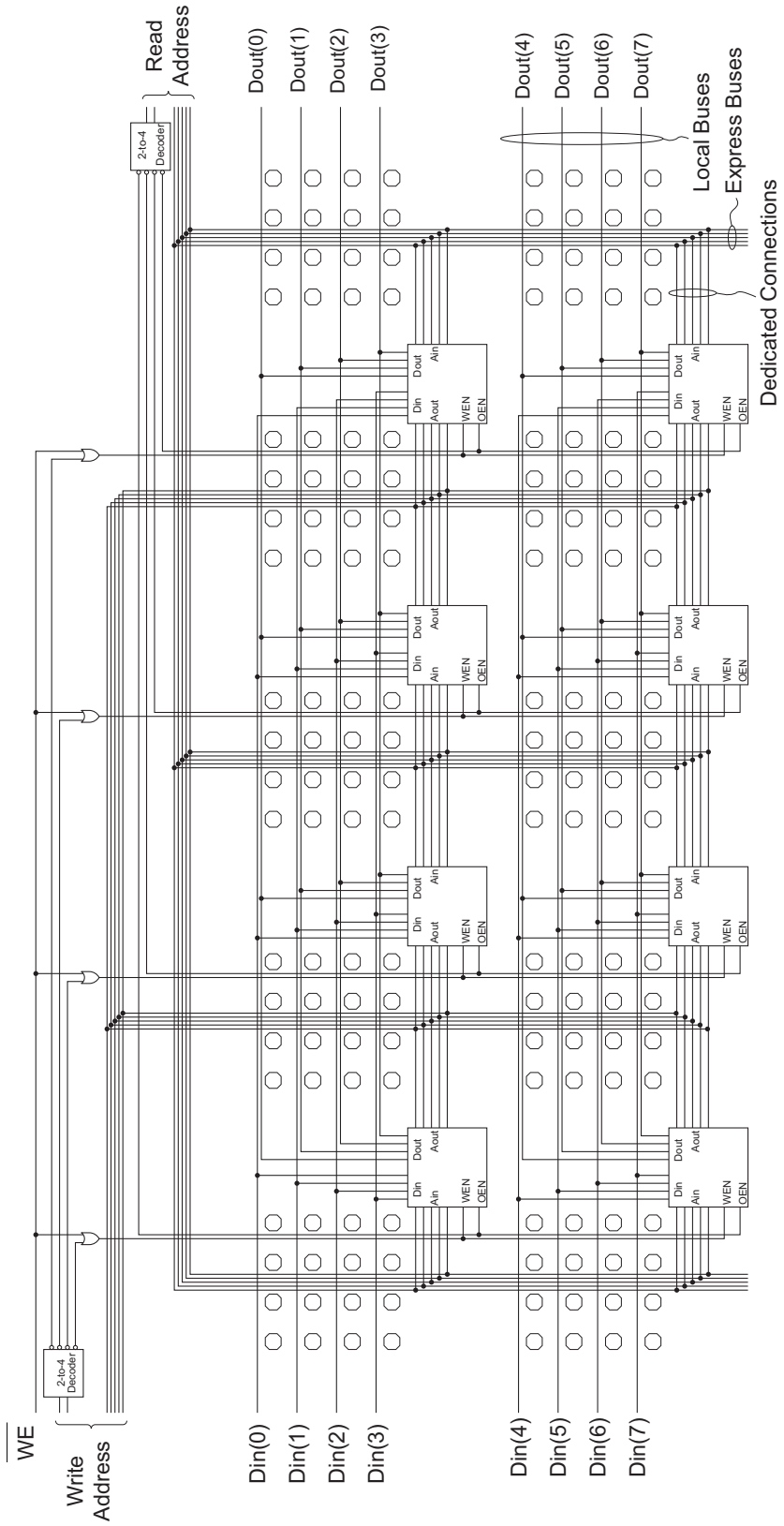


Figure 6-3 shows an example of a RAM macro constructed using the AT40K's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 6-3. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



7. Clocking Scheme

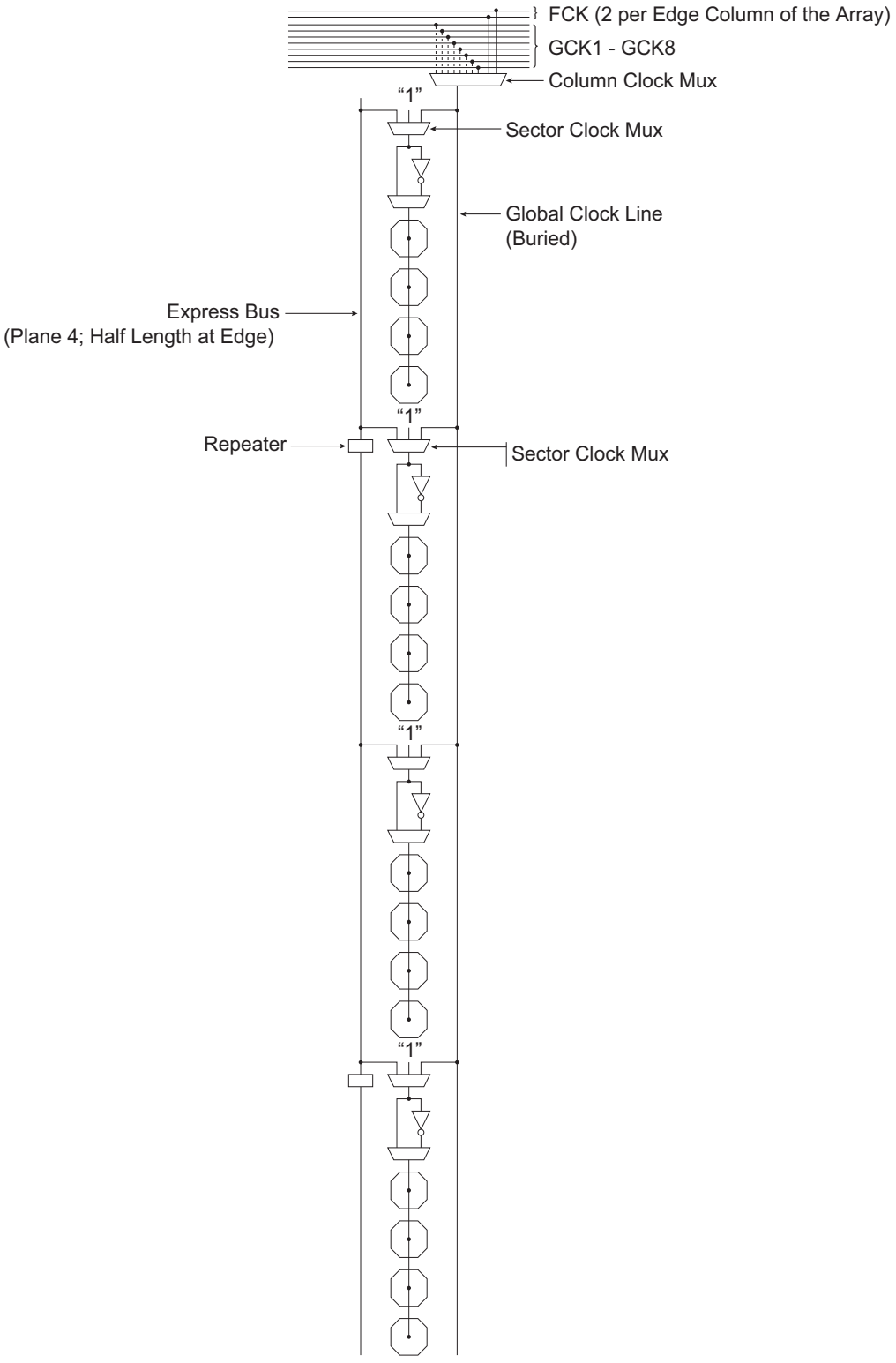
There are eight Global Clock buses (GCK1 – GCK8) on the AT40K FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 – FCK4), two per edge column of the array for PCI specification.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 7-1. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 7-1. Clocking (for One Column of Cells)



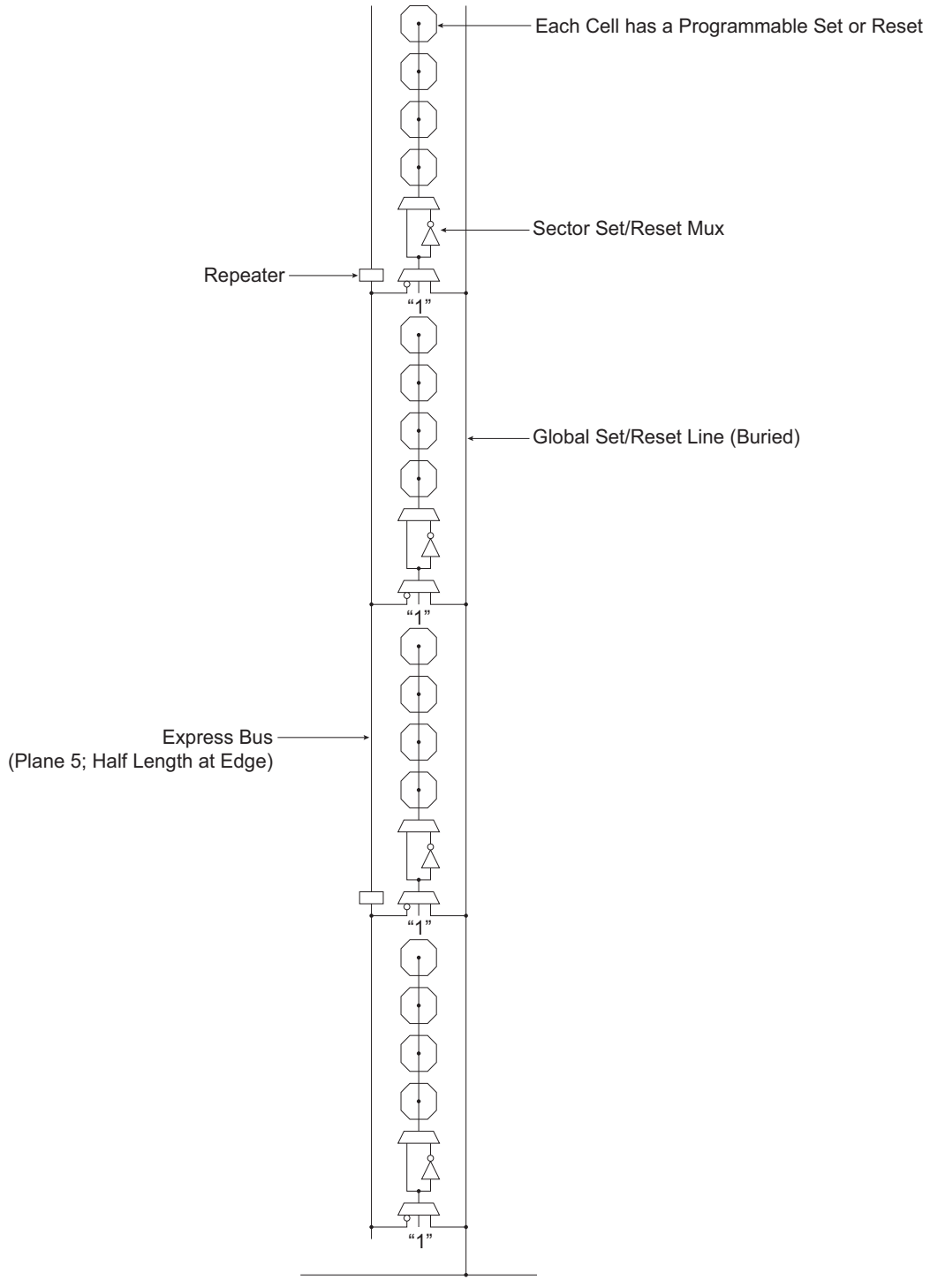
8. Set/Reset Scheme

The AT40K family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 8-1. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (Logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a Logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 8-1. Set/Reset (for One Column of Cells)



9. I/O Structure

9.1 PAD

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

9.2 PULL-UP/PULL-DOWN

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak “1” or “0” level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

9.3 TTL/CMOS

The threshold level can be set to either TTL/CMOS-compatible levels.

9.4 SCHMITT

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

9.5 DELAYS

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

9.6 DRIVE

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (20mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (14mA at 5V) buffer, while SLOW yields a standard (6mA at 5V) buffer.

9.7 TRI-STATE

The output of each I/O can be made tri-state (0, 1, or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O’s Source Selection mux. Of course, the output can be normal (0 or 1), as well.

9.8 SOURCE SELECTION MUX

The Source Selection mux selects the source for the output signal of an I/O, see Figure 9-1.

9.9 Primary, Secondary, and Corner I/Os

The AT40K has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40K has access to one Primary I/O and two Secondary I/Os.

9.10 Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 9-1 and Figure 9-2.

9.11 Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 9-1 and Figure 9-2.

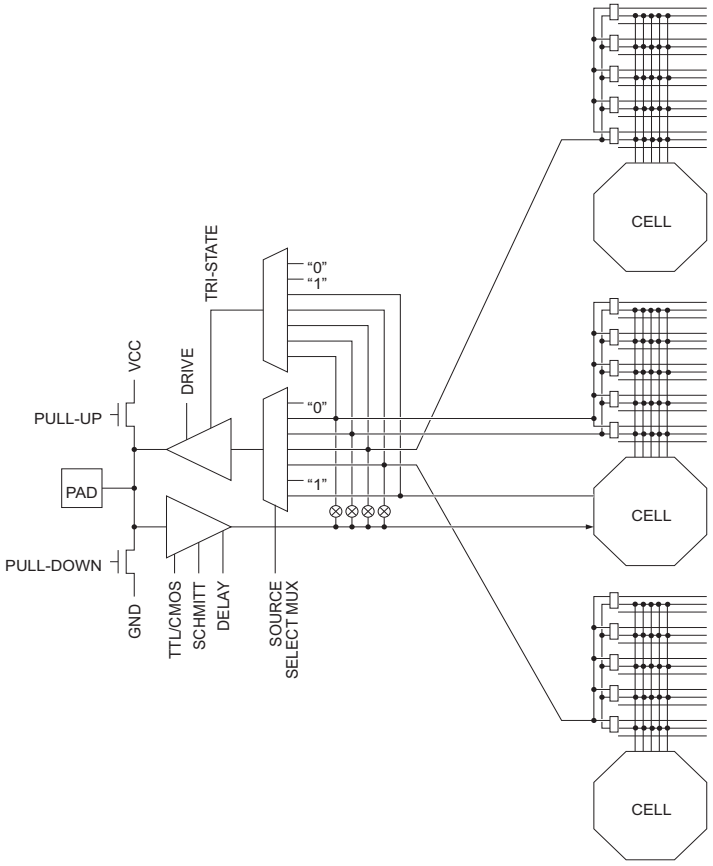
9.12 Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os:

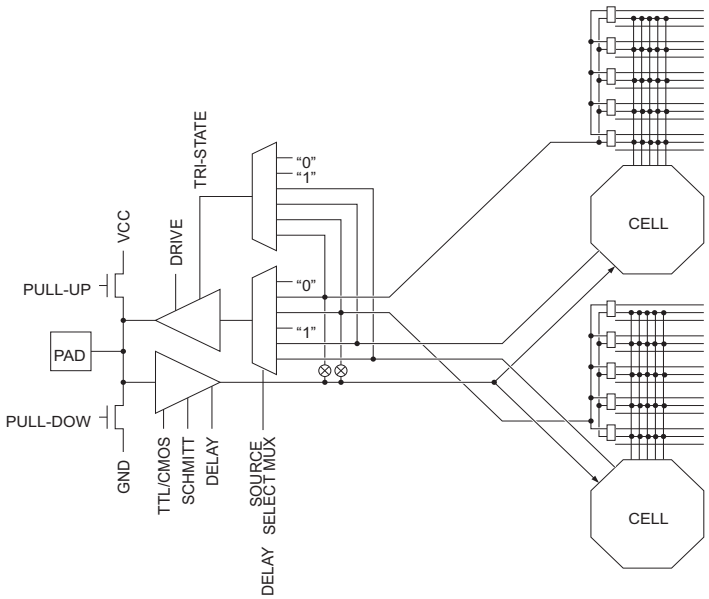
- Two Primary
- Two Secondary
- One Corner I/O

Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40K FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 9-3.

Figure 9-1. West I/O (Mirrored for East I/O) AT40K

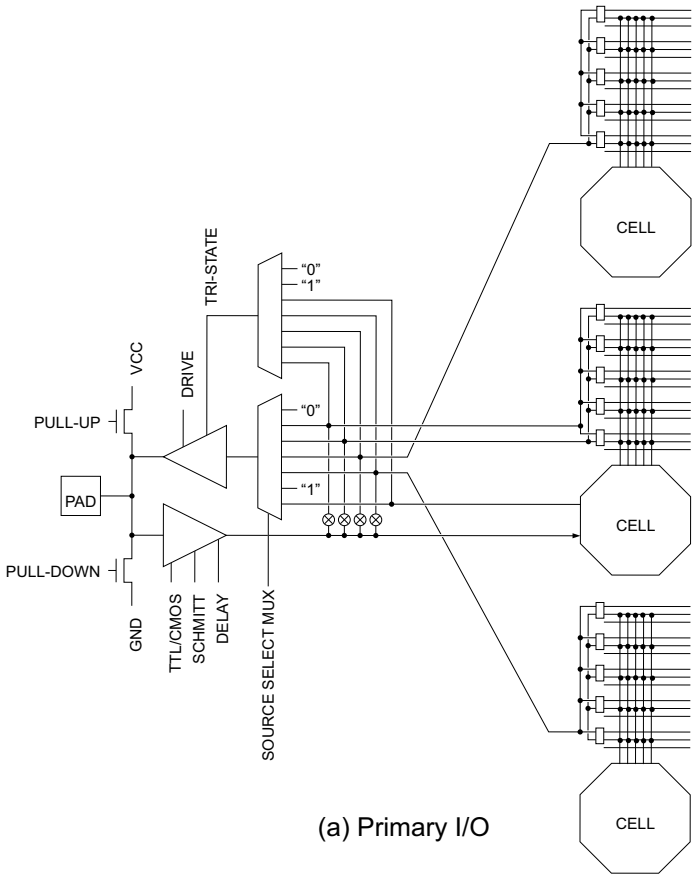


(a) Primary I/O

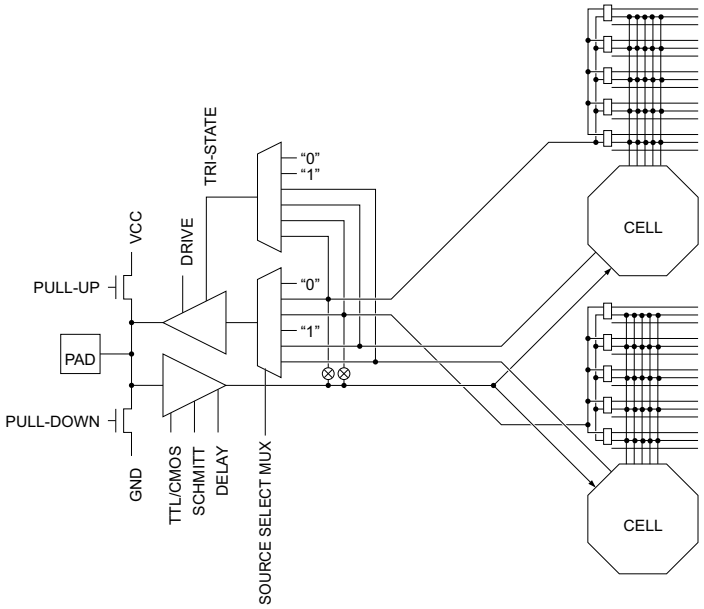


(b) Secondary I/O

Figure 9-2. South I/O (Mirrored for North I/O) AT40K

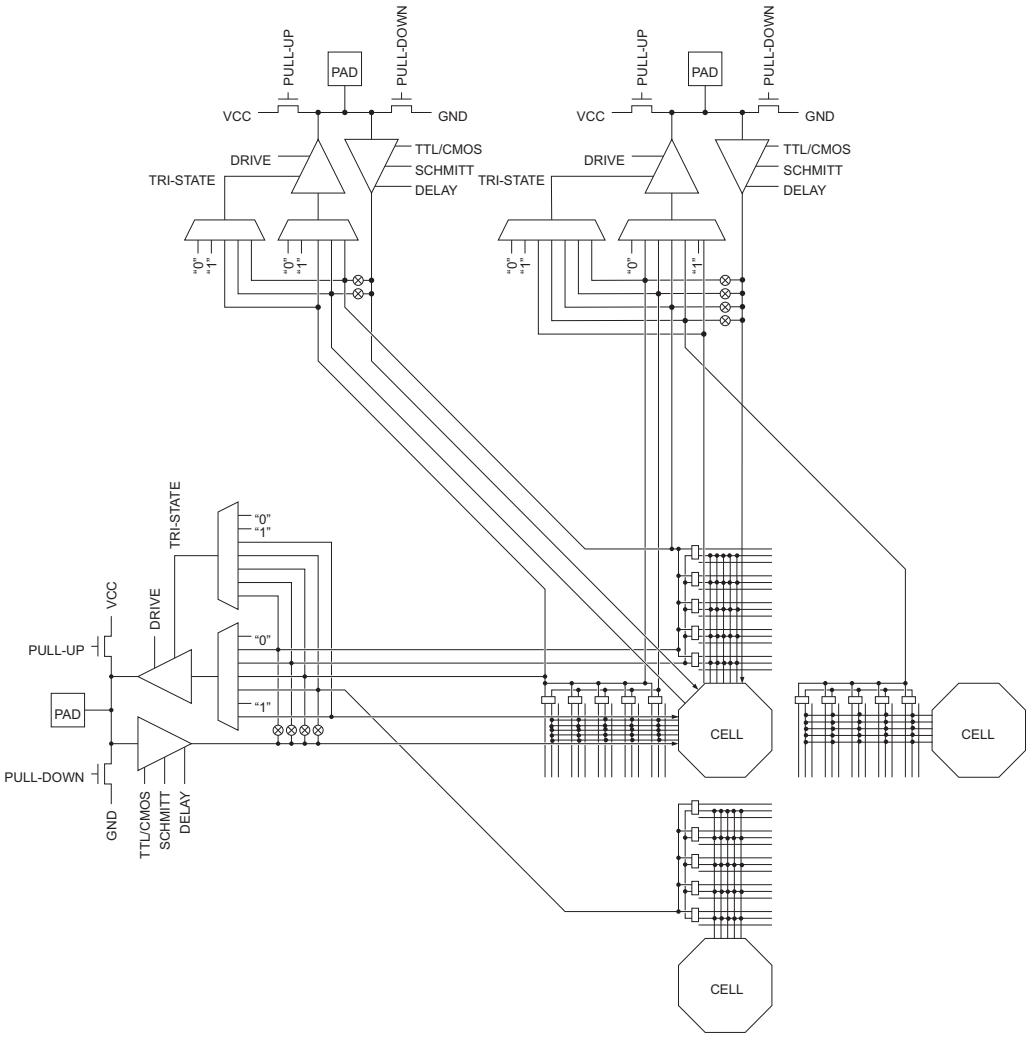


(a) Primary I/O



(a) Secondary I/O

Figure 9-3. Northwest Corner (Similar for NE/SE/SW Corners) AT40K



10. Electrical Specifications

10.1 Absolute Maximum Ratings — 5V Commercial/Industrial* AT40K

Operating Temperature	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} 7.0V
Supply Voltage (V_{CC})	-0.5V to 7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100pF)	2000V

*Notice: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

10.2 DC and AC Operating Range — 5V Operation AT40K

		Commercial -2	Industrial -2	Military -2
Operating Temperature (Case)		0°C to 70°C	-40°C to 85°C	-55°C to 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V to V_{CC}	2.0V to V_{CC}	2.0V to V_{CC}
	Low (V_{ILT})	0V to 0.8V	0V to 0.8V	0V to 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% to 100% V_{CC}	70% to 100% V_{CC}	70% to 100% V_{CC}
	Low (V_{ILC})	0 to 30% V_{CC}	0 to 30% V_{CC}	0 to 30% V_{CC}

10.3 DC Characteristics — 5V Operation Commercial/Industrial/Military AT40K

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 14mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 20mA Commercial = 4.75V Industrial/Military = 4.5V	Ind. = 3.15 4.0 Con = 3.325			V
V_{OL}	Low-level Output Voltage	I_{OL} = -6mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -14mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -20mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	CON = -1mA to -250µA	-250.0	CON = -1mA to -250µA	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC}			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS} Maximum	-10.0			µA
		With pull-up, V_{IN} = V_{SS} Maximum	-500.0	-250.0	-125.0	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

10.4 AC Timing Characteristics — 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y → x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z → x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w → x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z → x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y → y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x → y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y → x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x → x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w → y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w → x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z → y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z → x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q → x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R → x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S → x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q → w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y → L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe → L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe → L	1.8	ns	

10.5 AC Timing Characteristics — 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.
All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L → E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E → E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L → L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E → L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E → IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L → IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad → x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad → x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad → x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad → x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L → pad	5.9	ns	50pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L → pad	4.8	ns	50pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L → pad	3.9	ns	50pf load
Output, Slow	t_{PZX} (Maximum)	oe → pad	6.2	ns	50pf load
Output, Slow	t_{PXZ} (Maximum)	oe → pad	1.3	ns	50pf load
Output, Medium	t_{PZX} (Maximum)	oe → pad	4.8	ns	50pf load
Output, Medium	t_{PXZ} (Maximum)	oe → pad	1.9	ns	50pf load
Output, Fast	t_{PZX} (Maximum)	oe → pad	3.7	ns	50pf load
Output, Fast	t_{PXZ} (Maximum)	oe → pad	1.6	ns	50pf load

10.6 AC Timing Characteristics — 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.
Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-2	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad → clock pad → clock pad → clock pad → clock	AT40K05 AT40K10 AT40K20 AT40K40	1.1 1.2 1.2 1.4	ns ns ns ns	Rising edge clock
FCLK Input Buffer	t_{PD} (Maximum)	pad → clock pad → clock pad → clock pad → clock	AT40K05 AT40K10 AT40K20 AT40K40	0.7 0.8 0.8 0.8	ns ns ns ns	Rising edge clock
Clock Column Driver	t_{PD} (Maximum)	clock → colclk clock → colclk clock → colclk clock → colclk	AT40K05 AT40K10 AT40K20 AT40K40	0.8 0.9 1.0 1.1	ns ns ns ns	Rising edge clock
Clock Sector Driver	t_{PD} (Maximum)	colclk → secclk colclk → secclk colclk → secclk colclk → secclk	AT40K05 AT40K10 AT40K20 AT40K40	0.5 0.5 0.5 0.5	ns ns ns ns	Rising edge clock
GSRN Input Buffer	t_{PD} (Maximum)	pad → GSRN pad → GSRN pad → GSRN pad → GSRN	AT40K05 AT40K10 AT40K20 AT40K40	3.0 3.7 4.3 5.6	ns ns ns ns	From any pad to Global Set/Reset network
Global Clock to Output	t_{PD} (Maximum)	clock pad → out clock pad → out clock pad → out clock pad → out	AT40K05 AT40K10 AT40K20 AT40K40	8.3 8.4 8.6 8.8	ns ns ns ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20mA output buffer 50pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad → out clock pad → out clock pad → out clock pad → out	AT40K05 AT40K10 AT40K20 AT40K40	7.9 8.0 8.1 8.3	ns ns ns ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20mA output buffer 50pf pin load

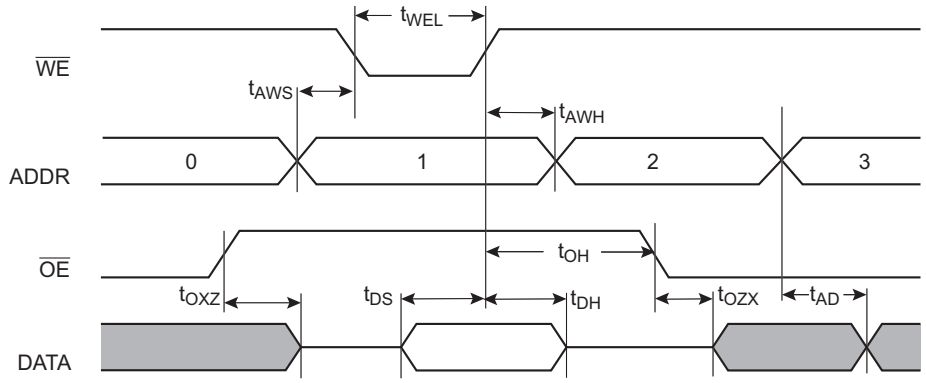
10.7 AC Timing Characteristics — 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

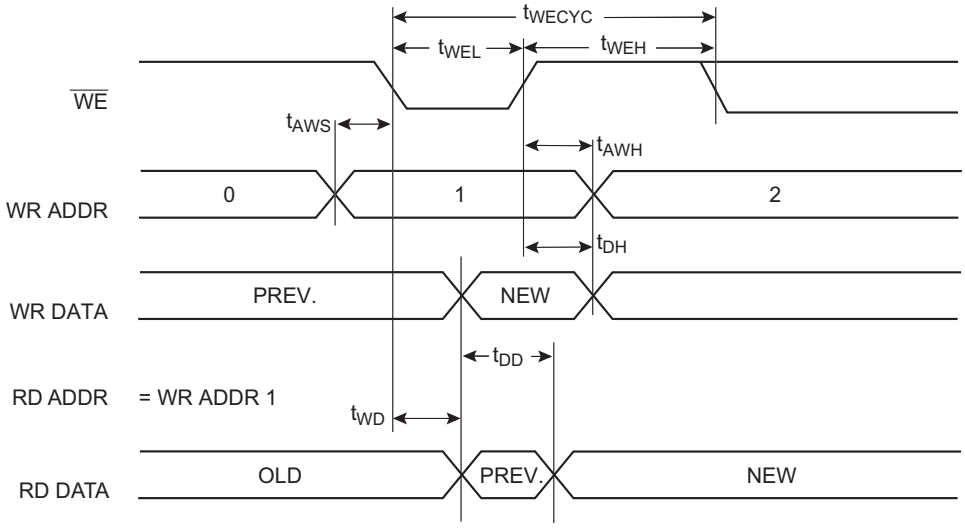
Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	8.0	ns	
Write	t_{WEL} (Minimum)	we	3.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	3.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup → we	2.0	ns	
Write	t_{AWH} (Minimum)	wr addr hold → we	0.0	ns	
Write	t_{DS} (Minimum)	din setup → we	2.0	ns	
Write	t_{DH} (Minimum)	din hold → we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din → dout	4.6	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr → dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe → dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe → dout	2.0	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	8.0	ns	
Write	t_{CLKL} (Minimum)	clk	3.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	3.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup → clk	2.0	ns	
Write	t_{WCH} (Minimum)	we hold → clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup → clk	2.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold → clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup → clk	2.0	ns	
Write	t_{DCH} (Minimum)	wr data hold → clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk → dout	3.5	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr → dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe → dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe → dout	2.0	ns	

11. FreeRAM Asynchronous Timing Characteristics

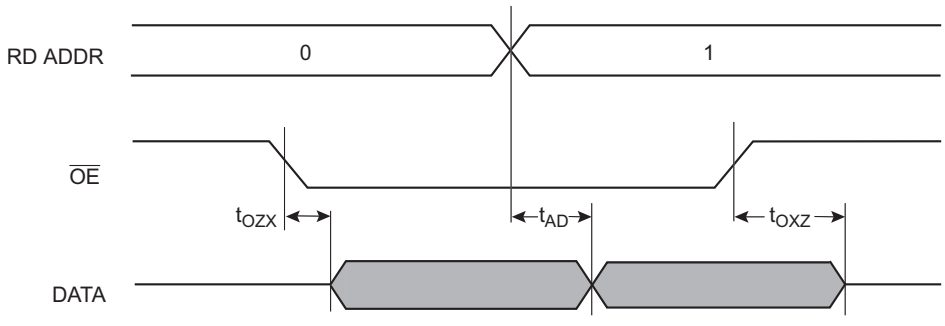
11.1 Single-port Write/Read



11.2 Dual-port Write with Read

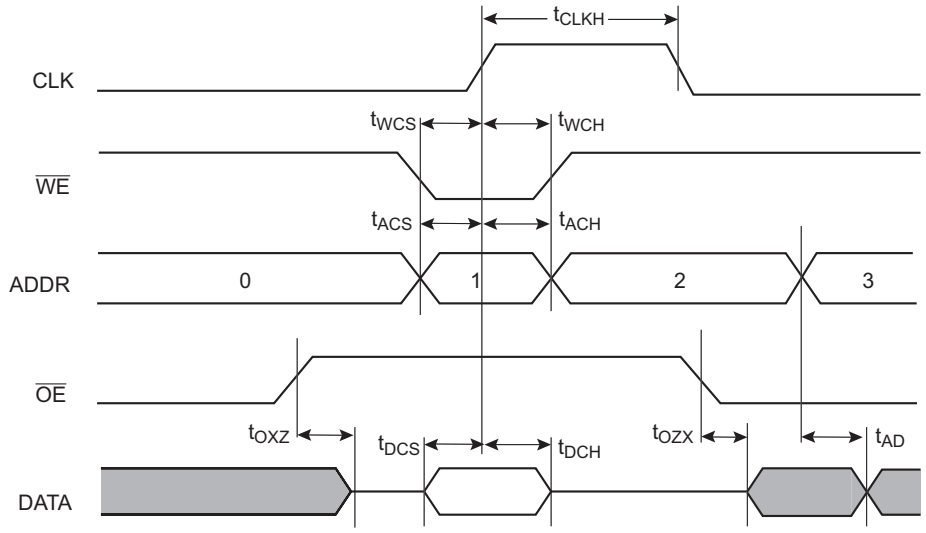


11.3 Dual-port Read

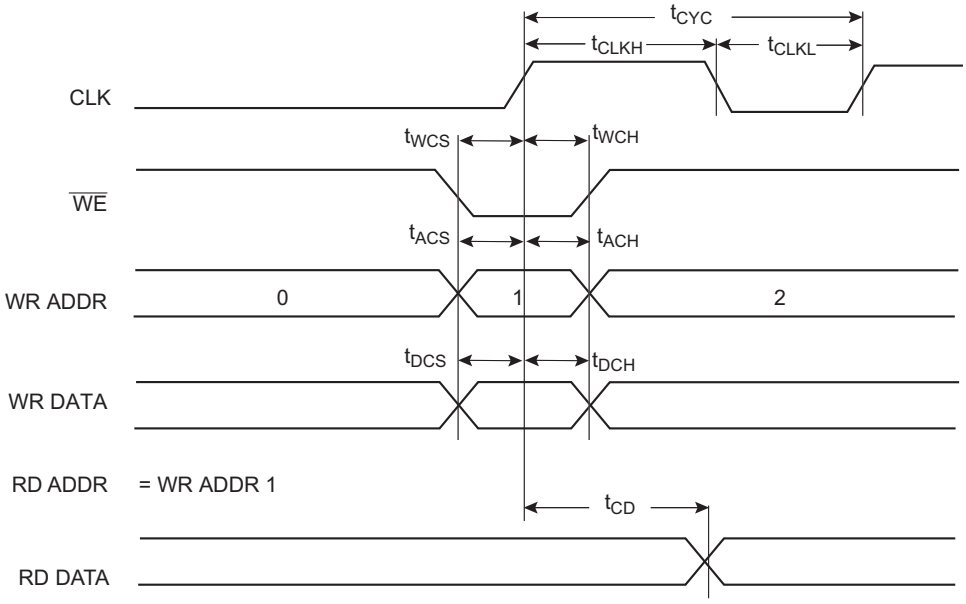


12. FreeRAM Synchronous Timing Characteristics

12.1 Single-port Write/Read



12.2 Dual-port Write with Read



12.3 Dual-port Read

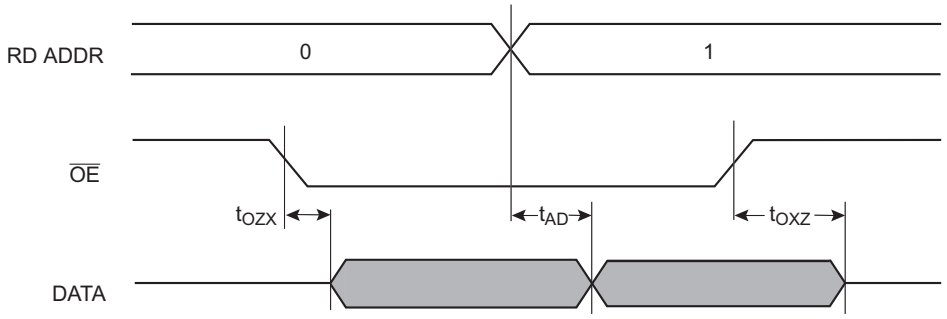


Table 12-1. Left Side (Top to Bottom)

AT40K20 256 I/O	304 PQFP[2]
GND	304
I/O1, GCK1 (A16)	303
I/O2 (A17)	302
I/O3	301
I/O4	300
I/O5 (A18)	299
I/O6 (A19)	298
I/O7	297
I/O8	296
VCC	
GND	
I/O9	295
I/O10	294
I/O11	293
I/O12	292
I/O13	291
I/O14	290
I/O15	289
I/O16	288

Notes:
1. Pads labeled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K20 256 I/O	304 PQFP[2]
GND	287
I/O17, FCK1	286
I/O18	285
I/O19 (A20)	284
I/O20 (A21)	283
VCC	282
I/O21	280
I/O22	279
I/O23	278
I/O24	277
GND	
I/O25	276
I/O26	275
I/O27	274
I/O28	273
I/O29	272
I/O30	271
I/O31 (A22)	270

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connection to any specific package pin.

2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K20 256 I/O	304 PQFP[2]
I/O32 (A23)	269
GND	268
VCC	267
I/O33	266
I/O34	265
I/O35	264
I/O36	263
I/O37	262
I/O38	261
I/O39	260
I/O40	259
GND	
I/O41	258
I/O42	257
I/O43	256
I/O44	255
VCC	253
I/O45	252
I/O46	251
I/O47	250

eled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have nc connection to any specific package pin.

2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K20 256 I/O	304 PQFP[2]
I/O48, FCK2	249
GND	248
I/O49	247
I/O50	246
I/O51	245
I/O52	244
I/O53	243
I/O54	242
I/O55	241
I/O56	240
GND	
VCC	
I/O57	239
I/O58	238
I/O59	237
I/O60	236
I/O61	235
I/O62	234
I/O63 ($\overline{OTS}$)[3]	233
I/O64, GCK2	232

eled GND or y have n
connection to any specific package pin.

2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K20 256 I/O	304 PQFP[2]
M1	231
GND	230
M0	229

eled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have nc
on to any specific package pin.

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ri-state.

de (Left to Right)

AT40K20 256 I/O	304 PQFP[1]
VCC	228
M2	227
I/O65, GCK3	226
I/O66 (HDC)	225
I/O67	224
I/O68	223
I/O69	222
I/O70 (LDC)	221
I/O71	220
I/O72	219
VCC	
GND	
I/O73	218
I/O74	217
I/O75	216

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-2. Bottom Side (Left to Right) (Continued)

AT40K20 256 I/O	304 PQFP[1]
I/O76	215
I/O77	
I/O78	
I/O79	214
I/O80	213
	212
	211
GND	210
I/O81	209
I/O82	208
I/O83	207
I/O84	206
VCC	204
I/O85	203
I/O86	202
I/O87	201
I/O88	200
GND	
I/O89	199
I/O90	198
I/O91	197
I/O92	196
I/O93	195
I/O94	194

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-2. Bottom Side (Left to Right) (Continued)

AT40K20 256 I/O	304 PQFP[1]
I/O95 (D15)	193
I/O96 (INIT)	192
VCC	191
GND	190
I/O97 (D14)	189
I/O98 (D13)	188
I/O99	187
I/O100	186
I/O101	185
I/O102	184
I/O103	183
I/O104	182
GND	
I/O105	181
I/O106	180

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-2. Bottom Side (Left to Right) (Continued)

AT40K20 256 I/O	304 PQFP[1]
I/O107	179
I/O108	178
VCC	177
I/O109 (D12)	175
I/O110 (D11)	174
I/O111	173
I/O112	172
GND	171
I/O113	170
I/O114	169
I/O115	168
I/O116	167
I/O117	166
I/O118	165
I/O119	164
I/O120	163
GND	
VCC	
I/O121	162
I/O122	161
I/O123 (D10)	160
I/O124 (D9)	159

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-2. Bottom Side (Left to Right) (Continued)

AT40K20 256 I/O	304 PQFP(1)
I/O125	158
I/O126	157
I/O127 (D8)	156
I/O128, GCK4	155
GND	154
$\overline{CON}$	153

eled GND or VCC are internally bonded to Ground or VCC planes within the package.
e no direct connection to any specific package pin.
age has an inverted die.

(Bottom to Top)

AT40K20 256 I/O	304 PQFP(2)
VCC	152
$\overline{RESET}$	151
I/O129 (D7)	150
I/O130, GCK5	149
I/O131	148
I/O132	147
I/O133	
I/O134	
I/O135	146
I/O136	145
	144
	143

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K20 256 I/O	304 PQFP[2]
VCC	
GND	
I/O137 (D6)	142
I/O138	141
I/O139	140
I/O140	139
I/O141	138
I/O142	137
I/O143	136
I/O144	135
GND	134
I/O145	133
I/O146	132
I/O147, FCK3	131
I/O148	130
VCC	129
I/O149 (D5)	127
I/O150 (CS0)	126
I/O151	125
I/O152	124
GND	

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K20 256 I/O	304 PQFP[2]
I/O153	123
I/O154	122
I/O155	121
I/O156	120
I/O157	119
I/O158	118
I/O159(D4)	117
I/O160	116
VCC	115
GND	114
I/O161 (D3)	113
I/O162 ($\overline{\text{CHECK}}$)	112
I/O163	111
I/O164	110
I/O165	109
I/O166	108
I/O167	107
I/O168	106
GND	
I/O169	105

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K20 256 I/O	304 PQFP(2)
I/O170	104
I/O171 (D2)	103
I/O172	102
VCC	101
I/O173	99
I/O174, FCK4	98
I/O175	97
I/O176	96
GND	95
I/O177	94
I/O178	93
I/O179	92
I/O180	91
I/O181	90
I/O182	89
I/O183	88
I/O184	87
GND	
VCC	
I/O185 (D1)	86
I/O186	85

led GND or
They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K20 256 I/O	304 PQFP(2)
I/O187	84
I/O188	83
I/O189	82
I/O190	81
I/O191 (D0)	80
I/O192, GCK6 ($\overline{\text{CSOUT}}$)	79
CCLK	78
VCC	77
TSTCLK	76

led GND or VCC are internally bonded to Ground or VCC planes within the package.
e no direct connection to any specific package pin.
age has an inverted die.

Right to Left)

AT40K20 256 I/O	304 PQFP(2)
GND	75
I/O193 (A0)	74
I/O194, GCK7 (A1)	73
I/O195	72
I/O196	71

led GND or VCC are internally bonded to Ground or VCC planes within the package. They have r
connection to any specific package pin.

2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Table 12-4. Top Side (Right to Left) (Continued)

AT40K20 256 I/O	304 PQFP[2]
I/O197 ($\overline{CS1}$,A2)	70
I/O198 (A3)	69
I/O199	68
I/O200	67
VCC	
GND	
I/O201[3]	66[3] NC
I/O202	65
I/O203	64
I/O204	63
I/O205	62
I/O206	61
I/O207	60
I/O208	59
GND	58
I/O209	57
I/O210	56
I/O211	55
I/O212	54
VCC	52
I/O213	51
I/O214	50

eled GND or ey have r
connection to any spe ific package pin.

2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Table 12-4. Top Side (Right to Left) (Continued)

AT40K20 256 I/O	304 PQFP[2]
I/O215	49
I/O216	48
GND	
I/O217 (A4)	47
I/O218 (A5)	46
I/O219	45
I/O220	44
I/O221	43
I/O222	42
I/O223 (A6)	41
I/O224 (A7)	40
GND	39
VCC	38
I/O225 (A8)	37
I/O226 (A9)	36

eled GND or
n to any spe

ey have n

2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Table 12-4. Top Side (Right to Left) (Continued)

AT40K20 256 I/O	304 PQFP(2)
I/O227	35
I/O228	34
I/O229	33
I/O230	32
I/O231 (A10)	31
I/O232 (A11)	30
GND	
I/O233	29
I/O234	28
I/O235	27
I/O236	26
VCC	25
I/O237	23
I/O238	22
I/O239	21
I/O240	20
GND	19
I/O241	18
I/O242	17
I/O243	16
I/O244	15

eled GND or ey have n connection to any specific package pin.

2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Table 12-4. Top Side (Right to Left) (Continued)

AT40K20 256 I/O		304 PQFP(2)
I/O245		14
I/O246		13
I/O247 (A12)		12
I/O248 (A13)		10
GND		
VCC		
I/O249		9
I/O250		8
I/O251		7
I/O252		6
I/O253		5
I/O254		4
I/O255 (A14)		3
I/O256, GCK8 (A15)		2
VCC		1

led GND or VCC are internally bonded to Ground or VCC planes within the package. They have n
n to any specific package pin.

age has an inverted die.

ith TSTCLK. No Connect.

13. Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package[1]	AT40K05	AT40K10	AT40K20
144 LQFP	114	—	114
208 LQFP	—	161	—
240 PQFP	—	—	193

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
144AA	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)

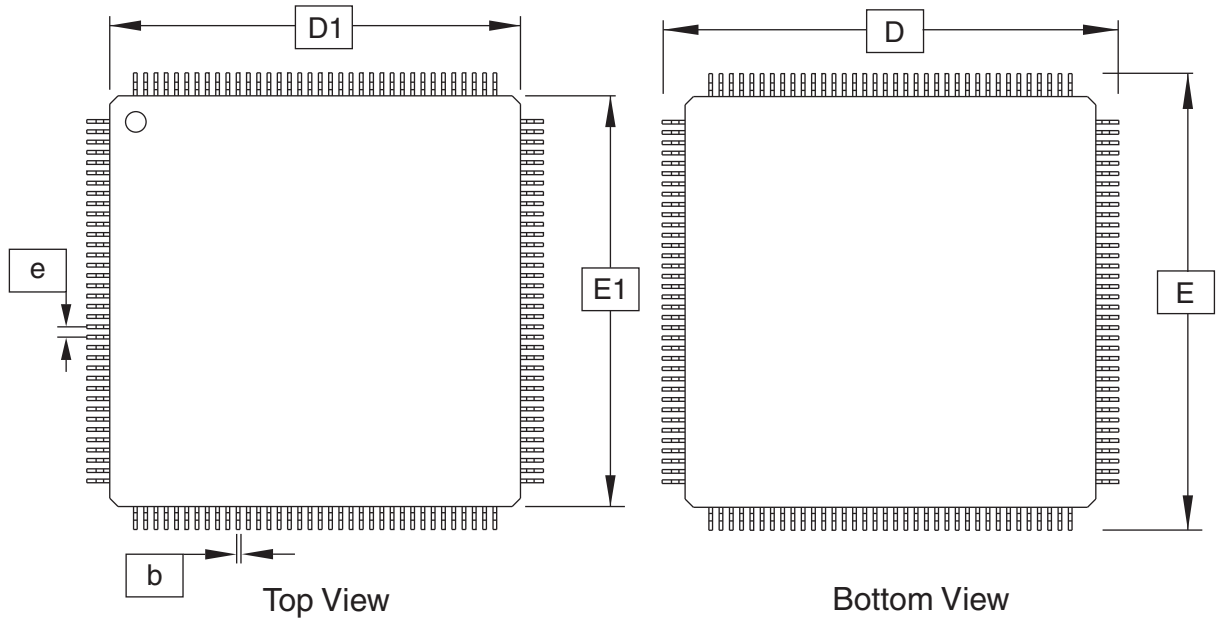
14. AT40K Series Ordering Information

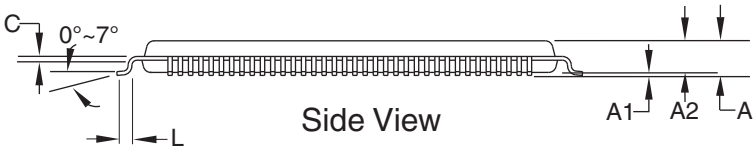
Atmel Ordering Code	Package	Usable Gates	Operating Voltage	Speed Grade (ns)	Operation Range
AT40K05-2BQJ[1]	144AA	5,000 – 10,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K10-W[2]	Wafer	10,000 – 20,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K10-2DQU[3]	208Q1	10,000 – 20,000			
AT40K20-2BQJ[1]	144AA	20,000 – 30,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K20-2EQJ[1]	240Q1	20,000 – 30,000			

Notes:
1. Devices are Pb-free but are *not* RoHS-compliant.
2. For Die Sales of AT40K10, please contact Atmel Sales.
3. Please contact Atmel Sales for availability.

15. Packaging Information

15.1 144AA — 144-lead LQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

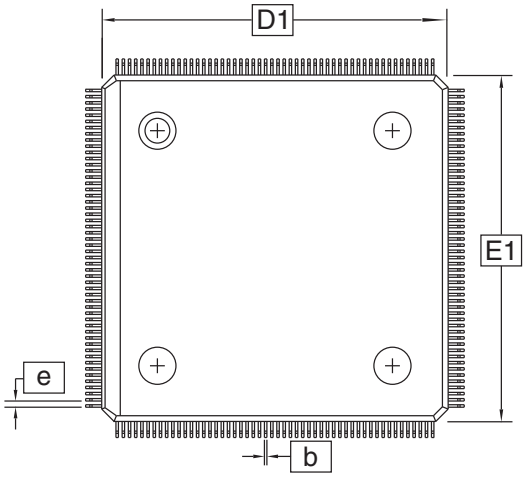
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D		22.00 BSC		
D1		20.00 BSC		Note 2
E		22.00 BSC		
E1		20.00 BSC		Note 2
b	0.17	0.22	0.27	
C	0.09	–	0.20	
L	0.45	0.60	0.75	
e		0.50 TYP		

Notes: 1. This package conforms to JEDEC reference MS-026, Variation BFB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/19/2011

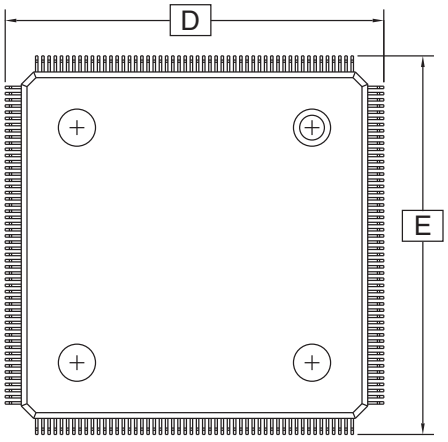
Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**144AA**, 144-lead, 20 x 20 x 1.4mm Body, 0.50mm lead pitch, 2.0mm footprint, Low-profile Plastic Quad Flat Package (LQFP)	AEI	144AA	D

15.2 208Q1 — 208-lead PQFP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

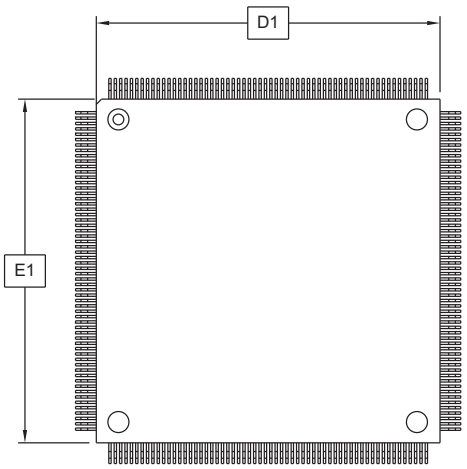
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		30.60 BSC		
D1		28.00 BSC		2, 3
E		30.60 BSC		
E1		28.00 BSC		2, 3
e		0.50 BSC		
b	0.17	–	0.27	4
L1		1.30 REF		

Notes: 1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

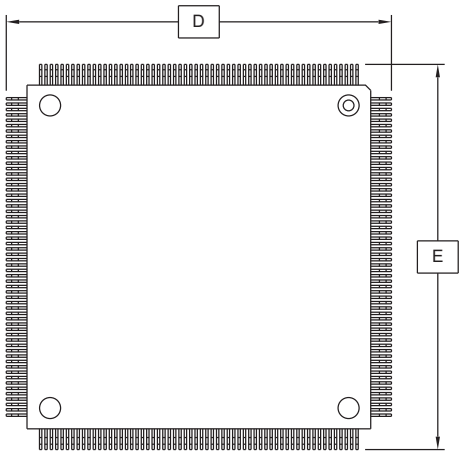
03/10/05

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	DRAWING NO. 208Q1	REV. C

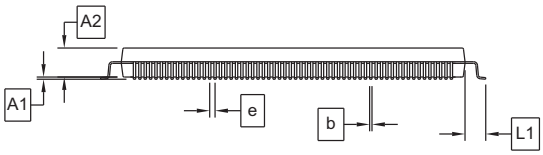
15.3 240Q1 — 240-lead PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

11/5/08

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 240Q1, 240-lead, 32 x 32 mm Body, 2.6 Form Opt, Plastic Quad Flat Pack (PQFP)	**GPC** QSW	**DRAWING NO.** 240Q1	**REV.** B

16. Revision History

Doc. No.	Date	Comments
0896E	06/2013	Added 208Q1 package option. Reinserted the Left Side (Top to Bottom) table. Updated footers and disclaimer page.
0896D	01/2013	Revised datasheet with lead-free package offering. Removed low voltage (AT40KLV) offering. Removed discontinued lead based package offering. Added AT40K010-W (for die sale program). Updated PDFQ – 240Q1 package drawing. Replaced LQFP – 144L1 with LQFP – 144AA package drawing.
0896C	04/2002	

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