Features

- Ultra High Performance
  - System Speeds to 100 MHz
  - Array Multipliers > 50 MHz
  - 10 ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 10 ns SRAM
  - 2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells
- 128 - 384 PCI Compliant I/Os
  - 3V/5V Capability
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
  - Pin-compatible with XC4000, XC5200 FPGAs
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
  - Unlimited Re-programmability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - QuickChange™ Tools for Fast, Easy Design Changes
- Pin-compatible Package Options
  - Plastic Leaded Chip Carriers (PLCC)
  - Thin, Plastic Quad Flat Packs (LQFP, TQFP, PQFP)
  - Ball Grid Arrays (BGAs)
- Industry-standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-annotation) with Concept®, Everest, Exemplar™, Mentor®, OrCAD®, Synario™, Synopsys®, Verilog®, Veribest®, Viewlogic®, Synplicity®
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic and RAM Functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI, FFT and Other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production
- Supply Voltage 5V for AT40K, and 3.3V for AT40KLV

5K - 50K Gates Coprocessor FPGA with FreeRAM™

AT40K05
AT40K05LV
AT40K10
AT40K10LV
AT40K20
AT40K20LV
AT40K40
AT40K40LV

Rev. 0896C–FPGA–04/02

Table 1. AT40K/AT40KLV Family[1]

Device	AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256[1]	576[1]	1,024[1]	2,304[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40K/AT40KLV is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 5V designs for AT40K and 3.3V designs for AT40KLV.

The AT40K/AT40KLV is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic.

The AT40K/AT40KLV can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K/AT40KLV FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40K/AT40KLV's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K/AT40KLV's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K/AT40KLV, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K/AT40KLV can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K/AT40KLV FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40K/AT40KLV series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 2,304 registers. Pin locations are consistent throughout the AT40K/AT40KLV series for easy design migration in the same package footprint. The AT40K/AT40KLV series FPGAs utilize a reliable 0.6µ single-poly, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40K/AT40KLV series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM[1], with either synchronous or asynchronous operation.

Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)

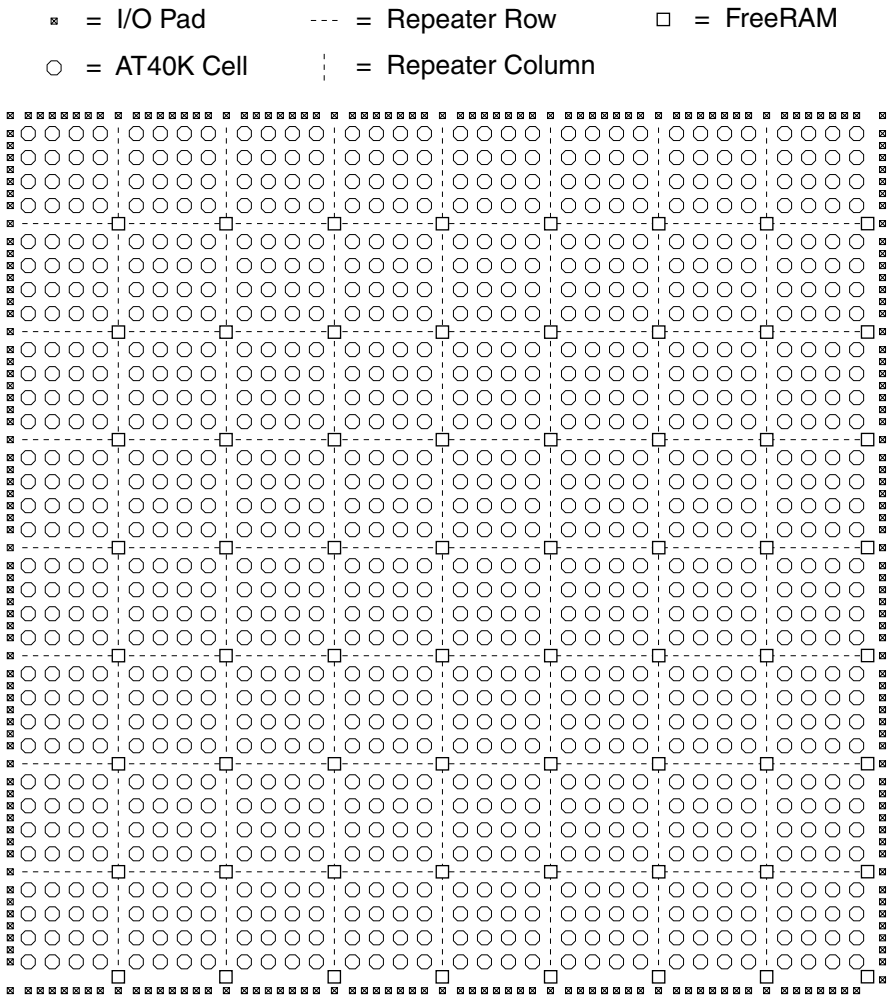
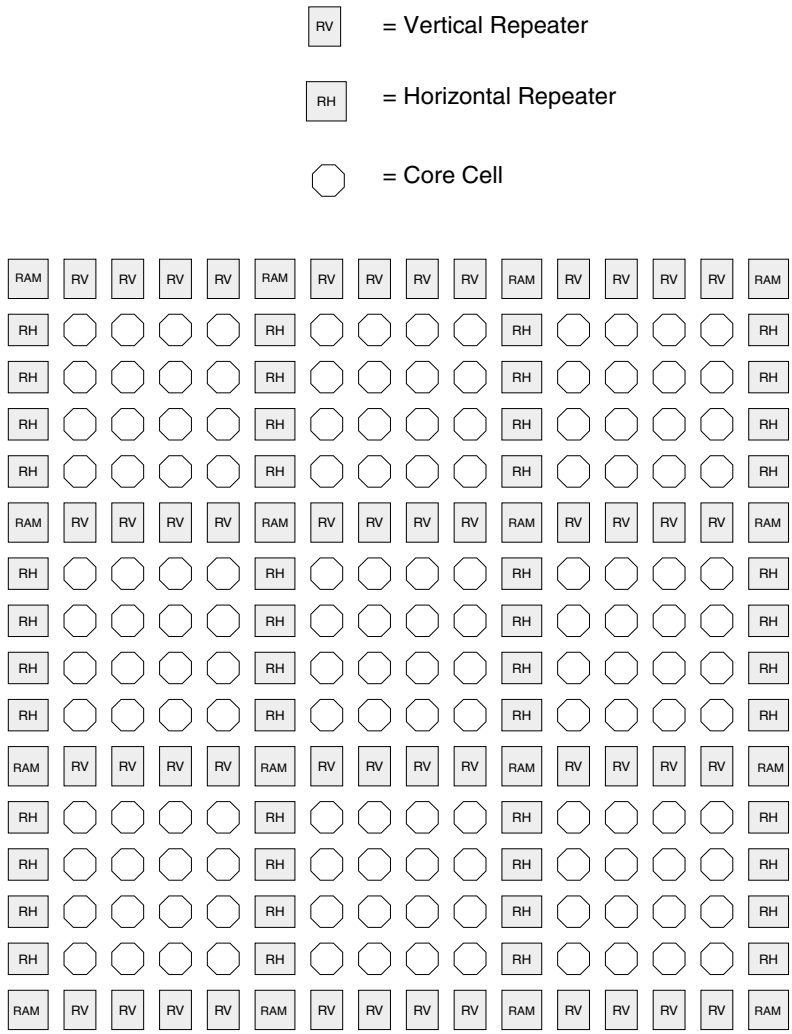


Figure 2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

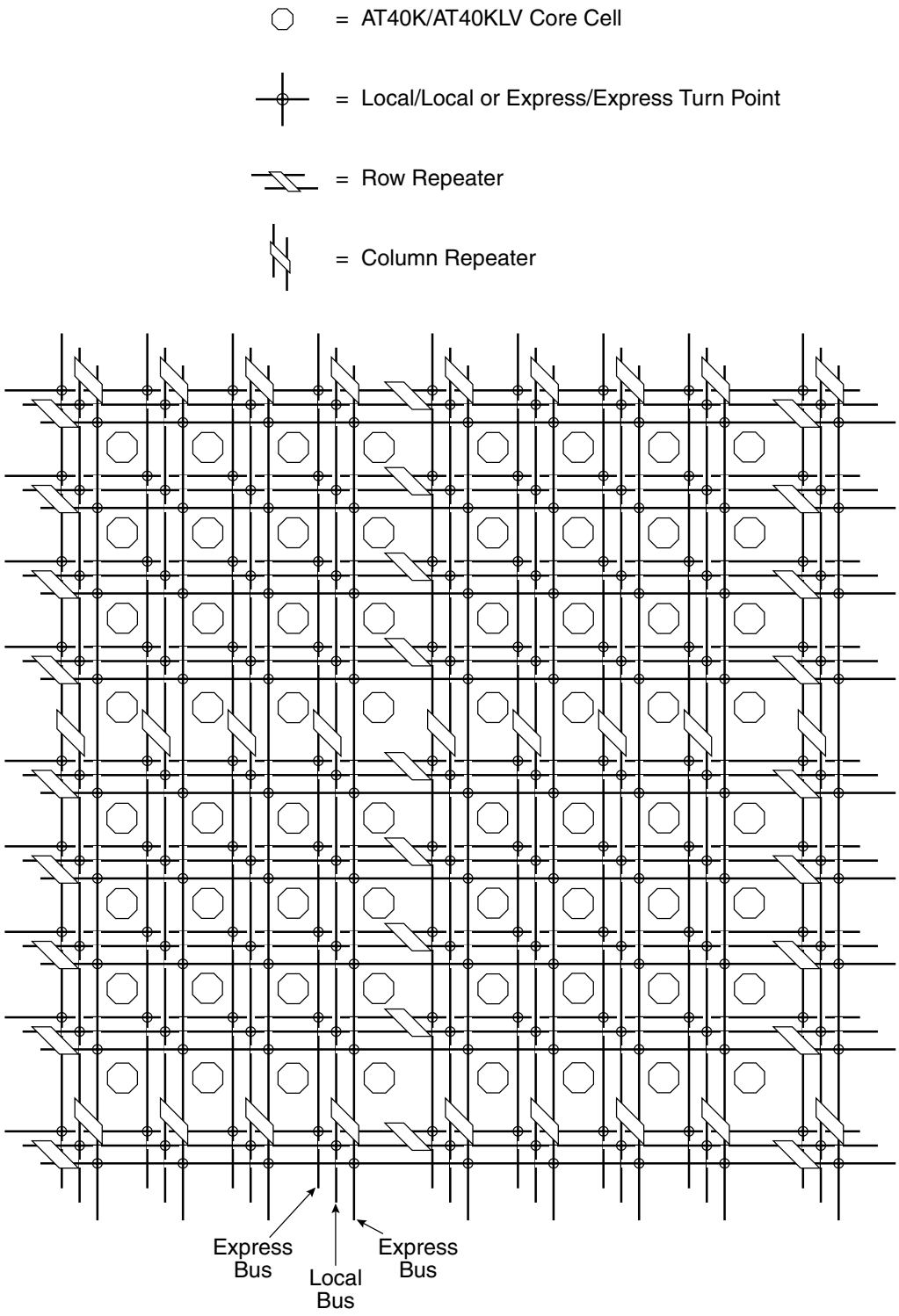
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and "leapfrogs" or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40K/AT40KLV are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40K/AT40KLV software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

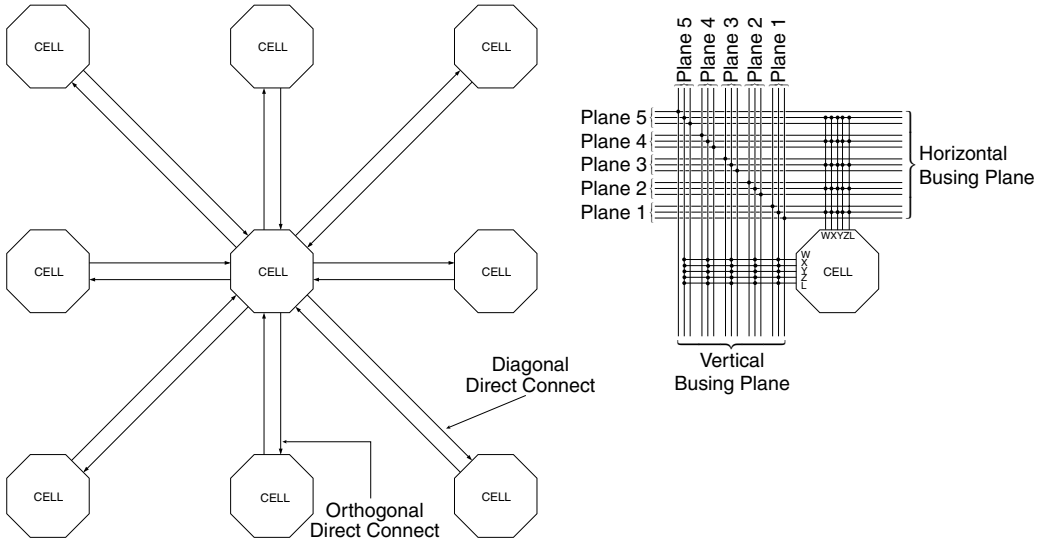
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

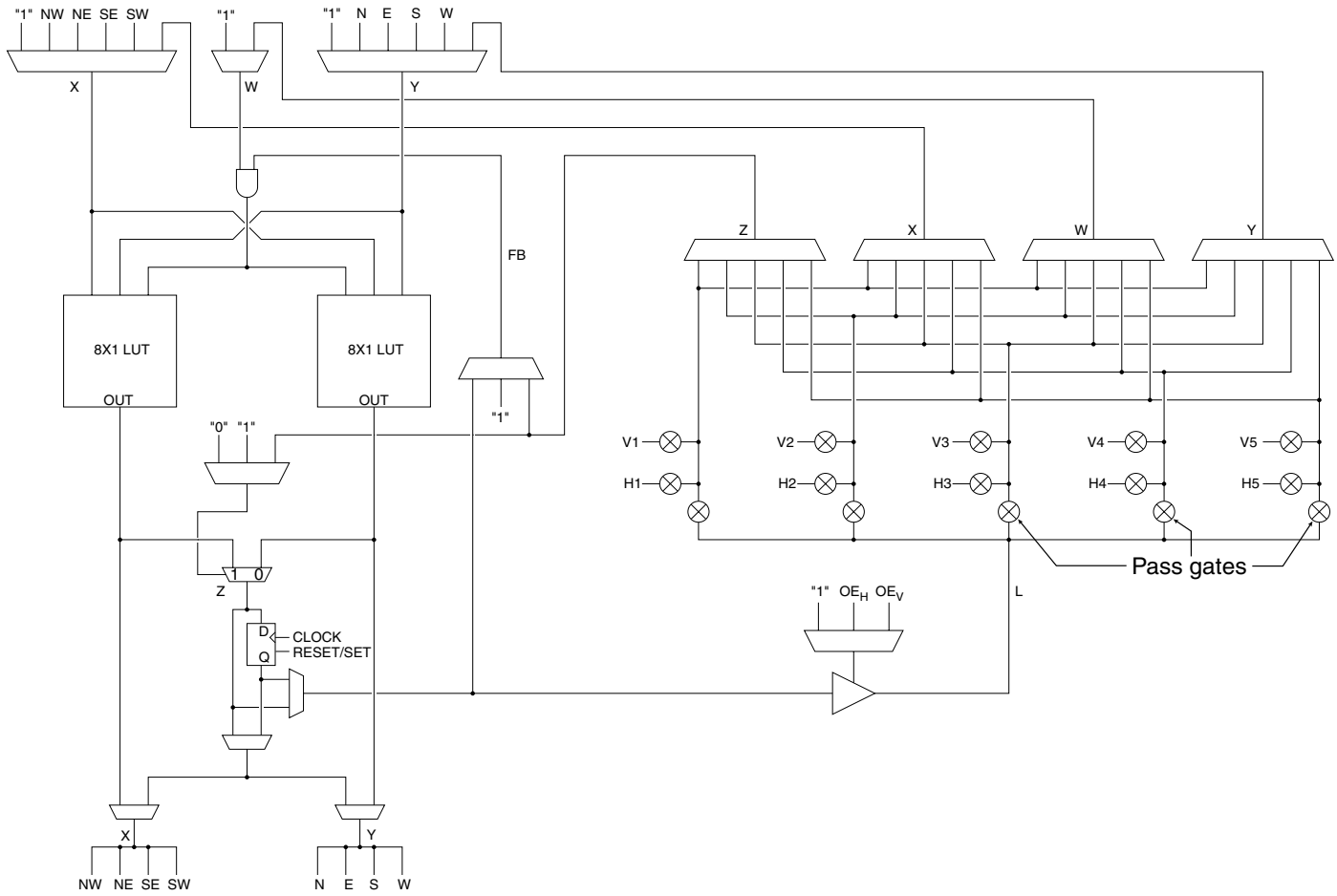
The Cell

Figure 5 depicts the AT40K/AT40KLV cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40K/AT40KLV FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

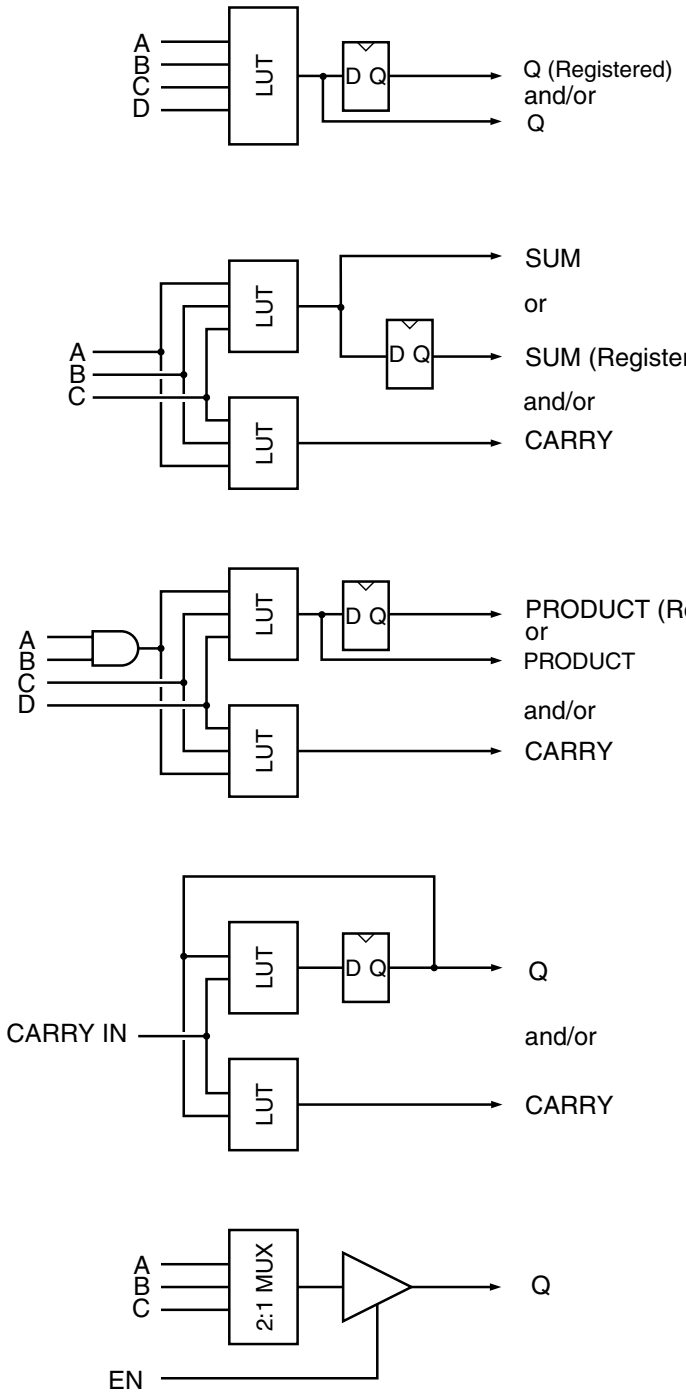
With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40K/AT40KLV architecture well suited to most digital design application areas, see Figure 6.

Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40K/AT40KLV core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K/AT40KLV architecture.

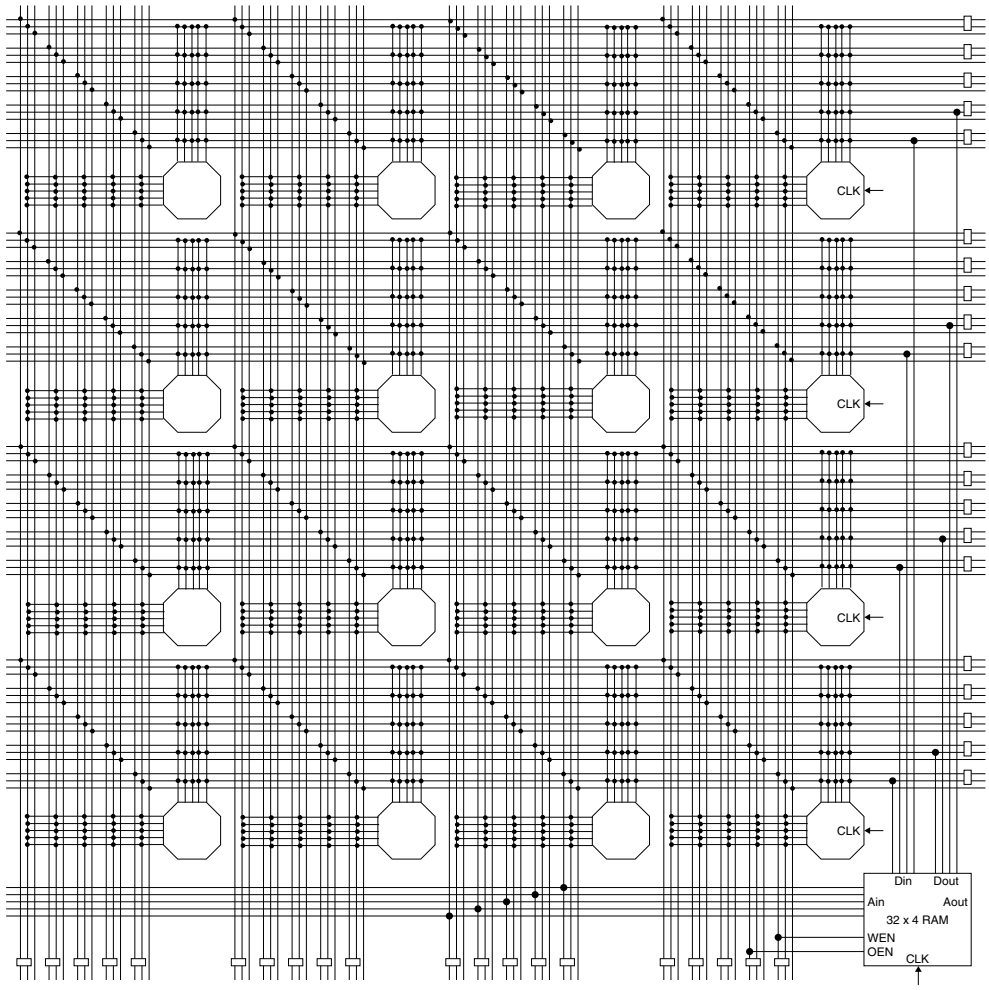
Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sectors in the same column. A 5-bit Output Address Bus connects to five vertical express buses in the same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)



Reading and writing of the 10 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{\text{WE}}$ is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "*AT40K Configuration Series"* application note at www.atmel.com).

Figure 8. RAM Logic

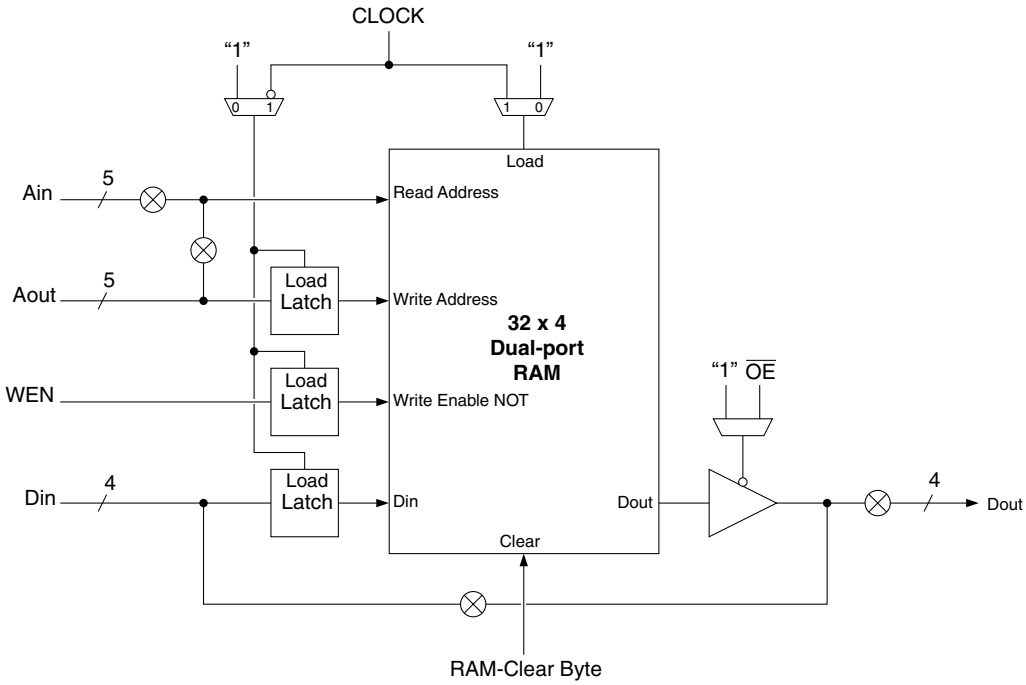
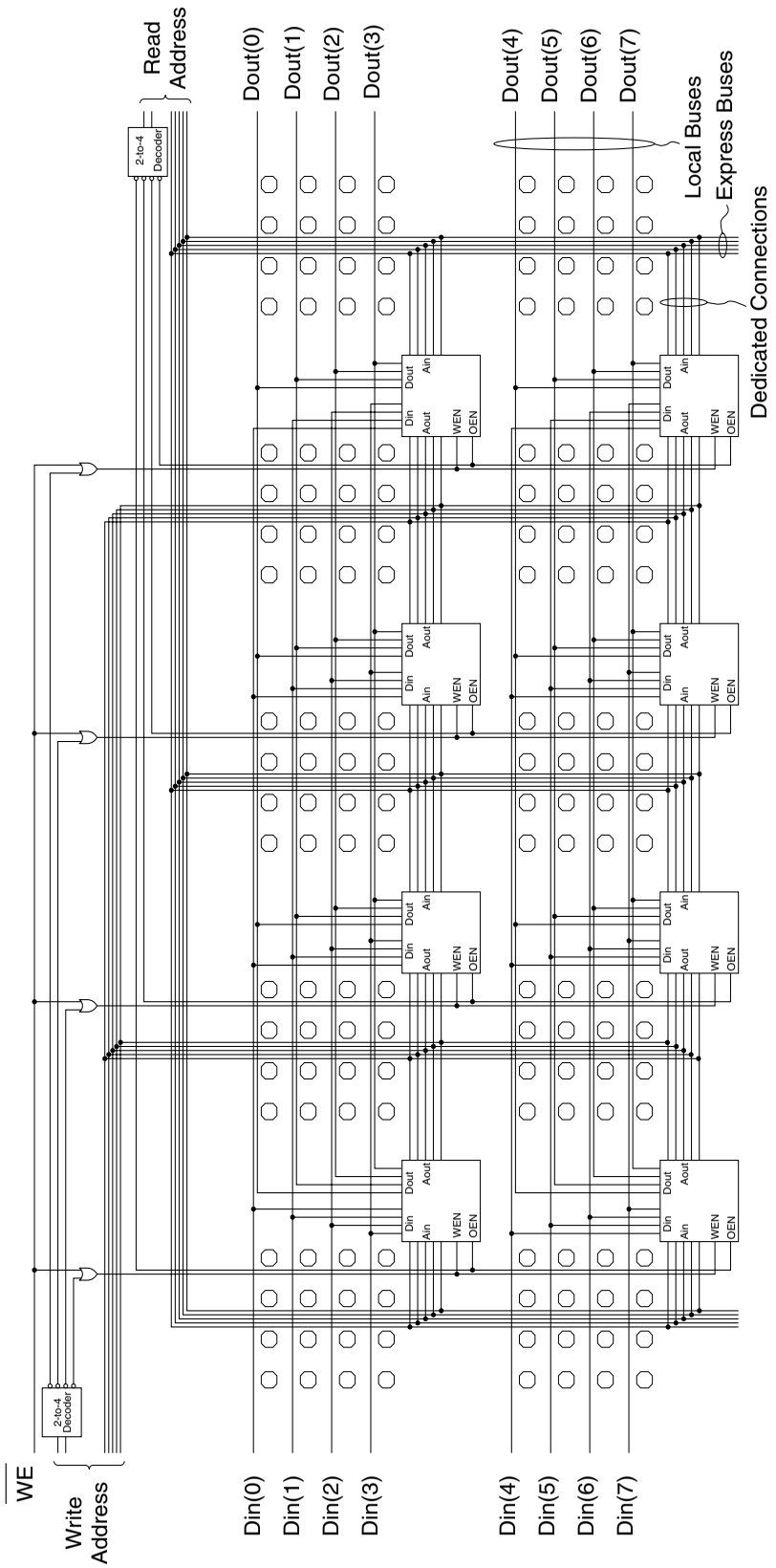


Figure 9 on page 13 shows an example of a RAM macro constructed using the AT40K/AT40KLV's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



Clocking Scheme

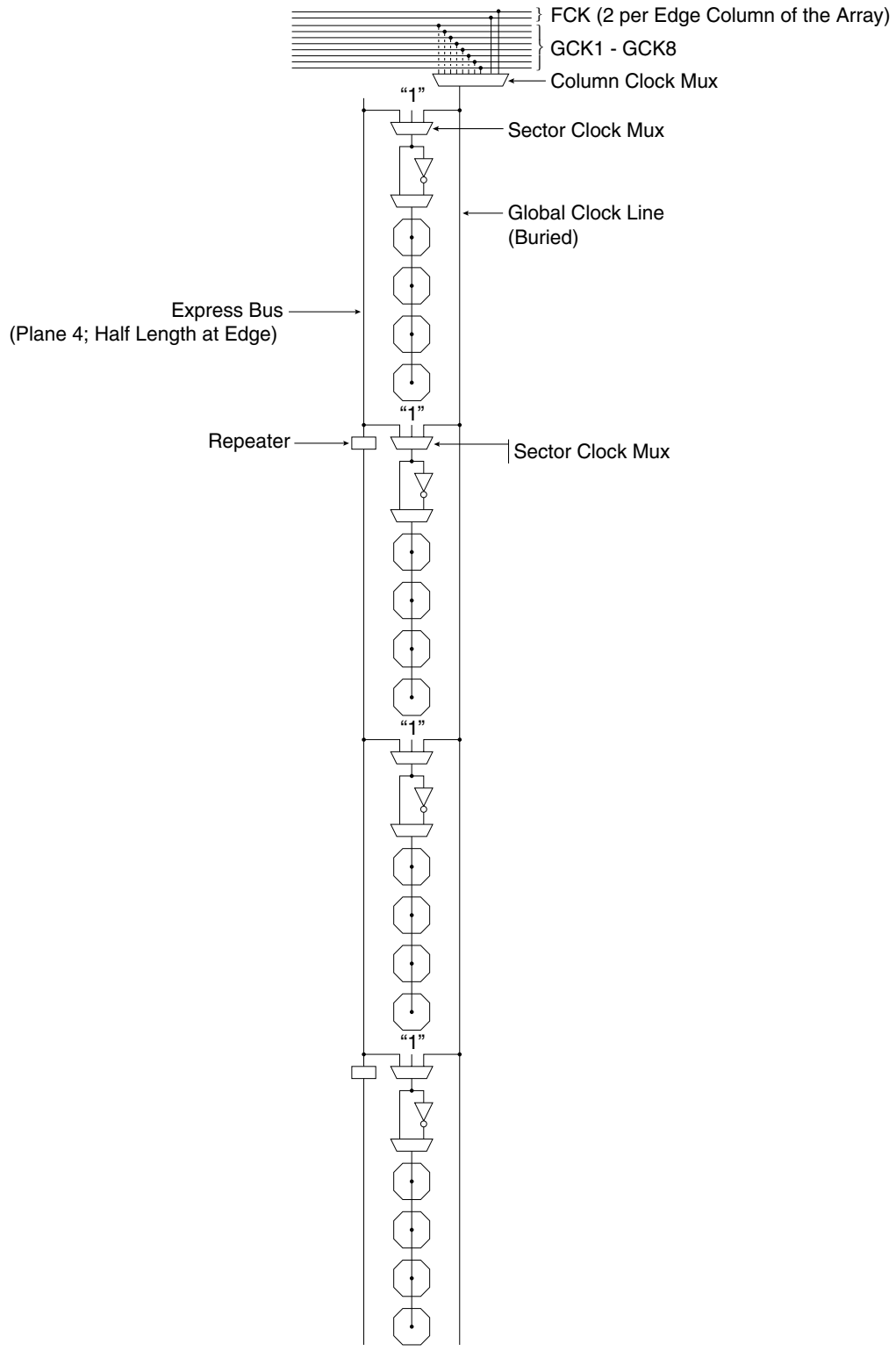
There are eight Global Clock buses (GCK1 - GCK8) on the AT40K/AT40KLV FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 10 on page 15. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 10. Clocking (for One Column of Cells)



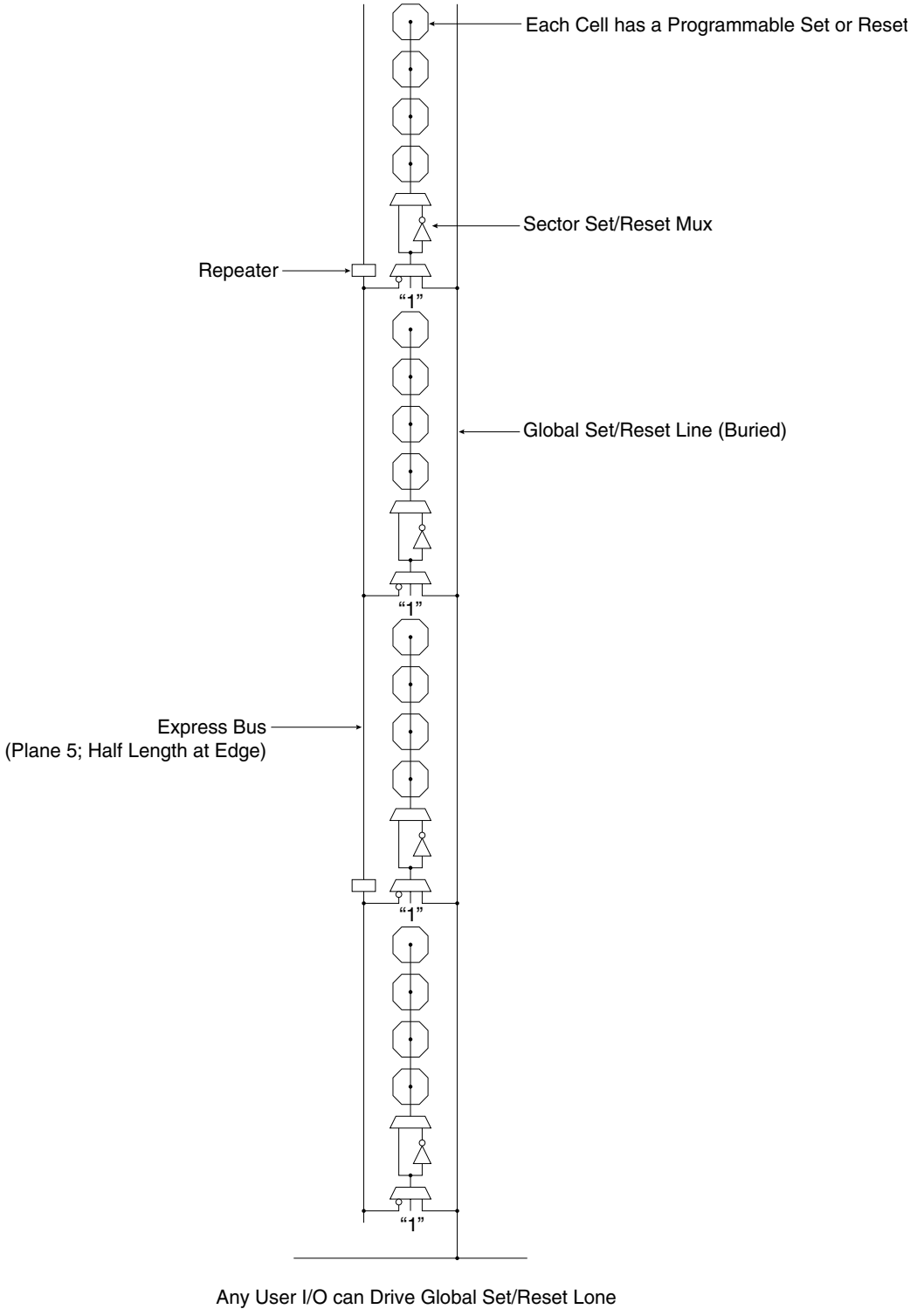
Set/Reset Scheme

The AT40K/AT40KLV family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



I/O Structure

PAD

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

PULL-UP/PULL-DOWN

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak “1” or “0” level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

TTL/CMOS

The threshold level can be set to either TTL/CMOS-compatible levels.

SCHMITT

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

DELAYS

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

DRIVE

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (20 mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (14 mA at 5V) buffer, while SLOW yields a standard (6 mA at 5V) buffer.

TRI-STATE

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O’s Source Selection mux. Of course, the output can be normal (0 or 1), as well.

SOURCE SELECTION MUX

The Source Selection mux selects the source for the output signal of an I/O, see Figure 12 on page 20.

Primary, Secondary and Corner I/Os

The AT40K/AT40KLV has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40K/AT40KLV has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figures 12a on page 20 and 13a on page 21.

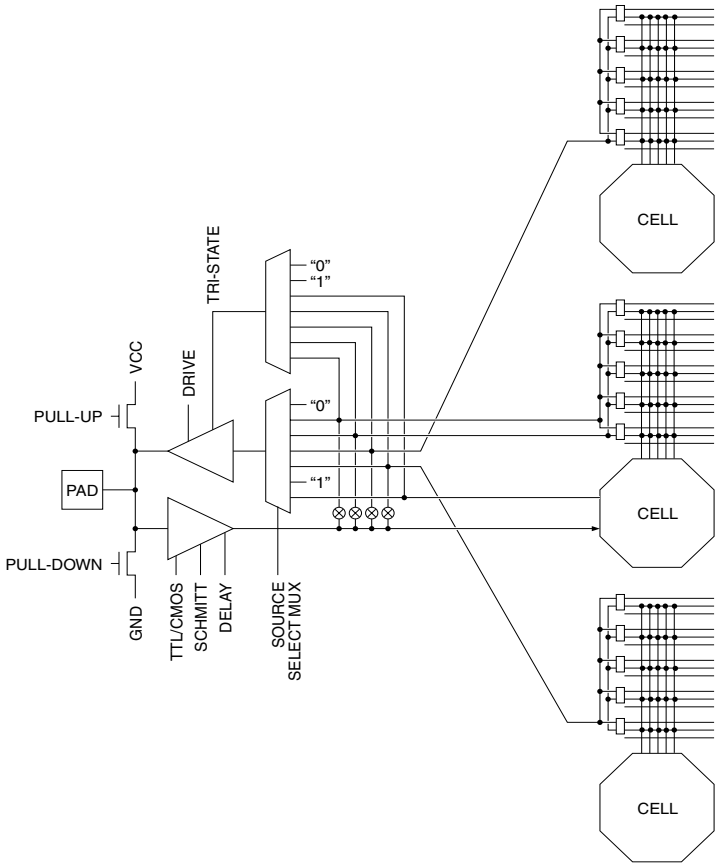
Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 12b on page 20 and Figure 13b.

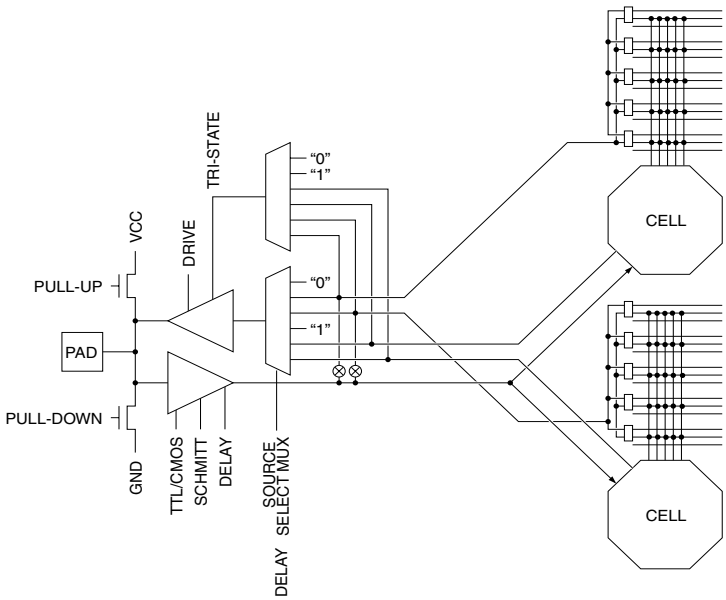
Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40K/AT40KLV FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 22.

Figure 12. West I/O (Mirrored for East I/O) AT40K/AT40KLV

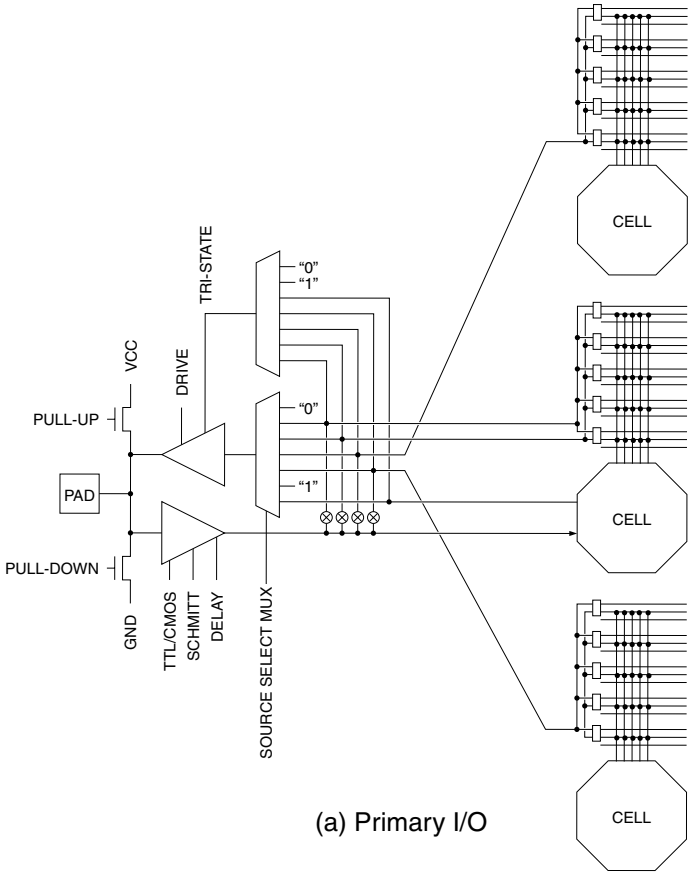


(a) Primary I/O

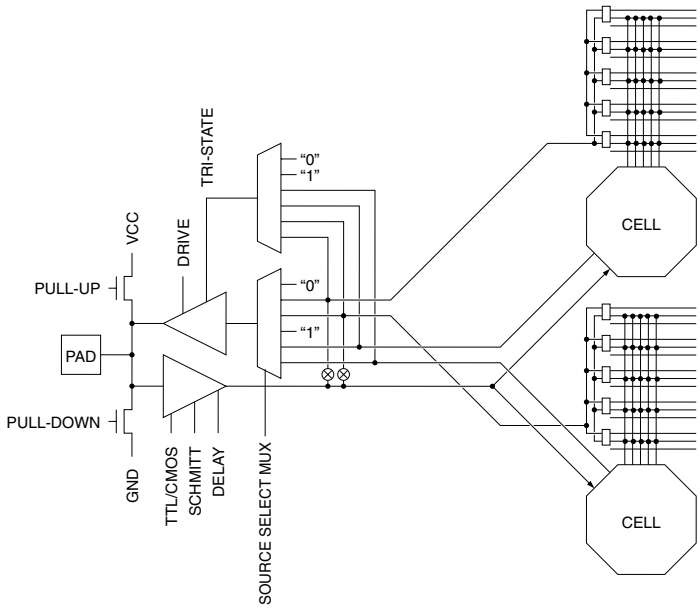


(b) Secondary I/O

Figure 13. South I/O (Mirrored for North I/O) AT40K/AT40KLV

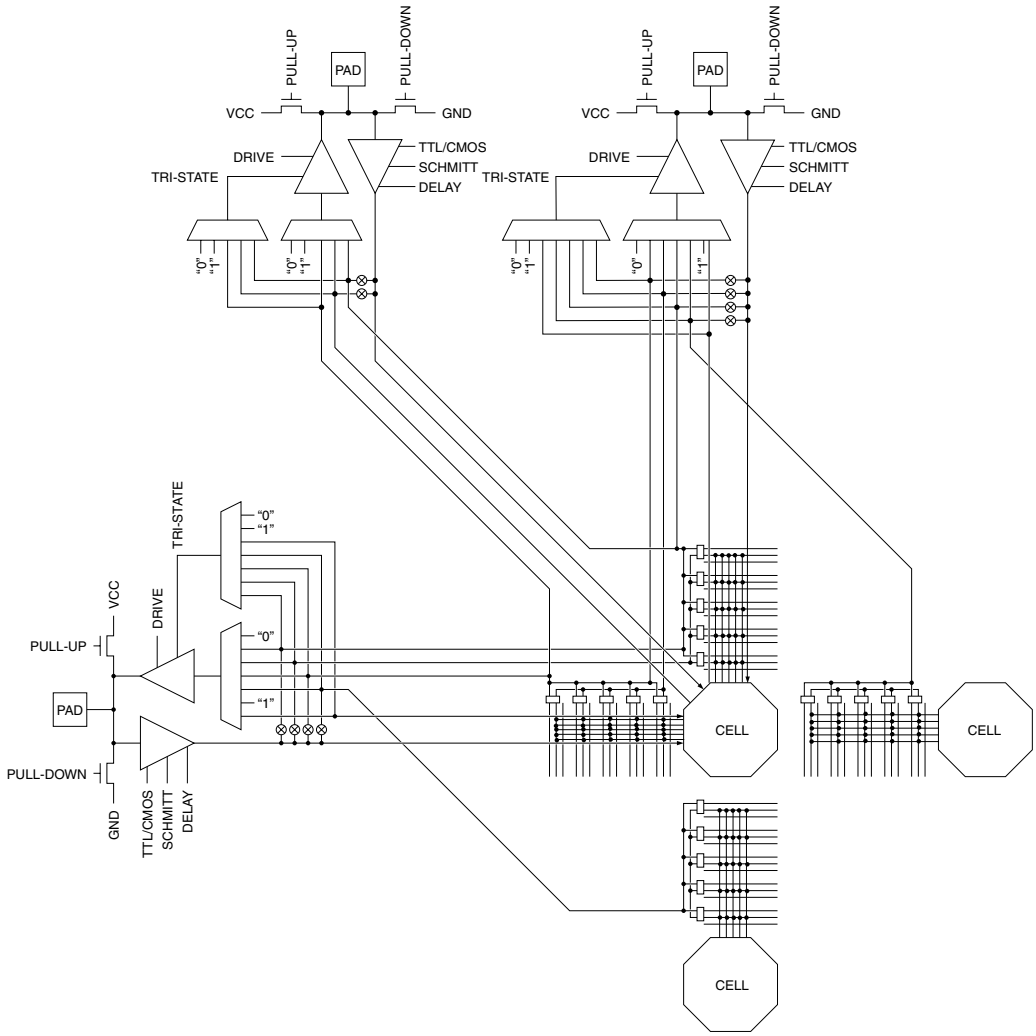


(a) Primary I/O



(a) Secondary I/O

Figure 14. Northwest Corner (Similar for NE/SE/SW Corners) AT40K/AT40KLV



Absolute Maximum Ratings – 5V Commercial/Industrial* AT40K

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 5V Operation AT40K

		Commercial -2	Industrial -2	Military -2
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 5V Operation Commercial/Industrial/Military AT40K

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 14mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 20mA Commercial = 4.75V Industrial/Military = 4.5V	Ind. = 3.15 4.0 Con = 3.325			V
V_{OL}	Low-level Output Voltage	I_{OL} = -6mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -14mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -20mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	CON = -1 mA to -250 µA	-250.0	CON = -1 mA to -250 µA	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC}			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS} Maximum	-10.0			µA
		With pull-up, V_{IN} = V_{SS} Maximum	-500.0	-250.0	-125.0	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-2	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05	1.1	ns	Rising edge clock
		pad -> clock	AT40K10	1.2	ns	
		pad -> clock	AT40K20	1.2	ns	
		pad -> clock	AT40K40	1.4	ns	
FCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05	0.7	ns	Rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.8	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05	0.8	ns	Rising edge clock
		clock -> colclk	AT40K10	0.9	ns	
		clock -> colclk	AT40K20	1.0	ns	
		clock -> colclk	AT40K40	1.1	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05	0.5	ns	Rising edge clock
		colclk -> secclk	AT40K10	0.5	ns	
		colclk -> secclk	AT40K20	0.5	ns	
		colclk -> secclk	AT40K40	0.5	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05	3.0	ns	From any pad to Global Set/Reset network
		pad -> GSRN	AT40K10	3.7	ns	
		pad -> GSRN	AT40K20	4.3	ns	
		pad -> GSRN	AT40K40	5.6	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05	8.3	ns	Rising edge clock
		clock pad -> out	AT40K10	8.4	ns	Fully loaded clock tree
		clock pad -> out	AT40K20	8.6	ns	Rising edge DFF
		clock pad -> out	AT40K40	8.8	ns	20 mA output buffer
						50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05	7.9	ns	Rising edge clock
		clock pad -> out	AT40K10	8.0	ns	Fully loaded clock tree
		clock pad -> out	AT40K20	8.1	ns	Rising edge DFF
		clock pad -> out	AT40K40	8.3	ns	20 mA output buffer
						50 pf pin load

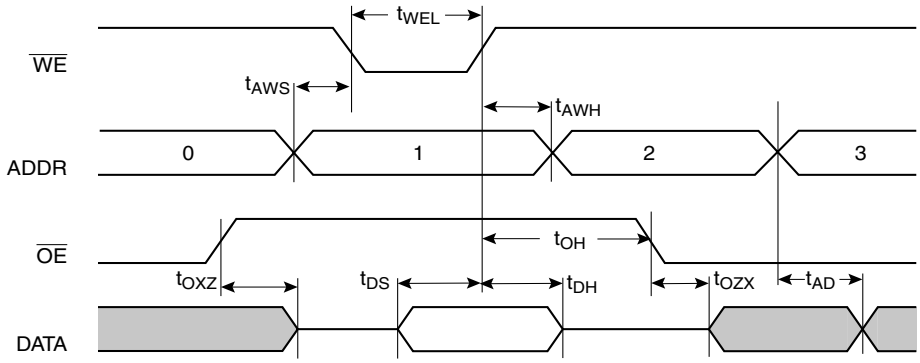
AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

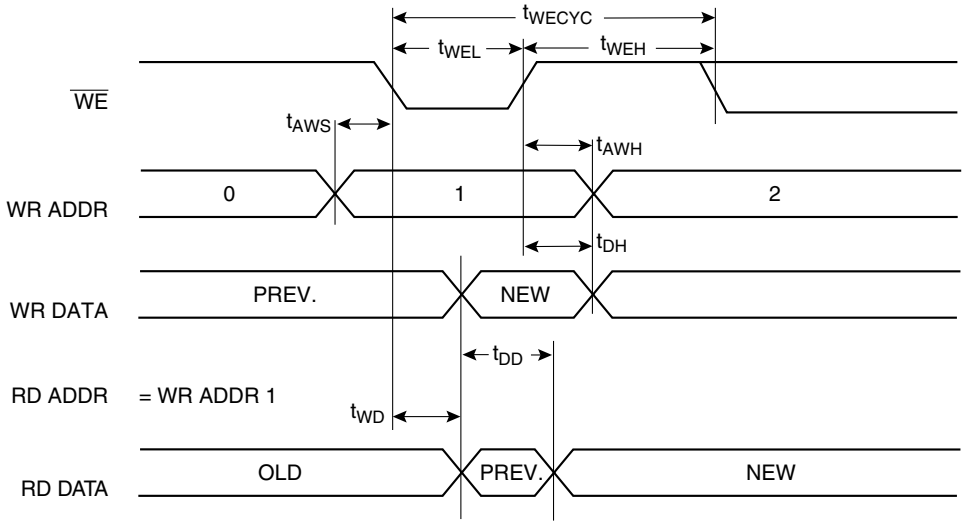
Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	8.0	ns	
Write	t_{WEL} (Minimum)	we	3.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	3.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	2.0	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	2.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	4.6	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe -> dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	2.0	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	8.0	ns	
Write	t_{CLKL} (Minimum)	clk	3.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	3.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	2.0	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	2.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	2.0	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	3.5	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe -> dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	2.0	ns	

FreeRAM Asynchronous Timing Characteristics

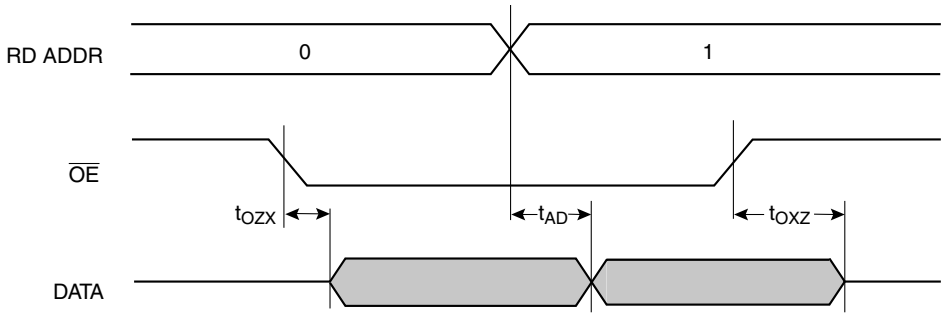
Single-port Write/Read



Dual-port Write with Read

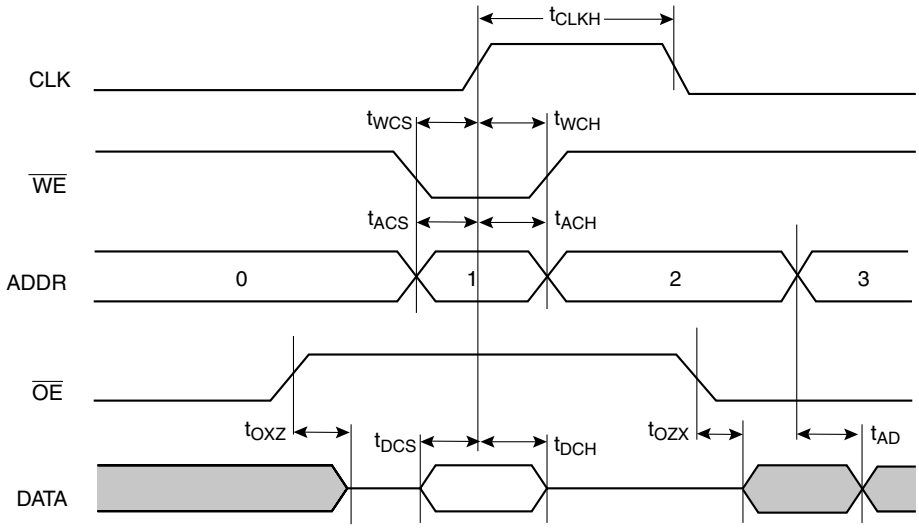


Dual-port Read

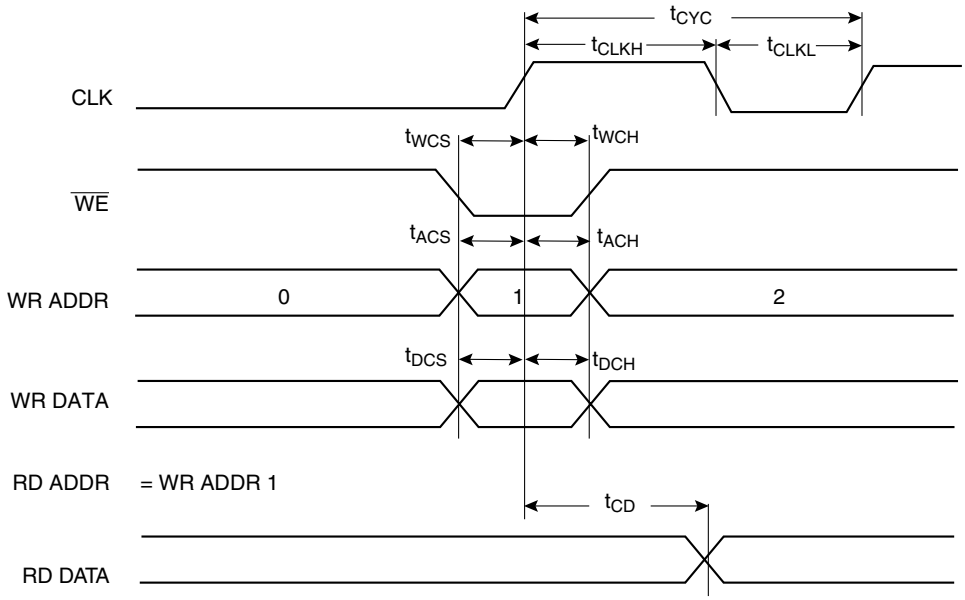


FreeRAM Synchronous Timing Characteristics

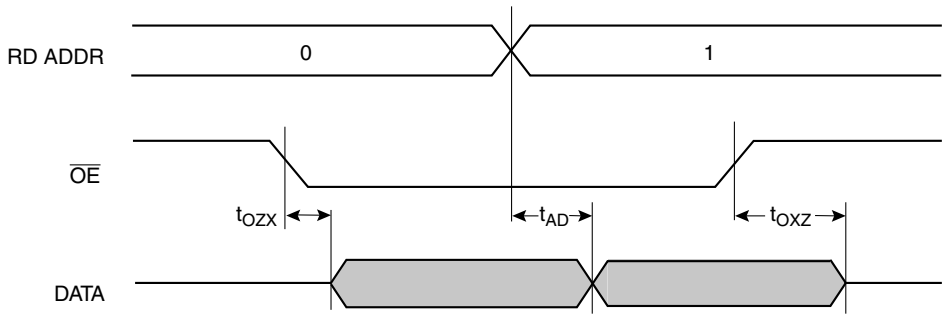
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



Absolute Maximum Ratings – 3.3V Commercial/Industrial* AT40KLV

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation AT40KLV

		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 3.3V Operation Commercial/Industrial AT40KLV

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} Minimum	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	75.0	150.0	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-150.0	-75.0	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC} Maximum	75.0	150.0	300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-10.0			mA
		With pull-up, V_{IN} = V_{SS}	CON = -500 µA TO -125 µA	-150.0	CON = -500 µA TO -125 µA-	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-3	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	2.9	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	3.4	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	2.9	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	3.0	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	2.4	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	2.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	3.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	3.0	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	2.7	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	2.4	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	2.8	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	2.4	ns	

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	1.4	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	1.4	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.9	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	5.8	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	11.5	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	17.4	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	9.1	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	7.6	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	6.2	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	9.5	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	2.1	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	7.4	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	2.7	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	5.9	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	2.4	ns	50 pf load

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-3	Units	Notes
Global Clocks and Set/Reset						
GCK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05LV	1.3	ns	Rising edge clock
		pad -> clock	AT40K10LV	1.5	ns	
		pad -> clock	AT40K20LV	1.6	ns	
		pad -> clock	AT40K40LV	1.9	ns	
FCK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05LV	0.7	ns	Rising edge clock
		pad -> clock	AT40K10LV	0.8	ns	
		pad -> clock	AT40K20LV	0.8	ns	
		pad -> clock	AT40K40LV	0.9	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05LV	1.5	ns	Rising edge clock
		clock -> colclk	AT40K10LV	1.8	ns	
		clock -> colclk	AT40K20LV	2.0	ns	
		clock -> colclk	AT40K40LV	2.5	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05LV	1.0	ns	Rising edge clock
		colclk -> secclk	AT40K10LV	1.0	ns	
		colclk -> secclk	AT40K20LV	1.0	ns	
		colclk -> secclk	AT40K40LV	1.0	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05LV	4.5	ns	
		pad -> GSRN	AT40K10LV	5.4	ns	
		pad -> GSRN	AT40K20LV	6.3	ns	
		pad -> GSRN	AT40K40LV	8.2	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05LV	13.0	ns	Rising edge clock
		clock pad -> out	AT40K10LV	13.4	ns	Fully loaded clock tree
		clock pad -> out	AT40K20LV	13.8	ns	Rising edge DFF
		clock pad -> out	AT40K40LV	14.5	ns	20 mA output buffer
						50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05LV	12.4	ns	Rising edge clock
		clock pad -> out	AT40K10LV	12.7	ns	Fully loaded clock tree
		clock pad -> out	AT40K20LV	13.0	ns	Rising edge DFF
		clock pad -> out	AT40K40LV	13.5	ns	20 mA output buffer
						50 pf pin load

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-3	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS}(Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

AT40K10 AT40K10LV	Left Side (Top to Bottom)
192 I/O	208 PQFP
GND	2
I/O1, GCK1 (A16)	4
I/O2 (A17)	5
I/O3	6
I/O4	7
I/O5 (A18)	8
I/O6 (A19)	9
I/O7	10
I/O8	11
I/O9	12
I/O10	13
I/O11	
I/O12	
GND	14
I/O13, FCK1	15
I/O14	16

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K10 AT40K10LV 192 I/O	ottom) 208 PQFP
I/O15 (A20)	17
I/O16 (A21)	18
VCC	
I/O17	
I/O18	
I/O19	19
I/O20	20
I/O21	21
I/O22	22
I/O23 (A22)	23
I/O24 (A23)	24
GND	25
VCC	26
I/O25	27
I/O26	28
I/O27	29

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K10 AT40K10LV	Left Side (Top to Bottom)
192 I/O	208 PQFP
I/O28	30
I/O29	31
I/O30	32
I/O31	
I/O32	
VCC	
I/O33	33
I/O34	34
I/O35	35
I/O36, FCK2	36
GND	37
I/O37	
I/O38	
I/O39	38
I/O40	39

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Left Side (Top to Bottom)
192 I/O			208 PQFP
I/O41			40
I/O42			41
I/O43			42
I/O44			43
I/O45			44
I/O46			45
I/O47 ($\overline{OTS}$)[3]			46
I/O48, GCK2			47
M1			48
GND			49
M0			50

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)
192 I/O			208 PQFP
VCC			55
M2			56
I/O49, GCK3			57
I/O50 (HDC)			58
I/O51			59
I/O52			60
I/O53			61

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)
192 I/O			208 PQFP
I/O54 (LDC)			62
I/O55			63
I/O56			64
I/O57			65
I/O58			66
I/O59			
I/O60			
GND			67
I/O61			68
I/O62			69
I/O63			70
I/O64			71
VCC			
I/O65			72
I/O66			73

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV	o Right)
192 I/O	208 PQFP
I/O67	
I/O68	
I/O69	74
I/O70	75
I/O71 (D15)	76
I/O72 (INIT)	77
VCC	78
GND	79
I/O73 (D14)	80
I/O74 (D13)	81
I/O75	82
I/O76	83
I/O77	84
I/O78	85

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV 192 I/O	o Right) 208 PQFP
I/O79	
I/O80	
VCC	
I/O81 (D12)	86
I/O82 (D11)	87
I/O83	88
I/O84	89
GND	90
I/O85	
I/O86	
I/O87	91
I/O88	92
I/O89	93
I/O90	94
I/O91 (D10)	95
I/O92 (D9)	96

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV 192 I/O	o Right) 208 PQFP
I/O93	97
I/O94	98
I/O95 (D8)	99
I/O96, GCK4	100
GND	101
$\overline{CON}$	103

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nection to a
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AT40K10 AT40K10LV 192 I/O	to Top) 208 PQFP
VCC	106
$\overline{RESET}$	108
I/O97 (D7)	109
I/O98, GCK5	110
I/O99	111
I/O100	112
I/O101	
I/O102	
I/O103 (D6)	113

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV	to Top)
192 I/O	208 PQFP
I/O104	114
I/O105	115
I/O106	116
I/O107	117
I/O108	118
GND	119
I/O109	
I/O110	
I/O111, FCK3	120
I/O112	121
VCC	
I/O113 (D5)	122
I/O114 (CS0)	123
I/O115	124
I/O116	125

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV	to Top)
192 I/O	208 PQFP
I/O117	126
I/O118	127
I/O119(D4)	128
I/O120	129
VCC	130
GND	131
I/O121 (D3)	132
I/O122 ($\overline{\text{CHECK}}$)	133
I/O123	134
I/O124	135
I/O125	136
I/O126	137
I/O127 (D2)	138
I/O128	139
VCC	
I/O129	140

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.

AT40K10 AT40K10LV 192 I/O	to Top) 208 PQFP
I/O130, FCK4	141
I/O131	
I/O132	
GND	142
I/O133	
I/O134	
I/O135	143
I/O136	144
I/O137	145
I/O138	146
I/O139 (D1)	147
I/O140	148
I/O141	149
I/O142	150
I/O143 (D0)	151
I/O144, GCK6 (CSOUT)	152

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nection to a

2. This package has an inverted die.

AT40K10 AT40K10LV	to Top)
192 I/O	208 PQFP
CCLK	153
VCC	154
TSTCLK	159
Pads label	ıe packag
nection to a	
This packa	

AT40K10 AT40K10LV	ɔ Left)
192 I/O	208 PQFP
GND	160
I/O145 (A0)	161
I/O146, GCK7 (A1)	162
I/O147	163
I/O148	164
I/O149 ($\overline{CS1}$,A2)	165
I/O150 (A3)	166
I/O151[3]	159[3] NC
I/O152	
I/O153	167
I/O154	168

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag nection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K10 AT40K10LV	› Left)
192 I/O	208 PQFP
I/O155	169
I/O156	170
GND	171
I/O157	172
I/O158	173
I/O159	
I/O160	
VCC	
I/O161 (A4)	174
I/O162 (A5)	175
I/O163	176
I/O164	177
I/O165	178
I/O166	179
I/O167 (A6)	180

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K10 AT40K10LV 192 I/O	) Left) 208 PQFP
I/O168 (A7)	181
GND	182
VCC	183
I/O169 (A8)	184
I/O170 (A9)	185
I/O171	186
I/O172	187
I/O173	188
I/O174	189
I/O175 (A10)	190
I/O176 (A11)	191
VCC	
I/O177	
I/O178	
I/O179	192
I/O180	193
GND	194

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the packag
nection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K10 AT40K10LV		) Left)
192 I/O		208 PQFP
I/O181		195
I/O182		196
I/O183		197
I/O184		198
I/O185 (A12)		199
I/O186 (A13)		200
I/O187		
I/O188		
I/O189		201
I/O190		202
I/O191 (A14)		203
I/O192, GCK8 (A15)		204
VCC		205

Pads label … ue packag…
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This packa…
Shared wit…

Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package[1]				AT40K40/AT40K40LV
84 PLCC	62	62	62	–
100 PQFP	78	78	77	–
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
160 PQFP	128	130	130	–
208 PQFP	128	161	161	161
240 PQFP	–	–	193	193
304 PQFP	–	–	–	256

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q4	100-lead, Plastic Quad Flat Package (PQFP)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
160Q1	160-lead, Plastic Quad Flat Package (PQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)
304Q1	304-lead, Plastic Quad Flat Package (PQFP)
352C1	252-ball, Enhanced, Low-profile Square Ball Grid Array Package (SBGA)

AT40K05/AT40K05LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
5,000 - 10,000	5.0V	2	AT40K05-2AJC	84J	Commercial
			AT40K05-2AQC	100T1	(0°C to 70°C)
			AT40K05-2RQC	100Q4	
			AT40K05-2BQC	144L1	
			AT40K05-2CQC	160Q1	
			AT40K05-2DQC	208Q1	
5,000 - 10,000	5.0V	2	AT40K05-2AJI	84J	Industrial
			AT40K05-2AQI	100T1	(-40°C to 85°C)
			AT40K05-2RQI	100Q4	
			AT40K05-2BQI	144L1	
			AT40K05-2CQI	160Q1	
			AT40K05-2DQI	208Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

AT40K10/AT40K10LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
10,000 - 20,000	5.0V	2	AT40K10-2AJC	84J	Commercial
			AT40K10-2AQC	100T1	(0°C to 70°C)
			AT40K10-2RQC	100Q4	
			AT40K10-2BQC	144L1	
			AT40K10-2CQC	160Q1	
			AT40K10-2DQC	208Q1	
10,000 - 20,000	5.0V	2	AT40K10-2AJI	84J	Industrial
			AT40K10-2AQI	100T1	(-40°C to 85°C)
			AT40K10-2RQI	100Q4	
			AT40K10-2BQI	144L1	
			AT40K10-2CQI	160Q1	
			AT40K10-2DQI	208Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

AT40K20/AT40K20LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
20,000 - 30,000	5.0V	2	AT40K20-2AJC	84J	Commercial
			AT40K20-2AQC	100T1	(0°C to 70°C)
			AT40K20-2RQC	100Q4	
			AT40K20-2BQC	144L1	
			AT40K20-2CQC	160Q1	
			AT40K20-2DQC	208Q1	
			AT40K20-2EQC	240Q1	
20,000 - 30,000	5.0V	2	AT40K20-2AJI	84J	Industrial
			AT40K20-2AQI	100T1	(-40°C to 85°C)
			AT40K20-2RQI	100Q4	
			AT40K20-2BQI	144L1	
			AT40K20-2CQI	160Q1	
			AT40K20-2DQI	208Q1	
			AT40K20-2EQI	240Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com

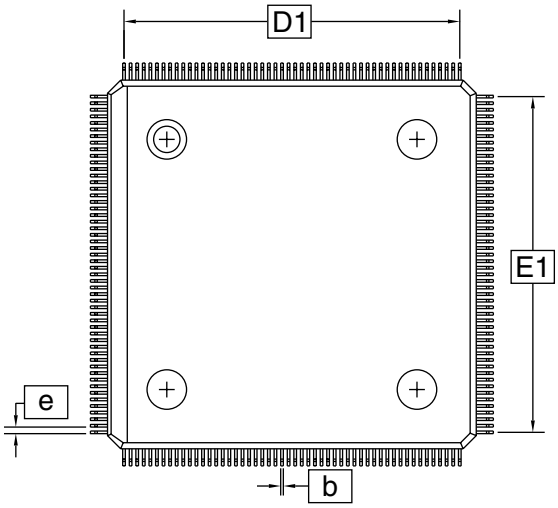
AT40K40/AT40K40LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
40,000 - 50,000	5.0V	2	AT40K40-2FQC	304Q1	Commercial (0°C to 70°C)
40,000 - 50,000	5.0V	2	AT40K40-2FQI	304Q1	Industrial (-40°C to 85°C)

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

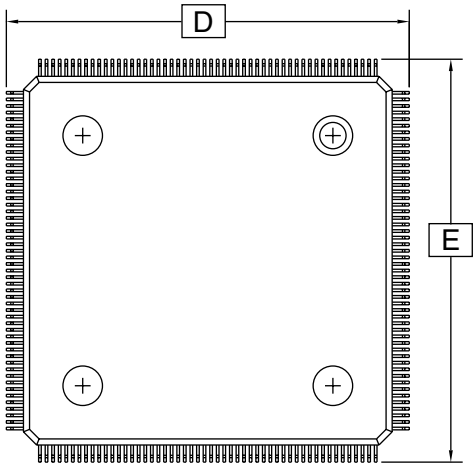
Packaging Information

208Q1 – TQFP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

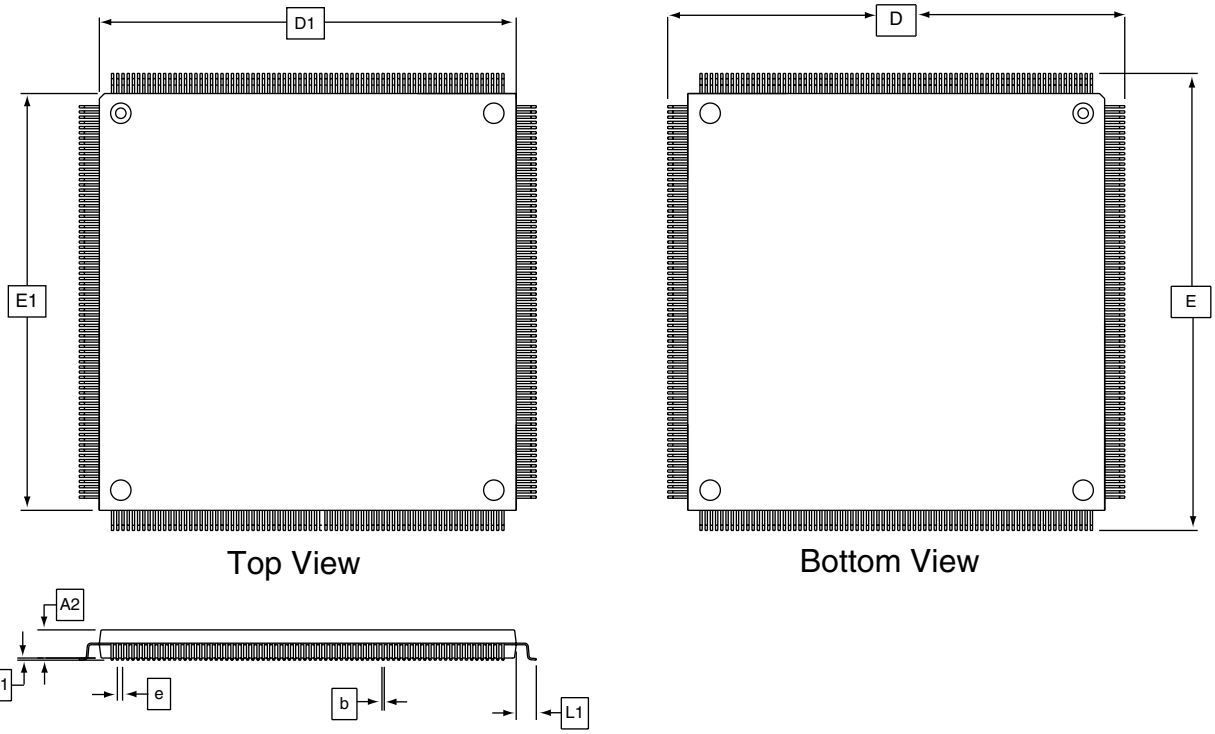
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25		0.50	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17		0.27	4
L1	1.30 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q1	A

304Q1 – PQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.55	3.80	4.05	
D		42.60 BSC		3
D1		40.00 BSC		2, 4
E		42.60 BSC		3
E1		40.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation JA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at Datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**304Q1,** 304-lead, 40 x 40 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	304Q1	A

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