YM2610 Datasheet

1. FM – 4 Channels on 4 operators, DAC compatable with YM3016
2. SSG – 3 operators, compatable with YM2149 (Atari ST), 4th operator is Noise
3. L/R – Sound channels out
4. ADPCM-A – 6 channels 18.5 KHz, 16 MB Sample ROM size, 256 B min size of sample, 1 MB max
5. ADPCM-B – 1 channel 1.8-55.5 KHz, 16 MB Sample ROM size, 256 B min size of sample, 16 MB max, compatable with YM2608
6. Master clock – 8MHz
7. 5V single power supply
8. 64-pin plastic SDIP

Prime function

The basic function of YM2610 can be divided roughly into four sound source part of FM sound source, SSG sound source, and ADPCM sound source.

1) FM sound source part

The basic function of the FM sound source part is the same as OPN(YM2203).

Pronunciation mode	Four operator FM method and six sound pronunciation simultaneously.
Algorithm	Eight kinds.
Parameter	The register address and refer to the FM sound source part.
LFO function	Sine wave LFO. Pitch (PM) and, it modulates amplitude (AM). The LFO frequency is changeable. AM on/off is possible of PMS, the AMS control, and each operator.
Compound sine wave synthesis	One sound is possible in six sounds. Timer function Two kinds of timers of A and B.
Output control	On/off of L and R.

2) SSG sound source part

The SSG sound source part is the same as OPN excluding the output method.

Pronunciation form	Three rectangular liquid sounds + white noise.
Function of each data	Refer to the register address.
Output	It outputs it from one terminal by internal mixing.
I/O port	Eight bit general purpose I/O port x2

3) ADPCM sound source part

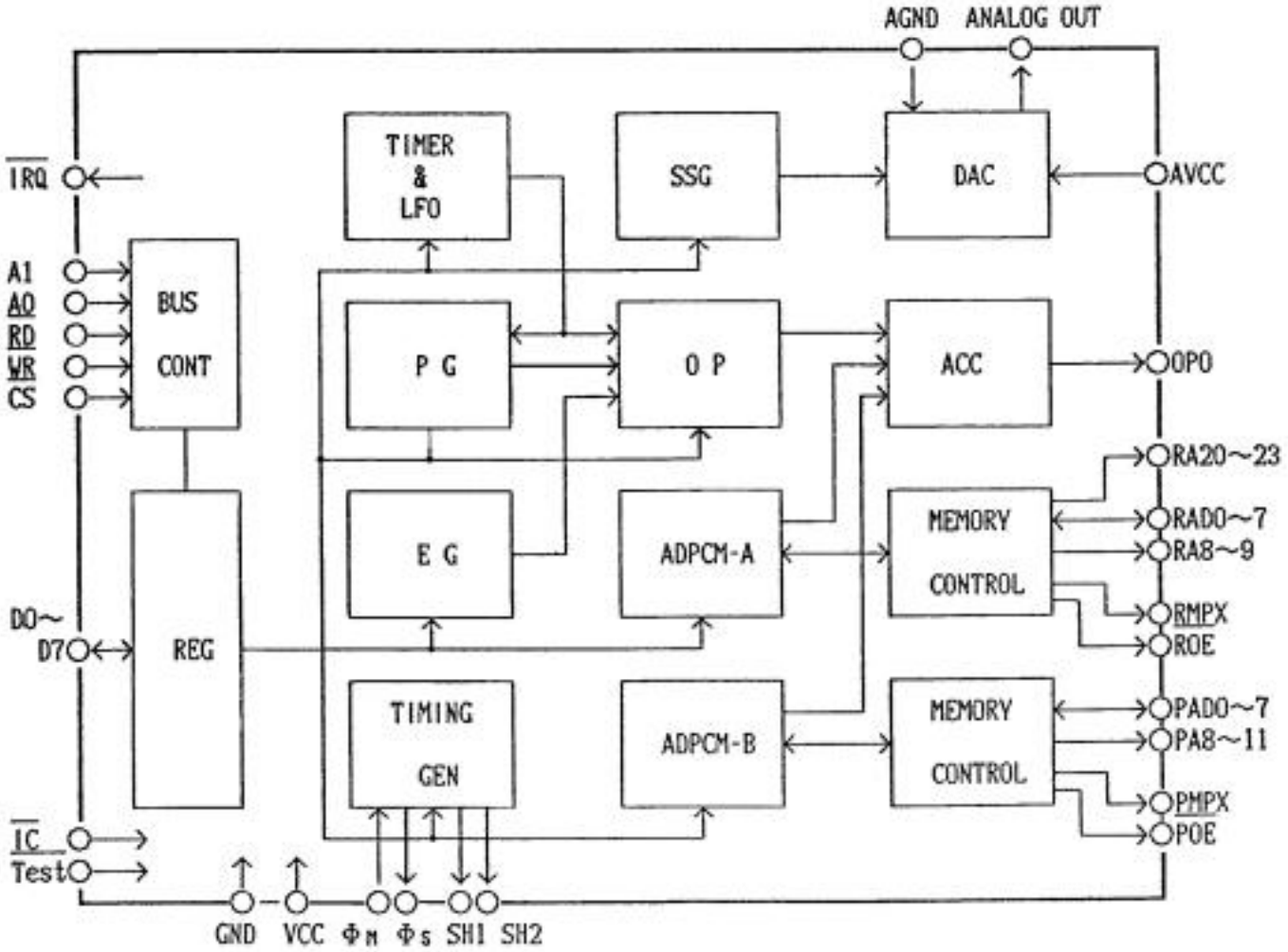
Speech analysis, synthesis, and external memory control of ADPCM sound source part. It is composed of the AD/DA conversion function.

Sampling rate	18.5 kHz , 1.8kHz-55.5kHz
AD/DA conversion	8-bit
ADPCM analysis	4-bit
Linear interpolation rate	55.5kHz
Data memory	Memory that external RAM-ROM
Output control	On/off of L and R.
No sound discrimination	The state under the analysis of a no sound can be identified.

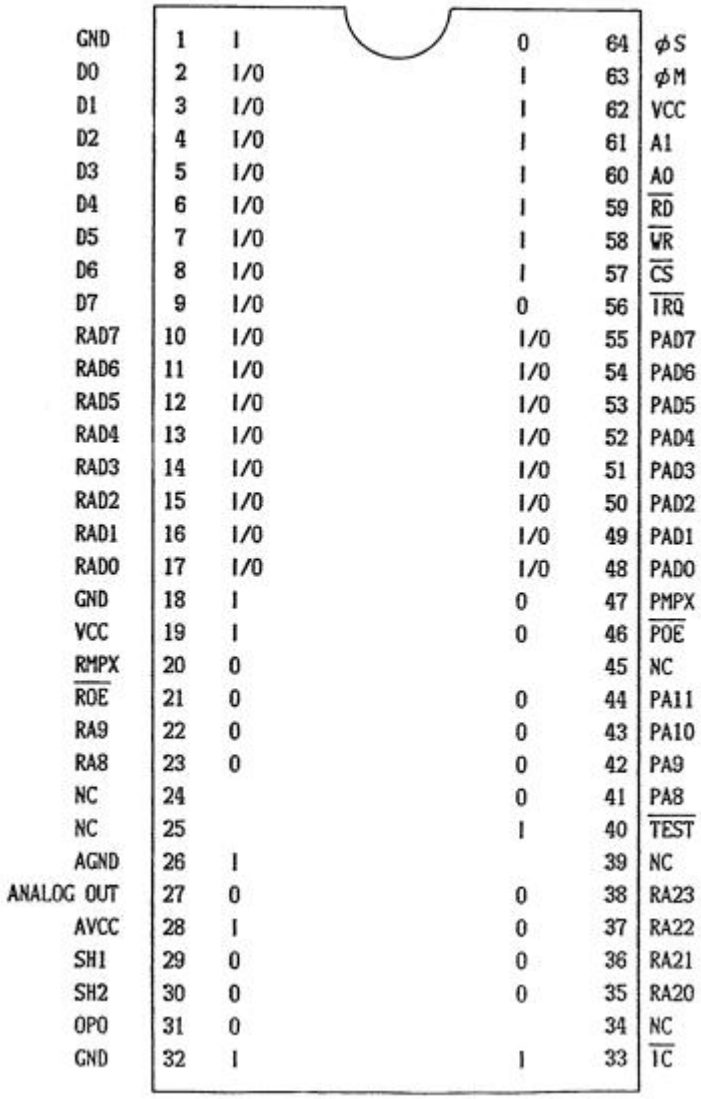
4) DAC

Exclusive use DAC YM3016 is used.

Block diagram



Terminal arrangement chart



GND	1	I	0	64	øS
D0	2	I/O	I	63	øM
D1	3	I/O	I	62	VCC
D2	4	I/O	I	61	A1
D3	5	I/O	I	60	A0
D4	6	I/O	I	59	/RD
D5	7	I/O	I	58	/WR
D6	8	I/O	I	57	/CS
D7	9	I/O	0	56	/IRQ
RAD7	10	I/O	I/O	55	PAD7
RAD6	11	I/O	I/O	54	PAD6
RAD5	12	I/O	I/O	53	PAD5
RAD4	13	I/O	I/O	52	PAD4
RAD3	14	I/O	I/O	51	PAD3
RAD2	15	I/O	I/O	50	PAD2
RAD1	16	I/O	I/O	49	PAD1
RAD0	17	I/O	I/O	48	PAD0
GND	18	I	0	47	PMPX
VCC	19	I	0	46	/POE
RMPX	20	0		45	NC
/ROE	21	0	0	44	PA11
RA9	22	0	0	43	PA10
RA8	23	0	0	42	PA9
NC	24		0	41	PA8
NC	25		I	40	/TEST
AGND	26	I		39	NC
ANALOG OUT	27	0	0	38	RA23
AVCC	28	I	0	37	RA22
SH1	29	0	0	36	RA21
SH2	30	0	0	35	RA20
OPO	31	0		34	NC
GND	32	I	I	33	/IC

Terminal function

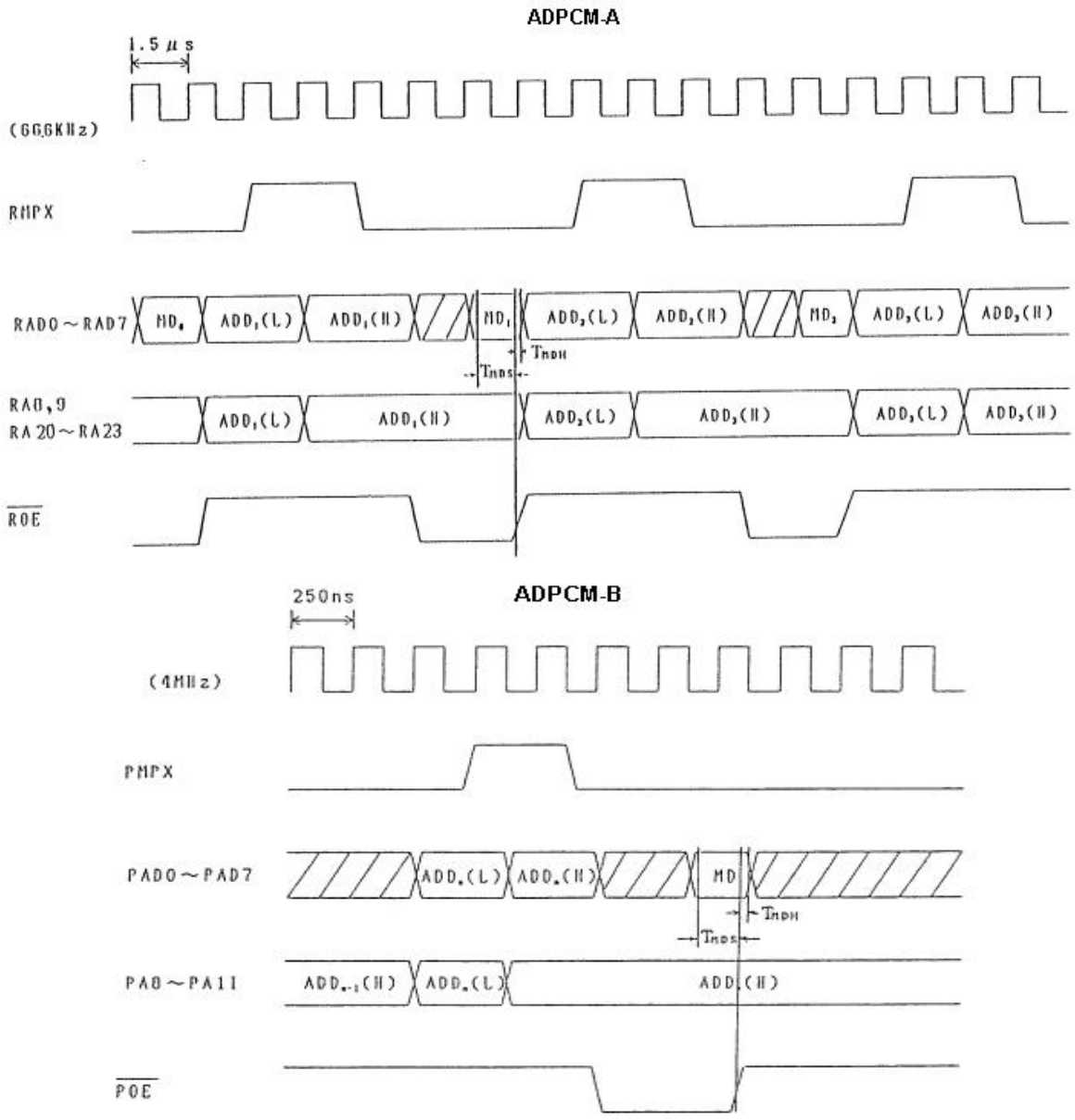
øM	Master clock (standard 8MHz) of OPNA is input.
øS,SH1,SH2	It is clock (øS) for DAC and signal (SH1, SH2) of the cycle.
OPO	It is a serial data of FM, ADPCM, and rhythm each sound source part output.
DO-D7	It is passing of interactive data of 8bit. CPU and data are exchanged.
/CS, /RD, /WR, A1, A0	Data passing (D0-D7) is controlled.
/IRQ	The interrupt signal is output. It is an open drain output.
ANALOG OUT	It is an analog output terminal in the SSG sound source part. It is source for an output.
RAD0-RAD7	Each signal of address (A0-A7), data input (D0-D7) of ADPCM-A
RA8-RA9	Each signal of address (A8-A9) of ADPCM-A
RA20-RA23	Each signal of address (A10-A14) of ADPCM-A
/ROE	ADPCM-A /OE
RMPX	Address control for data access of ADPCM-A
PAD0-PAD7	Each signal of address (A0-A7), data input (D0-D7) of ADPCM-B
PA8-PA11	Each signal of address (A8-A11)) of ADPCM-B
/POE	ADPCM-B /OE
PMPX	Address control for data access of ADPCM-B
/TEST	It is a terminal for the test of LSI.
GND,AGND	It is a ground terminal.
Vcc, AVcc	It is a power supply terminal of +5V.

Data bus control

The data bus control of read/write etc. of addressing and data is done with /CS, /WR, /RD, A1, A0.
The table shows the allocation of the register address at this time and the control mode of the register.

Content of data passing control

/CS	/RD	/WR	A1	A0	D0-D7	Mode
0	1	0	0	0	$00~ $10	SSG
					$1F~$20	ADPCM-B
					$2F~$30	FM
					$30~$B6	FM 1,2
0	1	0	0	1	$00~ $10	SSG
					$1F~$20	ADPCM-B
					$2F~$30	FM
					$30~$B6	FM 1,2
0	1	0	1	0	$00~$2F	ADPCM-A
					$30~$B6	FM 3,4
0	1	0	1	1	$00~$2F	ADPCM-A
					$30~$B6	FM 3,4
0	0	1	0	0	$00~$0D	SSG



ADPCM-A

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
00	DM	-	AON						DUMP/ADPCM-A On
01	-		ATL						Total Level
02	0	0	0	0	0	0	0	0	Test
08~0D	L	R	-	AC L					Output Select, Channel Select
10~15	Address								Start Address (L)
18~1D	Address								Start Address (H)
20~25	Address								End Address (L)
28~2D	Address								End Address (H)

ATL = all "0" – 0 db(silence)

ADPCM-B

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
10	Start	-		Repeat	-			Reset	Control 1
11	L	R	-						Control 2
12	Address								Start Address (L)
13	Address								Start Address (H)
14	Address								End Address (L)
15	Address								End Address (H)
16	-								-
17	-								-
18	-								-
19	Frequency								Delta-N (L)
1A	Frequency								Delta-N (H)
1B	Volume								EG Control
1C	B	-	A5	A4	A3	A2	A1	A0	Flag Control

Frequency ADPCM-B = [(Delta-N (H)+Delta-N (L)) / 256] x 55.5 KHz
(***Example:*** Delta-N (H)=85, Delta-N (L)=33, Frequency = 18,050 KHz)
(***Example:*** Delta-N (H)=101, Delta-N (L)=71, Frequency = 22,050 KHz)
(***Example:*** Delta-N (H)=203, Delta-N (L)=42, Frequency = 44,100 KHz)

YM2610 ADPCM-B Codec

```
#include <math.h>

static long stepsizeTable[ 16 ] =
{
        57, 57, 57, 57, 77,102,128,153,
        57, 57, 57, 57, 77,102,128,153
};
```

```
int YM2610_ADPCM-B_Encode( short *src , unsigned char *dest , int len )
{
	int lpc , flag;
	long i , dn , xn , stepSize;
	unsigned char adpcm;
	unsigned char adpcmPack;

	xn		= 0;
	stepSize	= 127;
	flag		= 0;

	for( lpc = 0 ; lpc < len ; lpc++ )
	{
		dn = *src - xn;
		src++;

		i = ( abs( dn ) << 16 ) / ( stepSize << 14 );
		if( i > 7 ) i = 7;
		adpcm = ( unsigned char )i;

		i = ( adpcm * 2 + 1 ) * stepSize / 8;

		if( dn < 0 )
		{
			adpcm |= 0x8;
			xn -= i;
		}
		else
		{
			xn += i;
		}

		stepSize = ( stepsizeTable[ adpcm ] * stepSize ) / 64;

		if( stepSize < 127 )
			stepSize = 127;
		else if( stepSize > 24576 )
			stepSize = 24576;

		if( flag == 0 )
		{
			adpcmPack = ( adpcm << 4 ) ;
			flag = 1;
		}
		else
		{
			adpcmPack |= adpcm;
			*dest = adpcmPack;
			dest++;
			flag = 0;
		}
	}

	return 0;
}
```

```
int YM2610_ADPCM-B_Decode( unsigned char *src , short *dest , int len )
{
	int lpc , flag , shift , step;
	long i , xn , stepSize;
	long adpcm;

	xn			= 0;
	stepSize	= 127;
	flag		= 0;
	shift		= 4;
	step		= 0;

	for( lpc = 0 ; lpc < len ; lpc++ )
	{
		adpcm = ( *src >> shift ) & 0xf;

		i = ( ( adpcm & 7 ) * 2 + 1 ) * stepSize / 8;
		if( adpcm & 8 )
			xn -= i;
		else
			xn += i;

		if( xn > 32767 )
			xn = 32767;
		else if( xn < -32768 )
			xn = -32768;

		stepSize = stepSize * stepsizeTable[ adpcm ] / 64;

		if( stepSize < 127 )
			stepSize = 127;
		else if ( stepSize > 24576 )
			stepSize = 24576;

		*dest = ( short )xn;
		dest++;

		src += step;
		step = step ^ 1;
		shift = shift ^ 4;
	}

	return 0;
}
```

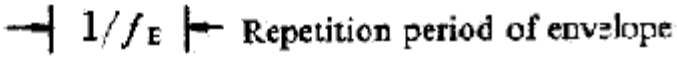
SSG

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
00	Fine Tune								Channel-A Tone Period
01	-				Coarse Tune				
02	Fine Tune								Channel-B Tone Period
03	-				Coarse Tune				
04	Fine Tune								Channel-C Tone Period
05	-				Coarse Tune				
06	-			Noise Frequency					Noise Period
07	-		/Noise			/Tone			/Enable
08	-			M	Level				Channel-A Amplitude
09	-			M	Level				Channel-B Amplitude
0A	-			M	Level				Channel-C Amplitude
0B	Fine Tune								Envelop Period
0C	Coarse Tune								
0D	-			CONT	ATT	ALT	HOLD		Envelop Shape Cycle

Fnoise = Fmaster / Noise Frequency
Fa,b,c = Fmaster / Fine Tune
M - Mode
When M=0, the level is determinated by 16 level selection
When M=1, the level is determinated by common 5 bit output of the envelope generator

D7	D6	D5	D4	D3	D2	D1	D0
/	/	/	/	SSG-EG			

No.	D3	D2	D1	D0	Envelope shape
0	1	0	0	0	
1	1	0	0	1	
2	1	0	1	0	
3	1	0	1	1	
4	1	1	0	0	
5	1	1	0	1	
6	1	1	1	0	
7	1	1	1	1	



FM

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
21	Test								LSI ,M Test Data
22	-				LFO	FREQ CONT			LFO ,M Freq Control
24	Timer-A								Timer-A 8
25	-				Timer-A				Timer-A 2
26	Timer-B								Timer-B ,M Data
27	Mode		Reset B A		Enable B A		Load B A		Timer-A/B ,M Control, 2 CH ,M Mode
28	Slot				-		CH		Key-ON/OFF
29~2F	-								
31~3E	-	DT			MULTI				Detune/Multiple
41~4E	-	TL							Total Level
51~5E	KS		-	AR					Key Scale/Attack Rate
61~6E	AM	-		DR					AMON/Decay Rate
71~7E	-			SR					Sustain Rate
81~8E	SL				RR				Sustain Level/Release Rate
91~9E	-				SSG-EG				SSG-Type Envelop Control
A1,A2	F-Num 1								F-Numbers/Block
A5,A6	-		Block		F-Num 2				
A9,AA	2 CH * F-Num 1								2 CH - 2 Slot F-Numbers/Block
AD,AE	-		2CH*Block		2CH*F-Num2				
B1,B2	-		FB		Connect				Self Feedback/Connection
B5,B6	L	R	AMS	-	PMS				LR SEL./AM,PM SENS

FREQ CONT = 0~7 - 3.98 | 5.56 | 6.02 | 6.37 | 6.88 | 9.63 | 48.1 | 72.2 (Hz)
LFO = “1” - On
PMS = 0~7 - 0 |±3.4|±6.7|±10 |±14 |±20 |±40 |±80
AMS = 0~3 - 0 | 1.44| 5.9 | 11.8 (dB)
AM = “1” - On