1. Pin description

1.1 System Interface

- PROC_RESET* Processor reset (input)

When asserted, this asynchronous active low input immediately halts and resets the processor and all on-chip peripherals. The processor restarts execution after the 5th rising edge of the clock after PROC_RESET* was de-asserted.

- **FPGA_RESET*** reconfigurable unit reset (input)

FPGA_RESET* is the manual reset of the FPGA. This function reset the configuration download logic. FPGA_RESET* is internally pulled up to VCC and is active at a low level. Each time FPGA_RESET* is activated, the FPGA enters Manual Reset lifephase.

- **ERROR*** Processor error (open-drain output with pull-up)

This active low output is asserted when the processor is halted in error mode.

- **WDOG*** Watchdog timeout (open-drain output with pull-up)

This active low output is asserted when the watchdog timer has expired and remains asserted until the watchdog timer is reloaded with a non-null value.

- **BEXC*** Bus exception (input)

This active low input is sampled simultaneously with the data during an access to the external memory. If asserted, a memory error is generated.

- **M0, M1, M2** reconfigurable unit configuration mode (Input)

[CFG] The configuration mode pins are used to define the configuration settings of the ATF697FF reconfiguration unit. ATF697FF reconfiguration unit samples the configuration mode pins each time a configuration clear cycle is ended.

Caution: The mode pins should not be changed during power-on-reset or manual reset.

- **CCLK** – Reconfigurable unit configuration clock (bi-directional)

CCLK function provides the clock signal used by the configuration logic. Depending on the mode used for configuration download procedure, CCLK function is configured as input or output. For slave mode, the CCLK is configured as an input whereas for master mode, it is configured as an output. When configured in input mode, CCLK is pulled up to VCC with an internal resistor

- **D0** Configuration Data Bus LSB (Input/Output)

D0 is used to transfer configuration data from or to the FPGA configuration SRAM. D0 is used for serial mode configuration.

- **INIT** (Input/Output)

INIT is used as an error indicator regarding configuration logic. INIT is a bidirectional open drain I/O pulled up to VCC with an internal resistor.

- **CON** Configuration Status Indicator (Input/Output)

CON is the FPGA configuration start and status pin. It is a bidirectional open drain I/O pulled up to VCC with an internal resistor.

- **HDC** High During Configuration (output)

HDC indicates that the configuration download is on-going. HDC is an output and is polarized to a high logic level during the configuration.

- **LDC** Low During Configuration (output)

LDC indicates that the configuration download is on-going. LDC is an output and is polarized to a low logic level during the configuration.

- **CS0*** Configuration Chip Select (Input/Output)

CS0* is an active low chip select used during configuration. It is only available configuration download slave serial mode 1

- **CSOUT** Configuration Cascade Output (Output)

CSOUT is the configuration pin used to enable the downstream device in an FPGA cascade chain.

- **CHECK*** Configuration Check (Input/Output)

CHECK* pin is used to enable the CHECK function when combined with a configuration download start.

- **OTS*** Dual Use Tri State (Input)

OTS* pin is used to tri-state all the FPGA pins configured as user I/Os.

1.2 Clock Interface

- **CLK** Processor reference clock (input)

This input provides a reference to generate the internal clock used by the processor and the internal peripherals.

- **BYPASS** Processor PLL bypass (input with pull-down)

This active high input is used to bypass the internal PLL. When asserted, the processor is directly clocked from the external reference clock. When de-asserted, the processor receives its clock from the internal PLL.

This signal shall be kept static and free from glitches while the processor is operating, as it is not sampled internally. Changing the signal shall only be performed while the processor is under reset otherwise the processor's behavior is not predictable.

- **LOCK** PLL lock (output)

When asserted, this active high output indicates the PLL of the processor is locked at a frequency corresponding to four times the frequency of the external processor reference clock.

Caution: this signal is de-asserted as soon as the PLL unlocks.

- **SKEW[1:0]** Clock tree skew (input with pull-down)

These input signals are used to programme the skew on the internal triplicated clock trees.

These signals shall be kept static and free from glitches while the processor is operating, as they are not sampled internally. Changing these signals shall only be performed while the processor is under reset otherwise the processor's behavior is not predictable.

- **GCK1 -GCK8** Global clock (input)

8 differential global clocks are available on the reconfigurable unit.

- **FCK3 – FCK4** Fast clock (input)

1 fast clock is available on the reconfigurable unit part. (The 2 pins are multiplexed all together).

1.3 Memory Interface

- **A[27:0]** Address bus (output)

The lower 28 bits of the 32 bit address bus carry instruction or data addresses during a fetch or a load/store operation to the external memory. The address of the last external memory access remains on the address bus whenever the current access can be made out of the internal cache.

- **D[31:0]** Data bus (bi-directional)

The 32-bit bi-directional data bus serves as the interface between the processor and the external memory. The data bus is only driven by the processor during the execution of integer & floating-point store instructions and the store cycle of atomic-load-store instructions. It is kept in high impedance otherwise. However: only D[31:24] are used during an access to an 8-bit area

D[15:0] are used as part of the general-purpose I/O interface whenever all the memory areas (ROM, SRAM & I/O) are 8-bit wide and the SDRAM interface is not enabled

- **CB[7:0]** Check bits (bi-directional)

These signals carry the EDAC checkbits[1] during a write access to the external memory and are kept in high impedance otherwise. This applies whatever the EDAC activation or not.

Note: 1. While only 7 bits are useful for EDAC protection, CB[7] is implemented to enable programming of FLASH memories and takes the value of MCFG3.tcb[7].

- **OE*** Output enable (output)

This active low output is asserted during a read access to the external memory. It can be used as an output enable signal when accessing PROM & I/O devices.

- **READ** Read enable (output)

This active high output is asserted during a read access to the external memory. It can be used as a read enable signal when accessing PROM & I/O devices.

- **WRITE*** Write enable (output)

This active low output is asserted during a write-access to the external memory. It can be used as a write enable signal when accessing PROM & I/O devices.

- **RWE*[3:0]** PROM & SRAM byte write-enable (output)

These active low outputs provide individual write strobes for each byte-lane on the data bus: RWE*[0] controls D[31:24], RWE*[1] controls D[23:16], RWE*[2] controls D[15:8] and RWE*[3] controls D[7:0], and they are set according to the transaction width (word/half-word/byte) and the bus width set for the respective area.

- **BRDY*** Bus ready (input)

When driven low, this input indicates to the processor that the current memory access can be terminated on the next rising clock edge. When driven high, this input indicates to the processor that it must wait and not end the current access.

1.3.1 PROM

- **ROMS*[1:0]** PROM chip-select (output)

These active low outputs provide the chip-select signals for decoding the PROM area. ROMS*[0] is asserted when the lower half of the PROM area is accessed (0x00000000 0x0FFFFFFF), while ROMS* [1] is asserted when the upper half is accessed (0x10000000 0x1FFFFFFF).

1.3.2 SRAM

- **RAMS*[4:0]** SRAM chip-select (output)