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Low power high performance priority encoder using 2D-array to 3D-array conversion

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Abstract

This paper discusses priority encoder and its designing complexity for higher number of input bits, i.e., 64, 128, 256, and so on. In order to reduce the complexity and power consumption of the circuit, a new circuit with three-directional (3D) array priority encoder is introduced. This 3D-array priority encoder circuit reduces the power consumption by 23.908 % and the transistors count by 19.572 % using 180nm technology, by using 45nm technology power consumption is reduced by 23.588% and transistors count remains same when compared to the existing two-directional (2D) array priority encoder. In this paper 64-bit input priority encoder is implemented using Cadence Virtuoso GPDK-180 nm and 45nm technology.

Keywords: Priority encoder; critical path; power delay product; GPDK-180nm and 45nm technology; power consumption; transistors

1. Introduction

Priority encoder plays a vital role in modern day digital circuits, which are usked extensively in the areas of network routing, data compressing and data matching. Number of circuits was proposed to reduce power, area and delay. A priority encoder takes "2^n" bits as input and gives "n" bit output. Priority encoder checks every input and gives the position inputs of the most significant one. High-performance priority encoder is important when the input data width is large, however there are problems like, high power and excessive delay.

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To reduce these problems some new circuits are implemented. The basic priority encoders are like 4:2 priority encoder, 8:3 priority encoder and so on. Prior studies focussed on reduction in the transistors count, latency and power consumption [1][2][3] but did not focus on optimized Power Delay Product (PDP). The previously improved circuits are applied in some applications like increments/decrements [4], comparators [5], ternary content-addressable memory, IP's [7][8][9], error detection and correction [9]. The drastic increase of incoming bits creates the priority encoder design to be complicated. In the design of multi-match priority encoder [11] Nguyen XT et al. converted the one-directional priority encoder into two-directional priority encoder. To implement this multi-match priority encoder a basic 4-bit or 8-bit or 16-bit priority encoder can be used to design the 64-bit priority encoder. 2D-array priority encoder [12] was used to reduce the delay.

The remaining part of this paper is arranged in the following format. Section 2 briefly deals with related work, section 3 gives the analysis of the circuit, section 4 describes implementation, and section 5 summarizes results and analysis.

2. Related work

For reducing the power consumption in electronic devices, several circuits were proposed in literature. In parallel priority look-ahead 64-bit priority encoder architecture [1], there are 64 bits which are divided into eight parts. Each part contains 8-bits hence total of 8 x 8 =64. The individual 8-bits are input to the 8-input OR gates, in this way, this design have eight 8-input OR gates placed in parallel. All eight OR gates take eight 8-bits and generate eight single bit outputs. The eight single bit output is input to the 8-input priority encoder, and that priority encoder output is connected to eight 8-bit priority encoders which will generates the 6-bit output, by using this look-ahead architecture, delay and power consumption were reduced.

Propagation delay is reduced by using the prefixing scheme [2] and also same circuit is used for high and low priority evaluation, with scalable design structure. The static CMOS priority encoder [3] design gives low power and better speed compared to dynamic domino circuit.

In this paper [4] a multilevel folding and multilevel look-ahead techniques are implemented using dynamic CMOS logic. This will decrease the power consumption and also increases the performance. The design of full parallel priority encoder [5] is enhanced in a way to improve the performance of comparator circuit. Some other techniques like GDI [6] are used to reduce the transistor count. If the transistor count is reduced automatically, usage of power is reduced. The performance of priority encoder depends on delay and power, these parameters reduced when the circuit is optimized by implementing a new circuit static-dynamic parallel priority look-ahead [7] architecture.

The large amount of data bits are divided and send the required bits to the input [8]. For example 1024 bits are divided into eight 128 bits and processes. These particular set of bits are separated bits used in IP's [9]. In the same way the data placed in matrix format, stored in memories and encoded in paper [10].

In multi match 64-input priority encoder [11] architecture, all the 64-bit inputs are divided into eight groups, each group contain 8-bits. The eight bits are input to the 8-input OR gates, in this way, there are eight OR gates placed in parallel, which generates eight single bit outputs.

The output of OR gates are input to the 8-input priority encoder, it will generates 3-bit output. In this multi-match circuit there is 8-input MUX circuit which takes same inputs given to OR gates. The output of 8-input MUX generates one 8-bit output, that is given to another 8-input priority encoder, it will generates another 3-bit output. Combination of both priority encoder outputs gives 6-bit output.

Figure 1 (a) shows the multi-match priority encoder and how the MUX selection pins are taken from the output of first priority encoder. For MUX selection lines the output of 8:3 priority encoder generates 3-bit, in that three bits the first bit is given to first column of four parallel multiplexers, second bit is connected to second column of multiplexers where two multiplexers are in parallel and third bit is connected to third stage of multiplexer's shows in figure 1 (b).

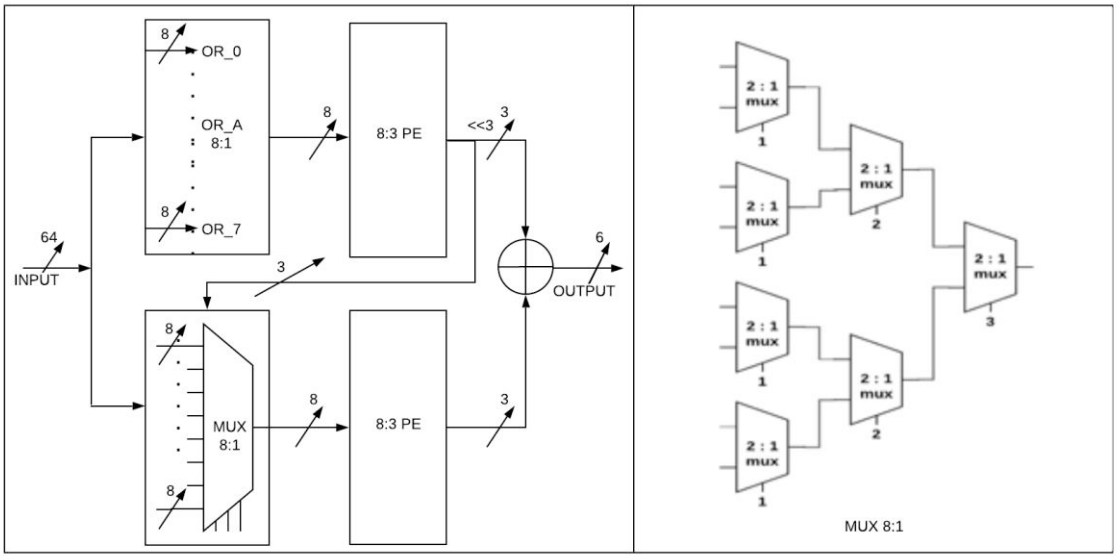

Fig. 1. (a) Multi-match priority encoder 64:6; (b) MUX 8:1 internal design [11].

The circuit design of 1D-array to 2D-array conversion priority encoder [12] is same as multi-match priority encoder [11], but selection pins for 2D-array MUX design is taken from output of OR gates. There are eight OR gates placed in parallel which generates eight single bit outputs used as selection pins for MUX. By this modification critical path of the circuit is reduced, but power consumption is increased by 27%. The circuit of 1D-array to 2D array priority encoder is shown in figure.2 (a), and selection pins for 8-input MUX is shown in figure.2 (b).

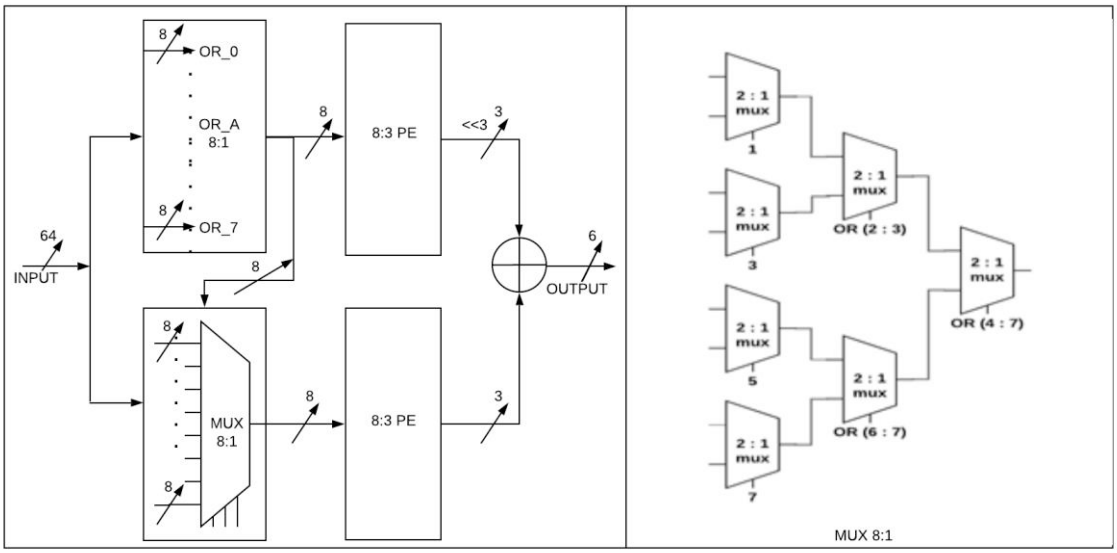

Fig. 2. (a) 2D array-priority encoder 64 : 6; (b) MUX 8:1interna design[12].

3. Architecture of 3D-array priority encoder

3D-array 64:6 priority encoder circuits consist of multiple blocks, which are OR_A, OR_B, PE_A, PE_B, MUX_A, MUX_B and PE 4:2. This OR_A block consists of sixteen 4-input OR gates those are OR0, OR1 and so on up to OR15, these sixteen 4-input OR gates are placed in parallel. PE_A block consists of sixteen 4:2 priority encoder, those are PE0, PE1 and so on up to PE15 are placed in parallel. Next block is OR_B block, which has four 4-input OR gates from OR0 to OR3, and the OR_B block take the input from OR_A block. The output from OR_B block is given to PE 4:2. Another block is PE_B, in this block there are four 4:2 priority encoder placed in parallel. MUX_A block consists of six 2:1 MUX which are placed to get 2-bit output, and the selection lines of MUX_A block is taken from PE 4:2. In the same manner MUX_B block is also designed, in this there are four 8-input MUX circuits which are placed in parallel and output of these 8:1 MUX are given to two 2-input MUX circuits. The selection lines for MUX_B circuit are taken from PE 4:2 priority encoder output and MUX_A output. The architecture of 3D-array priority encoder circuit is shown in figure 3.

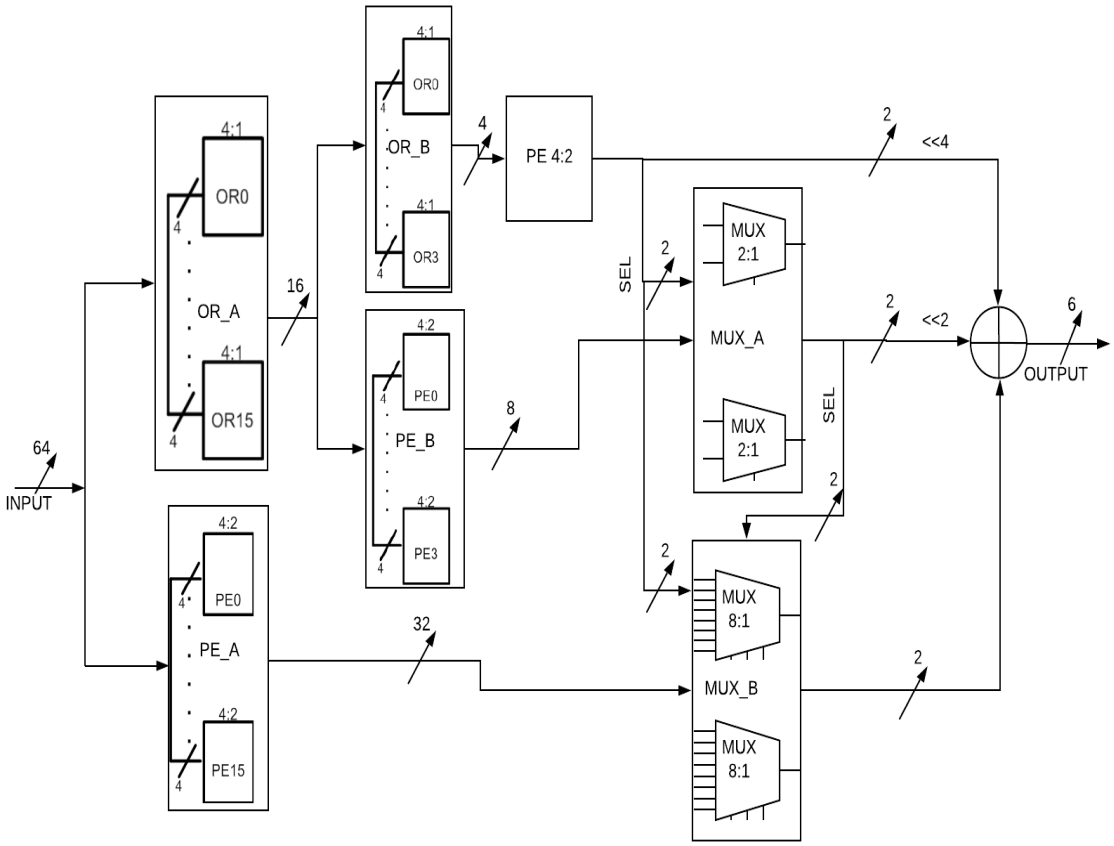

Fig. 3. 3D-array 64:6 priority encoder architecture.

4. Implementation

All the circuits are implemented in transistor level by using Cadence Virtuoso in CMOS 180nm technology, the input voltage of this circuit is 1.8v.

In the 3D-array 64:6 priority encoder, the 64 input bits are divided into sixteen groups, each group contains 4-

bits, total 16 x 4 = 64-bits. For example a0, a1, a2, a3 to p0, p1, p2, p3, are 64-inputs, these group of four bits are given to sixteen 4-input OR gates present in OR_A block as shown in figure 4. This OR_A block generates sixteen single bit outputs which are or0, or1, or2 so on up to or15. These or0, or1, or2, or3 till or15 are divided into four groups like or0, or1, or2, or3 into one group and or4, or5, or6, or7 into another group so on. These sixteen outputs are given to four 4:2 priority encoders present in PE_B block, which generates four 2-bit outputs. The outputs coming from PE_B are given to 4:1 MUX labelled as MUX_A block which generates 2-bit output.

In the meanwhile outputs which are generated by OR_A such as or0, or1, or2 so on up to or15 are given to another four 4-input OR gates labelled as OR_B block. OR_B block generates four single bit output, these outputs are given to one 4:2 priority encoder (PE 4:2). PE 4:2 generates 2-bits as output that is q4 and q5, this output acts as selection line for 4:1 mux's (MUX_A). This MUX_A generates one 2-bit output that is q2, q3. The internal structure of MUX_A block is shown in figure 5.

In parallel, all 64-input bits which are a0, a1, a2, a3, b0, b1, b2, b3 and so on, p0, p1, p2, p3 are given to sixteen 4:2 priority encoders which is named as PE_A block. PE_A block generates sixteen 2-bit outputs. The outputs coming from PE_A block is given to 16:1 MUX which is named as MUX_B block. The internal circuit of MUX_B 16:1 is shown in figure 6, where 2-bit 16:1 MUX generates one 2-bit output as q0 and q1. The selection line for 16:1 MUX (MUX_B) is taken from output of 4:2 priority encoder (PE 4:2) and 4:1 MUX (MUX_A) that is q2, q3, q4 and q5. The output of 4:1 MUX, 16:1 MUX and 4:2 priority encoder are combined to generate a 6-bit output.

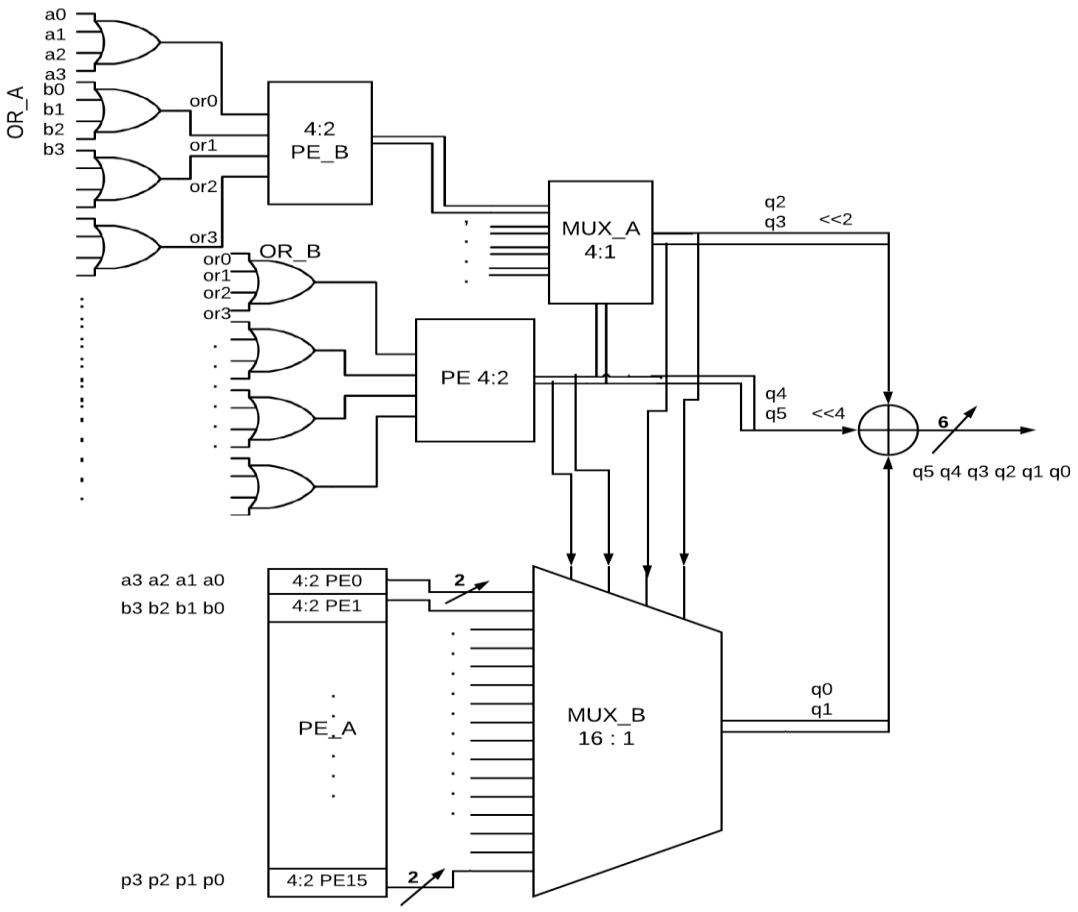

Fig. 4. 3D-array priority encoder circuit.

In normal priority encoder, one input bit is given to one input line, but in 3D-array priority encoder all the input bits are converted into matrix format. The L-bit input data is spitted into I × J bits, that look like 2D matrix format. The output of the conventional priority encoder comes from one direction but in 3D-array priority encoder the output comes from three different directions. Figure 4 shows the shifting of MUX_A output by 2<< and PE 4:2 output shifted by 4<< and by adding these output bits to MUX_B output gives 6-bit output. The internal circuit of MUX_A and MUX_B are shown below.

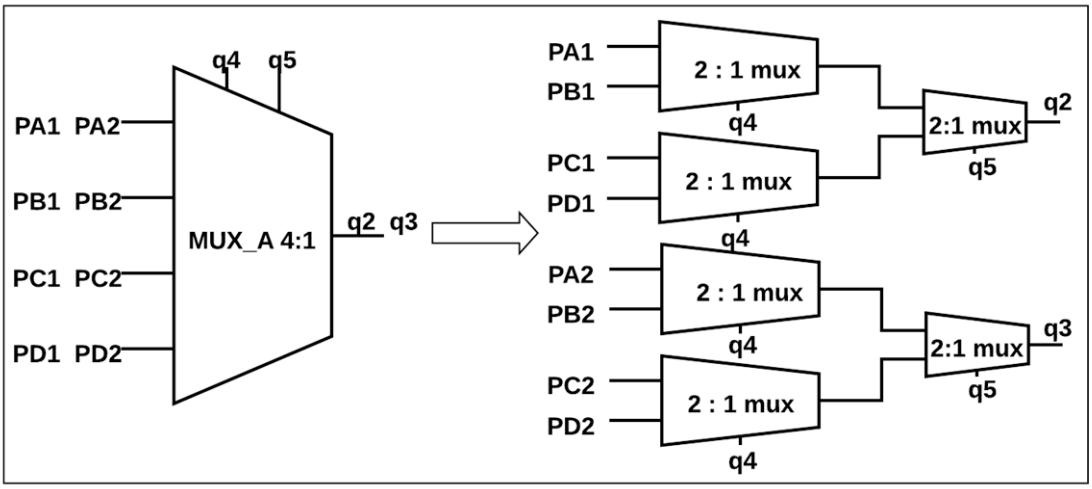

Fig. 5. MUX_A 4:1 internal design.

The 16:1 MUX design consists of four 8:1 MUX and two 2:1 MUX which generates 2-bit output. The internal circuit of MUX_B 16:1 is shown in figure 6.

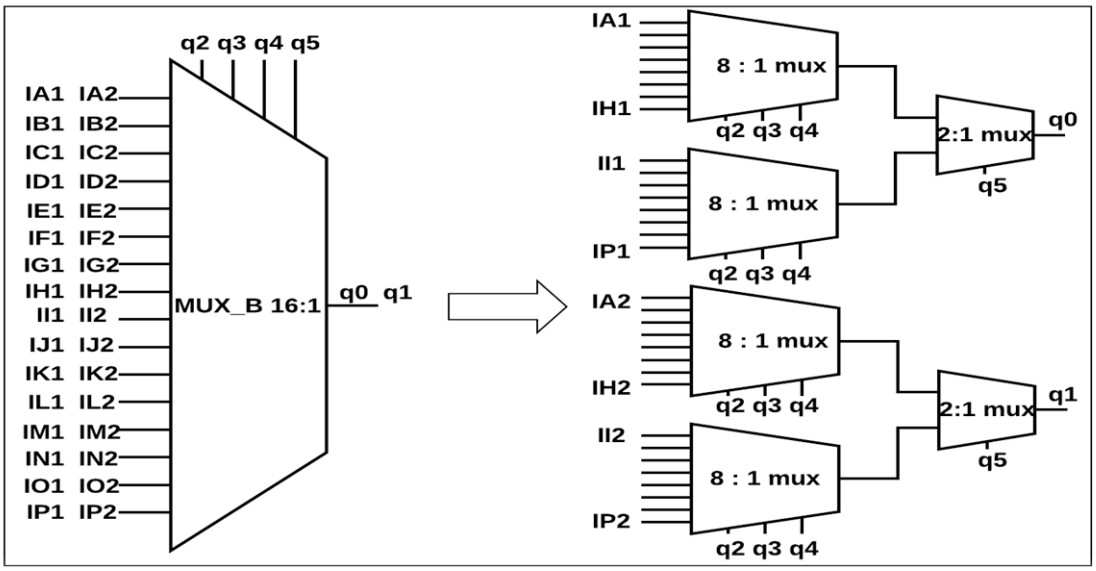

Fig. 6. MUX_B 16:1 internal design.

5. Results

By implementing and analyzing the both 2D-array priority encoder [12] and 3D-array priority encoder, power consumption of 2D-array priority encoder is 0.3480mW, 3D-array priority encoder is 0.2648mW. The reduction of power is 23.908 % for 3D-array priority encoder. In the same way the transistors required to implement the 2D-array priority encoder is 1686, and for 3D-array priority encoder is 1356. The number of transistors required is reduced by 19.572% when 3D-array priority encoder was used. Compared to the 2D-array priority encoder [12], 3D-array priority encoder delay is increased by 8.183 % and Power delay product is improved by 17.681%. Table 1 shows comparison for both 2D-array priority encoder [12] circuit and 3D-array priority encoder circuit.

Table 1. Comparison between 2D array and 3D array priority encoder using 180nm technology using 180nm technology.

Design	Power (mW)	Number of transistors	Delay (Ps)	PDP
2D-array 64 bit[12]	0.3480	1686	703.03	244.654
Proposed 3D-array 64 bit	0.2648	1356	760.56	201.396
Improvement %	23.908	19.572	-8.183	17.681

The critical path for the 2D-array priority encoder is given in table 2.

Table 2. Critical path for 2D array priority encoder[12] using 180nm technology

Module	Delay(Ps)
8-input OR	136.9
8-input MUX	482.2
8-input PE	83.93
Total	703.03

The critical path for 3D-array priority encoder is given in table 3.

Table 3. Critical path for 3D array priority encoder using 180nm technology.

Module	Delay(Ps)
4-input OR	83.92
4-input OR	83.92
4-input PE	39.52
4-input MUX	156
16-input MUX	397.2
Total	760.56

Table 4. Comparison between 2D array and 3D array priority encoder using 45nm technology.

Design	Power (mW)	Number of transistors	Delay (Ps)	PDP
2D-array 64 bit[12]	0.001488	1686	477.98	0.71123
Proposed 3D-array 64 bit	0.001137	1356	552.62	0.62832
Improvement %	23.588	19.572	-15.615	11.6572

The critical path for the 2D-array priority encoder is given in table 5.

Table 5. Critical path for 2D array priority encoder[12] using 45nm technology.

Module	Delay(Ps)
8-input OR	85.32
8-input MUX	363.1
8-input PE	29.56
Total	477.98

The critical path for 3D-array priority encoder is given in table 6.

Table 6. Critical path for 3D array priority encoder using 45nm technology.

Module	Delay(Ps)
4-input OR	18.33
4-input OR	18.33
4-input PE	29.56
4-input MUX	144.3
16-input MUX	342.1
Total	552.62

6. Conclusion

A new circuit has been designed, which is high-performance 2D to 3D array priority encoder. By using this 2D to 3D conversion, the consumption of power is reduced by 23.908%, transistor count is reduced by 19.572% and power delay product is improved by 17.681% by using 180nm technology, by using 45nm technology the power consumption is reduced by 23.588% and PDP is improved by 11.657% comparing with 2D-array priority encoder. But delay of the 3D-array priority encoder is increased 8.183% and 15.615% by simulating with 180nm and 45nm technology when compared to 2D-array priority encoder, it has shown that, by decreasing technology, power consumption is reduced and delay increased. In future the circuit is designed to reduce delay and maintain the power delay product much better.

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