POWER

PS_ON
PWR_OK

File: Ultra-MSX_Power.kicad_sch

MSX ENGINE

ENG_INT
M1
RD
WR
IORQ
RESET
WAIT
HALT
CAS_IN
CAS_MOT
CAS_OUT
KBD_WAIT
CAPS_LED
KANA_LED
KEY_CLICK
KEY_DIR
JOY_OUT_A
JOY_OUT_B
TRG1_A
TRG1_B
TRG2_A
TRG2_B
PRT_CMD_CS
PRT_STB_WR
PRT_BSY_RD
STROBE
PRT_BUSY
RFSH
MREQ
I2C_AD1
I2C_AD2
I2C_AD3
I2C_AD4
I2C_SCL
I2C_SDA
SLT_WAIT
SLTSL1
BUSDIR1
SLTSL2
BUSDIR2
SLTSL3
BUSDIR3
REDWC
INDEX
MOTEA
DRVSA
DRVSB
MOTEB
DIR
Step
WDATA
WGATE
TRK00
WPT
RDATA
SIDE1
DSKCHG
ROE
RMPX
POE
PMPX
ROM_A_EN
ROM_A_WP

MSXE_CS
SUP_INT
CAS0
RAS1
RAS0
OE_VT
CLK_IO
CLK_BUS
Z80M
BCK_B
BCK_A
RGT_B
RGT_A
LFT_B
LFT_A
FWD_B
FWD_A
AUD_RST
A[0..31]
MSIZE
ROM_CS
MCAS[0..3]
MRAS[0..3]
SD_DET_B
SD_MISO/DAT0
SD_CMD
SD_DAT3
SD_CLK
SD_DAT1
SD_MOSI/DAT2
SD_DET_A
PAL_CLK_IN
PAL_CLK_OUT
VDP_RD
VDP_WR
VDP_WAIT
NTSC_CLKO
VDP_RST
CS1
CS2
CS12
IORQ_Z80
MREQ_Z80
M1_Z80
D[0..15]
SLT_RST
SLT_DIR
Z80_D[0..7]
COL[0..7]
PD[0..7]
SSTX-
SSTX+
SSRX-
SSRX+
CC1/HPD
USB2_D-
USB2_D+
USB1_D-
USB1_D+
AUX-
AUX+
CLK_PSG
PSG_CS

File: Engine_FPGA.kicad_sch

PROCESSOR

RESET
RD
WR
ENG_INT
IORQ
M1
CLK_BUS
VDP_INT
HALT
WAIT
PWR_OK
SUP_INT
MSXE_CS
Z80M
PS_ON
RAS0
CAS0
RAS1
RAM_CS[0..7]
A[0..31]

D[0..15]
AUD_INT
CLK_IO
CLK_VDP
SLT_INT
MSIZE
UMCS
BHEN
BLEN
MEM_RD
MEM_WR

File: Ultra-MSX_CPU.kicad_sch

MEMORY

A[0..31]
D[0..15]
ROM_CS
RAM_CS[0..7]
MCAS[0..3]
MRAS[0..3]
SD_CMD
SD_CLK
SD_MISO/DAT0
SD_DAT1
SD_MOSI/DAT2
SD_DAT3
SD_DET_B
SD_DET_A

UMCS
MSIZED
BHEN
BLEN
MEM_RD
MEM_WR

File: Ultra-MSX_RAM.kicad_sch

VIDEO

A[0..31]
VDP_RST
VDP_RD
VDP_WR
VDP_WAIT
VDP_INT
NTSC_CLKO
PAL_CLK_IN
PAL_CLK_OUT

CLK_VDP
D[0..15]
ROUT
GOUT
BOUT
CSYNC
VSYNC
HSYNC

File: Ultra-MSX_VDP.kicad_sch

PERIPHERALS

AUD_L
AUD_R
CAS_MOT
CAS_OUT
CAS_IN
TRG1_A
TRG1_B
TRG2_A
TRG2_B
BCK_B
BCK_A
RGT_B
RGT_A
LFT_A
LFT_B
FWD_B
FWD_A
JOY_OUT_A
JOY_OUT_B
JOY_FWD
JOY_BCK
JOY_RGT
ROUT
GOUT
BOUT
CSYNC
HSYNC
VSYNC
SSRX-
SSRX+
SSTX-
SSTX+
CC1/HPD
USB2_D-
USB2_D+
AUX+
AUX-

PRT_BUSY
STROBE
PD[0..7]
KANA_LED
KEY_DIR
CAPS_LED
KBD_TYPE
COL[0..7]
REDWC
INDEX
MOTEA
DRVSA
DRVSB
MOTEB
DIR
Step
WDATA
WGATE
TRK00
WPT
RDATA
SIDE1
DSKCHG
USB1_D-
USB1_D+

File: Ultra-MSX_Peripherals.kicad_sch

SLOTS

A[0..31]
SLT_RST
CLK_BUS
RD
WR
IORQ_Z80
MREQ_Z80
SLT_DIR
RFSH
M1_Z80
SLT_WAIT
SLT_INT
CS1
SLTSL1
BUSDIR1
CS2
SLTSL2
BUSDIR2
CS12
SLTSL3
BUSDIR3

Z80_D[0..7]
SLT1_SND
SLT2_SND
SLT3_SND_L
SLT3_SND_R

File: Ultra-MSX_Slots.kicad_sch

AUDIO

A[0..31]
D[0..15]
CLK_PSG
AUD_RST
AUD_INT
PSG_CS
ROE
RMPX
POE
PMPX

OE_VT
RD
WR
FMA-CH1_L
FMA-CH2_R
PSG_SND
ROM_A_EN
ROM_A_WP

File: Ultra-MSX_Audio.kicad_sch

AUDIO AMPLIFIERS

SLT1_SND
SLT2_SND
SLT3_SND_L
SLT3_SND_R
PSG_SND
AUD_L
AUD_R
FMA-CH1_L
FMA-CH2_R
I2C_SCL
I2C_SDA
I2C_AD1
I2C_AD2
I2C_AD3
I2C_AD4
AUD_INT

File: Ultra-Amplifier.kicad_sch

LEGEND:

A[0..31]

CPU address
range 0-31.

BA[0..15]

Buffered
Adress range.

Tips:
1. Specify different Resets?

Floppy drive:
https://github.com/SukkoPera/OpenFlops

USB-chips
R5F10JGCAFB#V0
NUC123LD4AN0

ATF1502ASV-15JU44
(cpld)

Mechanical

Mounting Holes
H1 H2 H3 H4
GND

CPU HeatSink
HS1
GND

MSX Cartridge-dummies
Cart1 Cart2 Cart3

Case1

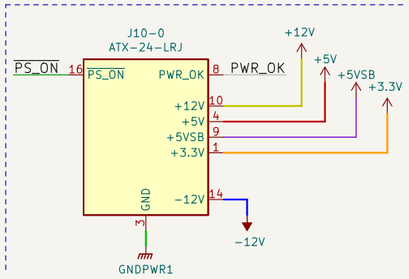
ULTRA-MSX

Size A3	Date 2022-06-05	Id 1/10	File Ultra-MSX.kicad_sch
KiCad E.D.A. kicad (6.0.5)			Rev A-A

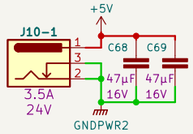
LICENSE

Primary Power input

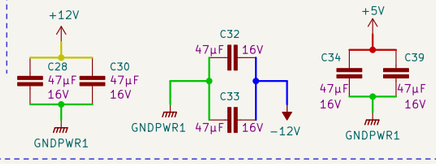
ATX connector



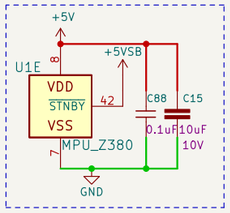
Barreljack Backup



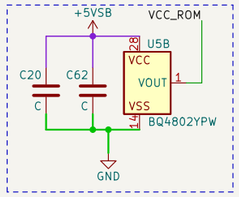
Main Decoupling



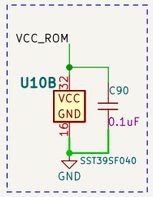
CPU Power



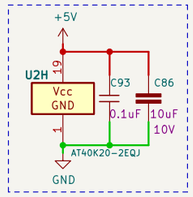
CLOCK & Supervisor Power



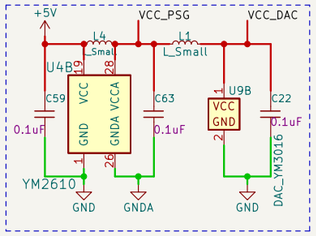
BIOS ROM Power



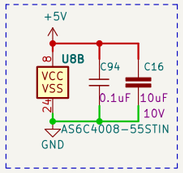
MSX Engine Power



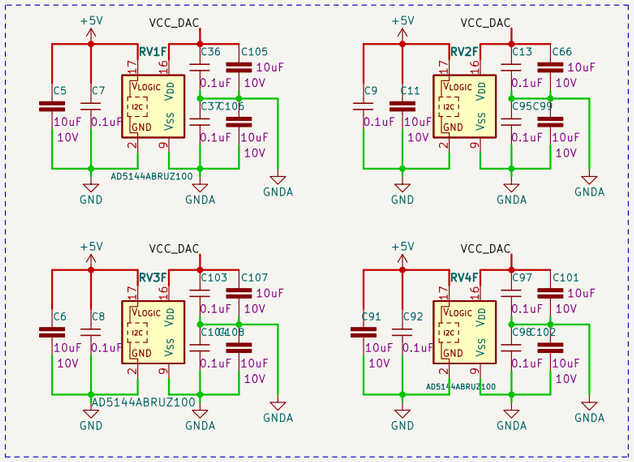
SOUND power



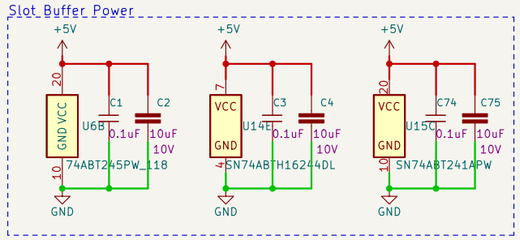
SRAM Power



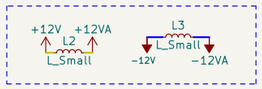
Digital Potentiometer power



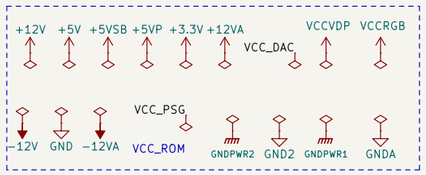
Slot Buffer Power



Filtering for analogue components



Power-nets:



LEGEND:

/PS_ON = from MB - when PSU is on,
this line will be grounded by a device on the MB.
PWR_OK = output from PSU, indicating that power-out
has stabilized

+5 VSB = Standby - supplies power when other lines are off.
can be used to power the device sending PS_ON.

GNDA = Analog ground.

GNDPWR1,2 = the incoming Ground from the PSU(s) connected to the board.

+5VP = External five volts from the CPLD-programmer.

Power-management:
----
https://www.embedded.com/adding-a-power-management-mcu-to-your-system-reduces-standby-energy-use/
--

EXTERNAL NETS:

PWR_OK ▷PWR_OK
PS_ON ◁PS_ON

ULTRA-MSX

/POWER/

Size	A3	Date	2022-06-05
KiCad E.D.A.	kicad (6.0.5)		

Rev	A-A
File	Ultra-MSX_Power.kicad_sch
Sheet	2/10

AT40K CPLD Configuration table:

CS	M2	M1	M0	
0	n/c	n/c	n/c	Pull CS to weak 1, when CS is User I/O
1	n/c	n/c	n/c	Pull CS to GND, for multi-fpga
n/c	1	1	1	Mode 0: Master Serial
n/c	1	1	0	Mode 1: Slave Serial
n/c	1	0	1	Mode 2: Slave Parallel
n/c	0	1	1	Mode 4: Synchronous RAM
n/c	0	0	1	Mode 6: Slave Parallel UP
n/c	0	0	0	Mode 7: Slave Serial, M(nr) pins free for direct control from DC(nr) and D(nr)-OUT connectors

U2A
AT40K20-2EQJ

U2B
AT40K20-2EQJ

U2D
AT40K20-2EQJ

U2E
AT40K20-2EQJ

U2C
AT40K20-2EQJ

U2F
AT40K20-2EQJ

U2G
AT40K20-2EQJ

SW1
SW_KJ06RTT

J12
Conn_02x05_Odd_Even

← CPLD Programming

SPI-converter chips for programming CPLD:

MCP23S08-E/SO

switch-examples:

KJ06RTT = 6,2 x 15,24 mm (6pos)
219-6LPSTR = 7,62 x 16,71 mm (6pos)
DS04-254-2-05BK-SMT = 6,2 x 16,24 mm (5 pos)

Suggestion for memory controller, instead of FPGA:
MKE14F512VLL16
(mcu)

DO (data out)
CHECK
CON
INIT/ERR
CI (clock in)
CO (clock out)

VCC (VTref)
GND
N/C

ATDH40M (motherboard)
+
ATDH40D208 (daughterboard)

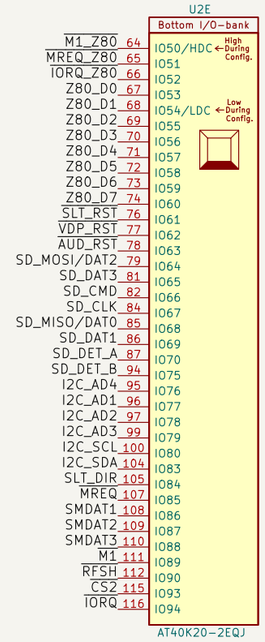
AT40KEL-DK

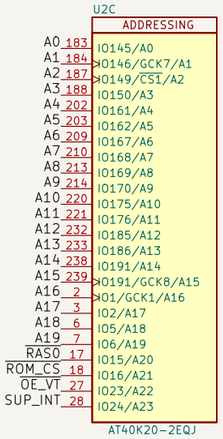
Internal signalling Guide:

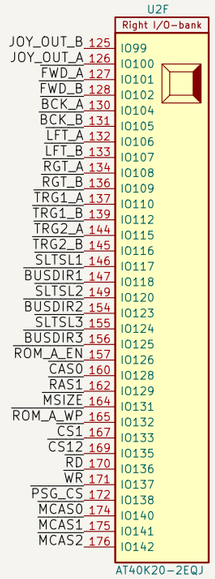
B_CLK -> CLK_IO

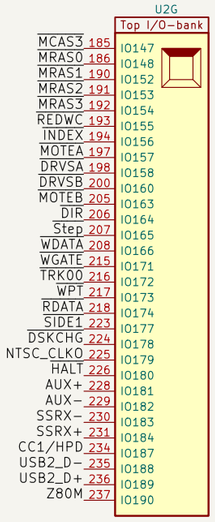
USB & Display Port
VIDEO-CHIP
KEYBOARD
JOYSTICK
PRINTER
ADDRESSING
DATA
SOUND-CHIP
Voltage-converters
Sample Rom
Micro-SD card
FLOPPY drive
Z80 inside of MSX-Engine

EXTERNAL NETS:
CLOCK SIGNALS
BIOS-CHIP
TAPE READER
EXPANSION SLOTS
RAM-CHIPS
System Control
I2C Signals

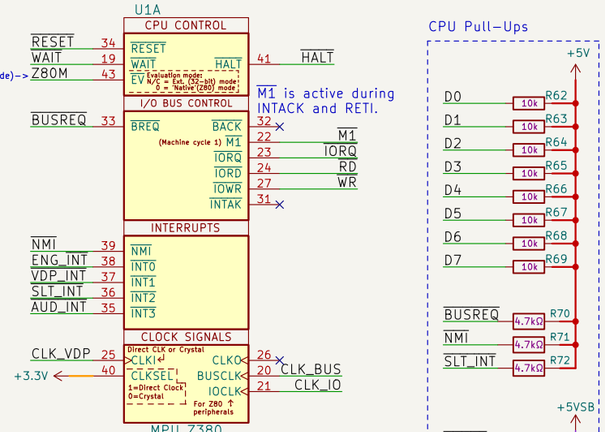


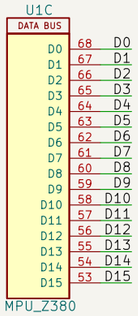


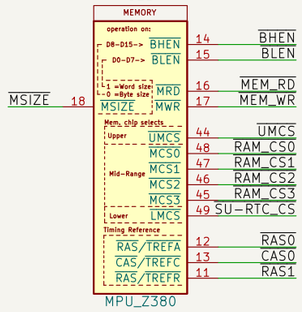


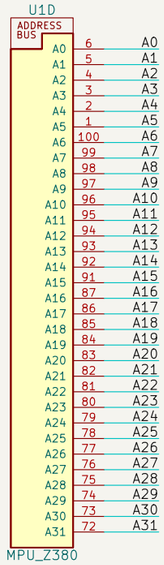


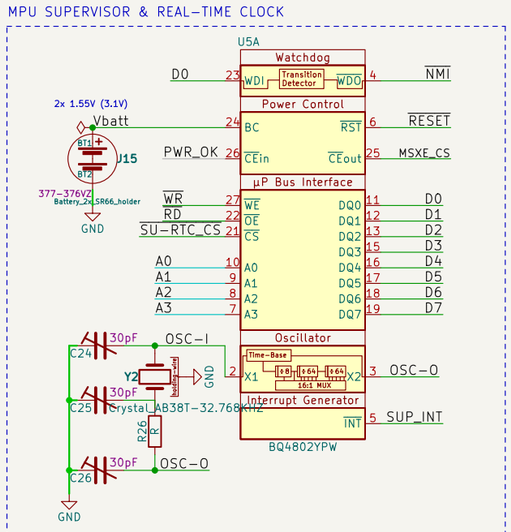
ULTRA-MSX			LICENSE
/MSX ENGINE/		Rev A-A	
Size A3	Date 2022-06-05	Id 3/10	File Engine_FPGA.kicad_sch
KiCad E.D.A. kicad (6.0.5)			

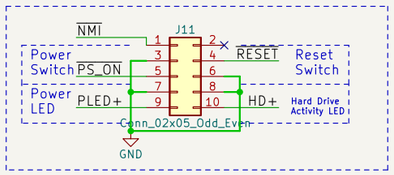












NMI address in MSX Bios:
0066h

You need a way to return the /NMI signal to
normal after the interrupt is accepted by the Z80,
otherwise you'd be having NMI's over & over again.
Probably would need some logic (a few 74xx IC's or something).

IIRC, address 0066h is used for a
File Control Block or something like that under DOS,
so that might be a problem. In BASIC a hook is called.

MEMORY MAPPING:

- have 512K available for direct addressing in combination with the standard FC/FD/FE/FF ports
- make another port available(which can accept 8bit,16bit, 32bit or even larger page numbers..fed sequentially)
for some sub-switching to a larger memory.
- to unload the processor with moving/clearing/copying one can add something as simple
as a microcontroller to move the memory around.

Reset-design:
https://semiengineering.com/respecting-reset/

Socket CPU:
--
M3 industries - 8468-21A1-RK-TP

https://www.digikey.se/en/products/detail/8468-21A1-RK-TP/3M6821A1-ND/1026489?utm_campaign=buynow&utm_medium=aggregator&curr=usd&utm_source=octopart

Reference design RTC:
https://e2e.ti.com/support/clock-timing-group/clock-and-timing/f/clock-timing-forum/792830/bq4802y-bq4802y-don-t-keep-clocking-in-vbc-mode

Chips integrated already into Z280:
---
256 byte Cache
High performance 16-bit Z-BUS interface or 8-bit Z80-compatible bus interface
MMU
Four 16-bit counter/timers
4 DMA channels
Full duplex UART
Burst mode memory access
Accelerated communication interface

MSX-engine chips:

PPI
---
v- 7400 (four 2-input NAND)
v- 7430 (x2) (8-input NAND)
v- 7432 (x3) (four 2-input OR)
v- 74273 (x2) (eight D-type flip-flop with reset; positive-edge trigger)
-74540 (Octal buffer/line driver; inverting)
-74541 (x3) (8-bit Buffer/Line Driver)
v- 74153 (x2) (two 4-input multiplexer)
v- 8255

Logic:
7x2 NAND + 4 NAND (18 NAND)
4x3 OR (36 NAND)
8x2 Flip-flop (96 NAND)
1x8-bit buffer +8 NOT (47 NAND)
3x8-bit buffer (117 NAND)
2x Mul (168 NAND)
2300 NAND

Total:
2782 GATES
--
Memory
---
v- 74138 (Decoder/demultiplexer, 3to8)
-74245 (x2) (octal Bus Transceiver)

Logic:
1x Dmul (84 NAND)
2x Tran (78 NAND)

Total:
162 GATES
--
VDP-support:
---
v- 7404 (hex inverter)

Logic:
6 NOT (6 NAND)
--

PSG
---
v- 7407 (hex-buffer)
v- 7474 (x3) (two D-type flip-flop with set & reset)
v- 7402 (four 2-input NOR)
v- 74157 x2 (four 2-input Multiplexer)

Logic:
1 buf (36 NAND)
3x2 Flip-flop (36 NAND)
4x NOR (16 NAND)
--
Total:
88 GATES
--
CPU

RP5C01 (x1) (real-time clock)
ATF16V8B (x3) (SPLD, 8 macrocell)
74175 (four D-type flip-flop with reset; positive-edge trigger)

Logic:
xx
3x8 MAC (1800 NAND)
4x Flip-Flop (24 NAND)

TOTAL GATES:
4862 GATES
@6 gates / LUT
811 LUTs

W. 25% overprovisioning
6078 Gates
1014 LUTs

Suggested chips:
3.3V:
XC95288XL-10BGG256C
XC95288XL-7FGG256I

--

TOTAL IO:
183 I/O

QUESTION:
--
How many of the chips are already replaced via the Z380?

Analogue chips:

74125 (four level-shifters - 3to5V)
ADM691A (Voltage monitor)
CXA1645 (RGB encoder)

EXTERNAL NETS:

A[0..31] D
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31

D[0..15] D
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

ENG_INT ENG_INT
WAIT WAIT
RESET RESET
HALT HALT
RD RD
WR WR
IORQ IORQ
M1 M1
CLK_BUS CLK_BUS
CLK_IO CLK_IO
CLK_VDP CLK_VDP
AUD_INT AUD_INT
SLT_INT SLT_INT
VDP_INT VDP_INT
Z80M Z80M
SUP_INT SUP_INT
MSXE_CS MSXE_CS

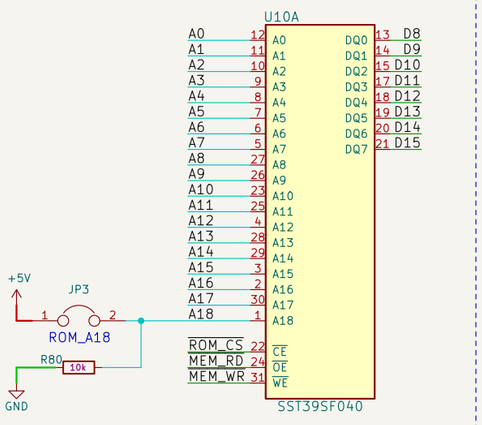
Memory Signals
MSIZE MSIZE
MEM_RD MEM_RD
MEM_WR MEM_WR
BHEN BHEN
BLEN BLEN
MEM_RD MEM_RD
MEM_WR MEM_WR
UMCS UMCS
RAM_CS[0..7] D
RAM_CS0 RAM_CS1 RAM_CS2 RAM_CS3
RAS0 RAS0
CAS0 CAS0
RAS1 RAS1

WATCHDOG signals
PWR_OK PWR_OK
PS_ON PS_ON

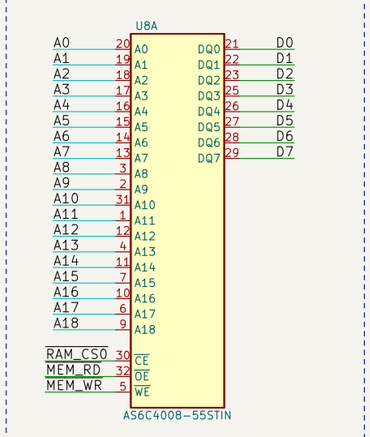
ULTRA-MSX

ULTRA-MSX			Listener
/PROCESSOR/		Rev A-A	
Size A3	Date 2022-06-05	Id 4/10	File Ultra-MSX_CPU.kicad_sch
KiCad E.D.A. kicad (6.0.5)			

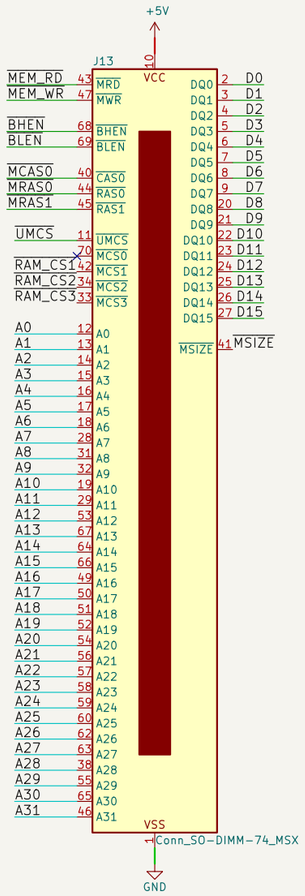
ROM/BIOS chip



RAM Chip



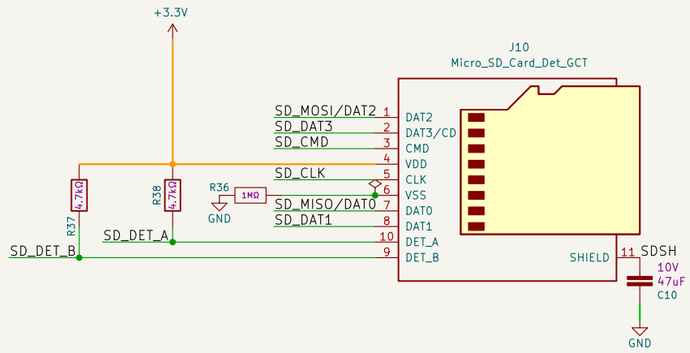
SDRAM module



MSX Memory-links:
---
https://hansotten.file-hunter.com/do-it-yourself/memory-mappers-slots/

Example of good Memory mapper
https://www.msx.org/wiki/Padial_LPE-4FMB-V8SKP

Talk to Jurjen Kranenborg
about the Z380 and system
design:
---
https://www.kranenborg.org/



MSX2SD
https://github.com/fbelavenuto/msxsdmapperv2

IDEtoSD:
https://goughlui.com/2019/02/03/tested-generic-sintechi-fc1307a-based-sd-to-ide-adapter-sd35vc0/

My own memory-module:
32 Address
16 Data
MHEN
LHEN
CS1
CS2
CS3
CS4
MEMRD
MEMWR

56 pins

SO-DIMM-144-modules:
64+4+8 = 76 I/O

Look into an address-decoder for interfacing
smaller address-bus memory chips with the CPU.

Priority Encoder is the name of one such.

Note:
The i80386SX uses 72-pin sims for memory-modules.

An example of an encoder/controller for a 386DX:
http://www.s100computers.com/My%20System%20Pages/80386%20Board/80386%20CPU%20Board.htm

Ram-chip suggestion:
CY62167ELL-45ZXIT (2 MB, 20 Address, 16 Data)

IS42S16320D-7BLI (512 MB, 14 Address, 16 Data)

Z80380 Evaluation Board

+CMOS 80380 MPU
*18.432 MHz Oscillator
+1 Socketed 48KB EPROM

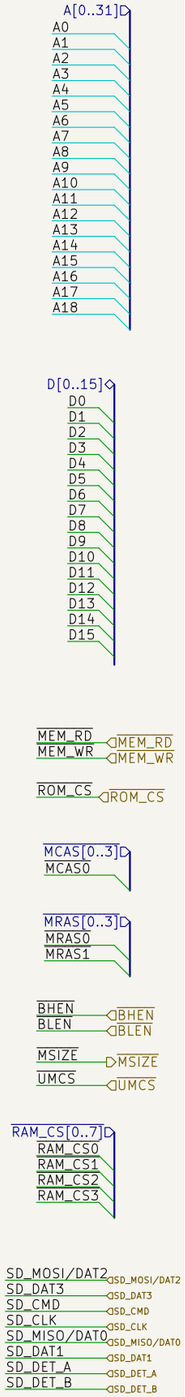
1 Socketed 128KB (128x8) SRAM

2 Unsocketed 128KB (1 Mb) DRAM Slots

Reset Switch
NMI Switch

Memory-slot suggestions:
G42V12352HR
HSEC8-137-01-L-DV-A

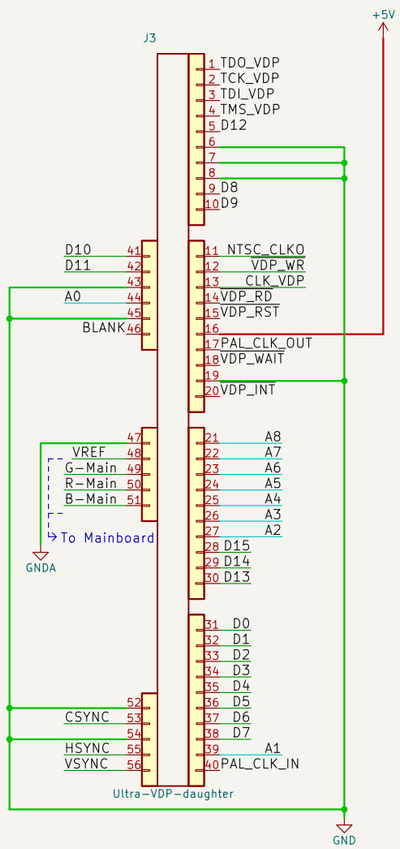
EXTERNAL NETS:



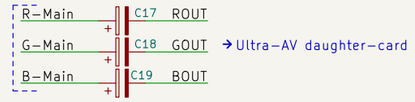
ULTRA-MSX

ULTRA-MSX		LICENSE
/MEMORY/	Rev: A-A	
Size: A3	Date: 2022-06-05	Id: 5/10	File: Ultra-MSX_RAM.kicad_sch
KiCad E.D.A. kicad (6.0.5)		

1.0. Daughter-card containing Video Display Processor



2. RGB-capacitors (big)

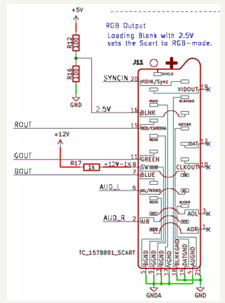


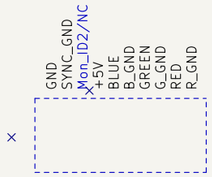
VTO – voltage Controlled Oscillator

Frequencies needed:
25.175 MHz
4.43361875 MHz
3.579545 MHz

3. SCART output

See 'Ultra-AV' daughter-card for schematics on connector.





Off-limits names

Headers:
J1
J2
J3
J4
J5
J6
J7
J11

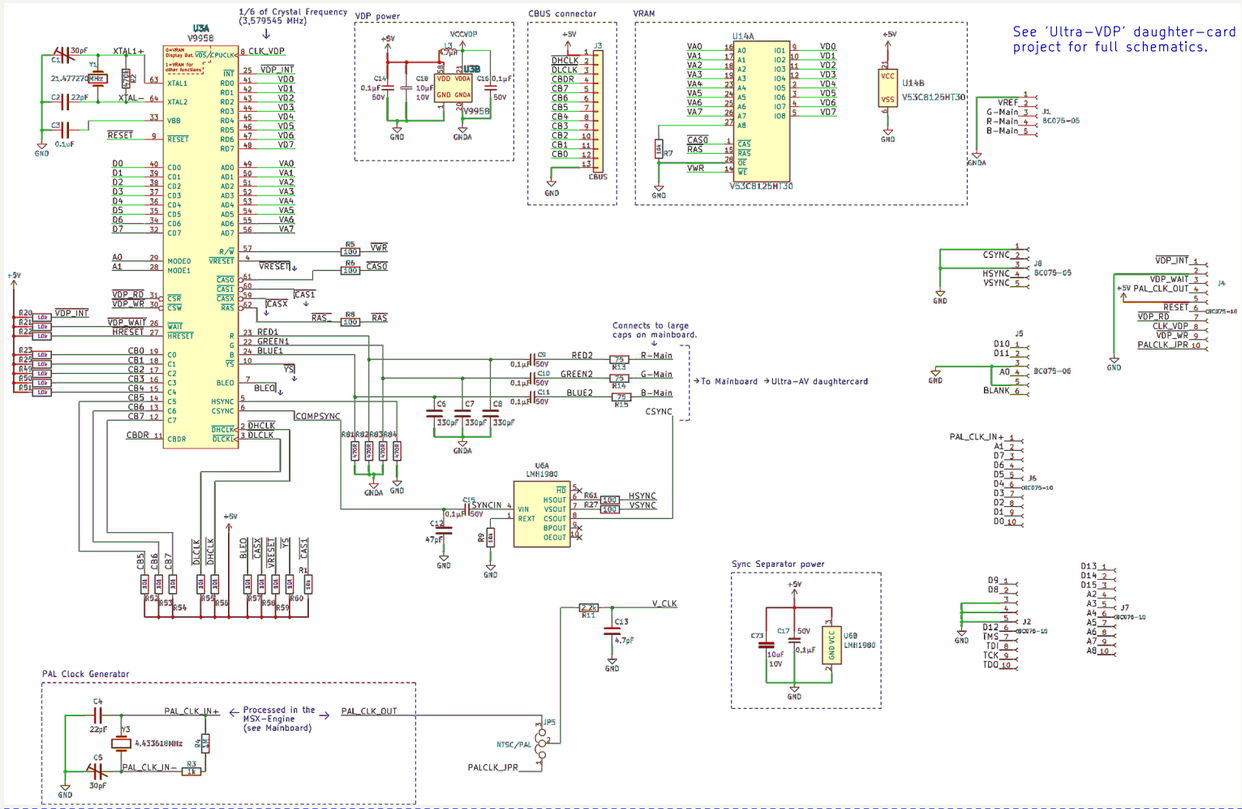
Chips:
U3
U6
U14

Crystals:
Y1
Y3

Caps:
C1
C2
C3
C9
C10
C11
C12
C13
C14
C15
C16
C73

Resistors:
R12
R16
R17

1.1. VDP-card schematic



Memory-suggestions:

Modern

IS42S16100H
IS45S16100H

Legacy

DisplayPort has a mode where it sends raw RGB down the wire, meaning a DP to VGA converter is "just" a DAC and maybe a presence detection EEPROM.

Example-chip:
PTN3356R1BSMP

VGA clocks:
640x400 (70Hz) – 25.175 MHz
640x480 (60Hz) – 25.175 MHz

Pal clocks:
704x576 (50Hz) – 4.43361875 MHz

NTSC clocks:
704x480 (60Hz) – 3.579545 MHz

https://www.msx.org/wiki/SCART_connector#Pinout_.28RGB_and_Composite_Video.29

EXTERNAL NETS:

VDP_INT ▷ VDP_INT
VDP_WAIT ▷ VDP_WAIT
VDP_RD ◁ VDP_RD
VDP_WR ◁ VDP_WR

NTSC_CLKO ◁ NTSC_CLKO
VDP_RST ◁ VDP_RST

CLK_VDP ◁ CLK_VDP
PAL_CLK_IN ◁ PAL_CLK_IN
PAL_CLK_OUT ◁ PAL_CLK_OUT

A[0..31]
A0
A1
A2
A3
A4
A5
A6
A7
A8

D[0..15]
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

ROUT ▷ ROUT
GOUT ▷ GOUT
BOUT ▷ BOUT

CSYNC ▷ CSYNC
HSYNC ▷ HSYNC
VSYNC ▷ VSYNC

ULTRA-MSX

ULTRA-MSX

/VIDEO/

Size A3	Date 2022-06-05	Sh 6/10	
KiCad E.D.A. kicad (6.0.5)			File Ultra-MSX_VDP.kicad_sch

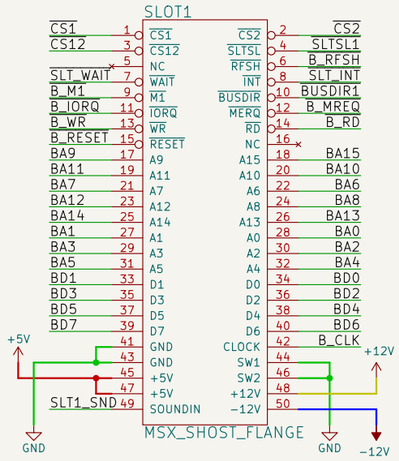
Rev A-A

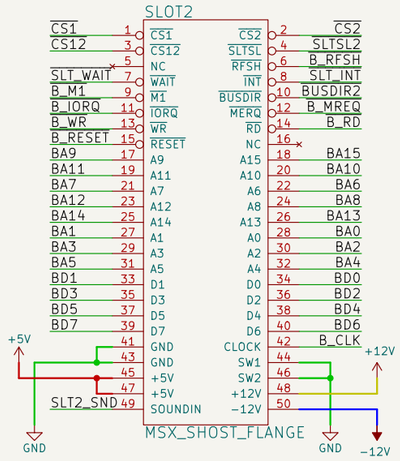
Jumpers

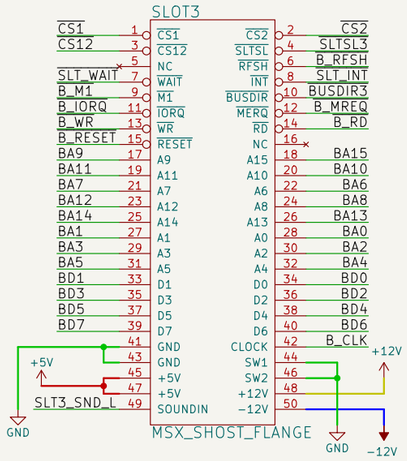
JP3, JP4: 1-2: V9938; 2-3: V9958 (Use a wire link)
JP4, JP5: 1-2: NTSC; 2-3: PAL (Use a wire link)

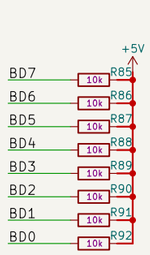
PAL: R9 – 16k, C91 – 18pF
R9 – Tolerance 1%

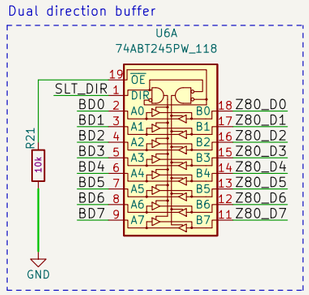
PCB Layout Notes:
Keep trace length between AD723 and 75 ohm resistors to minimum
AD723 bypass capacitors: VCC1(12), VREF(14) -> GND1(1), VCC2(19) -> GND2(24)

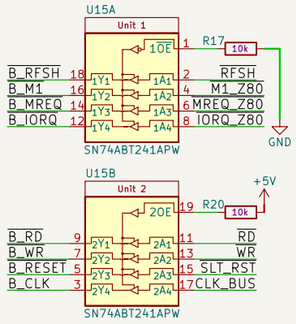


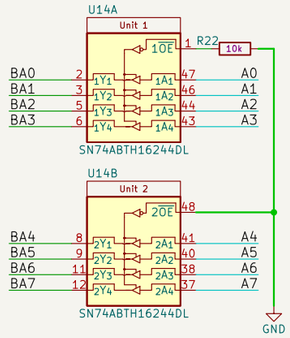


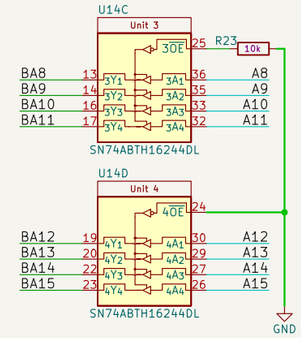


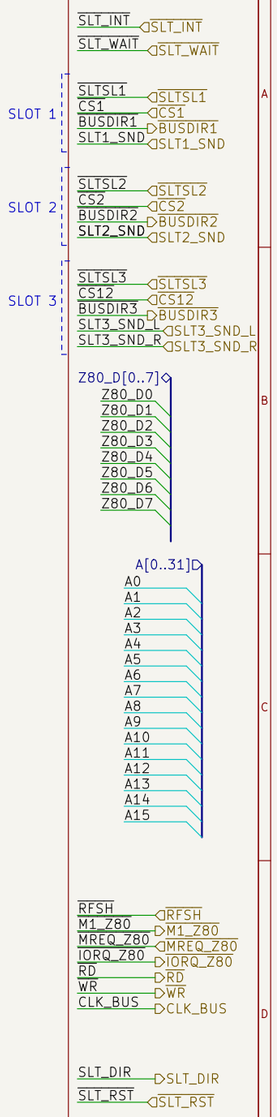










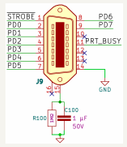


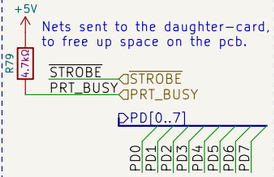
ULTRA-MSX

ULTRA-MSX			License
/SLOTS/		Rev: A-A	
Size: A3	Date: 2022-06-05	Id: 7/10	File: Ultra-MSX_Slots.kicad_sch
KiCad E.D.A. kicad (6.0.5)			

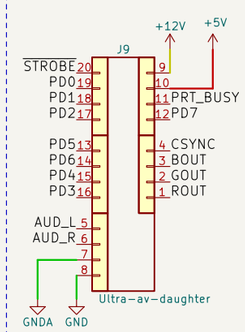
PRINTER

See 'Ultra-AV' daughter-card for schematics on connector.





ULTRA-AV daughter-card



ROUT ▷ ROUT
GOUT ▷ GOUT
BOUT ▷ BOUT

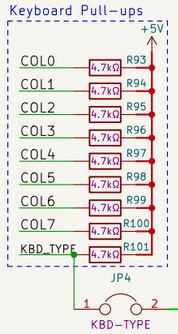
AUD_L ◁ AUD_L
AUD_R ◁ AUD_R

CSYNC ▷ CSYNC

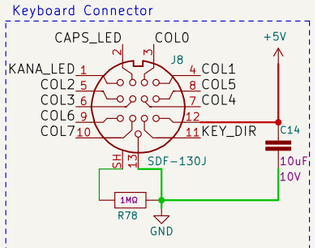
HSYNC ▷ HSYNC
VSYNC ▷ VSYNC

KEYBOARD

Keyboard Pull-ups



Keyboard Connector

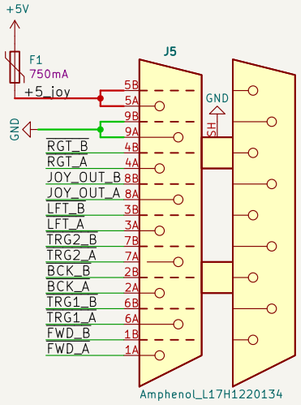


NOTE: Sony EU -style connector. SDF-130J

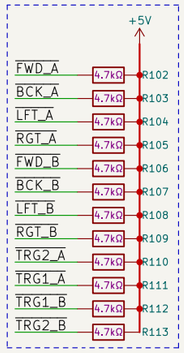
COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL[0..7]

KANA_LED ◁ KANA_LED
CAPS_LED ◁ CAPS_LED
KEY_DIR ◁ KEY_DIR
KBD_TYPE ◁ KBD_TYPE

JOYSTICKS



Joystick Pull-ups



FWD_A ◁ FWD_A
LFT_A ◁ LFT_A
RGT_A ◁ RGT_A
BCK_A ◁ BCK_A

FWD_B ◁ FWD_B
LFT_B ◁ LFT_B
RGT_B ◁ RGT_B
BCK_B ◁ BCK_B

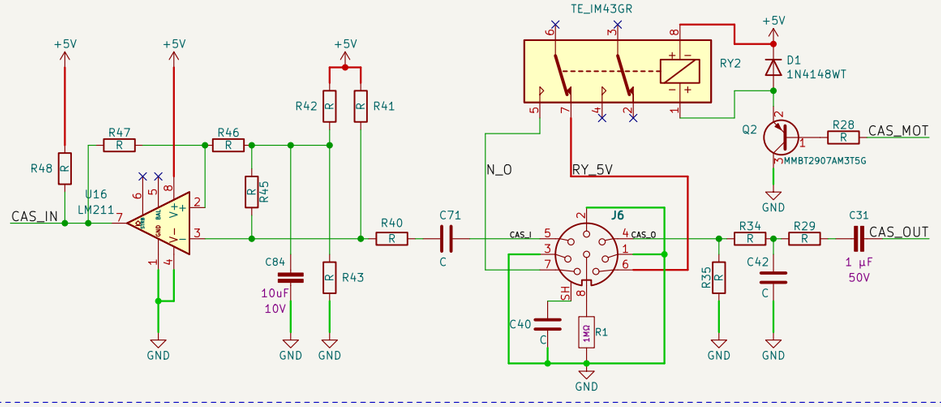
JOY_FWD ◁ JOY_FWD
JOY_BCK ◁ JOY_BCK

JOY_RGT ◁ JOY_RGT

TRG1_A ◁ TRG1_A
TRG1_B ◁ TRG1_B
TRG2_A ◁ TRG2_A
TRG2_B ◁ TRG2_B

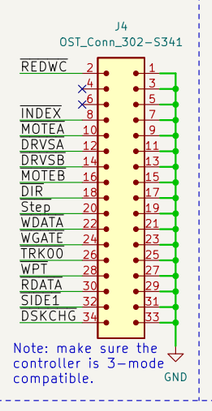
JOY_OUT_B ◁ JOY_OUT_B
JOY_OUT_A ◁ JOY_OUT_A

Cassette I/O (optional)



CAS_MOT ◁ CAS_MOT
CAS_OUT ◁ CAS_OUT
CAS_IN ▷ CAS_IN

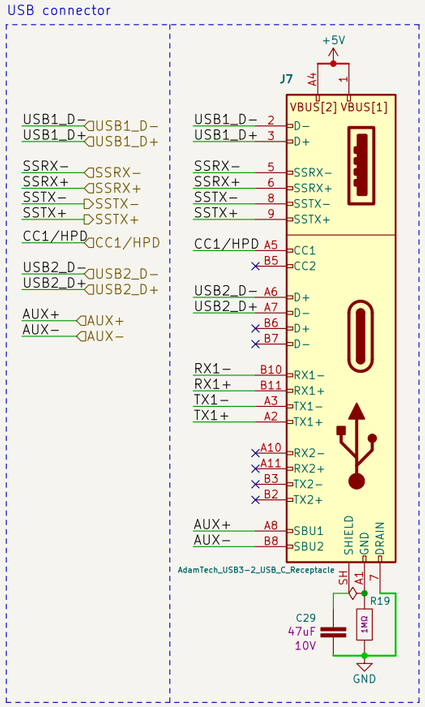
FLOPPY drive connector



Note: make sure the controller is 3-mode compatible.

REDWC ◁ REDWC
INDEX ◁ INDEX
MOTEA ◁ MOTEA
DRVSA ◁ DRVSA
DRVSB ◁ DRVSB
MOTEB ◁ MOTEB
DIR ◁ DIR
Step ◁ Step
WDATA ◁ WDATA
WGATE ◁ WGATE
TRK00 ◁ TRK00
WPT ◁ WPT
RDATA ◁ RDATA
SIDE1 ◁ SIDE1
DSKCHG ◁ DSKCHG

USB connector



Foss FPC:
https://github.com/keirf/Greaseweazle/wiki

Foss FP-sim:
https://github.com/SukkoPera/OpenFlops

http://cowlark.com/fluxengine/index.html

https://hackaday.com/2021/08/02/exps-2-keyboard-adapter-translates-ps-2-and-usb-to-msx/

IO-board - Tape + keyboard:
SD-80BV (tape)

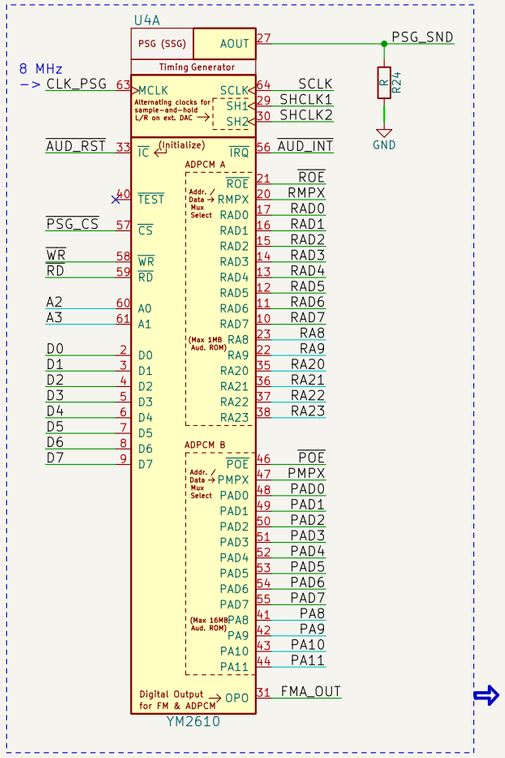
EXTERNAL NETS:

ULTRA-MSX

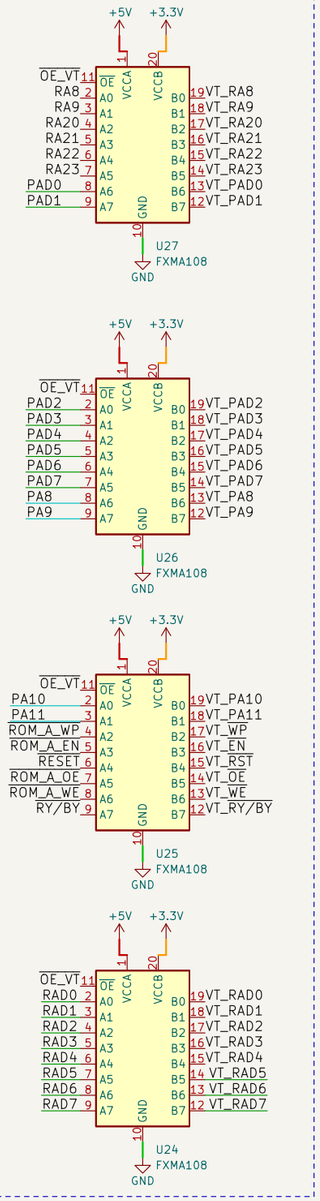
ULTRA-MSX			Licence
/PERIPHERALS/		Rev A-A	
Size A3	Date 2022-06-05	Id 8/10	File Ultra-MSX_Peripherals.kicad_sch
KiCad E.D.A. kicad (6.0.5)			

LEGEND:
COL = Column (keyboard)
PD = Printer Data
SLTx_SND = Slot 1-3, Sound

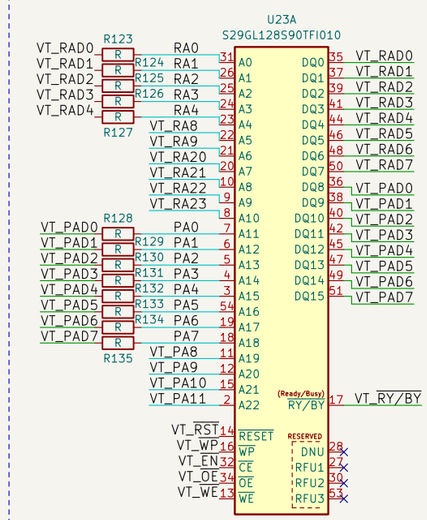
1. YAMAHA AUDIO CHIP



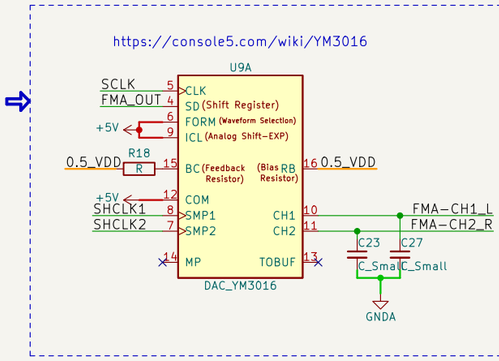
2. VOLTAGE TRANSLATORS for Audio sample-chip



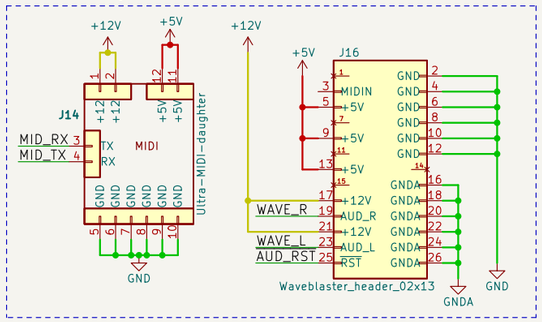
3. Audio SAMPLE-chip



4. YAMAHA DAC



MIDI AUDIO daughter card



SPI to Parallel (for using modern ROM's)
https://highfieldtales.wordpress.com/2011/12/04/very-fast-spi-to-parallel-interface-for-netduino/
--

FPGA-implementation of YM2610:
https://github.com/jotego/jt12
--

MSX-Midi:
http://map.grauw.nl/resources/midi/msx-midi.php
--

YM3016:
The YM3015 is nearly identical, except voltage-levels,
hence it can be used to figure out a replacement.

http://gendev.spritesmind.net/forum/viewtopic.php?t=386&start=180

LEGEND:

FMA = combined FM and ADPCM output

FM = Frequency Modulation synthesis
ADPCM = Adaptive differential pulse-code modulation

SMDAT = Serial Memory Data

EXTERNAL NETS:

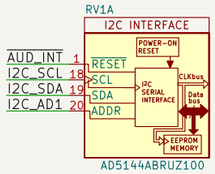
RD
WR
AUD_RST
ROE
RMPX
POE
PMPX
AUD_INT
CLK_PSG
PSG_CS
FMA-CH1_L
FMA-CH2_R
PSG_SND
Data
D[0..15]
D0 D1 D2 D3 D4 D5 D6 D7
A[0..31]
A2
A3
ROM_A_WP
ROM_A_EN
OE_VT

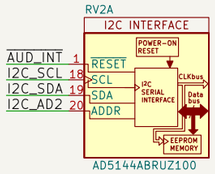
ULTRA-MSX

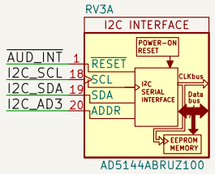
ULTRA-MSX	
/AUDIO/	Rev: A-A
Size: A3	Date: 2022-06-05
KiCad E.D.A. kicad (6.0.5)	Id: 9/10
	File: Ultra-MSX_Audio.kicad_sch

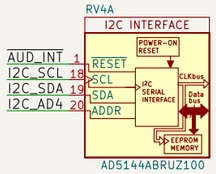
LICENSE

Slew Rate = 2* Pi * Freq_max * Vpeak
2* 3.14159 * 25000 * 48 = 7539822,368616 V/s
=> 7.54 V/uS

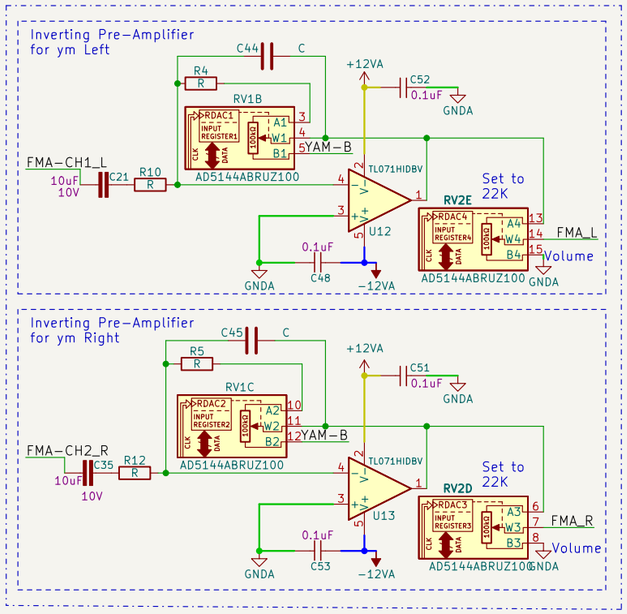




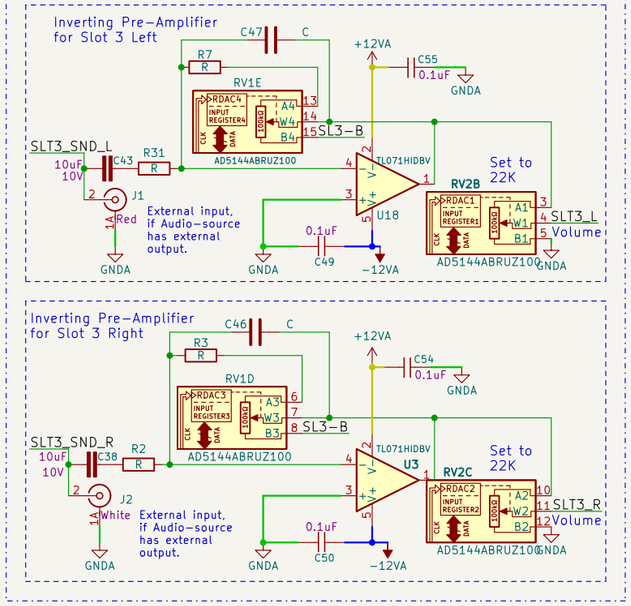


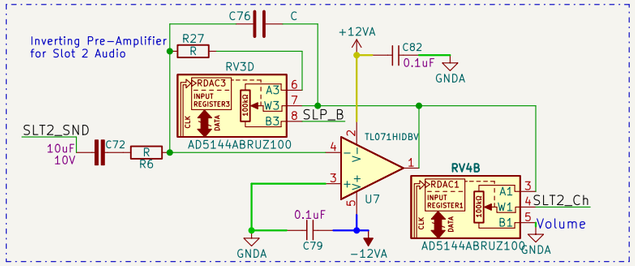


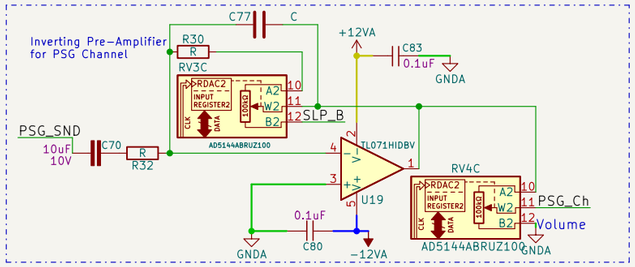
Input-Module for Yamaha Audio

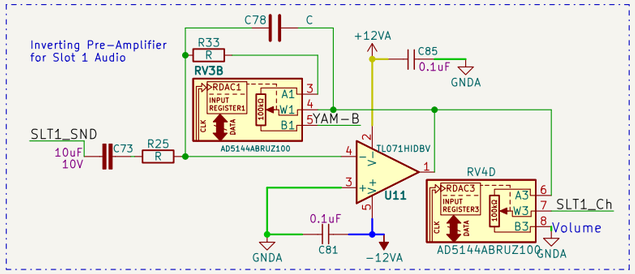


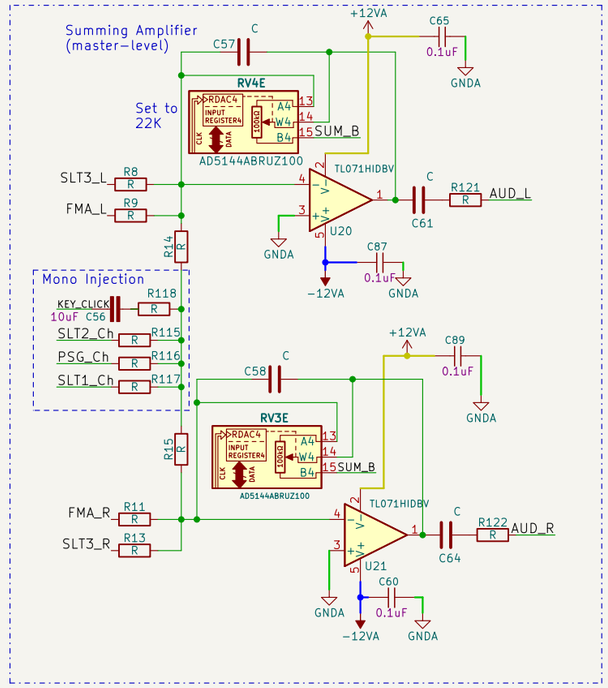
Input-Module for Slot 3 Audio











Suggested digital pots:
AD5121BCPZ100-RL7 (100Kohm, 1 circ.)
AD5122ABCPZ100-RL7 (100Kohm, 2 circ.)
AD5122ABRUZ100 (100Kohm, 2 circ.)
AD5122BRUZ100 (100Kohm, 2 circ.)
AD5144ABRUZ100 (100Kohm, 4 circ.)

EXTERNAL NETS:

SLT1_SND ◁ SLT1_SND
SLT2_SND ◁ SLT2_SND
SLT3_SND_L ◁ SLT3_SND_L
SLT3_SND_R ◁ SLT3_SND_R

FMA-CH1_L ▷ FMA-CH1_L
FMA-CH2_R ▷ FMA-CH2_R

PSG_SND ▷ PSG_SND

AUD_L ◁ AUD_L
AUD_R ◁ AUD_R

I2C_SCL ◇ I2C_SCL
I2C_SDA ◇ I2C_SDA

I2C_AD1 ◇ I2C_AD1
I2C_AD2 ◇ I2C_AD2
I2C_AD3 ◇ I2C_AD3
I2C_AD4 ◇ I2C_AD4

AUD_INT ▷ AUD_INT

ULTRA-MSX

ULTRA-MSX			Ultra-MSX
/AUDIO AMPLIFIERS/			Rev A-A
Size A3	Date 2022-06-05	Id 10/10	File Ultra-Amplifier.kicad_sch
KiCad E.D.A. kicad (6.0.5)			

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