Pin connections are based on the platform

* Decided based on the top entity,  
  wire mapping to the tool chain device configuration.

The core is portable to any reasonably sized FPGA. (83k lut’s?)

The code is based on the original “Number Nine Visual Technology” company’s ASICs, but rewritten code.

It has been used in a number of FPGA and also an ASIC implementation.

Software-wise, the creator recommends Verilator as it handles System Verilog and Verilog (some of the TB is in System-Verilog).

# Problems/issues:

There is no AMD compatible shader?

(what does this mean? The card can only work on Intel-systems?)

# HW-requirements for building a PCI card:

## VGA

w/ dumb framebuffer (PCI) - 10K LE

## Full 2D

- 20K LE

## 3D

(everything) - **85K LE**. (You actually end up becoming DSP block limited)

If you remove some components like PCI, and put it in an SOC part, you would save 1-3K LE.

These numbers are based on Intel/Altera parts.

# Register levels:

level 2 are the working registers for the current command.

Level 15 are the ones for the next command, 1.5 if you will.

These are processed by the setup engine to make the level 2's.

Level 1 are the ones in process of writing through the DLP or host.

# Walkthrough:

https://latchup.blogspot.com/2016/07/gplgpu-walkthrough.html