YAMAHA® LSI

V9990

E-VDP-III

APPLICATION MANUAL

YAMAHA

V9990 APPLICATION MANUAL
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1 OUTLINE

The V9990 is a video display processor (VDP) which features as follows. Having a high-speed drawing and animation functions, it provides various screen modes which can be used widely for games, audio-visual, office automation and other purposes. Also, as a monitor, it supports many types of display units such as home TV sets, CRT for personal computers and liquid crystal panels.

2 FEATURES

<Game Specifications>

For this type, two pattern display modes are available as follows.

- P1 (Display resolution 256×212, 2 screens)
- P2 (Display resolution 512×212)

Various highly advanced functions are available such as powerful sprite function and 2-screen independent omnidirectional scroll function.

<AV Specifications>

For this type, four kinds of bit map display modes are available as follows. They are capable of providing display on the NTSC or PAL frequency monitor.

- B1 (Display resolution 256×212)
- B2 (Display resolution 384×240)
- B3 (Display resolution 512×212)
- B4 (Display resolution 768×240)

*Capable of doubling the resolution in the vertical direction by using the interlace.

*Up to 32,768 colors/dot can be displayed.

*Built-in color palette (64 colors selected out of 32,768 colors)

*Omnidirectional smooth scrolling is possible.

*Superimposition and digitization are possible.

*Allows use of the monitor screen to the full extent in four directions as the display range by using the over-scan mode (B2, B4) in such application as for the telopper.

*Supports the high-speed hardware drawing commands such as the screen transfer, font color development and line.

*The hardware cursor display function is available.

<OA Specifications>

For this type, two kinds of bit map display modes are available as follows. They can be displayed on the high resolution monitor.

- B5 (Display resolution 640×400)
- B6 (Display resolution 640×480)

*Up to 16 colors/dot can be displayed. (Selectable out of 32,768 colors depending on the color palette)

*Omnidirectional smooth scrolling is possible.

*Supports the high-speed hardware drawing commands such as the screen transfer, font color development and line.

*The hardware cursor display function is available.

<Others>

*Built-in DA converter

*Linear RGB output

*Direct connection of CG ROM such as KANJI ROM is possible.

*Useable VRAM

64K×4

128K×8 Dual port DRAM (The access time is 120nS, but 100nS for the B6 mode.)

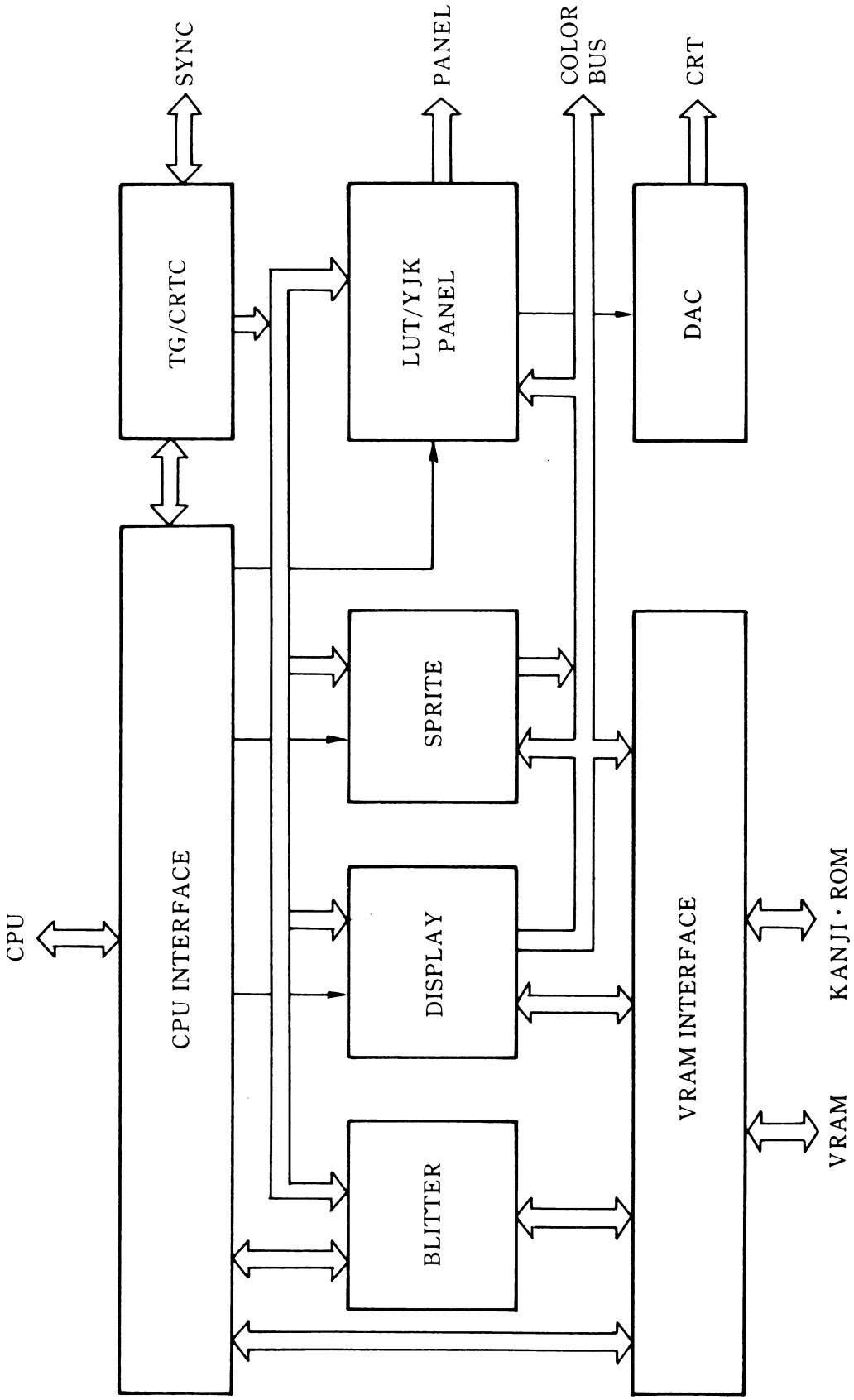
256K×4

*As the VRAM capacity, 128KB, 256KB and 512KB configurations are possible.

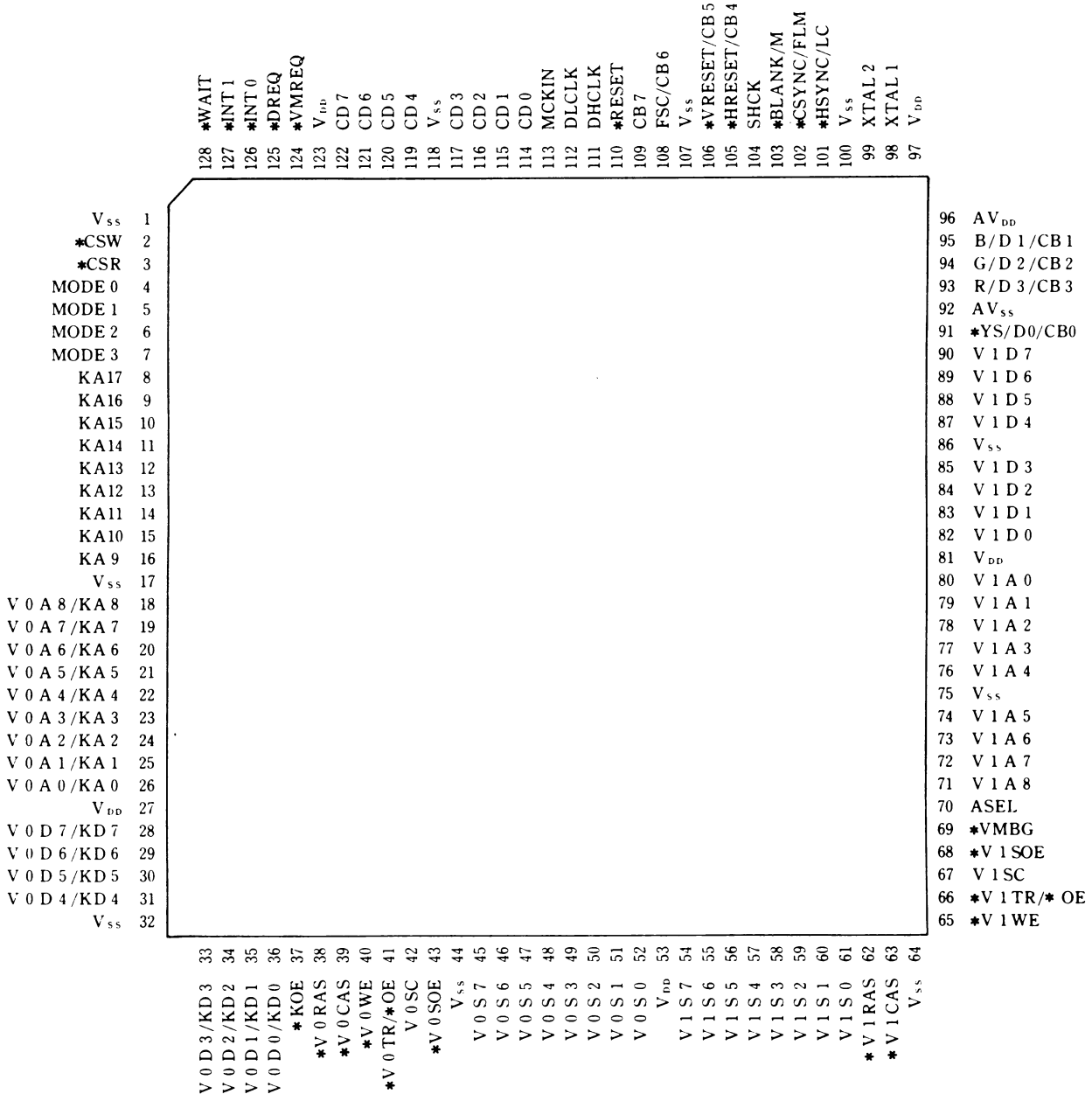
*Capable of direct access from CPU to VRAM by means of the 16 bit bus.

*Use of the LCD panel (1 screen panel and single drive type of 2 screen panel) is possible.

3 BLOCK DIAGRAM



4 PIN ASSIGNMENT



* : Low active

5 PIN DESCRIPTION

1) CPU Interface

- CD7-0 (I/O)

  8-bit bidirectional data bus of CPU

- MODE3-0 (I)

  Address for I/O port selection of CPU is inputted. Select P#0 to P#F of VDP.

- *CSR (I)

  CPU read signal which is chip-selected for VDP is inputted. VDP outputs data to CD7-0 when this signal is active (Low).

- *CSW (I)

  CPU write signal which is chip-selected for VDP is inputted. D7-0 data is set to VDP at the rise of this signal.

- *WAIT (O:Open drain output)

  Wait signal to CPU is output. This signal becomes active (Low) while VDP is busy when reading or writing from CPU is executed.

- *INT1, *INT0 (O:Open drain output)

  These signals become active (Low) when the interrupt condition exists in VDP. The interrupt condition can be obtained by reading P#6 and cancelled by writing "1" to an interrupt condition corresponding to P#6.

  INT0 is an interrupt for vertical retrace line interval and at command end.

  INT1 is an interrupt for display position.

- *DREQ (O:Open drain output)

  Data request signal is output. This signal becomes active (Low) when data ready occurs while command is executed and can be cancelled by means of P#2 access.

- *VMREQ (I)

  This signal set active(Low) when CPU makes an access to VRAM without using VDP. VDP makes WAIT signal active until VRAM access becomes possible. Then it makes VMBG signal active and releases data bus, address bus and WE signal of VRAM0 and VRAM1. After that,it cancels VMBG signal and then WAIT signal.

2) VRAM Interface

- *KOE (O)

  Data output enable signal for Kanji ROM is output. The data bus (VOD7-0) is used by both VRAM0 and kanji ROM and when this signal is active (Low), kanji ROM data bus becomes valid.

- KA17-9 (O)

  Address bus (A17-9) output of Kanji ROM

- V0A8-0/KA8-0 (O:3 state output)

  Address bus output of VRAM0. When *KOE is active, kanji ROM address bus output becomes valid.

- V1A8-0 (O:3 state output)

  Address bus output of VRAM1.

- V0D7-0/KD7-0 (I/O)

  Bidirectional data bus of VRAM0 RAM port. When *KOE is active, kanji ROM data bus input becomes valid.

- V1D7-0 (I/O)

  Bidirectional data bus of VRAM1 RAM port.

- V0S7-0, V1S7-0 (I)

  Data bus input of VRAM0, VRAM1 serial port.

- *V0RAS, *V1RAS (O)

  Low address strobe signal output of VRAM0 and VRAM1.

- *V0CAS, *V1CAS (O)

  Column address strobe signal output of VRAM0 and VRAM1.

- *V0WE, *V1WE (O:3 state output)

  Write strobe signal output of VRAM0 and VRAM1.

- *V0TR/*OE, *V1TR/*OE (O)

  Data transfer control signal of VRAM0 and VRAM1 or data output enable signal of RAM port.

- *V0SC, V1SC (O)

  Serial clock signal output of VRAM0 and VRAM1.

- *V0SOE, *V1SOE (O)

  Data enable signal of VRAM0 and VRAM1 serial port.

- *VMBG (O)

  When this signal is active (Low), VDP releases VRAM0, VRAM1 data bus, address bus and WE signal (resulting in high impedance).

- ASEL (O)

  Low address timing signal for VRAM when making an access to VRAM from outside.

3) CRT and Panel Interface

- *HSYNC/LC (O)

  Horizontal synchronous signal output (without equivalent pulse). Panel latch clock signal is output when VDP is in panel mode.

- *CSYNC/FLM (O)

  Combined synchronous signal output (with equivalent pulse). Panel scanning start signal is output when VDP is in panel mode.

- *BLANK/M (O)

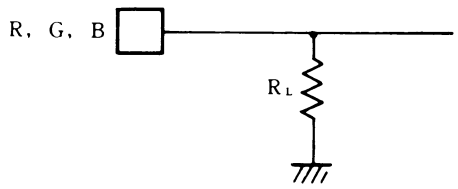
  This signal becomes active (Low) while retrace line blanking interval. Panel AC conversion signal output when VDP is in panel mode.

- SHCK (O)

  Panel shift clock signal output.

- R, G, B *YS/D3-0/CB3-0 (O)

  Linear RGB output and YS signal output. Panel data output or color bus output becomes valid when in panel mode. YS signal becomes active (Low) when VDP data is superimposed.



- *HRESET/CB4 (I/O)

  Internal horizontal timing is initialized when this signal falls. It can be used for synchronization when using two V9990's but cannot be used otherwise. when the horizontal cycle differs, normal operation of VDP is not assured.
  Color bus output becomes valid when in panel mode.

- *VRESET/CB5 (I/O)

  Internal vertical timing is initialized when this signal falls. It is possible to synchronize VDP from outside. Color bus output becomes valid when in panel mode.

- FSC/CB6 (O)

  NTSC sub-carrier (3.58MHz clock) output. Color bus output becomes valid when in panel mode.

・CB7 (O)

Color bus output. CB7-0 data is output as follows.

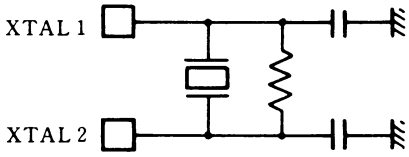
Mode	Dot Clock	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	CB Clock
P 1	5MHz	–	–	CC5	CC4	CC3	CC2	CC1	CC0	DLCLK
P 2	10MHz	–	–	CC5	CC4	CC3	CC2	CC1	CC0	DHCLK
8B/D	7,10MHz/5MHz	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	DHCLK/DLCLK
4B/D	14,21,25MHz	ECC3	ECC2	ECC1	ECC0	OCC3	OCC2	OCC1	OCC0	DHCLK
4B/D	7,10MHz/5MHz	–	–	–	–	CC3	CC2	CC1	CC0	DHCLK/DLCLK
2B/D	14,21,25MHz	–	–	ECC1	ECC0	–	–	OCC1	OCC0	DHCLK
2B/D	7,10MHz/5MHz	–	–	–	–	–	–	CC1	CC0	DHCLK/DLCLK

Note) B/D:Bit/Dot, ECC3-0:CC3-0 of even number dot, OCC3-0: CC3-0 of odd number dot

4) Clock Signal

・XTAL1 (I), XTAL2 (O)

Terminal for connecting 21MHz (MCK) crystal oscillator. Use XTAL1 terminal when inputting clock oscillated externally.



・MCKIN (I)

14MHz clock (MCK) is inputted. Use VDP internal register when selecting XTAL or MCKIN.

・DHCLK, DLCLK (O)

Dot clock output. 1/2MCK for DHCLK and 1/4MCK for DLCLK.

5) Others

・*RESET (I)

VDP is initialized when this signal is active (Low). All registers (except LUT) will be "0" cleared.

・AVDD, AVSS (I)

Analog power supply input for RGB.

・VDD, VSS (I)

Digital power supply input.

6 VIDEO MEMORY CONFIGURATION

64k×4bit VRAM×4chip=128kB (Access time:120ns, but 100ns when in B6 mode), or

128k×8bit VRAM×2chip=256kB (Access time:120ns, but 100ns when in B6 mode), or

256k×4bit VRAM×4chip=512kB (Access time:120ns, but 100ns when in B6 mode) and

2Mbit kanji ROM (16×16 dots, JIS Primary and Secondary standards)
(Access time:150ns)

7 BASIC INPUT/OUTPUT

Data is inputted and output to and from the V9990 through the I/O ports (P#0 to P#F). Basically, as an access, both Read and Write are possible at all ports. But only Read is possible with the STATUS port (P#5) and Write only with the SYSTEM CONTROL port (P#7)and KANJI ROM LOW ORDER ADDRESS SPECIFYING ports (P#8, P#A).

7.1 ACCESS OF REGISTERS R#0 to R#28, R#32 to R#54

To set a value in the register, have the register No. output at REGISTER SELECT port (P#4) and then the data at REGISTER DATA port (P#3).
To obtain the value from the register, have the register No. output at P#4 and then read P#3.
The register No. is specified by using the lower 6 bits of the value at P#4 and the bit 7 (MSB) functions as WII (Write Increment Inhibit) and bit 6 as RII (Read Increment Inhibit). If WII is "1", automatic increment of the register No. by writing the data to the register is prohibited. If RII is "1", automatic increment of the register No. by reading the data of the register is prohibited.

	b7	b6	b5	b4	b3	b2	b1	b0
P#4(Write)	NII	RII	Register No. (R#N)					
P#3(Read/Write)	Register data							

7.2 ACCESS OF VRAM

To write a value in VRAM, set the target address to VRAM Write Base Address registers (R#0~R#2)and have the data output at VRAM DATA port (P#0). As the bit 7 (MSB) of R#2 functions as AII (Address Increment Inhibit), if it is "1", automatic address increment by writing the data is inhibited.
To read the data of VRAM, set the target address to VRAM Read Base Address registers (R#3~R#5)and read in the data of VRAM DATA port (P#0). As the bit 7 (MSB) of R#5 functions as AII (Address Increment Inhibit), if it is "1", automatic address increment by reading in the data is inhibited.
The address can be specified up to 19 bits (512K bytes), with lower 8 bits set to R#0 (or R#3),center 8 bits to R#1 (or R#4) and upper 3 bits to R#2 (or R#5).

●VRAM Write

	b7	b6	b5	b4	b3	b2	b1	b0	
P#4(Write)	0	0	0	0	0	0	0	0	
P#3(Write)	VRAM lower address								(R#0 set)

	b7	b6	b5	b4	b3	b2	b1	b0	
P#3(Write)	VRAM center address								(R#1 set)
P#3(Write)	AII	VRAM upper address							(R#2 set)
P#0(Write)	Data								

●VRAM Read

	b7	b6	b5	b4	b3	b2	b1	b0	
P#4(Write)	0	0	0	0	0	0	1	1	
P#3(Write)	VRAM lower address								(R#3 set)
P#3(Write)	VRAM center address								(R#4 set)
P#3(Write)	AII	VRAM upper address							(R#5 set)
P#0(Read)	Data								

7.3 ACCESS OF PALETTE

The palette data can be set or checked by setting the palette No. and RGB specification to the palette pointer (R#14) and reading or writing at the palette data port (P#1).
The palette No. is specified by using the upper 6 bits of R#14 and RGB by using the lower 2 bits (R=0, G=1, B=2). The lower 2 bits constitute a ternary counter which undergoes automatic increment in the order of RGB through the port access.
It should be noted that how the palette setting is actually displayed also depends on the palette control register (R#13) setting.

	b7	b6	b5	b4	b3	b2	b1	b0	
P#4(Write)	0	0	0	0	1	1	1	0	
P#3(Write)	Palette No.						0	0	(R#14 set)
P#1(Write)	$\overline{YS}$	—	—	RED data					
P#1(Write)	—	—	—	GREEN data					
P#1(Write)	—	—	—	BLUE data					

7.4 EXECUTION OF COMMAND

With the necessary parameter set to the command registers, set the operation code. For transfer from CPU (or to CPU), the data is output at the command data port (P#2) by the amount required after this stage.

7.5 STATUS PORT

Only by reading the status port (P#5, Read Only), the status of the V9990 can be checked.

7.6 INTERRUPT PORT

The cause of interrupt can be determined by reading the interrupt port (P#6). As the flag is not reset automatically, "1" should be written to the applicable bit to reset it.

7.7 SYSTEM CONTROL PORT

The system control port (P#7) is only for writing. It can be used to reset the system and to select the master clock.

7.8 KANJI ROM

The kanji font can be obtained in the same manner as the MSX kanji ROM.
For the primary standard kanji, have the upper address output at P#9 and the lower address at P#8 and obtain the font data by reading in P#9 32 times. For the secondary standard kanji, use P#A and P#B in the same way.
The data is provided in the order of upper left, upper right, lower left and lower right blocks (8 bytes each) of the 16×16 font.

1st 8bytes	2nd 8bytes
3rd 8bytes	4th 8bytes

Font : 16 dots vertical×16 dots horizontal

	b7	b6	b5	b4	b3	b2	b1	b0
P#9(Write)	—	—	Font upper address					
P#8(Write)	—	—	Font lower address					
P#9(Read)	Data							

8 V9990 DISPLAY MODES

8.1 PATTERN DISPLAY MODE

Pattern Display Function

Mode name	P1	P2
Master clock frequency	21.5MHz	21.5MHz
Dot clock frequency	5.4MHz	10.7MHz
Horizontal cycle	15.7KHz (NTSC)	15.7KHz (NTSC)
Display resolution	32×26.5 patterns (256×212 dots)	64×26.5 patterns (512×212 dots)
Number of screens	2 screens	1 screen
Pattern size	8×8 dots	8×8 dots
Simultaneously displayed colors	15 colors + clear color	15 colors + clear color
Color palette	4 palettes of 16 colors out of 32768 clors	4 palettes of 16 colors out of 32768 colors
Pattern name Display space Image space Number of selected patterns	 32×26.5 patterns 64×64 patterns 16384 patterns (Max.)	 64×26.5 patterns 128×64 patterns 16384 patterns (Max.)
Pattern generator	2 screens independently 1535units (VRAM128Kbyte) 3583units (VRAM256Kbyte) 7679units (VRAM512Kbyte)	 3071units (VRAM128Kbyte) 7167units (VRAM256Kbyte) 15359units (VRAM512Kbyte)

*) All items except No. of pattern generators are irrelevant to the VRAM capacity.

Sprite Display Function

- Size: 16×16 dots
- Limited No. of displayed units: 125 in 1 screen
16 on 1 line
- Displayed colors: 15 colors + clear color (for each dot)
Palette can be selected for each sprite (1 palette selected out of 4)
- Specification of display priority: Priority between sprite and pattern screen can be set for each sprite.
The sprite No. order is used for priority order among sprites.
- Pattern: Selected from among 256 patterns
The pattern generators are used commonly with the pattern screen (the base address should be set at the register R#25.)

8.2 BIT MAP DISPLAY MODE

Bit map screen display function

VRAM 128Kbyte

Mode	Master clock (MHz)	Dot clock (MHz)	Horizontal cycle (KHz)	Display resolution ( )interlace (dotXdot)	Number of displayed colors (bit/dot)	Image size (dotXdot)
B1	21.5	5.4	NTSC 15.7	256x212 (256x424)	16	256x256
					8	256x512 512x256
					4	256x1024 512x512 1024x256
					2	256x2048 512x1024 1024x512 2048x256
B2	14.3	7.2	NTSC 15.7	OVER SCAN 384x240 (384x480)	8	512x256
					4	512x512 1024x256
					2	512x1024 1024x512 2048x256
B3	21.5	10.7	NTSC 15.7	512x212 (512x424)	8	512x256
					4	512x512 1024x256
					2	512x1024 1024x512 2048x256
B4	14.3	14.3	NTSC 15.7	OVER SCAN 768x240 (768x480)	4	1024x256
					2	1024x512 2048x256
B5	21.5	21.5	25.3	640x400	2	1024x512
B6	25.2	25.2	31.5	640x480	2	1024x512

VRAM 256Kbyte

Mode	Master clock (MHz)	Dot clock (MHz)	Horizontal cycle (KHz)	Display resolution ( )interlace (dotXdot)	Number of displayed colors (bit/dot)	Image size (dotXdot)
B1	21.5	5.4	NTSC 15.7	256x212 (256x424)	16	256x512 512x256
					8	256x1024 512x512 1024x256
					4	256x2048 512x1024 1024x512 2048x256
					2	256x4096 512x2048 1024x1024 2048x512
B2	14.3	7.2	NTSC 15.7	OVER SCAN 384x240 (384x480)	16	512x256
					8	512x512 1024x256
					4	512x1024 1024x512 2048x256
					2	512x2048 1024x1024 2048x512
B3	21.5	10.7	NTSC 15.7	512x212 (512x424)	16	512x256
					8	512x512 1024x256
					4	512x1024 1024x512 2048x256
					2	512x2048 1024x1024 2048x512
B4	14.3	14.3	NTSC 15.7	OVER SCAN 768x240 (768x480)	4	1024x512 2048x256
					2	1024x1024 2048x512
B5	21.5	21.5	25.3	640x400	4	1024x512
					2	1024x1024 2048x512
B6	25.2	25.2	31.5	640x480	4	1024x512
					2	1024x1024 2048x512

VRAM 512Kbyte

Mode	Master clock (MHz)	Dot clock (MHz)	Horizontal cycle (KHz)	Display resolution ( )interlace (dotXdot)	Number of displayed colors (bit/dot)	Image size (dotXdot)
B1	21.5	5.4	NTSC 15.7	256x212 (256x424)	16	256x1024 512x512 1024x256
					8	256x2048 512x1024 1024x512 2048x256
					4	256x4096 512x2048 1024x1024 2048x512
					2	256x8192 512x4096 1024x2048 2048x1024
B2	14.3	7.2	NTSC 15.7	OVER SCAN 384x240 (384x480)	16	512x512 1024x256
					8	512x1024 1024x512 2048x256
					4	512x2048 1024x1024 2048x512
					2	512x4096 1024x2048 2048x1024
B3	21.5	10.7	NTSC 15.7	512x212 (512x424)	16	512x512 1024x256
					8	512x1024 1024x512 2048x256
					4	512x2048 1024x1024 2048x512
					2	512x4096 1024x2048 2048x1024
B4	14.3	14.3	NTSC 15.7	OVER SCAN 768x240 (768x480)	4	1024x1024 2048x512
					2	1024x2048 2048x1024
B5	21.5	21.5	25.3	640x400	4	1024x1024 2048x512
					2	1024x2048 2048x1024
B6	25.2	25.2	31.5	640x480	4	1024x1024 2048x512
					2	1024x2048 2048x1024

Displayed color (RGB conversion system)

	PLTM (R#13)	RGB conversion system	Number of displayed colors
16bit/dot	0	Direct RGB ($\overline{YS}$:1bit, G:5bit, R:5bit, B:5bit)	32768 colors
8bit/dot	0	Color Palette	64 colors out of 32768 colors
	1	Direct RGB (G:3bit, R:3bit, B:2bit)	256 colors
	2	YJK Decoder	19268 colors
	3	YUV Decoder	19268 colors
4bit/dot	0	Color Palette	16 colors out of 32768 colors
2bit/dot	0	Color Palette	4 colors out of 32768 colors

Cursor function

- Size 32×32 dots
- Number of displayed units 2 in 1 screen
- Displayed color 3 colors + EOR color on bit map screen + clear color
- Pattern Any form

8.3 REGISTER SETTING VALUES FOR EACH DISPLAY MODE

	P#7	R#6				R#7						
Mode	MCS	DSPM	DCKM	XIMM	CLRM	C25M	SM1	SM	PAL	EO	IL	HSCN
P1	0	0	0	1	1	0	0/1	0/1	0/1	0/1	0/1	0
P2	0	1	1	2	1	0	0/1	0/1	0/1	0/1	0/1	0
B1	0	2	0	0~3	0~3	0	0/1	0/1	0/1	0/1	0/1	0
B2	1	2	1	1~3	0~3	0	0/1	0/1	0/1	0/1	0/1	0
B3	0	2	1	1~3	0~3	0	0/1	0/1	0/1	0/1	0/1	0
B4	1	2	2	2~3	0~1	0	0/1	0/1	0/1	0/1	0/1	0
B5	0	2	2	2~3	0~1	0	0	0	0	0	0	1
B6	0	2	2	2~3	0~1	1	0	0	0	0	0	1

9 CONTROL OF PALETTE

For the V9990, there are 10 types (display types) by which the data (2 to 16 bits) obtained from VRAM is transmitted to the D/A converter with 5 bits for each RGB as follows.

1. PP

Display type when the display mode is P1 or P2

2. BYUV

Display type when the display mode uses full YUV on the bit map

3. BYUVP

Display type when the display mode uses YUV and palette mixed on the bit map

4. BYJK

Display type when the display mode uses full YJK on the bit map

5. BYJKP

Display type when the display mode uses YJK and palette mixed on the bit map

6. BD16

Display type when the display mode uses 16 bit data directly on the bit map (5 bits for each RGB+Ys)

7. BD8

Display type when the display mode uses 8 bit data directly on the bit map (3, 3, 2 bits for each RGB, Ys at ALL 0)

8. BP6

Display type when the display mode uses 8 bit data on the bit map through the palette

9. BP4

Display type when the display mode uses 4 bit data and offset 2 bits on the bit map through the palette.

10. BP2

Display type when the display mode uses 2 bit data and offset 4 bits on the bit map through the palette.

9.1 SELECTION OF DISPLAY TYPE

PALETTE CONTROL(WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#13	PLTM1	PLTM0	VAE	PLTAIH	PLTO5	PLTO4	PLTO3	PLTO2

SPRITE PALETTE CONTROL(WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#28	0	0	0	0	CSPO5	CSPO4	CSPO3	CSPO2

BACK DROP COLOR(READ/WRITE)

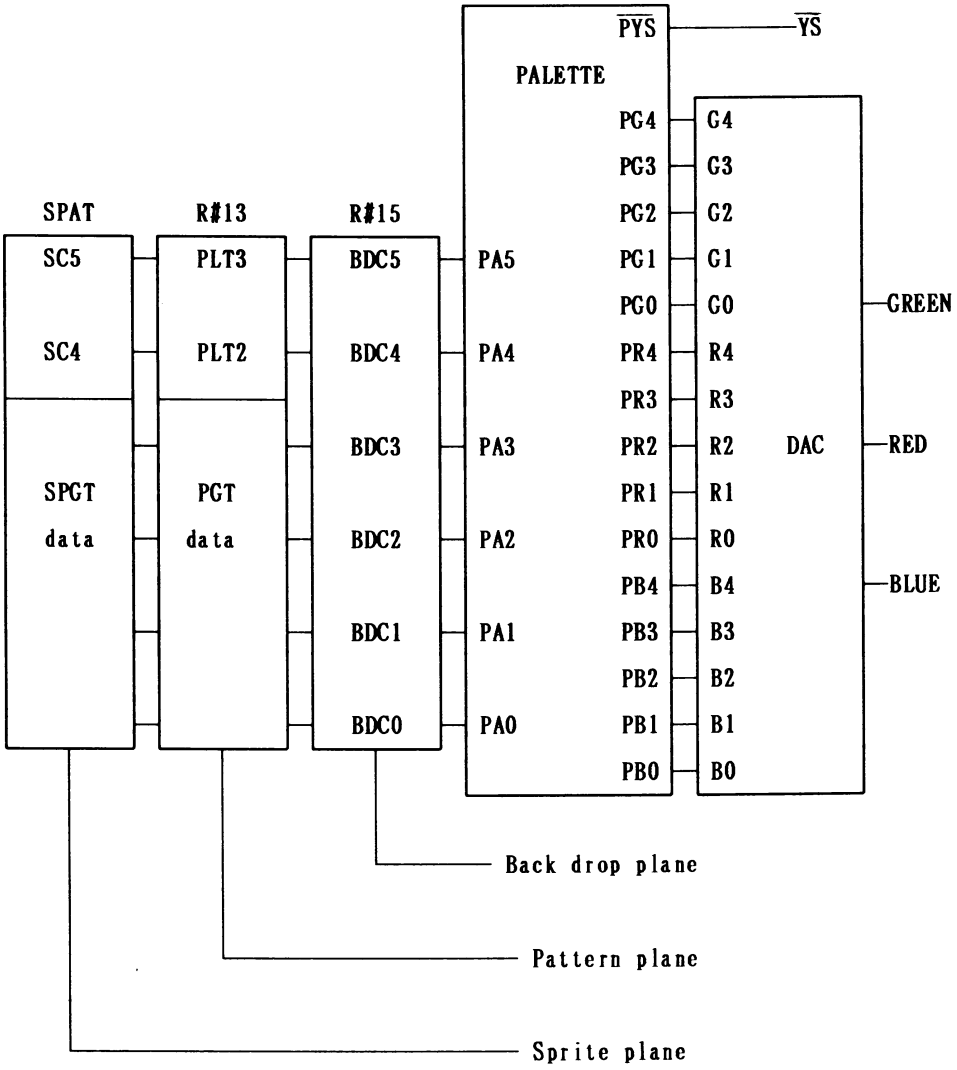
	b7	b6	b5	b4	b3	b2	b1	b0
R#15	0	0	BDC5	BDC4	BDC3	BDC2	BDC1	BDC0

SCREEN MODE(READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R# 6	DSPM1	DSPM0	DCKM1	DCKM0	XIMM1	XIMM0	CLRM1	CLRM0

	DSPM	PLTM	CLRM	YAE
(1)PP	0,1	0	1	0
(2)BYUV	2	3	2	0
(3)BYUVP	2	3	2	1
(4)BYJK	2	2	2	0
(5)BYJKP	2	2	2	1
(6)BD16	2	0	3	0
(7)BD8	2	1	2	0
(8)BP8	2	0	2	0
(9)BP4	2	0	1	0
(10)BP2	2	0	0	0

9.1.1 PP

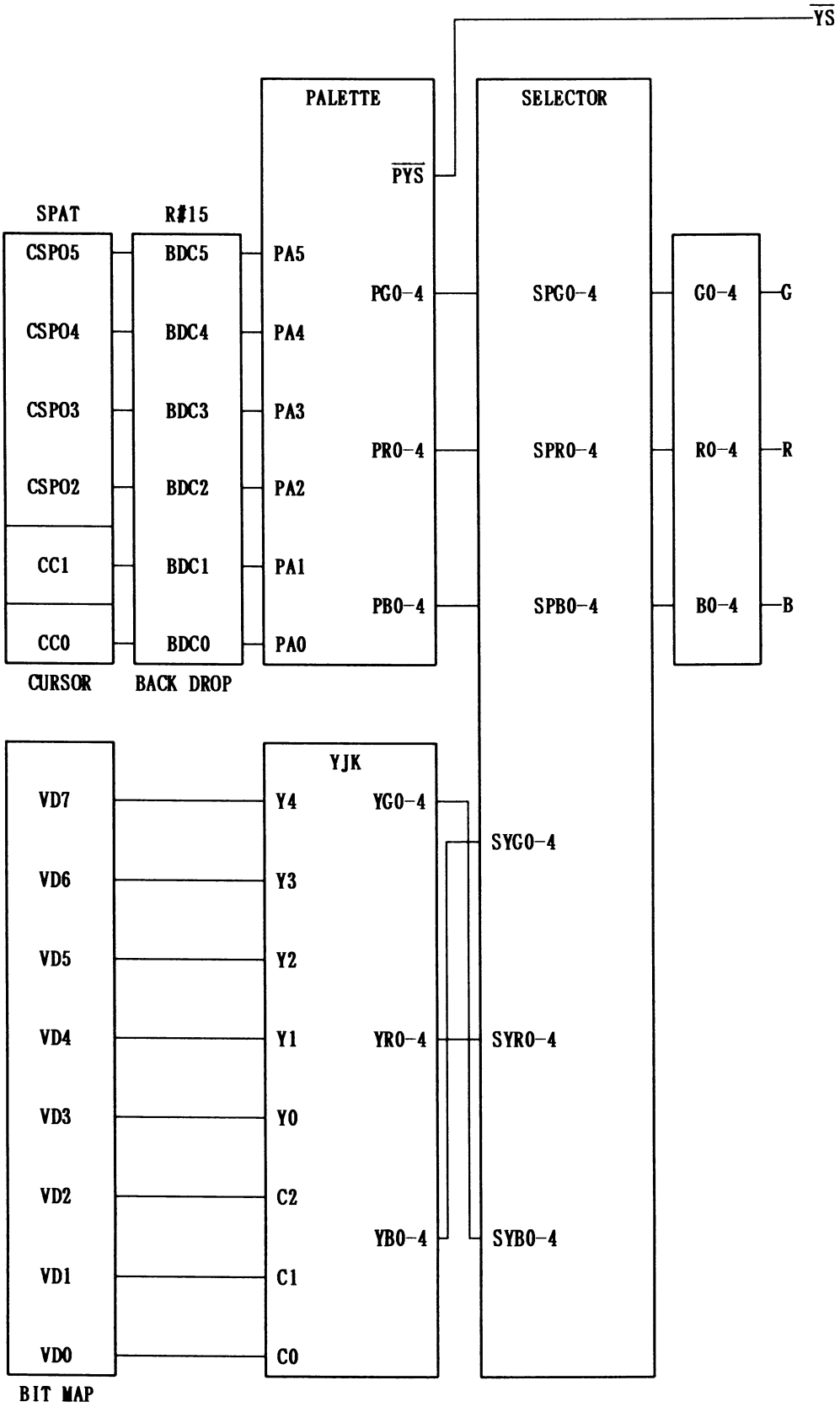


- PLT3 and 2 will be as follows depending on display modes.

	PLT3	PLT2
P1 mode, plane "A"	PLTO3	PLTO2
P1 mode, plane "B"	PLTO5	PLTO4
P2 mode, 8n plus 0, 1, 4, 5th dot	PLTO3	PLTO2
P2 mode, 8n plus 2, 3, 6, 7th dot	PLTO5	PLTO4

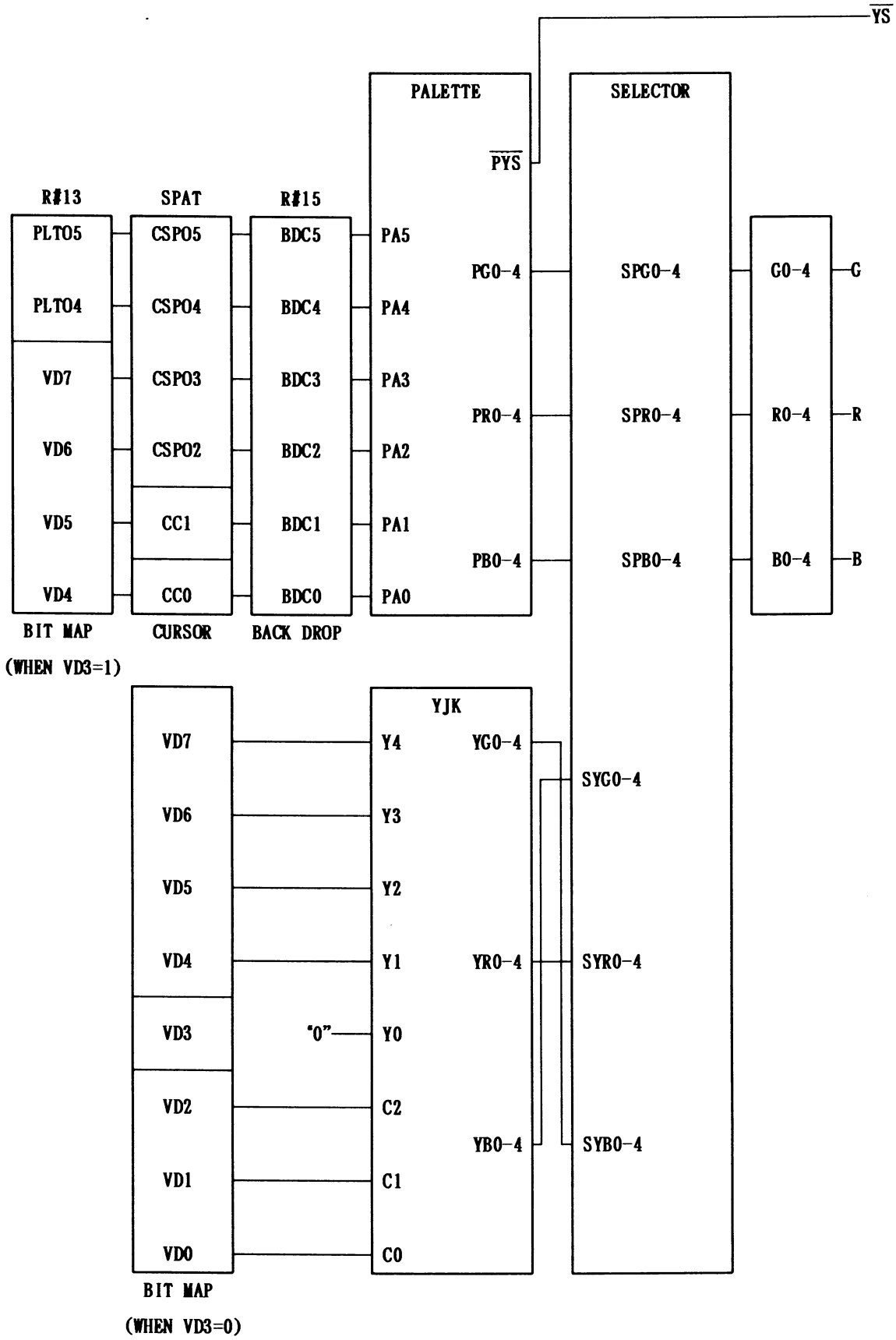
- SC5 and 4 are data of sprite attribute table
- PGT data is data of pattern generator table
- SPGT data is data of sprite generator table (used commonly with pattern generator table)

9.1.2 BYUV



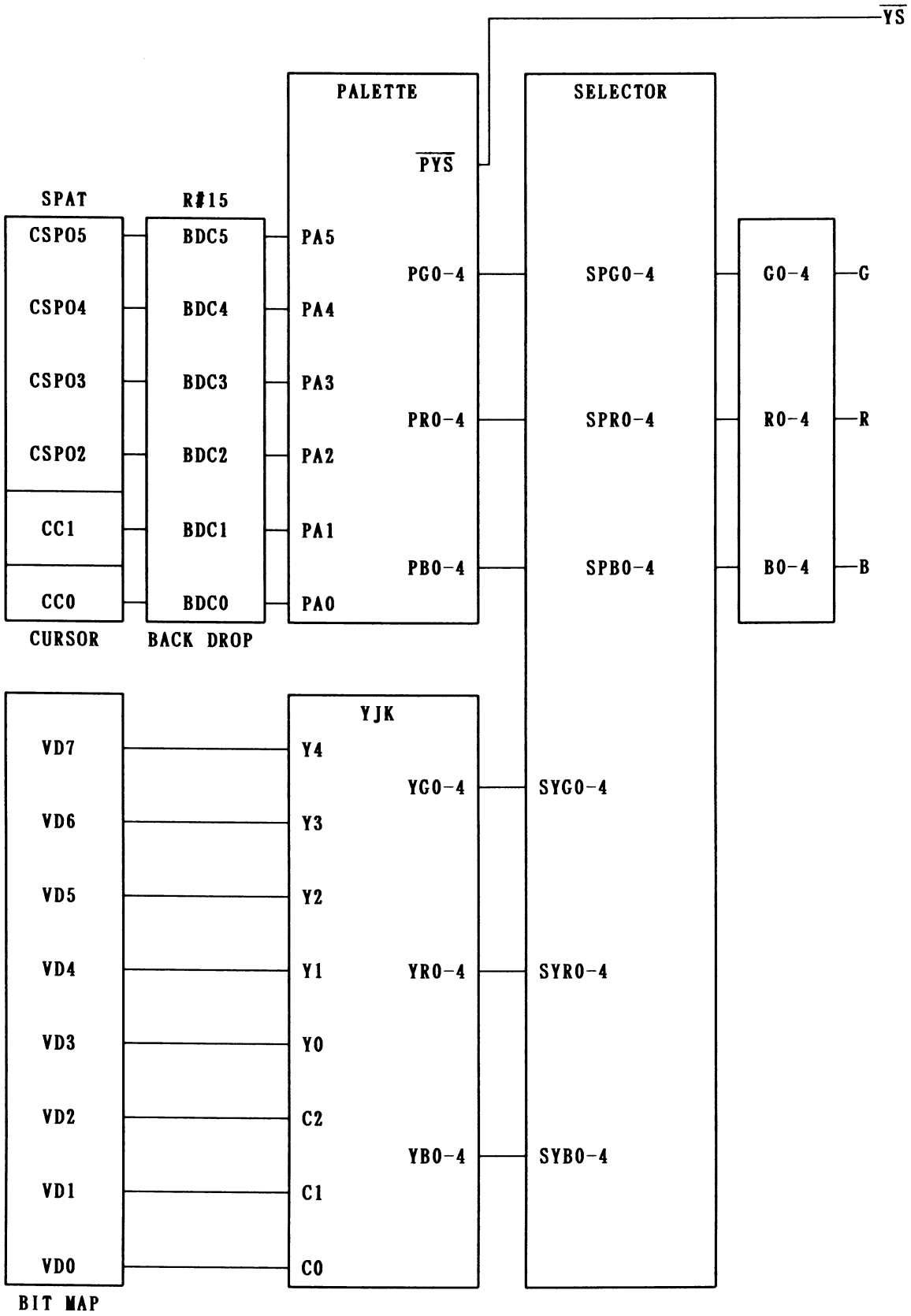
・CC1 and CC0 are data of cursor attribute table.

9.1.3 BYUVP



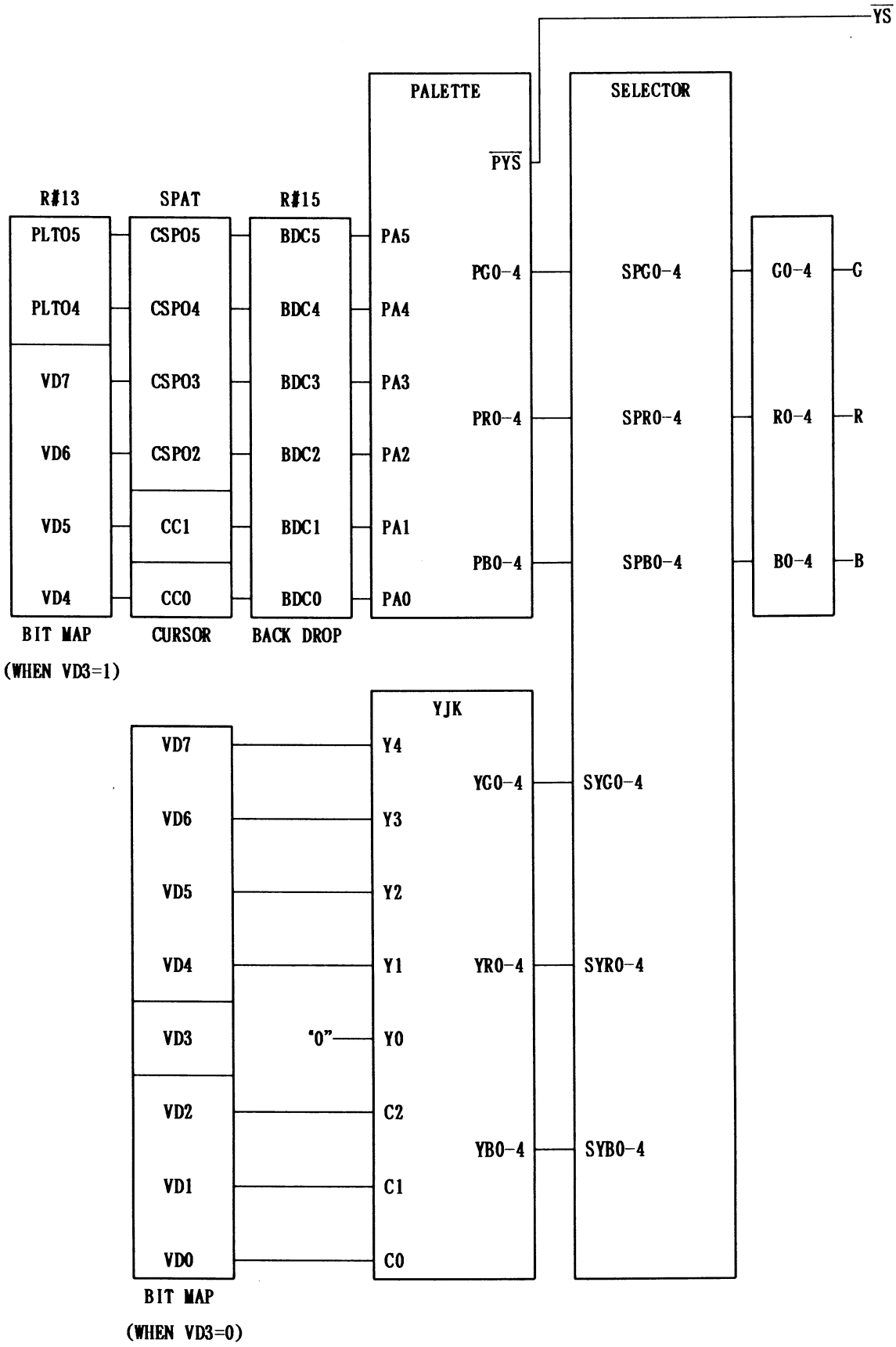
・CC1 and CC0 are data of cursor attribute table.

9.1.4 BYJK



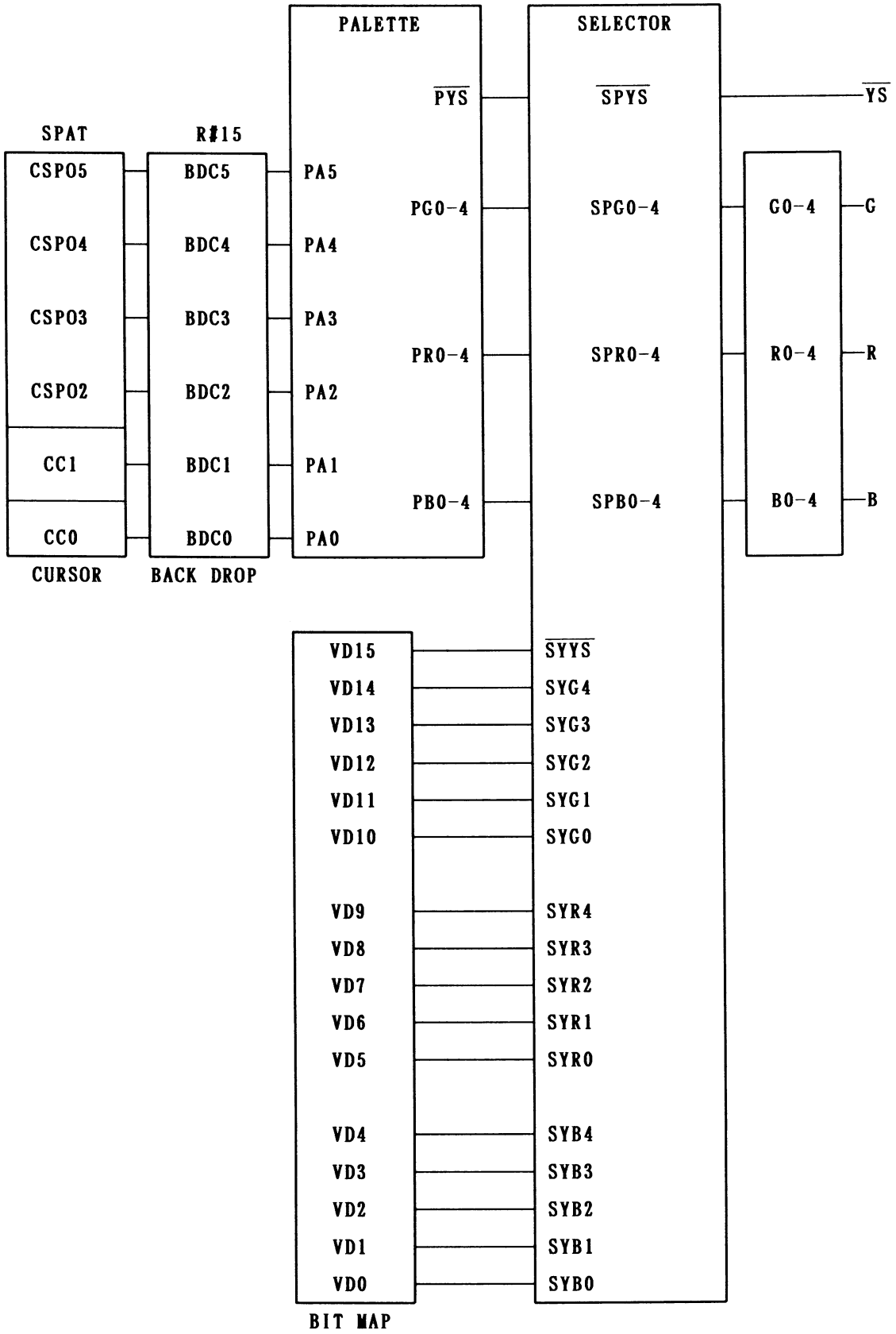
・CC1 and CC0 are data of cursor attribute table.

9.1.5 BYJKP



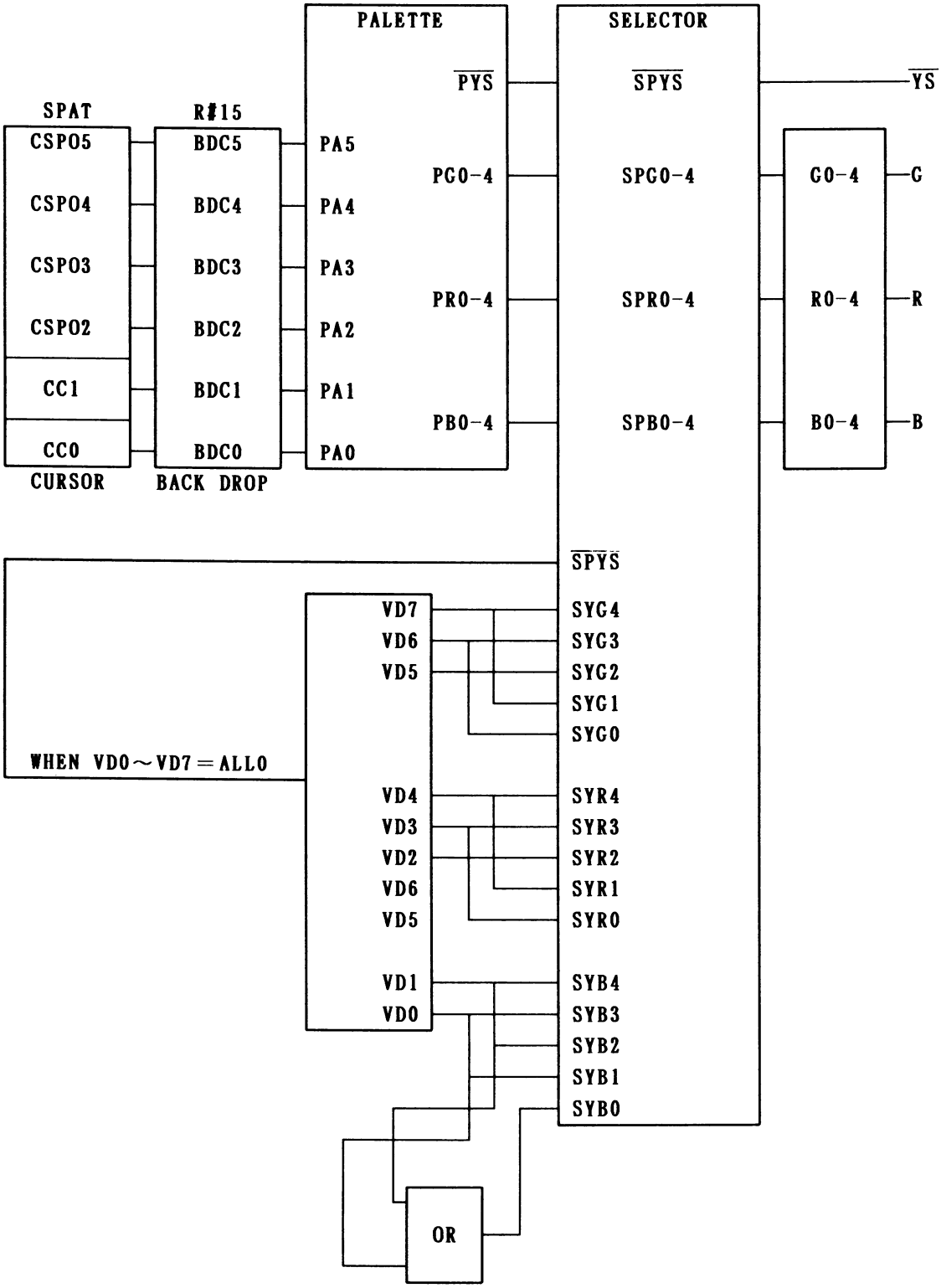
・CC1 and CC0 are data of cursor attribute table.

9.1.6 BD16



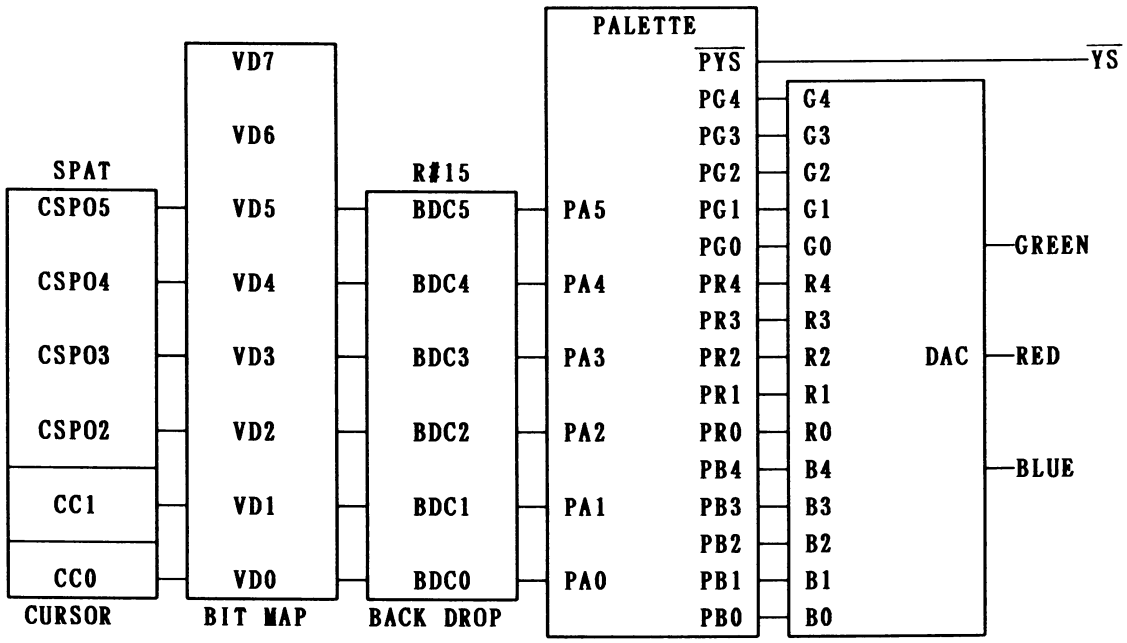
・CC1 and CC0 are data of cursor attribute table.

9.1.7 BD8



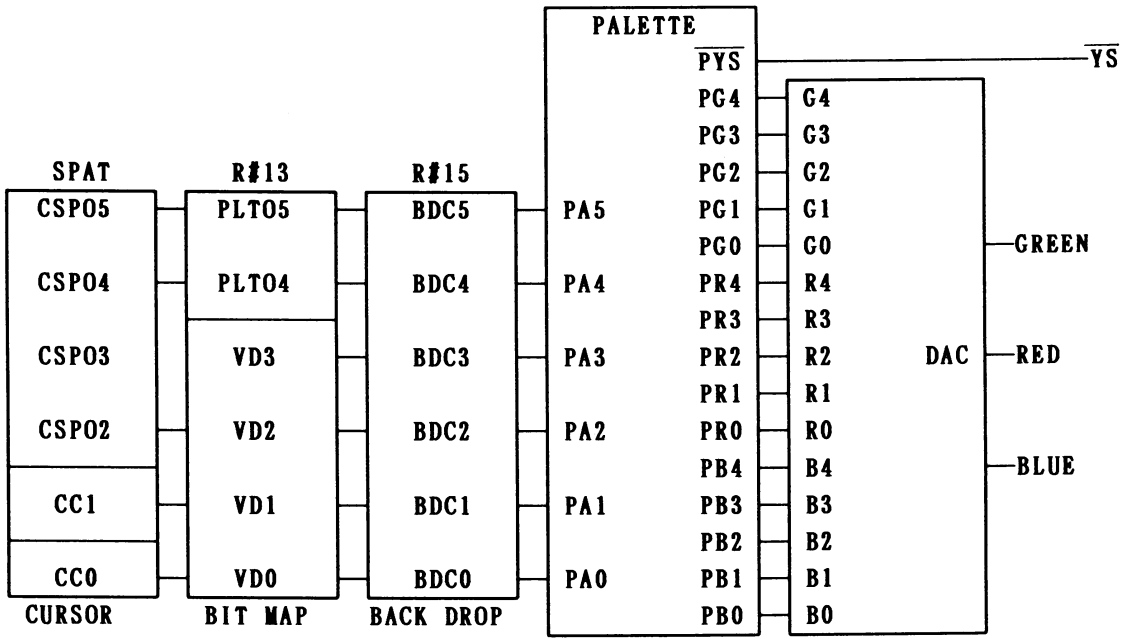
・CC1 and CC0 are data of cursor attribute table.

9.1.8 BP6



・CC1 and CC0 are data of cursor attribute table.

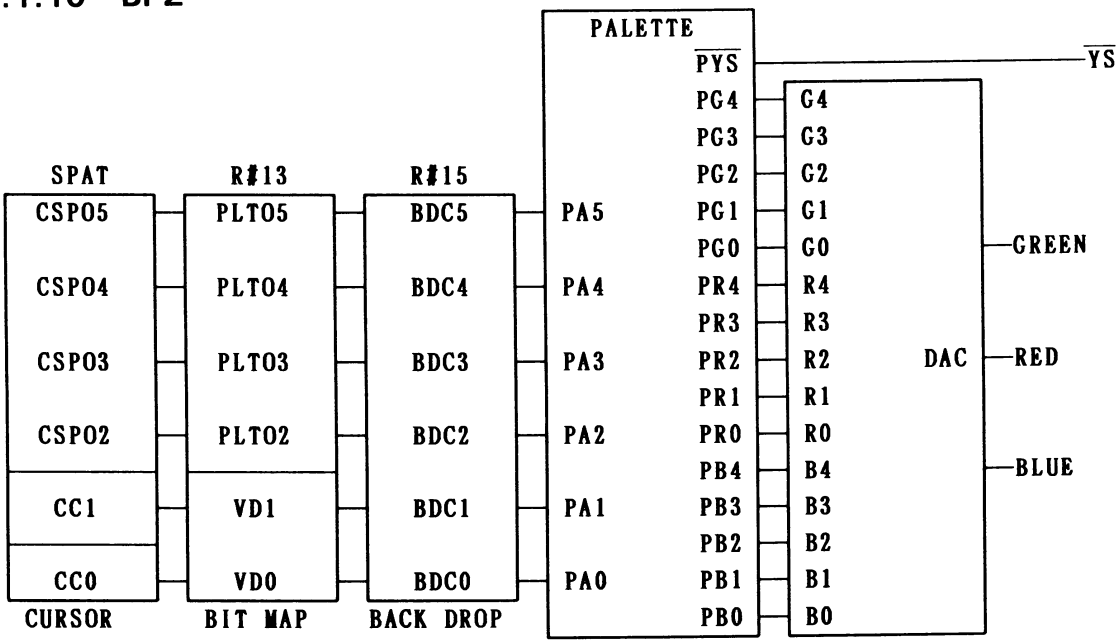
9.1.9 BP4



・CC1 and CC0 are data of cursor attribute table.

Note: When setting the color palette data in the B4, B5 and B6 modes, use the same value for each corresponding pair of palette addresses 0 to 31 and 32 to 63, that is, 0 and 32, 1 and 33 and so on.

9.1.10 BP2



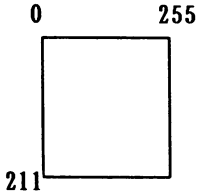
・CC1 and CC0 are data of cursor attribute table.

Note: When setting the color palette data in the B4, B5 and B6 modes, use the same value for each corresponding pair of palette addresses 0 to 31 and 32 to 63, that is, 0 and 32, 1 and 33 and so on.

10 DETAILS OF EACH SCREEN MODE

10.1 P1 MODE

10.1.1 Display area



When EO=0

Impossible when EO=1

10.1.2 Dot clock

MSC=0 DCKM=0 : 5.4MHz

10.1.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.1.4 Correspondence of image space and display area

The display start point (by dot) in the image space can be selected freely by using the scroll control register A (R#17 to 20) for the screen "A" and the scroll control register B (R#21 to 24) for the screen "B".

10.1.5 Allotment of screens "A" and "B" to the front and the rear

The priority control register (R#27) is used.

PRX1,PRX0 On the right side of the X co-ordinate specified by these bits, the front is "B" and the rear is "A".

PRY1,PRY0 On the lower side of the Y co-ordinate specified by these bits, the front is "B" and the rear is "A".

For the area where the above conditions are not met, the front is "A" and the rear is "B".

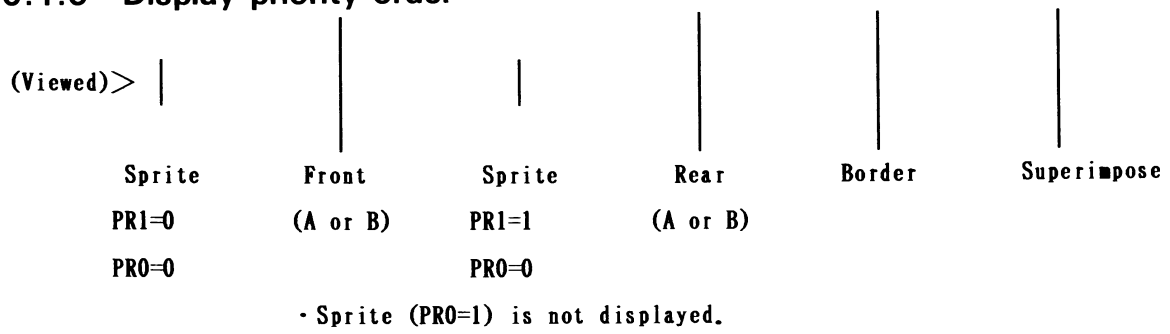
When PRX1=0 and PRX0=0, and PRY1=0 and PRY0=0, the front is "A" through the whole area.

		1	2	3	0	(PRX)
		64	128	192	256	(DOT)
	0	A	A	B	B	
1	64	A	A	B	B	
2	128	B	B	B	B	
3	192	B	B	B	B	
0	256					(211)

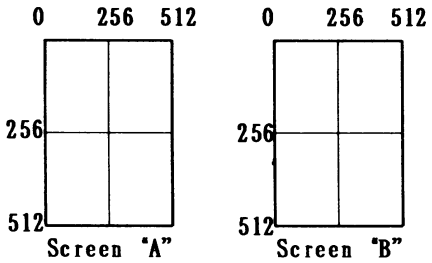
(PRY) (DOT)

(Example) When PRX1=1, PRX0=0 and PRY1=1, PRY0=0

10.1.6 Display priority order



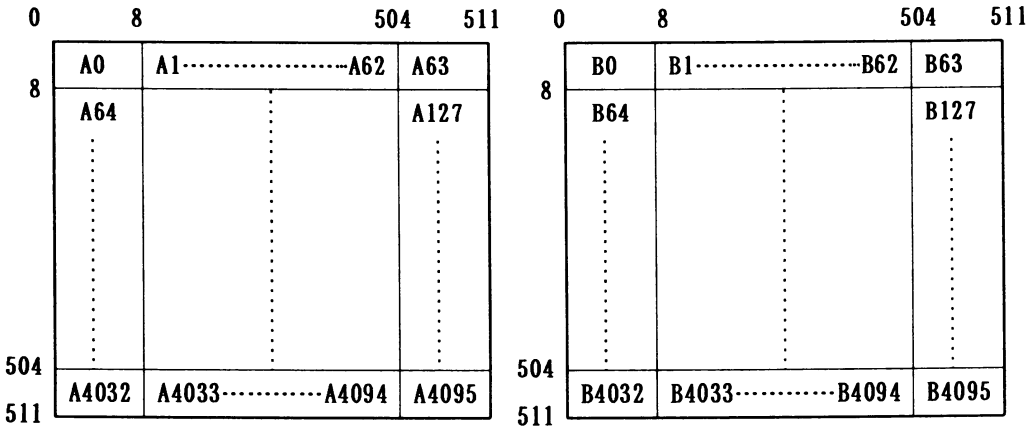
10.1.7 P1 image space



10.1.8 Correspondence of image space and name table

Each image space in screen "A" and screen "B" consists of 4096 (64×64) patterns each unit of which is 8×8 dots (16 colors/dot).

To each one of 0 to 4095 patterns on screen "A" and screen "B", 2 bytes on the pattern name table are assigned and by means of the value (pattern No.) to be written here, the font on the pattern generator table can be selected.



10.1.9 VRAM Pattern name table

7C000	A0	(LOW)
7C001	A0	(HIGH)
	⋮	
7DFFF	A4095	(HIGH)
7E000	B0	(LOW)
	⋮	
7FFFF	B4095	(HIGH)

10.1.10 Pattern No. maximum value

VRAM	Screen "A"	Screen "B"
128K	2015	1535
256K	4063	3583
512K	8159	7679

10.1.11 P1.VRAM pattern generator table

Screen A pattern generator table

00000	A0～31	
00400	A32～A63	
007FF	⋮	
0F800	A1984～A2015	VRAM128K
0FBFF	⋮	
1F800	A4032～A4063	VRAM256K
1FBFF	⋮	
3F800	A8128～A8159	VRAM512K
3FBFF		

Screen B pattern generator table

40000	B0～B31	
40400	B32～B63	
407FF	⋮	
4B800	B1504～B1535	VRAM128K
4BFFF	⋮	
5B800	B3552～B3583	VRAM256K
5BFFF	⋮	
7B800	B7648～B7679	VRAM512K
7BFFF		

10.1.12 P1 pattern generator table, bit assign

The bit map configuration is based on 256 dots (4bits/dot) in the X direction.

00000	A0～A31
003FF	

00000	LINE0	A0～A31,LINE0
00080	LINE1	A0～A31,LINE1
00100	⋮	
00380	LINE7	A0～A31,LINE7
003FF	LINE0	A32～A63,LINE0

MSB 7 6 5 4	3 2 1 0	LSB
00000 PC0	PC1	
00001 PC2	PC3	
00002 PC4	PC5	A0 LINE0
00003 PC6	PC7	
00004 PC0	PC1	A1 LINE0
⋮		
0007F PC6	PC7	A31 LINE0
00080 PC0	PC1	A0 LINE1

10.1.13 P1 sprite

- The sprite size of 16×16 dots can be used up to 125 pieces.
- The lower 4 bits of the palette address belong to 1 dot of the sprite and the upper 2 bits to 1 sprite and 64 colors (16 colors on one sprite) can be used simultaneously.

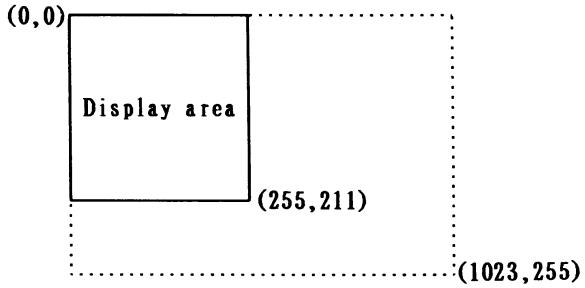
- Up to 16 sprites can be displayed on one horizontal line. (The smaller the sprite No. is, the higher priority the sprite has.)
- The priority between the sprite and pattern screens (front and rear) can be specified. (The priority is higher when on the horizontal line.)

10.1.14 P1 sprite attribute table

3FE00	SP0
3FE04	SP1
3FE08	
3FFF0	SP124
3FFF3	

	D7	D6	D5	D4	D3	D2	D1	D0	
3FE00	SOY7	SOY6	SOY5	SOY4	SOY3	SOY2	SOY1	SOY0	Y co-ordinate
3FE01	SOP7	SOP6	SOP5	SOP4	SOP3	SOP2	SOP1	SOP0	Pattern No.
3FE02	SOX7	SOX6	SOX5	SOX4	SOX3	SOX2	SOX1	SOX0	X co-ordinate
3FE03	SC5	SC4	PR1	PR0	—	—	SOX9	SOX8	Additional information

- Co-ordinates space



Both X and Y co-ordinate spaces roll in this size.
The vertical display position is the specified Y co-ordinate plus "1".

- Displayed color Palette Address

A5	A4	A3 A2 A1 A0
SC5	SC4	SGT data

Clear color when SGT data are all "0".

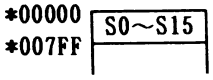
- Display priority order

PR1	PR0	Priority order
0	0	SP>A>B>BD
1	0	A>SP>B>BD
—	1	A>B>BD

SP:Sprite plane
A :Front
B :Rear
BD:Back drop plane
Sprite is not displayed when PR0=1.

10.1.15 P1 sprite generator table

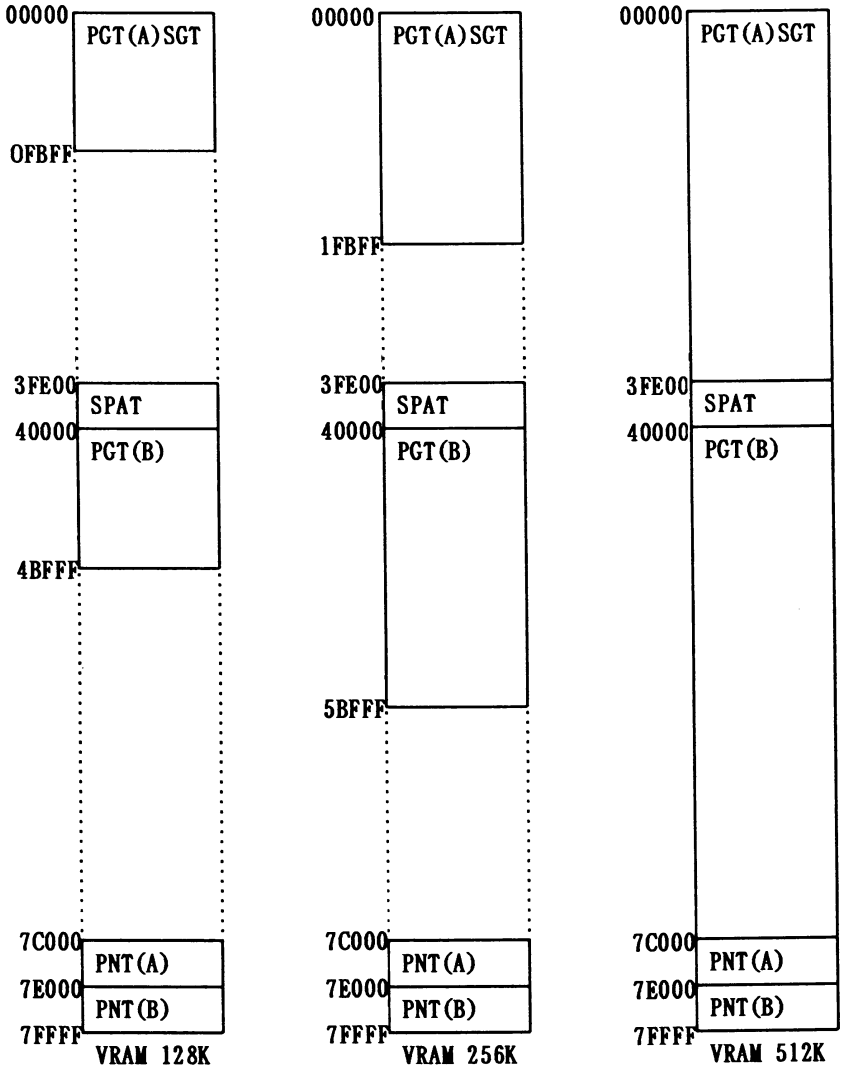
*The base address (SGBA) is specified with R#25.



*00000	LINE0	S0~S15,LINE0
*00080	LINE1	S0~S15,LINE1
*00100	⋮	
*00780	LINE15	S0~S15,LINE15
*007FF	LINE0	S16~S31,LINE0

	MSB 7 6 5 4	3 2 1 0 LSB	
*00000	SC0	SC1	
	⋮		S0 LINE0
*00007	SC14	SC15	
*00008	SC0	SC1	S1 LINE0
	⋮		
*0007F	SC14	SC15	S15 LINE0
*00080	SC0	SC1	S0 LINE1

10.1.16 P1.VRAM MAP



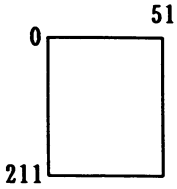
・The physical address of VRAM is divided at the uppermost bit of the logical address.

Uppermost bit=0:VRAM0

Uppermost bit=1:VRAM1

10.2 P2 mode

10.2.1 Display area



When EO=0
Impossible when EO=1

10.2.2 Dot clock

MSC=0 DCKM=1 : 10.7MHz

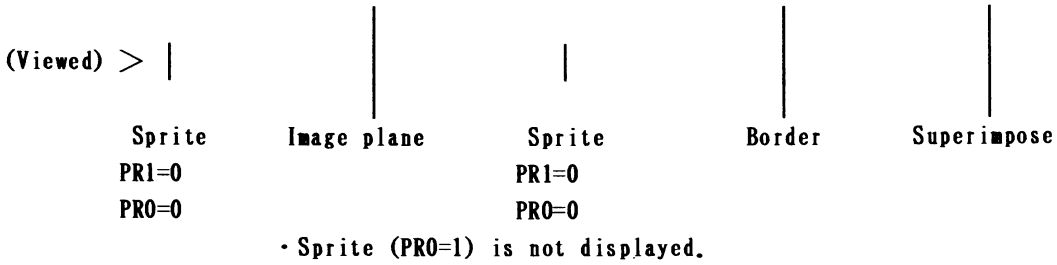
10.2.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.2.4 Correspondence of image space and display area

The display start point (by dot) in the image space can be selected freely by using the scroll control register A (R#17 to 20).

10.2.5 Display priority order

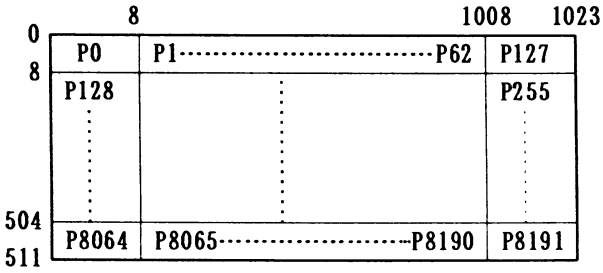


・Sprite (PR0=1) is not displayed.

10.2.6 Correspondence of image space and pattern name table

The image space consists of 8192 (128×128) patterns each unit of which is 8×8 dots (16 colors/dot).

To each one of 0 to 8191 patterns, 2 bytes on the pattern name table are assinged and by means of the value (pattern No.) to be written here, the font on the pattern generator table can be selected.



10.2.7 VRAM pattern name table

7C000	P0	(LOW)
7C001	P0	(HIGH)
	⋮	
7FFFF	P8191	(HIGH)

10.2.8 Pattern No. maximum value

VRAM	
128K	3071
256K	7167
512K	15359

・Maximum value that can be written into the pattern generator table.

10.2.9 P2.VRAM pattern generator table

Pattern generator table

00000	P0～P63	
00800	P64～P127	
00FFF	⋮	
17800	P3008～P3071	VRAM128K
17FFF	⋮	
37800	P7104～P7167	VRAM256K
37FFF	⋮	
77800	P15296～P15359	VRAM512K
77FFF		

10.2.10 P2 pattern generator table, bit assign

The bit map configuration is based on 512 dots (4bits/dot) in the X direction.

00000	A0～A63
007FF	

00000	LINE0	P0～P63,LINE0
00100	LINE1	P0～P63,LINE1
00200	⋮	
00700	LINE7	P0～P63,LINE7
007FF	LINE0	P64～P128,LINE0

MSB 7 6 5 4 3 2 1 0 LSB			
00000	PC0	PC1	.....
00001	PC2	PC3	P0 LINE0
00002	PC4	PC5	
00003	PC6	PC7	.....
00004	PC0	PC1	P1 LINE0
	⋮		
000FF	PC6	PC7	P63 LINE0
00100	PC0	PC1	..... P0 LINE1

10.2.11 P2 sprite

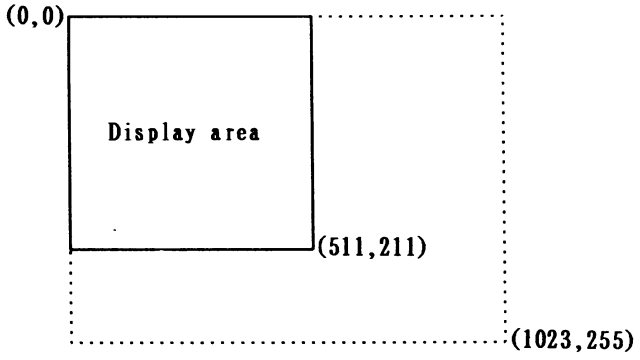
- The sprite size of 16×16 dots can be used up to 125 pieces.
- The lower 4 bits of the palette address belong to 1 dot of the sprite and the upper 2 bits to 1 sprite and 64 colors (16 colors on one sprite) can be used simultaneously.
- Up to 16 sprites can be displayed on one horizontal line. (The smaller the sprite No. is, the higher priority the sprite has.)

10.2.12 P2 sprite attribute table

7BE00	SP0
7BE04	SP1
7BE08	
7BFF0	SP124
7BFF3	

	D7	D6	D5	D4	D3	D2	D1	D0	
7BE00	SOY7	SOY6	SOY5	SOY4	SOY3	SOY2	SOY1	SOY0	Y co-ordinate
7BE01	SOP7	SOP6	SOP5	SOP4	SOP3	SOP2	SOP1	SOP0	Pattern No.
7BE02	SOX7	SOX6	SOX5	SOX4	SOX3	SOX2	SOX1	SOX0	X co-ordinate
7BE03	SC5	SC4	PR1	PR0	—	—	SOX9	SOX8	Additional Information

- Co-ordinate space



Both X and Y co-ordinate spaces role in this size.

The vertical display position is the specified Y co-ordinate plus 1.

- Displayed color Palette Address

A5	A4	A3 A2 A1 A0
SC5	SC4	SGT data

Clear color when SGT data are all "0".

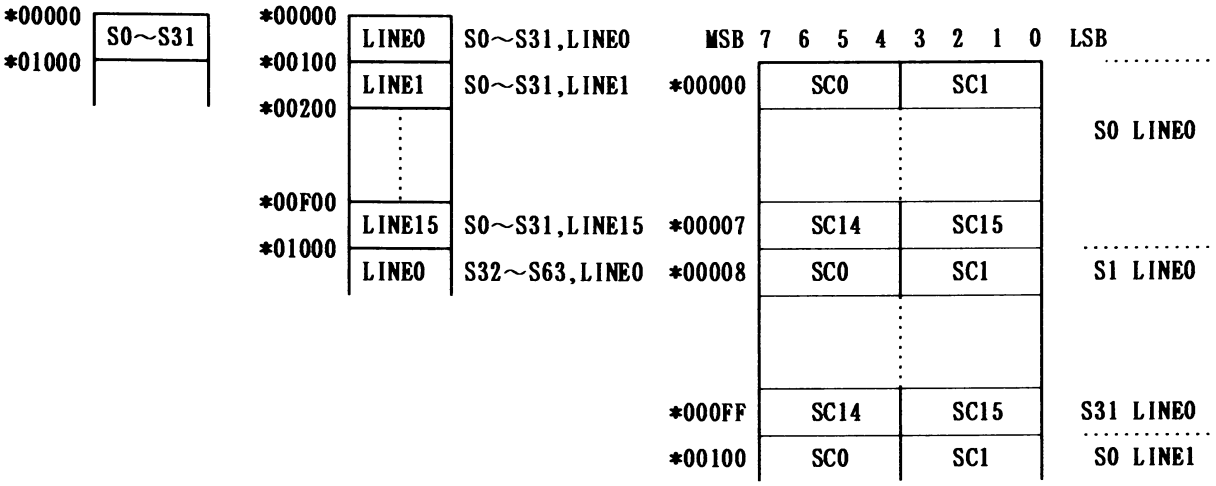
- Display priority order

PR1	PR0	Priority order
0	0	SP>A>BD
1	0	A>SP>BD
—	1	A>BD

SP:Sprite plane
A :Image plane
BD:Back drop plane
Sprite is not displayed when PR0=1.

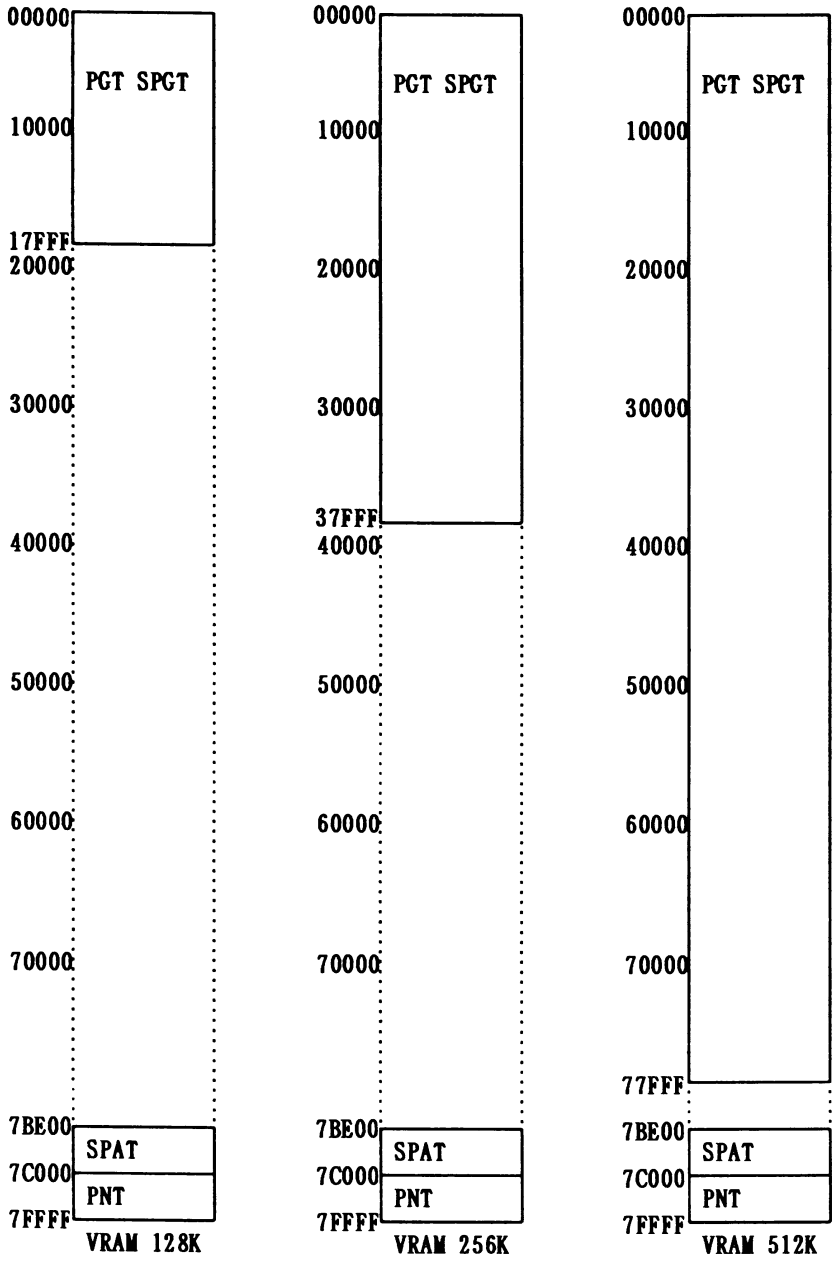
10.2.13 P2 sprite generator table

*The base address (SGBA) is specified with R#25.



・The same VRAM address is commonly used with the pattern generator table.

10.2.14 P2.VRAM MAP



・Physical address of VRAM

PGT Lowermost bit=0:VRAM0

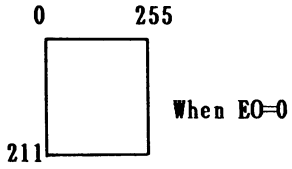
Lowermost bit=1:VRAM1

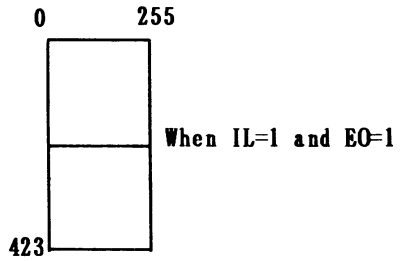
SPAT VRAM0

PNT VRAM1

10.3 B1 mode

10.3.1 Display area





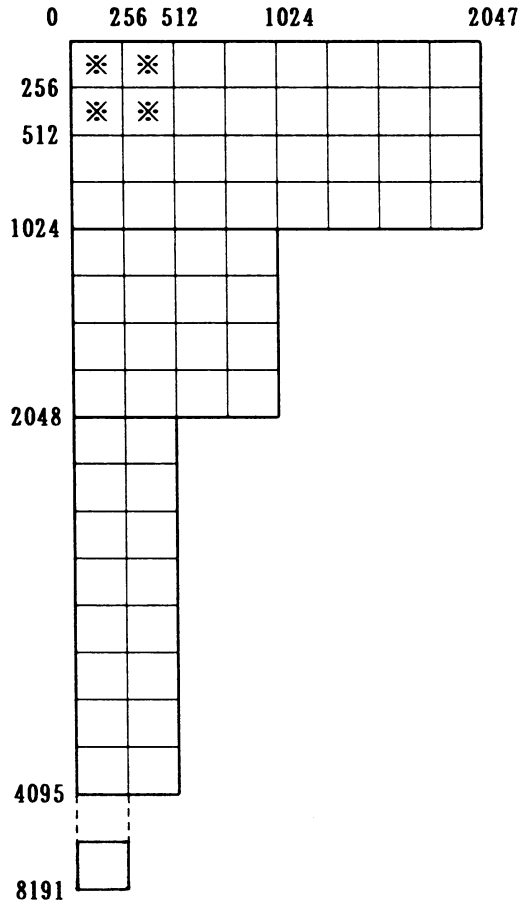
10.3.2 Dot clock

MCS=0 DCKM=0 : 5.4MHz

10.3.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.3.4 Image space



10.3.5 Number of usable screens

Supposing that 1 screen consists of 256×256 dots:

	【COLOR】		16	8	4	2 (BIT/DOT)
	CLRM1		1	1	0	0
	CLRM0		1	0	1	0
【VRAM】	VSL1	VSL0				
512K	1	0	4	8	16	32
256K	0	1	2	※4	8	16
128K	0	0	1	2	4	8
(BYTE)						

XIMM1	XIMM0	:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots
0	1	:	512 dots※
0	0	:	256 dots

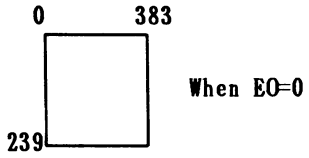
Number of dots in Y direction is automatically calculated from the above 6 bits.

※ (Example) Image space when CLRM1=1,CLRM0=0 VSL1=0,VSL0=1 XIMM1=0,XIMM0=1.

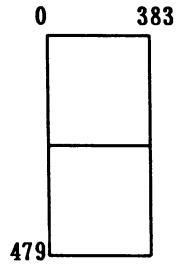
10.4 B2 mode

10.4.1 Display area

With over scan applied



When EO=0



When IL=1 and EO=1

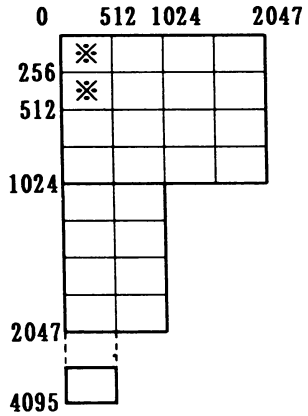
10.4.2 Dot clock

MCS=1 DCKM=1 : 7.2MHz

10.4.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.4.4 Image space



10.4.5 Number of usable screens

Supposing that 1 screen consists of 512×256 dots :

	[COLOR]		16	8	4	2	(BIT/DOT)
	CLRM1		1	1	0	0	
	CLRM0		1	0	1	0	
[VRAM]	VSL1	VSL0					
512K	1	0	2	4	8	16	
256K	0	1	1	※2	4	8	
128K	0	0	0	1	2	4	
(BYTE)							

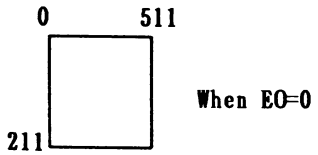
XIMM1	XIMM0	:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots
0	1	:	512 dots ※

Number of dots in Y direction is automatically calculated from the above 6 bits.

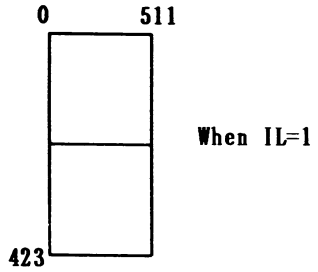
※ (Example) Image space when CLRM1=1,CLRM0=0 VSL1=0,VSL0=1 XIMM1=0,XIMM0=1.

10.5 B3 mode

10.5.1 Display area



When EO=0



When IL=1 and EO=1

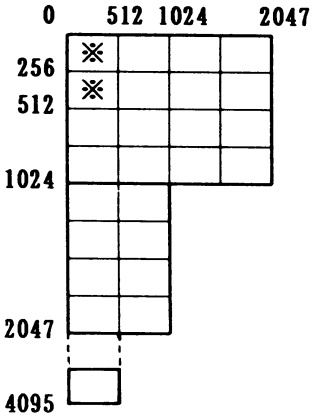
10.5.2 Dot clock

MCS=0 DCKM=1 : 10.7MHz

10.5.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.5.4 Image space



10.5.5 Number of usable screens

Supposing that 1 screen consists of 512×256 dots:

	[COLOR]		16	8	4	2 (BIT/DOT)
	CLRM1		1	1	0	0
	CLRM0		1	0	1	0
[VRAM]	VSL1	VSL0				
512K	1	0	2	4	8	16
256K	0	1	1	※2	4	8
128K (BYTE)	0	0	0	1	2	4

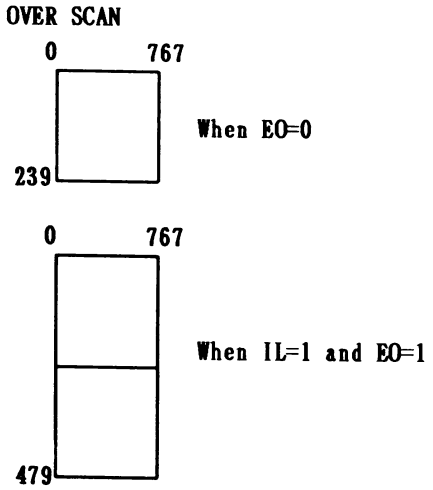
XIMM1	XIMM0	:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots
0	1	:	512 dots ※

Number of dots in Y direction is automatically calculated from the above 6 bits.

※ (Example) Image space when CLRM1=1,CLRM0=0 VSL1=0,VSL0=1 XIMM1=0,XIMM0=1.

10.6 B4 mode

10.6.1 Display area



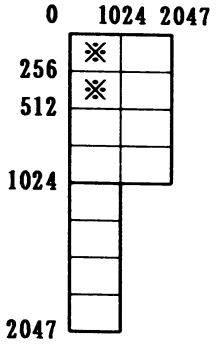
10.6.2 Dot clock

MCS=1 DCKM=2 : 14.3MHz

10.6.3 Horizontal synchronous frequency

HSCN=0 : 15.7KHz

10.6.4 Image space



10.6.5 Number of usable screens

Supposing that 1 screen consists of 1024×256 dots:

	[COLOR]		4	2
	CLRM1		0	0
	CLRM0		1	0
[VRAM]	VSL1	VSL0		
512K	1	0	4	8
256K	0	1	※2	4
128K	0	0	1	2
(BYTE)				

(BIT/DOT)

XIMM1	XIMM0		
		:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots ※

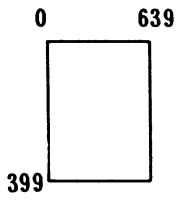
Number of dots in Y direction is automatically calculated from the above 6 bits.

※ (Example) Image space when CLRM1=0,CLRM0=1 VSL1=0,VSL0=1 XIMM1=1,XIMM0=0.

Note: When setting the color palette data, use the same value for each corresponding pair of palette addresses 0 to 31 and 32 to 63, that is, 0 and 32, 1 and 33 and so on.

10.7 B5 mode

10.7.1 Display area



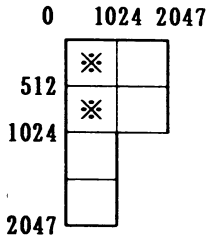
10.7.2 Dot clock

MCS=0 DCKM=2 : 21.5MHz

10.7.3 Horizontal synchronous frequency

HSCN=1 : 24.8KHz

10.7.4 Image space



10.7.5 Number of usable screens

Supposing that 1 screen consists of 1024×256 dots:

	[COLOR]		4	2 (BIT/DOT)
	CLRM1		0	0
	CLRM0		1	0
[VRAM]	VSL1	VSL0		
512K	1	0	2	4
256K	0	1	1	※2
128K (BYTE)	0	0	0	1

XIMM1	XIMM0	:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots ※

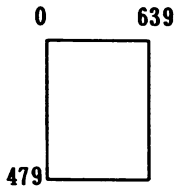
Number of dots in Y direction is automatically calculated from the above 6 bits.

※ (Example) Image space when CLRM1=0,CLRM0=0 VSL1=0,VSL0=1 XIMM1=1,XIMM0=0.

Note: When setting the color palette data, use the same value for each corresponding pair of palette addresses 0 to 31 and 32 to 63, that is, 0 and 32, 1 and 33 and so on.

10.8 B6 mode

10.8.1 Display area



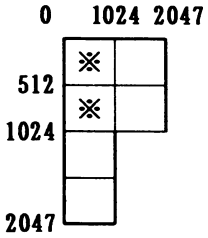
10.8.2 Dot clock

MCS=0 DCKM=2,C25M=1 : 25.2MHz

10.8.3 Horizontal synchronous frequency

HSCN=1 : 31.5KHz

10.8.4 Image space



10.8.5 Number of usable screens

Supposing that 1 screen consists of 1024×256 dots:

	[COLOR]		4	2 (BIT/DOT)
	CLRM1		0	0
	CLRM0		1	0
[VRAM]	VSL1	VSL0		
512K	1	0	2	4
256K	0	1	1	※2
128K	0	0	0	1
(BYTE)				

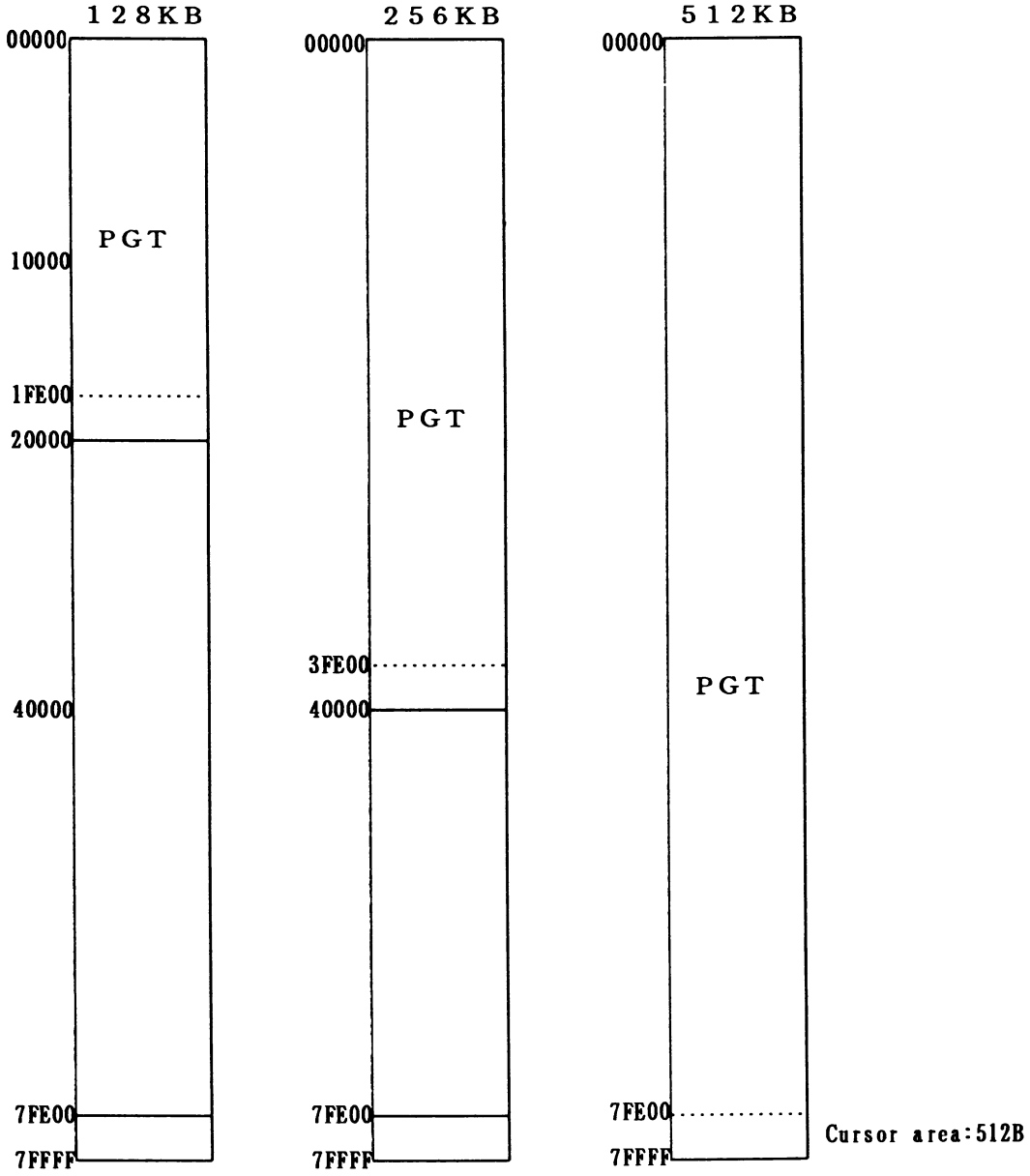
XIMM1	XIMM0		
		:	Number of dots in X direction in image space selected
1	1	:	2048 dots
1	0	:	1024 dots ※

Number of dots in Y direction is automatically calculated from the above 6 bits.

※ (Example) Image space when CLRM1=0,CLRM0=0 VSL1=0,VSL0=1 XIMM1=1,XIMM0=0.

Note: When setting the color palette data, use the same value for each corresponding pair of palette addresses 0 to 31 and 32 to 63, that is, 0 and 32, 1 and 33 and so on.

10.9 VRAM MAP (B1～B6)



VRAM (256KB) to image space correspondence when the dot Number in the X direction of the image space is 512 at 8BIT/DOT in B1 mode.

	0	1		511	
0	0	1	.....	1FE	1FF
	200				3FF
511	3FE00	3FE01	.....	3FFFE	3FFFF

- When using a cursor, 512 bytes from the upper address of VRAM are used as the data area for the cursor. Display is also possible in this area.(No skipping occurs during display.)

- Access to the cursor data area should be done by making use of the image (7FE00~) of upper 512 bytes of the entire VRAM space. By doing so, compatibility of the software between different VRAM models can be retained.

10.10 PGT bit assign (B1 ~ B6)

2BIT/DOT

	D7 D6	D5 D4	D3 D2	D1 D0
00000	0,0	1,0	2,0	3,0
00001	4,0	5,0	6,0	7,0
00002	8,0	9,0	10,0	11,0

4BIT/DOT

	D7 D6	D5 D4	D3 D2	D1 D0
00000	0,0		1,0	
00001	2,0		3,0	
00002	4,0		5,0	

8BIT/DOT

	D7 D6	D5 D4	D3 D2	D1 D0
00000	0,0			
00001	1,0			
00002	2,0			

16BIT/DOT

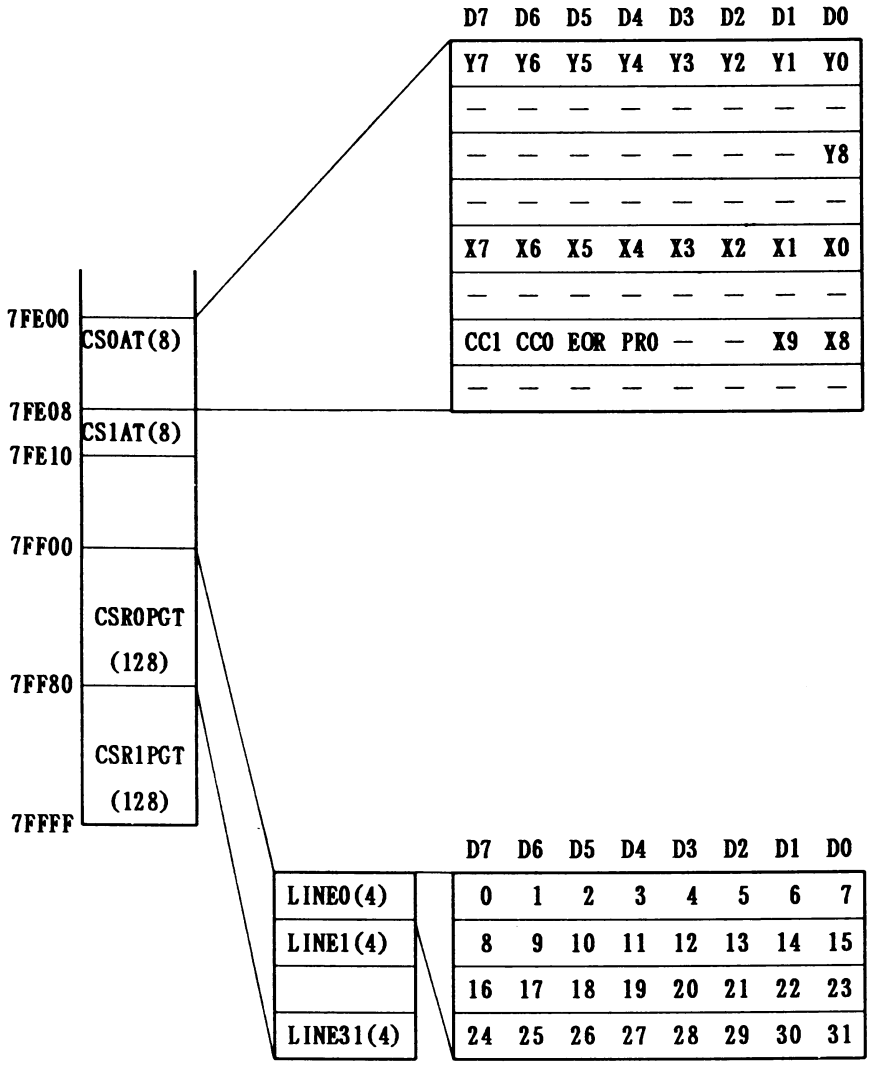
	D7 D6	D5 D4	D3 D2	D1 D0
00000	0,0 LOW			
00001	0,0 HIGH			
00002	1,0 LOW			

10.11 VRAM physical address (B1 ~ B6)

VRAM0 is mapped to the address (even address) where LSB of the logical address is "0" and VRAM1 to the address where LSB is "1".

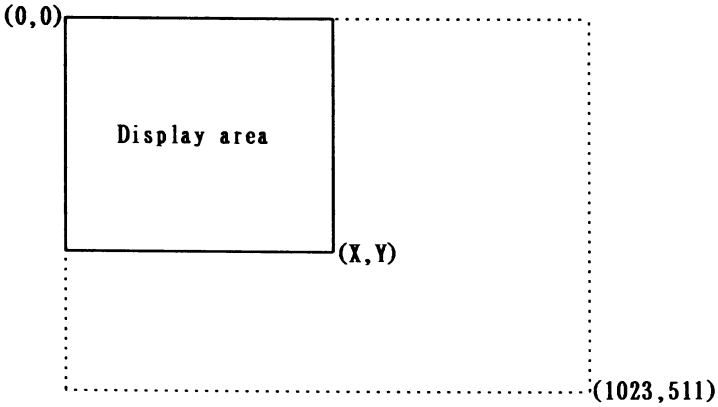
Each physical address of VRAM0 and VRAM1 becomes a logical address divided by 2.

10.12 Cursor area bit assign (B1～B6)



10.13 Cursor display specifications (B1～B6)

・Co-ordinate space



Both X and Y co-ordinate spaces roll in this size.

The vertical display position is the specified Y co-ordinate plus "1" (plus "2" for interlace).

・Displayed color

Palette Address

A5	A4	A3	A2	A1	A0
CSPO5	CSPO4	CSPO3	CSPO2	CC1	CC0

Clear color : PGT data="0" or (CC1,CC0,EOR)=("0","0","0")

EOR color displayed on image screen : (CC1,CC0,EOR)=("0","0","1")

・Display control

PRO="1" : Not displayed

PRO="0" : Displayed

11 COMMAND

11.1 Command execution method

After setting the necessary parameter register, set the command to the operation code register, and it will be executed. As soon as execution is started, the status CE is set to "1" and upon completion, it is reset to "0". Furthermore, the interrupt flag CE is set to "1".

Most commands are issued after the necessary registers out of the following parameters are set. Also some commands require output and input of the necessary data at and through the command data port after they are issued.

1. Source (for transfer) co-ordinate
2. Destination (for transfer) co-ordinate
3. Transfer range co-ordinates
4. Argument, logical operation and write mask
5. Font color

11.2 Parameter setting

Source (for transfer) co-ordinate · address

	b7	b6	b5	b4	b3	b2	b1	b0
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	KA7	KA6	KA5	KA4	KA3	KA2	KA1	KA0
R#33						SX10	SX9	SX8
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
	KA15	KA14	KA13	KA12	KA11	KA10	KA9	KA8
R#35					SY11	SY10	SY9	SY8
						SA18	SA17	SA16
							KA17	KA16

· There are 3 ways of setting depending on types of command as follows.

1) LMCM、LMMM、BMLX、SRCH、POINT

SX0-10 : Specified with the X co-ordinate of the image co-ordinate space (by dots) and rolling to "0" occurs when a larger value than the image size is used for setting. (When in P1 mode, screen "A" is selected at SX9=0 and screen "B" at SX9=1.)

SY0-11 : Specified with the Y co-ordinate of the image co-ordinate space (by dots) and rolling to "0" occurs when a larger value than the image size is used for setting.

2) CMMM、BMXL、BMLL

SA0-18 : Specified with the address on the VRAM map (by bytes).

3) CMMK

KA0-17 : Specified with the kanji ROM address (by bytes).

Destination (for transfer) co-ordinate · address

	b7	b6	b5	b4	b3	b2	b1	b0
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0
	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R#37						DX10	DX9	DX8
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0
	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
R#39					DY11	DY10	DY9	DY8
						DA18	DA17	DA16

· There are 2 ways of setting depending on types of command as follows.

1) LMMC、LMMV、LMMM、CMMC、CMMK、CMMM、BMXL、LINE、PSET、ADVN

DX0-10 : Specified with the X co-ordinate of the image co-ordinate space (by dots) and rolling to "0" occurs when a larger value than the image size is used for setting (When in P1 mode, screen "A" is selected at DX9=0 and screen "B" at DX9=1.)

DY0-11 : Specified with the Y co-ordinate of the image co-ordinate space (by dots) and rolling to "0" occurs when a larger value than the image size is used for setting.

2) BMLX、BMLL

DA0-18 : Specified with the address on the VRAM map (by bytes).

Transfer range co-ordinate · address

	b7	b6	b5	b4	b3	b2	b1	b0
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0
	NA7	NA6	NA5	NA4	NA3	NA2	NA1	NA0
	MJ7	MJ6	MJ5	MJ4	MJ3	MJ2	MJ1	MJ0
R#41						NX10	NX9	NX8
					MJ11	MJ10	MJ9	MJ8
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0
	NA15	NA14	NA13	NA12	NA11	NA10	NA9	NA8
	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
R#43					NY11	NY10	NY9	NY8
						NA18	NA17	NA16
					MI11	MI10	MI9	MI8

· There are 3 ways of setting depending on types of command as follows.

1) LMMC、LMMV、LMCM、LMMM、CMMC、CMMK、CMMM、BMXL、BMLX

NX0-10 : The number of dots in X direction of the image co-ordinate space is specified and rolling to "0" occurs when the specified range exceeds the image size. (Maximum value is 2048 dots when all "0".)

NY0-11 : The number of dots in Y direction of the image co-ordinate space is specified and rolling to "0" occurs when the specified range exceeds the image size. (Maximum value is 4096 dots when all "0".)

2) BMLL

NA0-18 : The number of bytes on the VRAM map is specified and rolling to address "0" occurs when the specified range exceeds the VRAM capacity. (Maximum value is 512K bytes when all "0".)
Note) 256 bytes when NA7 to NA0 are all "0".

3) LINE

MJ0-11 : The length of the longer side of the rectangle whose diagonal line is the same as the drawn line is specified by dots. When the specified range exceeds the image size, rolling to "0" occurs.

MI0-11 : The length of the shorter side of the rectangle whose diagonal line is the same as the drawn line is specified by dots. When the specified range exceeds the image size, rolling to "0" occurs.

Argument

	b7	b6	b5	b4	b3	b2	b1	b0
R#44					DIY	DIX	NEQ	MAJ

· DIY DIX : The transfer direction (plus direction at "0" and minus direction at "1") from the base co-ordinates is specified. With BMXL and BMLX, however, the linear address specified side is fixed to "plus" and with BMLL, both X and Y are specified to the same direction.

· NEQ : In the border color specification for SRCH, "0" is for specified color detection and "1" is for non-specified color detection.

· MAJ : In the line inclination specification for LINE, X is the longer side and Y the shorter side at "0" while Y is the longer side and X the shorter side at "1".

Logical operation

	b7	b6	b5	b4	b3	b2	b1	b0
R#45				TP	L11	L10	L01	L00

- When drawing by means of commands, it is possible to write the value (WC) obtained through the logical operation using the value to be drawn (SC) and the target value (DC). The content of the operation is specified as follows.
  - L00 : WC value for the bit with SC=0 and DC=0
  - L01 : WC value for the bit with SC=0 and DC=1
  - L10 : WC value for the bit with SC=1 and DC=0
  - L11 : WC value for the bit with SC=1 and DC=1
  - TP : When this bit is "1", the data with SC as all "0" (by dot for the X-Y co-ordinates and by byte for the linear address) is not transferred.

<Example>

Logical operation	L11	L10	L01	L00
WC=SC	1	1	0	0
WC=$\overline{SC}$	0	0	1	1
WC= (SC AND DC)	1	0	0	0
WC= (SC OR DC)	1	1	1	0
WC= (SC EOR DC)	0	1	1	0

Write mask

	b7	b6	b5	b4	b3	b2	b1	b0
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8

- When drawing by means of commands, writing can be prohibited by bits. With WM0-7 and WM8-15, VRAM0 bit and VRAM1 bit are specified respectively. Then "1" is for write enable and "0" is for write prohibit.
- In P1 mode, writing is prohibited on the side not specified as the transfer destination. (Screen "A":R#46, Screen "B":R#47)

Font color

	b7	b6	b5	b4	b3	b2	b1	b0
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8
R#50	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
R#51	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

- The font color (color code) is specified for CMMC, CMMK and CMMM. Also, the drawing color for LMMV, LINE and PSET and the border color for SRCH are specified by using FC0-15. Correspondence with VRAM bit position is the same as write mask.
  - FC0-15 : Color code of font data "1"
  - BC0-15 : Color code of font data "0"

Note) Depending on conditions of R#6 (CLRM1, CLRM0), use the following data setting for FC0 - 15 of R#48 and R#49 (BC0 - 15 of R#50 and R#51).
- 16 bit/dot ··· Write 16 bit data for FC0 - FC15.
- 8 bit/dot ··· Write the same data for FC0 - 7 and FC8 -15.
- 4 bit/dot ··· Write the same data for FC0 - 3, FC4 - 7, FC8 - 11 and FC12 - 15.
- 2 bit/dot ··· Fill FC0 - 15 with the same eight 2-bit unit data.

11.3 Setting of operation code

Operation code

	b7	b6	b5	b4	b3	b2	b1	b0
R#52	OP3	OP2	OP1	OP0	AYM	AYE	AXM	AXE

- When a code from the list below is written in this register, the corresponding command will be executed.

OP3	OP2	OP1	OP0	AYM	AYE	AXM	AXE	Mnemonic	Operation
0	0	0	0	0	0	0	0	STOP	Command being executed is stopped.
0	0	0	1	0	0	0	0	LMMC	Data is transferred from CPU to VRAM rectangle area.
0	0	1	0	0	0	0	0	LMMV	VRAM rectangle area is painted out.
0	0	1	1	0	0	0	0	LMCM	VRAM rectangle area data is transferred to CPU.
0	1	0	0	0	0	0	0	LMMM	Rectangle area data is transferred from VRAM to VRAM.
0	1	0	1	0	0	0	0	CMMC	CPU character data is color-developed and transferred to VRAM rectangle area.
0	1	1	0	0	0	0	0	CMMK	Kanji ROM data is color-developed and transferred to VRAM rectangle area.
0	1	1	1	0	0	0	0	CMMM	VRAM character data is color-developed and transferred to VRAM rectangle area.
1	0	0	0	0	0	0	0	BMXL	Data on VRAM linear address is transferred to VRAM rectangle area.
1	0	0	1	0	0	0	0	BMLX	VRAM rectangle area data is transferred onto VRAM linear address.
1	0	1	0	0	0	0	0	BMLL	Data on VRAM linear address is transferred onto VRAM linear address.
1	0	1	1	0	0	0	0	LINE	Straight line is drawn on X-Y co-ordinates.
1	1	0	0	0	0	0	0	SRCH	Border color co-ordinates on X-Y space are detected.
1	1	0	1	0	0	0	0	POINT	Color code of specified point on X-Y co-ordinates is read out.
1	1	1	0	1/0	1/0	1/0	1/0	PSET	Drawing is executed at drawing point on X-Y co-ordinates.
1	1	1	1	1/0	1/0	1/0	1/0	ADVN	Drawing point on X-Y co-ordinates is shifted.

- With PSET and ADVN, the drawing point can be shifted after executing the command.

AXE	AXM	
0	0	(DX, DY) is used as a pointer.
0	1	The pointer is not shifted.
1	0	The pointer is shifted to the right by 1 dot.
1	1	The pointer is shifted to the left by 1 dot.

AYE	AYM	
0	0	The pointer is not shifted.
0	1	The pointer is not shifted.
1	0	The pointer is shifted down by 1 dot.
1	1	The pointer is shifted up by 1 dot.

11.4 Command data

Border color co-ordinates

	b7	b6	b5	b4	b3	b2	b1	b0
R#53	BX7	BX6	BX5	BX4	BX3	BX2	BX1	BX0
R#54	"0"	"0"	"0"	"0"	"0"	BX10	BX9	BX8

- When the border color is detected after the SRCH command has been executed, the X co-ordinate then can be read.

Command data port

	b7	b6	b5	b4	b3	b2	b1	b0
P#2	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

- The command data can be inputted and output by making an access to this port after issuing the LMMC, LMCM or POINT command. The data format varies depending on the type of command and number of colors.

LMMC、LMCM

When 2bit/dot

	CD7 CD6	CD5 CD4	CD3 CD2	CD1 CD0
1st byte	1stdot	2nddot	3rddot	4thdot
2nd byte	5thdot	6thdot	7thdot	8thdot

⋮

When 4bit/dot

	CD7 CD6 CD5 CD4	CD3 CD2 CD1 CD0
1st byte	1st dot	2nd dot
2nd byte	3rd dot	4th dot

⋮

When 8bit/dot

	CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0
1st byte	1st dot
2nd byte	2nd dot

⋮

When 16bit/dot

	CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0
1st byte	1st dot color code low
2nd byte	1st dot color code high
3rd byte	2nd dot color code low

⋮

POINT

When 2bit/dot

CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
col.code		unspecified					

When 4bit/dot

CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
color code				unspecified			

When 8bit/dot

CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
color code							

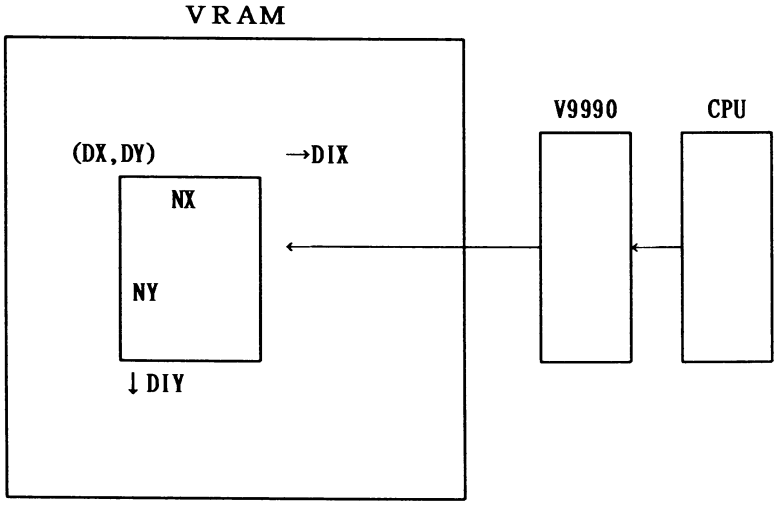
When 16bit/dot

	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
1st byte	color code low							
2nd byte	color code high							

11.5 Outline of commands

11.5.1 LMMC (Logical Move to Memory from CPU)

The data is transferred from CPU to VRAM rectangle area.



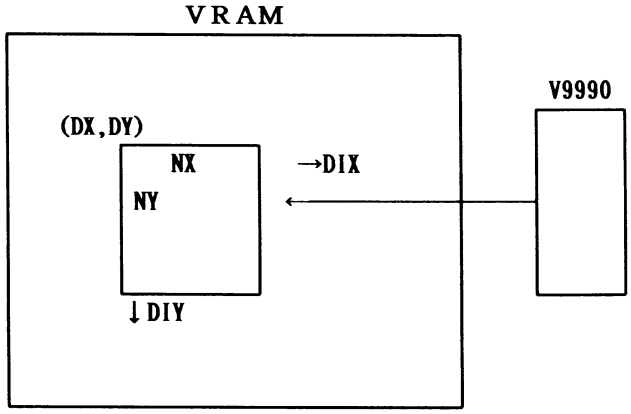
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#52	0	0	0	1	0	0	0	0	OP-CODE

After this, the data for necessary number of bytes is output at the command data port(P#2).

11.5.2 LMMV (Logical Move to Memory from VDP)

The VRAM rectangle area is painted out by using the color code.

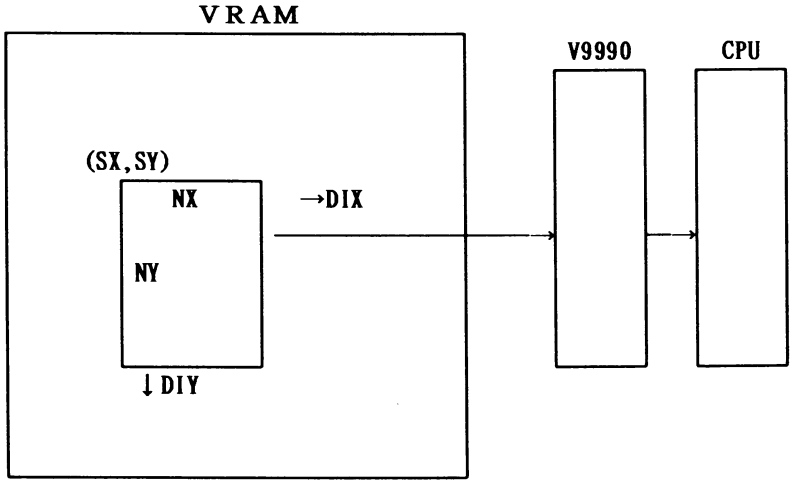


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#52	0	0	1	0	0	0	0	0	OP-CODE

11.5.3 LMCM (Logical Move to CPU from Memory)

The data of the rectangle area in VRAM is transferred to CPU.



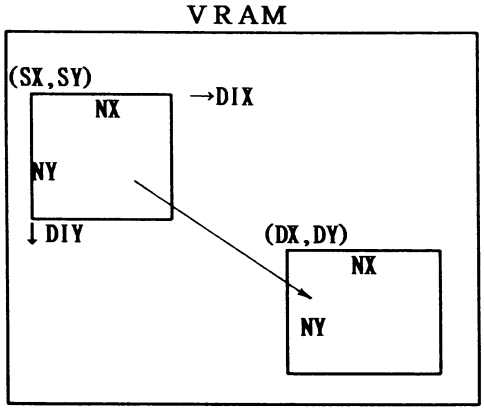
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	SX L
R#33	0	0	0	0	0	SX10	SX9	SX8	SX H
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	SY L
R#35	0	0	0	0	SY11	SY10	SY9	SY8	SY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#52	0	0	1	1	0	0	0	0	OP-CODE

After this, the data for necessary number of bytes is inputted through the command data port (P#2).

11.5.4 LMMM (Logical Move to Memory from Memory)

The rectangle area data is transferred from VRAM to VRAM.

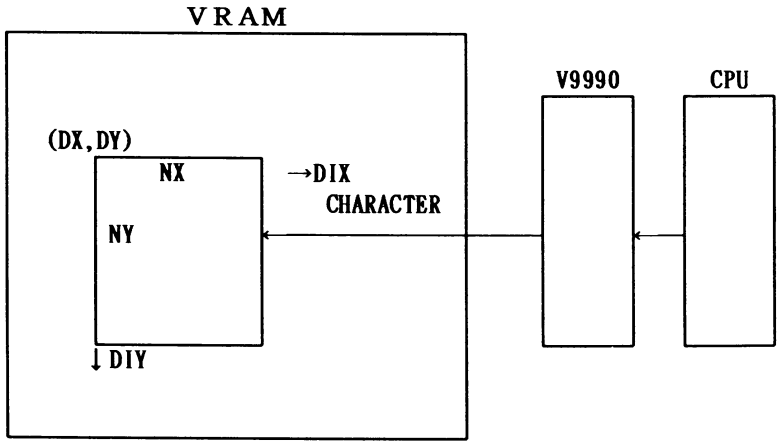


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	SX L
R#33	0	0	0	0	0	SX10	SX9	SX8	SX H
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	SY L
R#35	0	0	0	0	SY11	SY10	SY9	SY8	SY H
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#52	0	1	0	0	0	0	0	0	OP-CODE

11.5.5 CMMC (Character Move to Memory from CPU)

The data for each character is transferred from CPU to the rectangle area in VRAM.



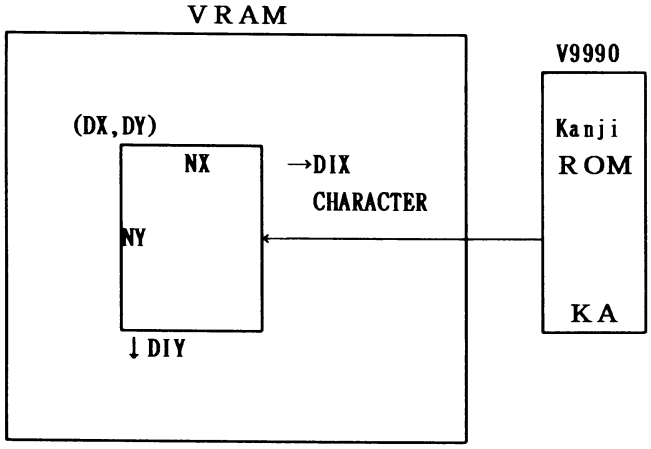
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#50	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	BC L
R#51	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC H
R#52	0	1	0	1	0	0	0	0	OP-CODE

After this, the data for necessary number of bytes is output at the command data port (P#2).

11.5.6 CMMK (Character Move to Memory from Kanji)

The data for each character is transferred from the kanji ROM to the rectangle area in VRAM.

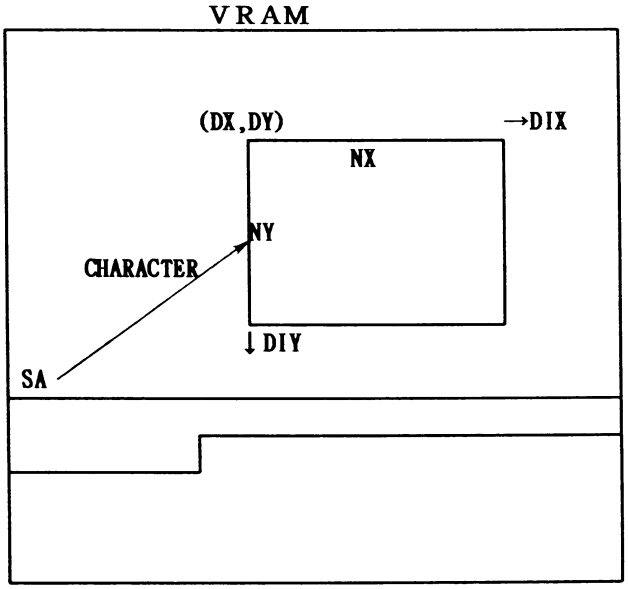


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	KA7	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KA L
R#34	KA15	KA14	KA13	KA12	KA11	KA10	KA9	KA8	KA M
R#35	0	0	0	0	0	0	KA17	KA16	KA H
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#50	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	BC L
R#51	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC H
R#52	0	1	1	0	0	0	0	0	OP-CODE

11.5.7 CMMM (Character Move to Memory from Memory)

The rectangle area data for each character is transferred from VRAM to VRAM.

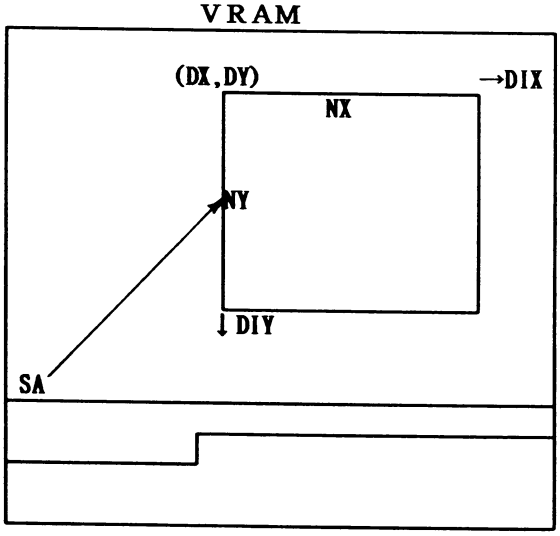


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	SA L
R#34	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA M
R#35	0	0	0	0	0	SA18	SA17	SA16	SA H
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#50	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	BC L
R#51	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC H
R#52	0	1	1	1	0	0	0	0	OP-CODE

11.5.8 BMXL (Byte Move to XY from Linear)

The data on the linear address in VRAM is transferred to the rectangle area.

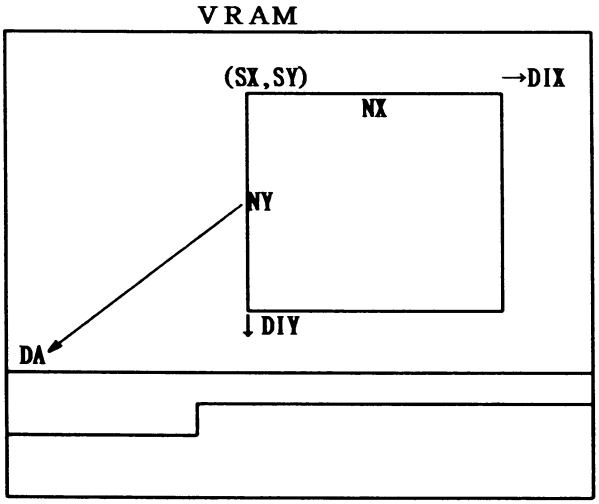


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	SA L
R#34	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA M
R#35	0	0	0	0	0	SA18	SA17	SA16	SA H
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#52	1	0	0	0	0	0	0	0	OP-CODE

11.5.9 BMLX (Byte Move to Linear from XY)

The data of the rectangle area in VRAM is transferred onto the linear address.

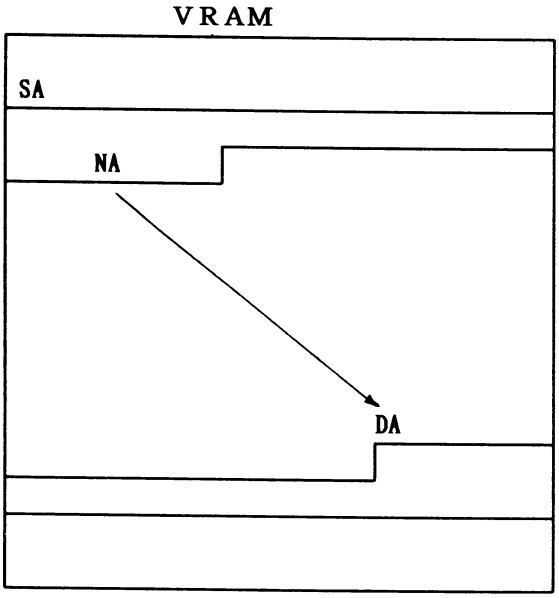


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	SX L
R#33	0	0	0	0	0	SX10	SX9	SX8	SX H
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	SY L
R#35	0	0	0	0	SY11	SY10	SY9	SY8	SY H
R#36	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DA L
R#38	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA M
R#39	0	0	0	0	0	DA18	DA17	DA16	DA H
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0	NX L
R#41	0	0	0	0	0	NX10	NX9	NX8	NX H
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0	NY L
R#43	0	0	0	0	NY11	NY10	NY9	NY8	NY H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#52	1	0	0	1	0	0	0	0	OP-CODE

11.5.10 BMLL (Byte Move to Linear from Linear)

The data on the linear address in VRAM is transferred onto the linear address.



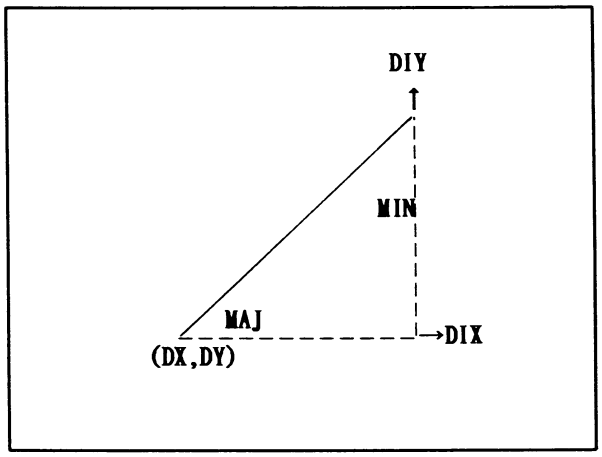
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	SA L
R#34	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA M
R#35	0	0	0	0	0	SA18	SA17	SA16	SA H
R#36	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DA L
R#38	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA M
R#39	0	0	0	0	0	DA18	DA17	DA16	DA H
R#40	NA7	NA6	NA5	NA4	NA3	NA2	NA1	NA0	NA L
R#42	NA15	NA14	NA13	NA12	NA11	NA10	NA9	NA8	NA M
R#43	0	0	0	0	0	NA18	NA17	NA16	NA H
R#44	0	0	0	0	DIY	DIX	0	0	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#52	1	0	1	0	0	0	0	0	OP-CODE

11.5.11 LINE

A straight line is drawn from the reference point on VRAM.

VRAM

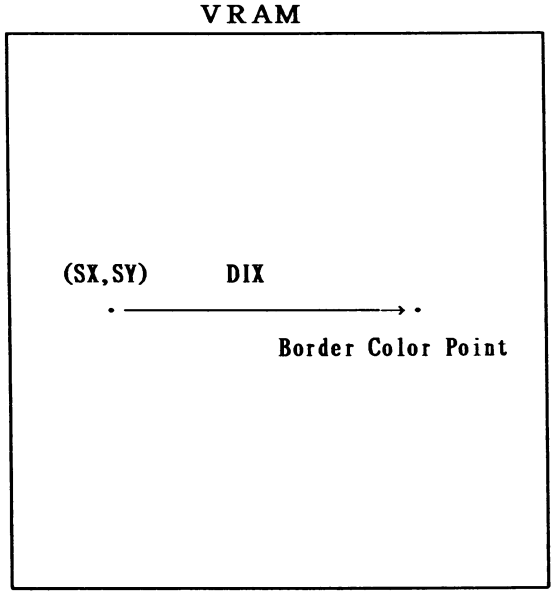


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#40	MJ7	MJ6	MJ5	MJ4	MJ3	MJ2	MJ1	MJ0	MJ L
R#41	0	0	0	0	MJ11	MJ10	MJ9	MJ8	MJ H
R#42	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0	MI L
R#43	0	0	0	0	MI11	MI10	MI9	MI8	MI H
R#44	0	0	0	0	DIY	DIX	0	MAJ	ARG
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#52	1	0	1	1	0	0	0	0	OP-CODE

11.5.12 SRCH

A border color (or non-border color) is searched for toward the right (or left) of the base point on VRAM.

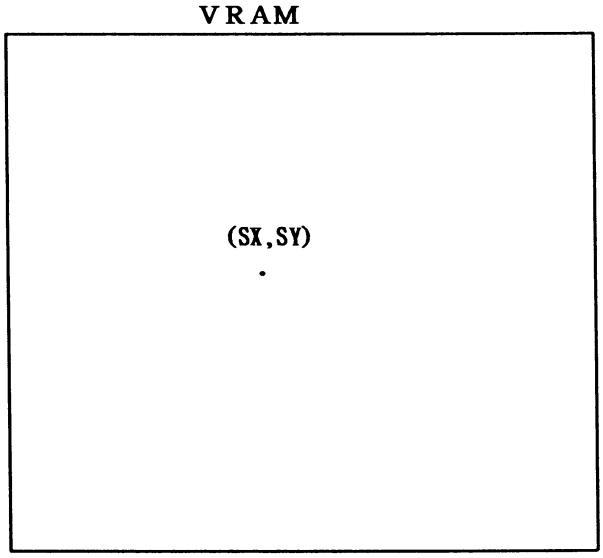


Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	SX L
R#33	0	0	0	0	0	SX10	SX9	SX8	SX H
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	SY L
R#35	0	0	0	0	SY11	SY10	SY9	SY8	SY H
R#44	0	0	0	0	0	DIX	NEQ	0	ARG
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#52	1	1	0	0	0	0	0	0	OP-CODE
R#53	BX7	BX6	BX5	BX4	BX3	BX2	BX1	BX0	BX L
R#54	0	0	0	0	0	BX10	BX9	BX8	BX H

11.5.13 POINT

The color code at the base point on VRAM is read out.



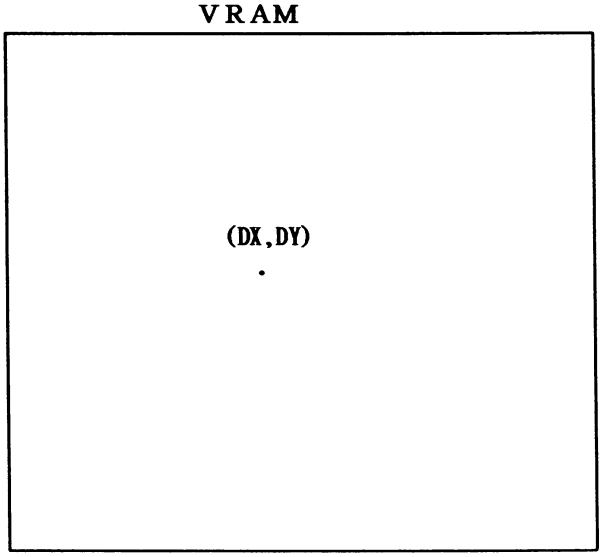
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	SX L
R#33	0	0	0	0	0	SX10	SX9	SX8	SX H
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	SY L
R#35	0	0	0	0	SY11	SY10	SY9	SY8	SY H
R#52	1	1	0	1	0	0	0	0	OP-CODE

The (SX, SY) color code is inputted through the command data port (P#2).

11.5.14 PSET

A point is drawn on VRAM. After that, the pointer can be advanced.



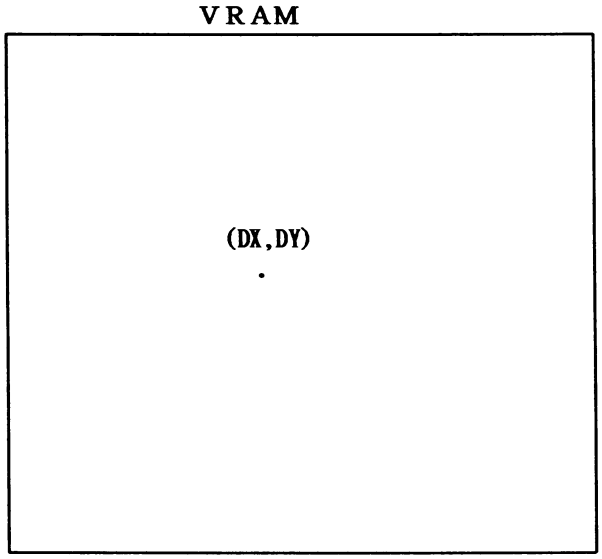
Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#45	0	0	0	TP	L11	L10	L01	L00	LOP
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	WM L
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM H
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	FC L
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC H
R#52	1	1	1	0	AYM	AYE	AXM	AXE	OP-CODE

DX, DY should not be set when drawing in the current pointer.

11.5.15 ADVANCE

This is the same as PSET except that bit 4 of OP-CODE is "1". Only the pointer is moved without performing PSET.



Register set-up

	b7	b6	b5	b4	b3	b2	b1	b0	
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	DX L
R#37	0	0	0	0	0	DX10	DX9	DX8	DX H
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	DY L
R#39	0	0	0	0	DY11	DY10	DY9	DY8	DY H
R#52	1	1	1	1	AYM	AYE	AXM	AXE	OP-CODE

DX, DY should not be set when using the current pointer.

12 V9990 REGISTER SPECIFICATIONS

12.1 I/O PORT SPECIFICATIONS

P#0	VRAM DATA	(R/W)
P#1	PALETTE DATA	(R/W)
P#2	COMMAND DATA	(R/W)
P#3	REGISTER DATA	(R/W)
P#4	REGISTER SELECT	(W)
P#5	STATUS	(R)
P#6	INTERRUPT FLAG	(R/W)
P#7	SYSTEM CONTROL	(W)
P#8	Primary standard kanji ROM lower order address	(W)
P#9	Primary standard kanji ROM higher order address	(W)
P#9	Primary standard kanji ROM data	(R)
P#A	Secondary standard kanji ROM lower order address	(W)
P#B	Secondary standard kanji ROM higher order address	(W)
P#B	Secondary standard kanji ROM data	(R)
P#C～F	Reserve	

●VRAM DATA PORT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
P#0	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0

- The data written in this port is written in the VRAM address specified by using R#0 to 3. If writing to this port has taken place before completion of data write in VRAM, a WAIT signal is output.
- By reading through this port, the VRAM address data specified by using R#3 to 5 is obtained. If reading has taken place at this port before data preparation, a WAIT signal is output. When VRAM read address has been modified to prepare the VRAM address data at completion of data write to R#5, it must be written in R#5.

●PALETTE DATA PORT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
P#1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

- The data written in this port is written in the internal palette RAM.
- By reading through this port, the internal palette RAM data can be obtained. A WAIT signal is output till the data has been prepared.
- The palette RAM address is specified by using R#14.
- The data format is as follows.

	b7	b6	b5	b4	b3	b2	b1	b0
RED	$\overline{YS}$	—	—	R4	R3	R2	R1	R0
GREEN	—	—	—	G4	G3	G2	G1	G0
BLUE	—	—	—	B4	B3	B2	B1	B0

●COMMAND DATA PORT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
P#2	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

- The command data is read and written through this port. Access to this port when the status TR bit is "0" while the command is being executed will result in an output of WAIT signal.

●REGISTER DATA PORT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
P#3	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

- The data written in this port is written in the register specified by using P#4.
- By reading through this port, the register data specified by using P#4 can be obtained.

●REGISTER SELECT PORT (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#4	WII	RII	RA5	RA4	RA3	RA2	RA1	RA0

- Using RA5 to 0, the register No. to which access is made through P#3 is specified.
- The register No. undergoes a plus "1" increment through P#3 access. However, when WII is "1", increment in writing at P#3 is prohibited and when RII is "1", increment in reading at P#3 is prohibited.

●STATUS PORT (READ ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#5	TR	VR	HR	BD	0	MCS	EO	CE

- Various types of status data can be read out as follows.
  - TR : Command data transfer ready. It is reset through P#2 access.
  - VR : Vertical non-display period
  - HR : Horizontal non-display period
  - BD : Border color detect at completion of SRCH command (becomes "1" when detected)
  - EO : In the second field period during interlace
  - CE : Command being executed
  - MCS : Content of P#7 MCS

●INTERRUPT FLAG PORT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
P#6	0	0	0	0	0	CE	HI	VI

- The interrupt flags can be read out as follows.
  - CE : Command completion flag
  - HI : Display position flag
  - VI : Vertical display period completion flag
- By writing "1" , the related bit flag is reset.

●SYSTEM CONTROL PORT (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#7	0	0	0	0	0	0	SRS	MCS

SRS : Writing "1" will set all ports except this one in "power ON reset" state. "0" should be written to cancel it.

MCS : The internally used master clock is selected.
- 1 : MCKIN terminal
- 0 : XTAL1 terminal

NOTE) XTAL1 terminal is selected when "power ON reset". If specification is not made properly when either XTAL1 or MCKIN terminal is used, specifications for external input clock timing will not be fulfilled and a chip will be damaged in the worst case. As a measure to prevent this, it is necessary to supply clock signals to both terminals. The above does not apply when both terminals are used.

●Primary standard kanji ROM ADDRESS PORT (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#8	—	—	K1A10	K1A9	K1A8	K1A7	K1A6	K1A5
P#9	—	—	K1A16	K1A15	K1A14	K1A13	K1A12	K1A11

- The font (16×16 bits) address for the primary standard kanji ROM which is read through P#9 is specified.
- It is necessary to write in the order of P#9 and P#8 to prepare data for the kanji ROM address at completion of writing to P#8.

●Primary standard kanji ROM DATA PORT (READ ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#9	K1D7	K1D6	K1D5	K1D4	K1D3	K1D2	K1D1	K1D0

- It is possible to read the data of the font address specified by using P#8 and P#9 of the primary standard kanji ROM. A WAIT signal is output till the data has been prepared.
- By reading 32 times continuously, it is possible to obtain 32 bytes data in the order of the upper left, upper right, lower left and lower right blocks (of 8 bytes each) of the 16×16 bits font.

●Secondary standard kanji ROM ADDRESS PORT (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#A	—	—	K2A10	K2A9	K2A8	K2A7	K2A6	K2A5
P#B	—	—	K2A16	K2A15	K2A14	K2A13	K2A12	K2A11

- The font (16×16 bits) address for the secondary standard kanji ROM which is read through P#B is specified.
- It is necessary to write in the order of P#B and P#A to prepare data for the kanji ROM address at completion of writing to P#A.

●Secondary standard kanji ROM DATA PORT (READ ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
P#B	K2D7	K2D6	K2D5	K2D4	K2D3	K2D2	K2D1	K2D0

- It is possible to read the data of the font address specified by using P#A and P#B of the secondary standard kanji ROM. A WAIT signal is output till the data has been prepared.
- By reading 32 times continuously, it is possible to obtain 32 bytes data in the order of the upper left, upper right, lower left and lower right blocks (of 8 bytes each) of the 16×16 bits font.

Correspondence with terminals KA17 to 0

・When reading P#9

Terminal name	KA8	KA7	KA6	KA5	KA4	KA3	KA2	KA1	KA0
	K1A8	K1A7	K1A6	K1A5	*	*	*	*	*

KA17	KA16	KA15	KA14	KA13	KA12	KA11	KA10	KA9
0	K1A16	K1A15	K1A14	K1A13	K1A12	K1A11	K1A10	K1A9

・When reading P#B

Terminal name	KA8	KA7	KA6	KA5	KA4	KA3	KA2	KA1	KA0
	K2A8	K2A7	K2A6	K2A5	*	*	*	*	*

KA17	KA16	KA15	KA14	KA13	KA12	KA11	KA10	KA9
1	K2A16	K2A15	K2A14	K2A13	K2A12	K2A11	K2A10	K2A9

・((MSB) KA4, 0, 3, 2, 1 (LSB)) are reset(0,0,0,0,0) by writing to P#8 to B and undergo a plus "1" increment by reading P#9 or P#B.

・KA17 is reset to "0" by writing to P#9 and set to "1" by writing to P#B.

Connect so that a pattern configuration as shown below is obtained.

				KA0=0	KA0=1
KA4	KA3	KA2	KA1	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0
0	0	0	0	Upper left	Upper right
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Lower left	Lower right
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

12.2 Register specifications

R#0～2	VRAM WRITE ADDRESS	(W)
R#3～5	VRAM READ ADDRESS	(W)
R#6、7	SCREEN MODE	(R/W)
R#8	CONTROL	(R/W)
R#9～12	INTERRUPT	(R/W)
R#13	PALETTE CONTROL	(W)
R#14	PALETTE POINTER	(W)
R#15	BACK DROP COLOR	(R/W)
R#16	DISPLAY ADJUST	(R/W)
R#17～24	SCROLL CONTROL	(R/W)
R#25	SPRITE PATTERN GENERATOR BASE ADDRESS	(R/W)
R#26	LCD CONTROL	(R/W)
R#27	PRIORITY CONTROL	(R/W)
R#28	SPRITE PALETTE CONTROL	(W)
R#32～52	COMMAND	(W)
R#53、54	COMMAND	(R)

●VRAM WRITE ADDRESS (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#0	CVWA7	CVWA6	CVWA5	CVWA4	CVWA3	CVWA2	CVWA1	CVWA0
R#1	CVWA15	CVWA14	CVWA13	CVWA12	CVWA11	CVWA10	CVWA9	CVWA8
R#2	CVWAIH	0	0	0	0	CVWA18	CVWA17	CVWA16

- CVWA0～18 : VRAM write address
- CVWAIH =0 : CVWA undergoes an increment of plus "1" only at the end of writing to P#0.
  =1 : No increment.

●VRAM READ ADDRESS (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#3	CVRA7	CVRA6	CVRA5	CVRA4	CVRA3	CVRA2	CVRA1	CVRA0
R#4	CVRA15	CVRA14	CVRA13	CVRA12	CVRA11	CVRA10	CVRA9	CVRA8
R#5	CVRAIH	0	0	0	0	CVRA18	CVRA17	CVRA16

- CVRA0～18 : VRAM read address
- CVRAIH =0 : CVRA undergoes an increment of plus "1" only at the end of reading at P#0.
  =1 : No increment.

●SCREEN MODE (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#6	DSPM1	DSPM0	DCKM1	DCKM0	XIMM1	XIMM0	CLRM1	CLRM0
R#7	0	C25M	SM1	SM	PAL	EO	IL	HSCN

- DSPM1 DSPM0 Display mode selection

1	1 : Stand-by mode (non-display, no VRAM refresh, kanji ROM readable)
1	0 : Bit map mode (B1～6)
0	1 : P2 mode
0	0 : P1 mode

- DCKM1 DCKM0 Dot clock selection (used in combination with MCS of P#7)

		MCS=0	MCS=1	
1	0 :	XTAL1	MCKIN	
0	1 :	XTAL1/2	MCKIN/2	
0	0 :	XTAL1/4	—	(Number of division of master clock)

- XIMM1 XIMM0 Selection of number of dots in X direction of image space

1	1 :	2048 dots
1	0 :	1024 dots
0	1 :	512 dots
0	0 :	256 dots

CLRM1	CLRM0	Selection of bit number per dot
1	1	: 16 bits/dot
1	0	: 8 bits/dot
0	1	: 4 bits/dot
0	0	: 2 bits/dot

- C25M
  - 1 : B6 mode
  - 0 : P1, P2, B1～5 mode

- SM1
  - 1 : 263 lines (In combination with SM, the sub-carrier phase is inverted for each frame.)
  - 0 : 262 lines

- SM
  - 1 : 1H=fsc/227.5 (the sub-carrier phase is inverted for each line.)
  - 0 : 1H=fsc/228

- PAL
  - 1 : Vertical frequency becomes PAL specification.
  - 0 : Vertical frequency becomes NTSC specification.

- EO
  - 1 : Twice the vertical resolution during interlace (invalid when in B5 and B6 modes)
  - 0 : Same as during Non- interlace

- IL
  - 1 : Interlace
  - 0 : Non-interlace

- HSCN
  - 1 : B5, B6 modes
  - 0 : P1, P2, B1～4 modes

●CONTROL (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#8	DISP	SPD	YSE	VWTE	VWM	DMAE	VSL1	VSL0

- DISP
  - 1 : Display appears on screen according to the VRAM content.
  - 0 : Back drop color is displayed all over the screen.

- SPD
  - 1 : Sprite (cursor) is not displayed.
  - 0 : Sprite (cursor) is displayed.

- YSE — $\overline{YS}$ signal output enable
  - 1 : $\overline{YS}$ signal is output.
  - 0 : $\overline{YS}$ signal is not output. ($\overline{YS}$ terminal constantly remains as low level.)

- VWTE — VRAM serial data bus input/output control during digitization
  - 1 : Dummy write transfer is executed during horizontal retrace line interval. (The serial data bus of VRAM becomes an input terminal.)
  - 0 : Read transfer is executed during horizontal retrace line interval. (The serial data bus of VRAM becomes an output terminal.)

- VWM — VRAM write control during digitization
  - 1 : Write transfer is executed during horizontal retrace line interval. (The data inputted into the serial data bus of VRAM during display period undergoes write transfer.)
  - 0 : Write transfer is not executed.

- DMAE — $\overline{DREQ}$ signal output enable
  - 1 : The signal is synchronized to the status TR while command is executed and output at $\overline{DREQ}$ terminal.
  - 0 : $\overline{DREQ}$ terminal remains as high level.

- VSL1 VSL0 — Selection of video memory configuration
  - 1 0 : 256k word × 4 bit VRAM, 4 units (512k byte)
  - 0 1 : 128k word × 8 bit VRAM, 2 units (256k byte)
  - 0 0 : 64k word × 4 bit VRAM, 4 units (128k byte)

●INTERRUPT (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#9	0	0	0	0	0	IECE	IEH	IEV
R#10	IL7	IL6	IL5	IL4	IL3	IL2	IL1	IL0
R#11	IEHM	0	0	0	0	0	IL9	IL8
R#12	0	0	0	0	IX3	IX2	IX1	IX0

- IECE — Command end interrupt enable control
  - 1 : $\overline{INT0}$ terminal becomes low level when CE flag of P#6 is "1".
  - 0 : $\overline{INT0}$ terminal does not change according to CE flag.

- IEV — Interrupt enable during vertical retrace line interval.
  - 1 : $\overline{INT0}$ terminal becomes low level when VI flag of P#6 is "1".
  - 0 : $\overline{INT0}$ terminal does ot change according to VI flag.

- IEH — Display position interrupt enable (Interrupt position is specified with IL0-9, IX0-3 and IEHM.)
  - 1 : $\overline{INT1}$ terminal becomes low level when HI flag of P#6 is "1".
  - 0 : $\overline{INT1}$ terminal does not change according to HI flag.

- ILO-9 : Specification of vertical position where display position interrupt occurs (Specified by means of line No. with the display start line as "0".)

- IXO-3 : Specification of horizontal position where display position interrupt occurs (Specified by unit of 64 master clock with the display start position as "0")

- IEHM Seletion of vertical position for display position interrupt
  - 1 : Every line (ILO-9 are ignored.)
  - 0 : Specified line

●PALETTE CONTROL (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#13	PLTM1	PLTM0	YAE	PLTAIH	PLTO5	PLTO4	PLTO3	PLTO2

- PLTM1 PLTM0 Selection of color palette mode
  - 1 1 : YUV mode
  - 1 0 : YJK mode
  - 0 1 : 256 color mode
  - 0 0 : Palette mode

NOTE) For the details,refer to item [17] DISPLAY FUNCTION FOR YUV,YJK FORM DATA.

- YAE Selection of YJK (YUV) and RGB mixing mode (valid when in YUV and YJK modes)
  - 1 : YJK (YUV) and RGB images are displayed together.
  - 0 : Only YJK (YUV) image is displayed.

- PLTAIH Palette No. increment control at color palette read-out
  - 1 : R#14 palette pointer is not changed by P#1 read-out.
  - 0 : After P#1 read-out, R#14 palette pointer undergoes an increment.

- PLTO5-2 : Still screen palette No. offset

●PALETTE POINTER (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#14	PLTA5	PLTA4	PLTA3	PLTA2	PLTA1	PLTA0	PLTP1	PLTP0

- PLTA5-0 : Palette No.(color code)

- PLTP1 PLTP0 Specification of RGB
  - 1 0 : BLUE
  - 0 1 : GREEN
  - 0 0 : RED

After completion of access to P#1, an increment takes place by plus 1 only. PLTP1 and 0 are used as a 0 to 2 ternary counter.

●BACK DROP COLOR (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#15	0	0	BDC5	BDC4	BDC3	BDC2	BDC1	BDC0

・BDC5-0 : Palette No. of back drop color

●DISPLAY ADJUST (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#16	ADJV3	ADJV2	ADJV1	ADJV0	ADJH3	ADJH2	ADJH1	ADJH0

・ADJV3-0 : Vertical display position adjustment (by line)

8	9・・・15	0	1・・・6	7
Down		Standard		Up

・ADJH3-0 : Horizontal display position adjustment

8	9・・・15	0	1・・・6	7
Right		Standard		Left

(P1 and B1 by 1 dot unit, P2, B2 and B3 by 2-dot unit, B4, B5 and B6 by 4-dot unit)

●SCROLL CONTROL (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#17	SCAY7	SCAY6	SCAY5	SCAY4	SCAY3	SCAY2	SCAY1	SCAY0
R#18	R512	R256	0	SCAY12	SCAY11	SCAY10	SCAY9	SCAY8
R#19	0	0	0	0	0	SCAX2	SCAX1	SCAX0
R#20	SCAX10	SCAX9	SCAX8	SCAX7	SCAX6	SCAX5	SCAX4	SCAX3
R#21	SCBY7	SCBY6	SCBY5	SCBY4	SCBY3	SCBY2	SCBY1	SCBY0
R#22	0	0	0	0	0	0	0	SCBY8
R#23	0	0	0	0	0	SCBX2	SCBX1	SCBX0
R#24	0	0	SCBX8	SCBX7	SCBX6	SCBX5	SCBX4	SCBX3

・SCAY12-0
SCAX10-0 : As display start co-ordinates for screen "A" of P1 mode and screens of other modes, X-Y co-ordinates in the image space are specified by dots. (When 16 bit/dot is used in B2 and B3 modes, however, SCAX0 is ignored and X co-ordinate is specified by 2-dot unit.)

・SCBY8-0
SCBX8-0 : For screen "B" of p1, X-Y co-ordinates are specified in the same way as for screen "A".

・R512 R256 Number of roll page line in Y direction is specified.

R512	R256	
1	0	: Displayed page is rolled by 512 lines.
0	1	: Displayed page is rolled by 256 lines.
0	0	: Rolling by image space size takes place.

●SPRITE PATTERN GENERATOR TABLE BASE ADDRESS (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0	
R#25	0	0	0	0	SGBA17	SGBA16	SGBA15	0	P1 mode
R#25	0	0	0	0	SGBA18	SGBA17	SGBA16	SGBA15	P2 mode

・SGBA18-15 : Base address of P1, P2 mode sprite pattern generator

●LCD CONTROL (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#26	0	0	0	VRI	PNSL	PLVO	PDUAL	PNEN

・VRI Selection of number of lines during vertical retrace line interval when in panel mode
- 1 : 1 line (Frame frequency increases.)
- 0 : Same as CRT mode

・PNSL Selection of number of vertical direction dot in panel
- 1 : 480 dots
- 0 : 400 dots

・PLVO Selection of Gray Scaling
- 1 : Display data is output at color codes to terminals of CB7 to 0.
- 0 : Binary converted data is output to terminals of D3 to 0.

・PDUAL Selection of panel type
- 1 : 2 screen panel (single drive type)
- 0 : 1 screen panel

・PNEN Selection of panel display mode
- 1 : Display cycle and terminal function used for panel
- 0 : Display cycle and terminal function used for CRT

●PRIORITY CONTROL (READ/WRITE)

	b7	b6	b5	b4	b3	b2	b1	b0
R#27	0	0	0	0	PRY1	PRY0	PRX1	PRX0

・PRY1,0 : When in P1 mode, the display Y co-ordinate to exchange display priority order between screens "A" and "B" is specified. A unit of 64 lines is used and in the range lower than the specified line (including that line), screen "B" has a priority. At "0", screen "A" has a priority throughout the range.

・PRX1,0 : When in P1 mode, the display X co-ordinate to exchange display priority order between screens "A" and "B" is specified. A unit of 64 dots is used and in the range to the right of the specified dot (including that dot), screen "B" has a priority. At "0", screen "A" has a priority throughout the range.

●SPRITE PALETTE CONTROL (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#28	0	0	0	0	CSPO5	CSPO4	CSPO3	CSPO2

・CSPO5-2 : Palette No. offset of sprite (cursor)

●COMMAND PARAMETER (WRITE ONLY, READ ONLY)

For the details, refer to Chapter 11 COMMAND.

· SOURCE XY-COORDINATE/LINEAR ADDRESS/KANJI-ROM ADDRESS (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#32	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	KA7	KA6	KA5	KA4	KA3	KA2	KA1	KA0
R#33	0	0	0	0	0	SX10	SX9	SX8
R#34	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
	KA15	KA14	KA13	KA12	KA11	KA10	KA9	KA8
R#35	0	0	0	0	SY11	SY10	SY9	SY8
	0	0	0	0	0	SA18	SA17	SA16
	0	0	0	0	0	0	KA17	KA16

· DESTINATION XY-COORDINATE/LINEAR ADDRESS (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#36	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0
	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R#37	0	0	0	0	0	DX10	DX9	DX8
R#38	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0
	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
R#39	0	0	0	0	DY11	DY10	DY9	DY8
	0	0	0	0	0	DA18	DA17	DA16

· TRANSFER DOT NUMBER XY/LINEAR/LINE MINER, MAJOR (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#40	NX7	NX6	NX5	NX4	NX3	NX2	NX1	NX0
	NA7	NA6	NA5	NA4	NA3	NA2	NA1	NA0
	MJ7	MJ6	MJ5	MJ4	MJ3	MJ2	MJ1	MJ0
R#41	0	0	0	0	0	NX10	NX9	NX8
	0	0	0	0	MJ11	MJ10	MJ9	MJ8
R#42	NY7	NY6	NY5	NY4	NY3	NY2	NY1	NY0
	NA15	NA14	NA13	NA12	NA11	NA10	NA9	NA8
	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
R#43	0	0	0	0	NY11	NY10	NY9	NY8
	0	0	0	0	0	NA18	NA17	NA16
	0	0	0	0	MI11	MI10	MI9	MI8

· ARGUMENT (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#44	0	0	0	0	DIY	DIX	NEQ	MAJ

· LOGICAL OPERATION (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#45	0	0	0	TP	L11	L10	L01	L00

· WRITE MASK (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#46	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
R#47	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8

· FONT COLOR (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#48	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
R#49	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8
R#50	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
R#51	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

· OPERATION CODE (WRITE ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#52	OP3	OP2	OP1	OP0	AYM	AYE	AXM	AXE

· BORDER X-COORDINATE (READ ONLY)

	b7	b6	b5	b4	b3	b2	b1	b0
R#53	BX7	BX6	BX5	BX4	BX3	BX2	BX1	BX0
R#54	0	0	0	0	0	BX10	BX9	BX8

13 ELECTRICAL CHARACTERISTICS

13.1 Absolute maximum ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.5 ~ +7.0	V
Input terminal voltage	V_I	-0.5 ~ V_{DD}+0.5	V
Output terminal voltage	V_O	-0.5 ~ V_{DD}+0.5	V
Storage temperature	Tstg	-65 ~ +150	℃

13.2 Recommended operating conditions

Symbol	Item	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{SS}	Supply voltage		0		V
V_{IL1}	Low level input voltage (Group 1)	-0.3		1.5	V
V_{IH1}	High level input voltage (Group 1)	3.5		V_{DD}	V
V_{IL2}	Low level input voltage (Group 2)	-0.3		0.8	V
V_{IH2}	High level input voltage (Group 2)	2.2		V_{DD}	V
T_{OP}	Operating temperature	0		70	℃

Group1 : XTAL1, MCKIN
Group2 : Input terminals other than group 1

13.3 Electrical characteristics under recommended operating conditions

13.3.1 DC characteristics

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	I_{OL}=1.6mA			0.4	V
V_{OH}	High level output voltage (except OPEN DRAIN terminal)	I_{OH}=-0.1mA	2.7			V
I_{LI}	Input leak current				10	μA
I_{LO}	Output leak current				25	μA
I_{DD}	Power consumption			100	140	mA

13.3.2 Terminal capacitance

Symbol	Item	Min.	Typ.	Max.	Unit
C_I	Input terminal capacity			8	pF
C_O	Output terminal capacity			10	
C_{IO}	Input/output terminal capacity			12	

13.3.3 External input clock timing

No.	Symbol	Item	Min.	Typ.	Max.	Unit
1	fXTAL	XTAL clock frequency	19.33	21.48	25.18	MHz
2	twhX	XTAL pulse width, high	6			ns
3	twlX	XTAL pulse width, low	6			
4	trCI	Input clock rise time			10	
5	tfCI	Input clock fall time			10	
6	fMCKIN	MCKIN clock frequency	12.88	14.32	15.75	MHz
7	twhM	MCKIN pulse width, high	15			ns
8	twlM	MCKIN pulse width, low	15			
9	twRST	RESET input pulse width	10			μs

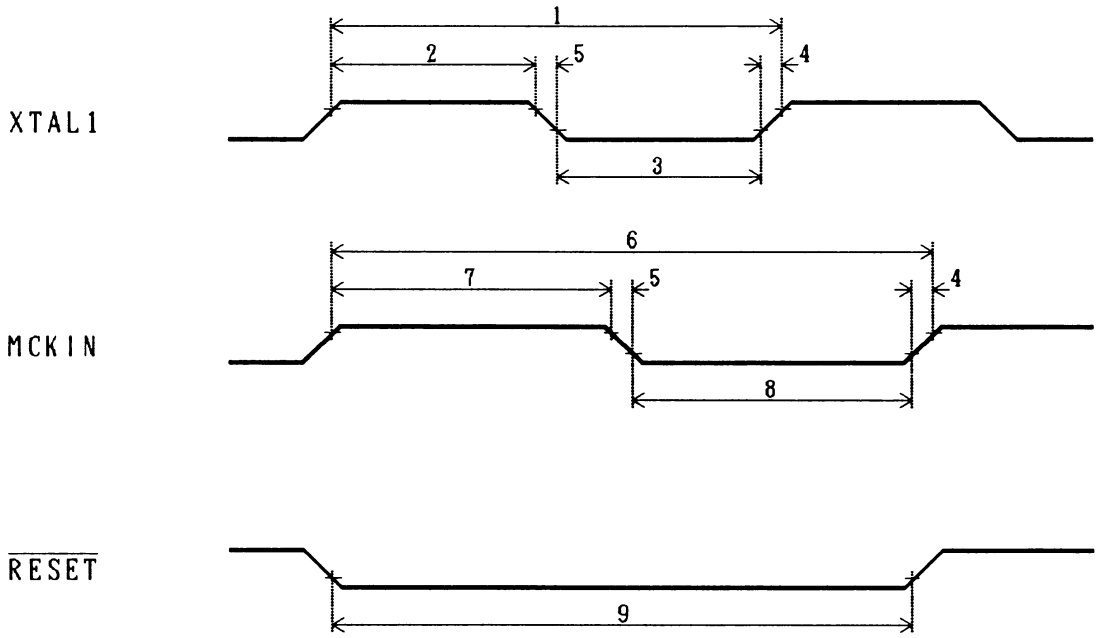
Note) For the following timing values, the clock cycle inputted in XTAL1 or MCKIN terminal is used as TC (nsec).

MCS(P#7 b0)=0 : TC=46.56ns when XTAL1 is 21.477MHz
=0 : TC=39.72ns when XTAL1 is 25.175MHz
=1 : TC=69.84ns when MCKIN is 14.318MHz

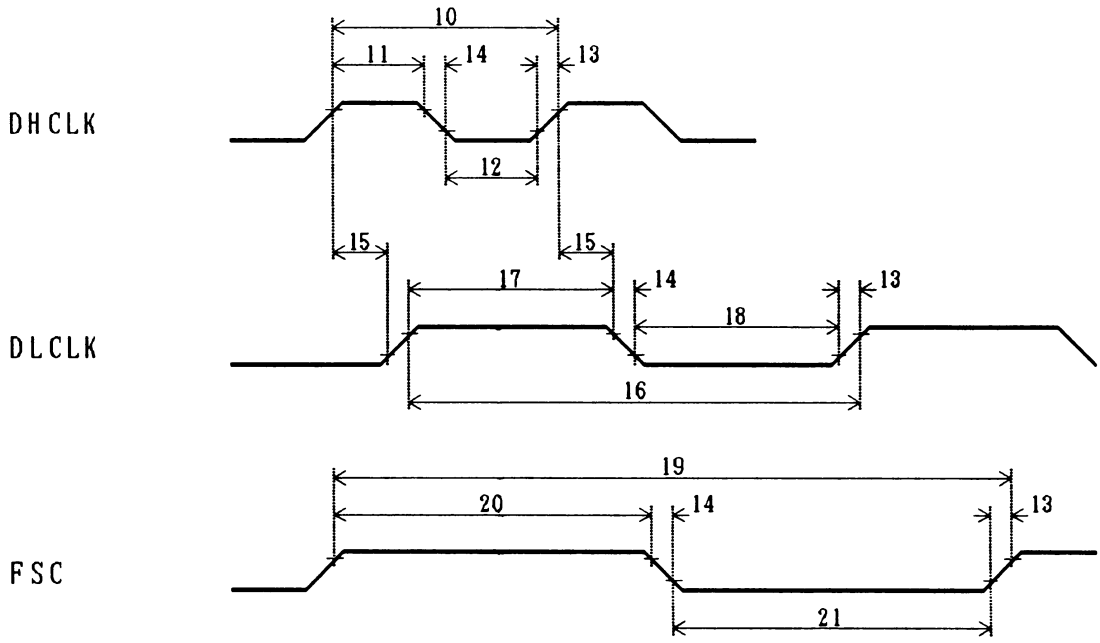
13.3.4 External output clock timing

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
10	fDHCLK	DHCLK clock cycle	CL=50PF		2TC		ns
11	twhDH	DHCLK pulse width, high		TC-15			
12	twlDH	DHCLK pulse width, low		TC-15			
13	trCO	Output clock rise time				10	
14	tfCO	Output clock fall time				10	
15	tdHL	DHCLK-DLCLK delay time		0		15	
16	fDLCLK	DLCLK clock cycle			4TC		
17	twhDL	DLCLK pulse width, high		2TC-15			
18	twlDL	DLCLK pulse width, low		2TC-15			
19	fFSC	FSC clock frequency (1)			3.58		MHz
20	twhSC	FSC pulse width, high (1)		125			ns
21	twlSC	FSC pulse width, low (1)		125			

(1) Indicates the value when 21.48MHz is inputted to XTAL1 and 14.32MHz to MCKIN.



CLOCK INPUT TIMING



CLOCK OUTPUT TIMING

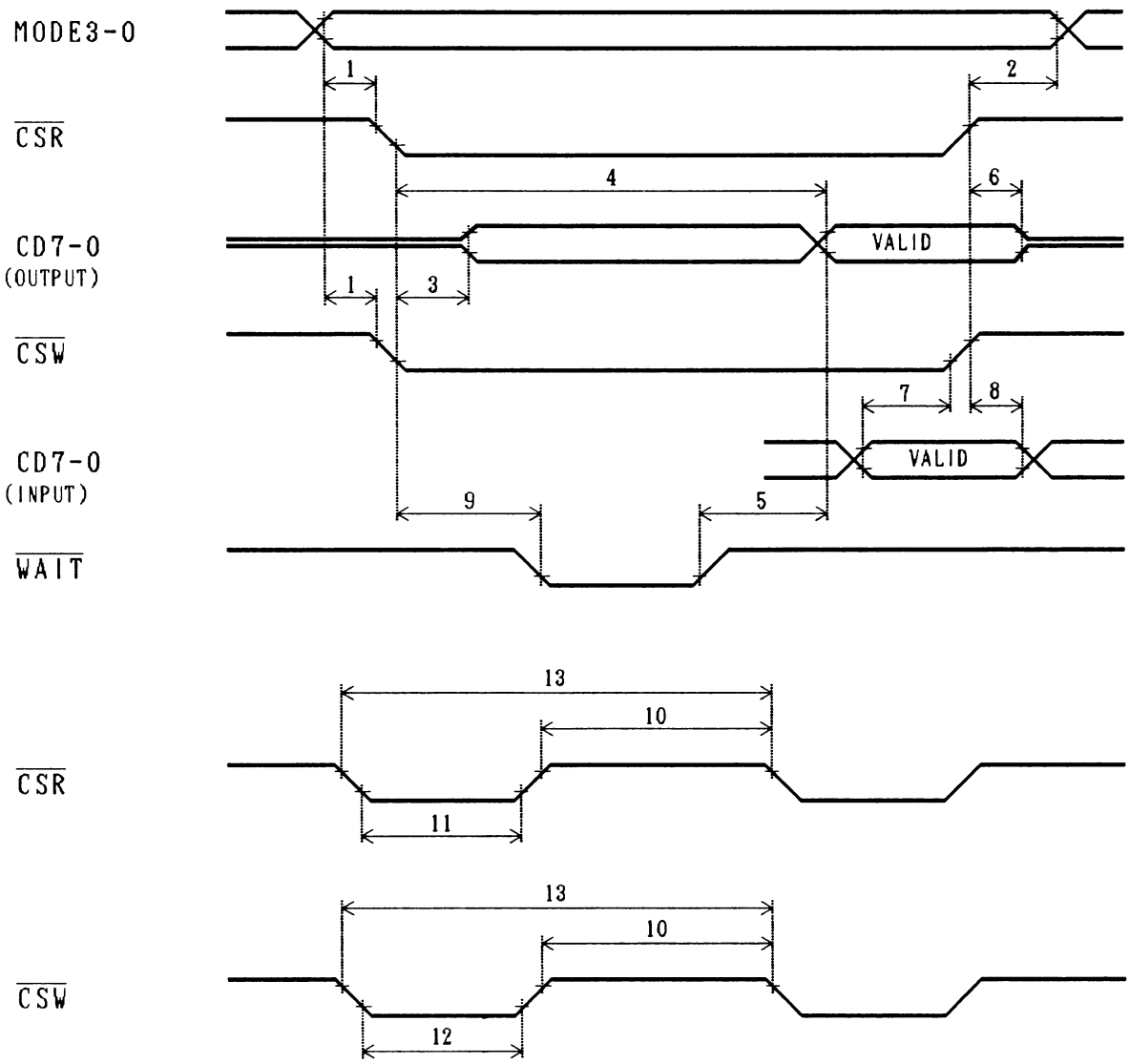
13.3.5 CPU-VDP interface

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	tsMODE	MODE set-up time	CL=150PF	30			ns
2	thMODE	MODE hold time		30			
3	tdxCD	Data active time		0			
4	tdaCSR	Data access time (from CSR) (1)		100			
5	tdaWT	Data access time (from WAIT)		0			
6	thRD	Read data hold time		0			
7	tsWD	Write data set-up time		30			
8	thWD	Write data hold time		30			
9	tdWCS	WAIT delay time (from CSR and CSW)				60	
10	twhCS	CSR, CSW pulse width, high (1)		5TC			
11	twlCSR	CSR pulse width, low		100			
12	twlCSW	CSW pulse width, low		30			
13	tcCS	CSR, CSW cycle time		8TC			

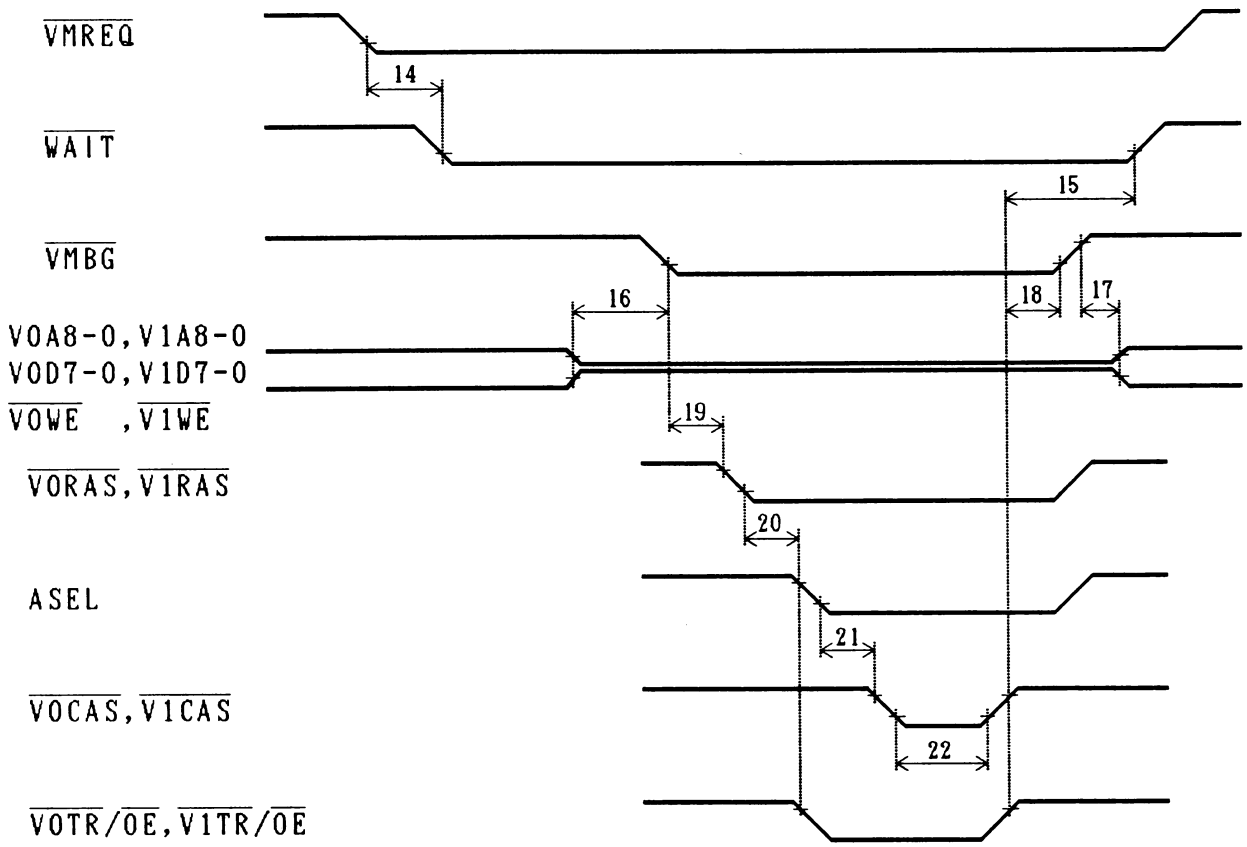
(1) Time required when reading at P#3 is (tdaCSR + twhCS) > (100ns + 8TC)

13.3.6 VRAM bus arbitration

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
14	tdWVMR	WAIT delay time (for VMREQ)	CL= 50PF			60	ns
15	thWAIT	WAIT hold time		-TC			
16	tdxB	Bus·high Z·VMBG delay time		0			
17	thxB	Bus·high Z hold time		0			
18	thVMBG	VMBG hold time		0			
19	tdRAS	VMBG·RAS delay time		2TC-5			
20	tdASEL	RAS·ASEL delay time		TC-20			
21	tdCAS	ASEL·CAS delay time		2TC-10			
22	twCAS	CAS pulse width		4TC-10			



CPU-VDP INTERFACE



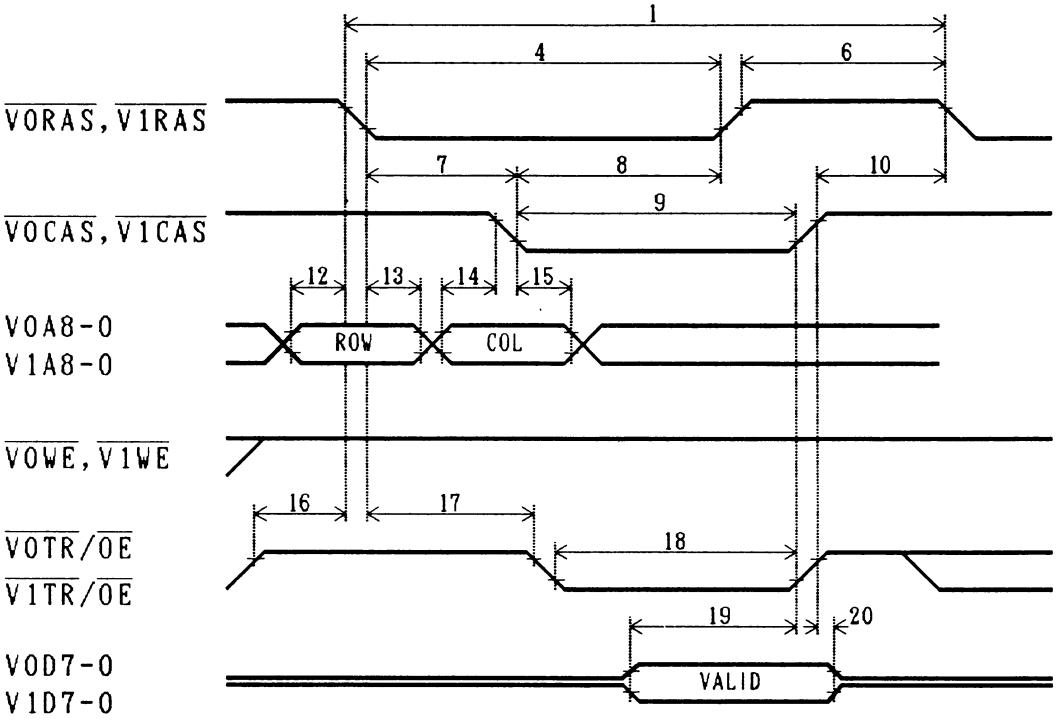
VRAM BUS ARBITRATION

13.3.7 VRAM interface

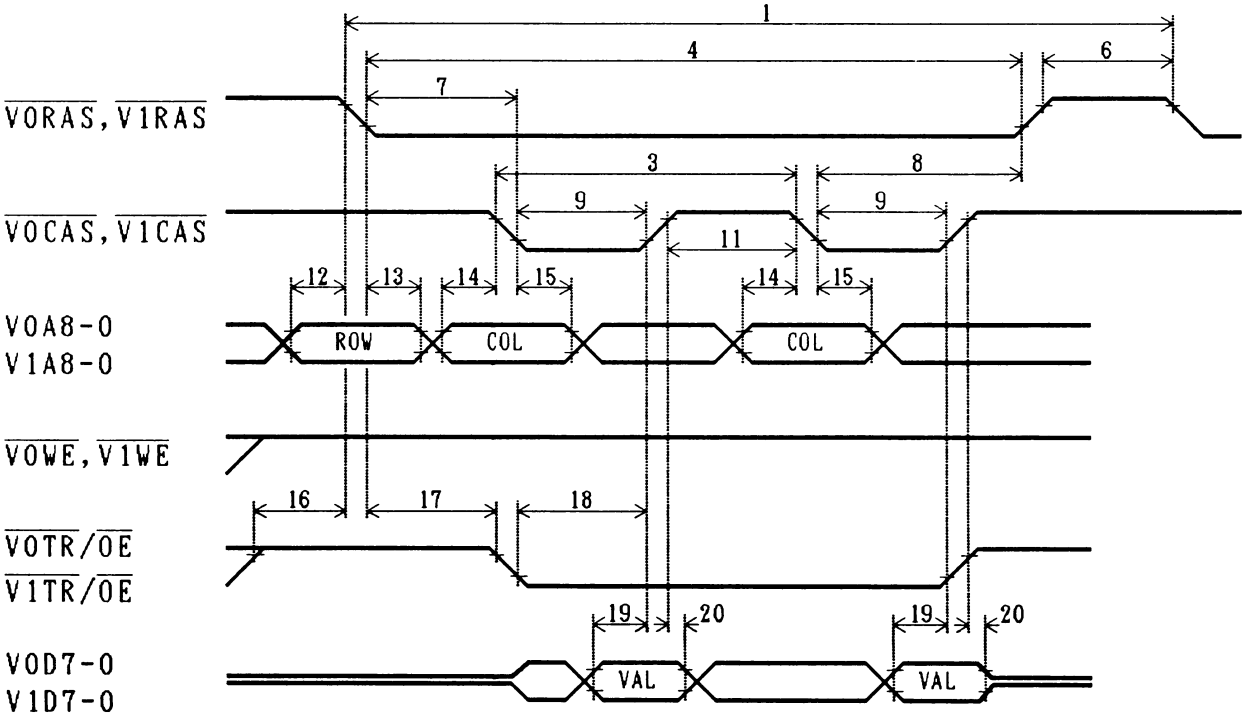
No.	Symbol	Item	Condition	Min.	Typ.	Unit
1	tRC	Random read·write cycle time		6TC		
2	tRWC	Read modify write cycle time		8TC		
3	tPC	Page mode cycle time		4TC		
4	tRAS	RAS pulse width		4TC-25	4TC-10	
5	tRWS	RAS pulse width (read modify write)		6TC-25	6TC-10	
6	tRP	RAS precharge time		2TC+5	2TC+10	
7	tRCD	RAS·CAS delay time		TC+20	TC+10	
8	tRSH	RAS hold time		3TC-40	3TC-20	
9	tCAS	CAS pulse width		2TC-10	2TC	
10	tCRP	CAS·RAS precharge time		2TC-25	2TC-10	
11	tCP	CAS precharge time		2TC-10	2TC	
12	tASR	Low address set-up time		TC	TC+10	
13	tRAH	Low address hold time		TC-25	TC-10	
14	tASC	Column address set-up time		0	10	
15	tCAH	Column address hold time		2TC-40	2TC-20	
16	tOES	OE·RAS set-up time		3TC-10	3TC	
17	tOEH	OE·RAS hold time		TC-10	TC	
18	tOE	OE pulse width		2TC-10	2TC	
19	tRDS	Random read data set-up time		20		
20	tRDH	Random read data hold time		0		
21	tODD	OE·data output delay time		TC-15	TC-5	
22	tDS	Data output set-up time		0	10	
23	tDH	Data output hold time	CL=50PF	2TC-40	2TC-20	ns
24	tWP	Write command pulse width		2TC-10	2TC	
25	tRWL	Write command·RAS read time		2TC-40	2TC-20	
26	tCWL	Write command·CAS read time		2TC-10	2TC	
27	tCWD	CAS·WE delay time		3TC-10	3TC	
28	tRPC	RAS precharge·CAS hold time		3TC+5	3TC+20	
29	tCSR	CAS set-up time		TC-20	TC-10	
30	tDTS	TR·RAS set-up time		TC-10	TC	
31	tRDH	TR·RAS hold time (read data transfer)		3TC-10	3TC	
32	tCDH	TR·CAS hold time		2TC-25	2TC-10	
33	tSDD	Last SC·TR delay time		TC	TC+10	
34	tSDH	First SC·TR hold time		TC-20	TC-10	
35	tSCC	Serial clock cycle time		2TC		
36	tSC	SC pulse width		TC-20	TC	
37	tSCP	SC precharge width		TC-10	TC	
38	tSESC	SE set-up time		70		
39	tSRDS	Serial read data set-up time		20		
40	tSRDH	Serial read data hold time		0		
41	tWS	WE·RAS set-up time		TC-10	TC	
42	tWH	WE·RAS hold time		TC-10	TC	
43	tDTH	TR·RAS hold time		3TC-10	3TC	
44	tES	SOE·RAS set-up time		TC	TC+10	
45	tEH	SOE·RAS hold time		TC-25	TC-10	
46	tSRS	SC·RAS set-up time		40		
47	tSRD	RAS·SC delay time		30		

13.3.8 Kanji ROM interface

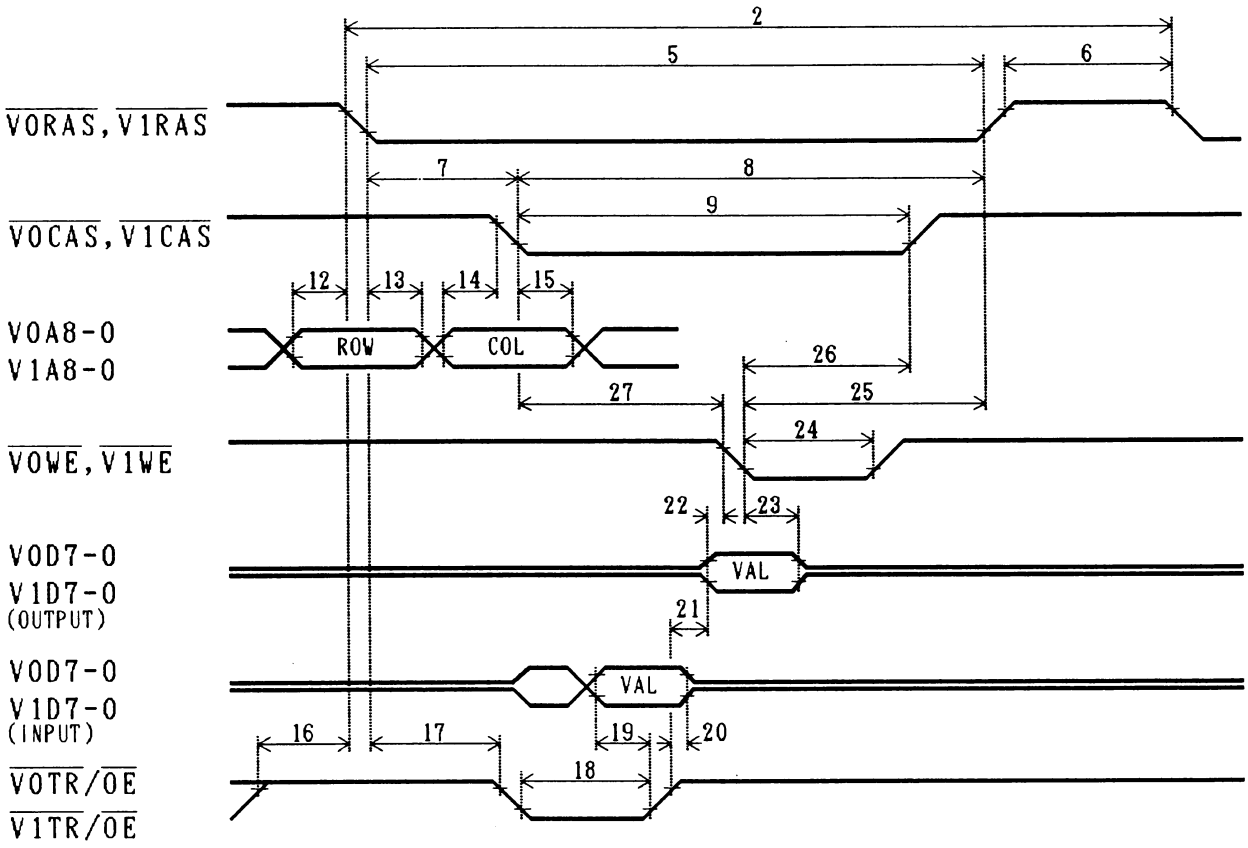
No.	Symbol	Item	Condition	Min.	Typ.	Unit
48	tKAV	Address fixed time	CL= 50PF	8TC-20	8TC	ns
49	tKOEH	KOE hold time		5TC-20	5TC	
50	tKAH	Address hold time		3TC-20	3TC	
51	tKOE	KOE pulse width		4TC-10	4TC	
52	tKDX	Data active time		0		
53	tKDS	Data set-up time		30		
54	tKDH	Data hold time		0		



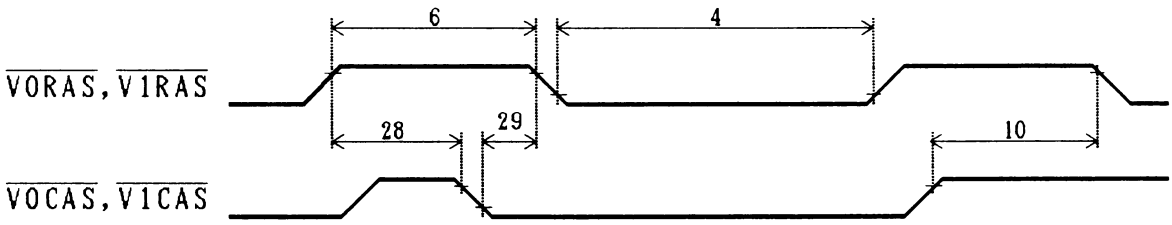
VRAM READ CYCLE



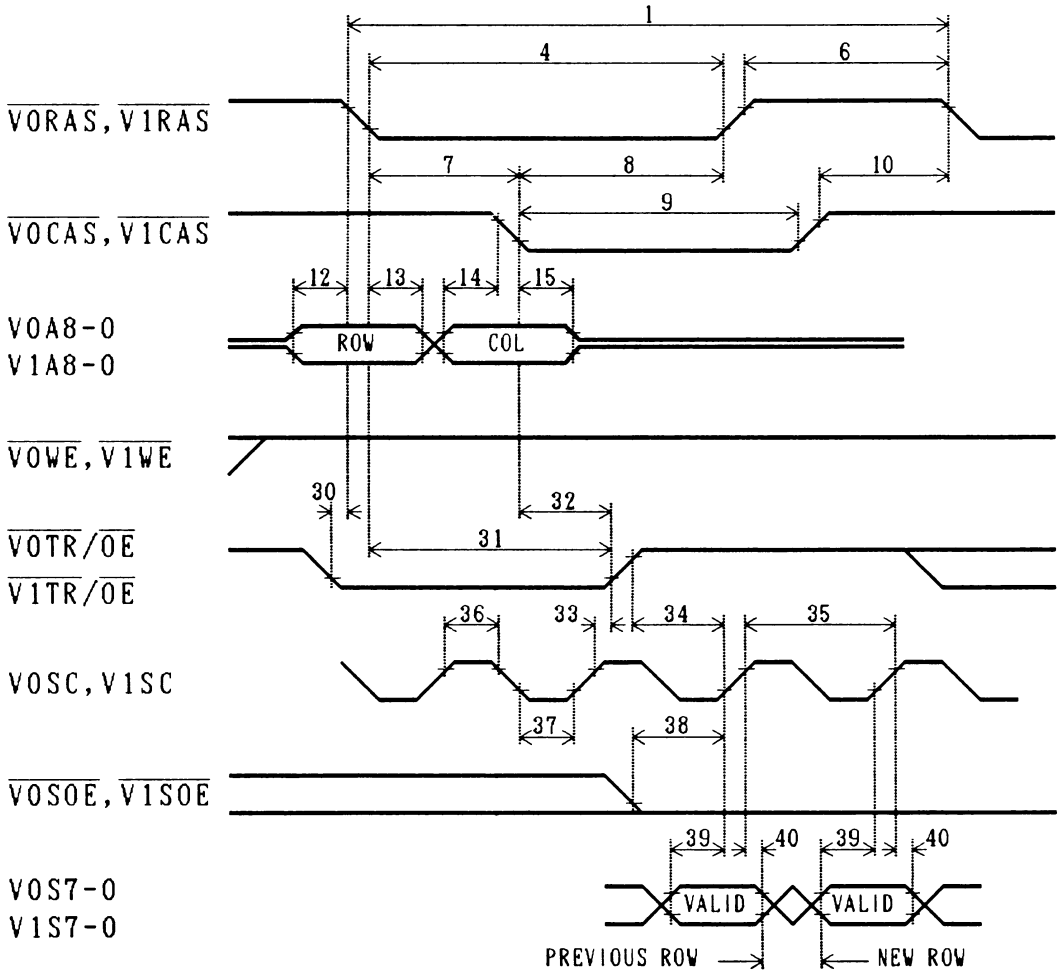
VRAM PAGE MODE READ CYCLE



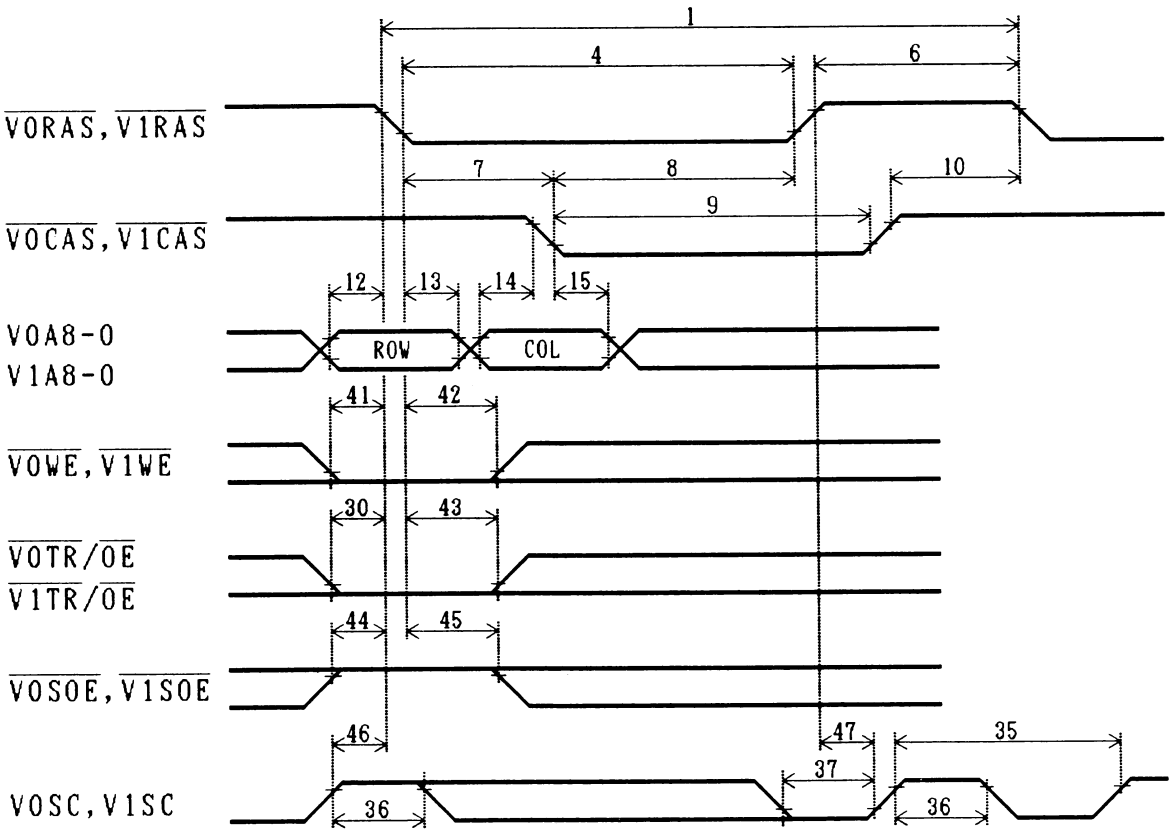
VRAM READ MODIFY WRITE CYCLE



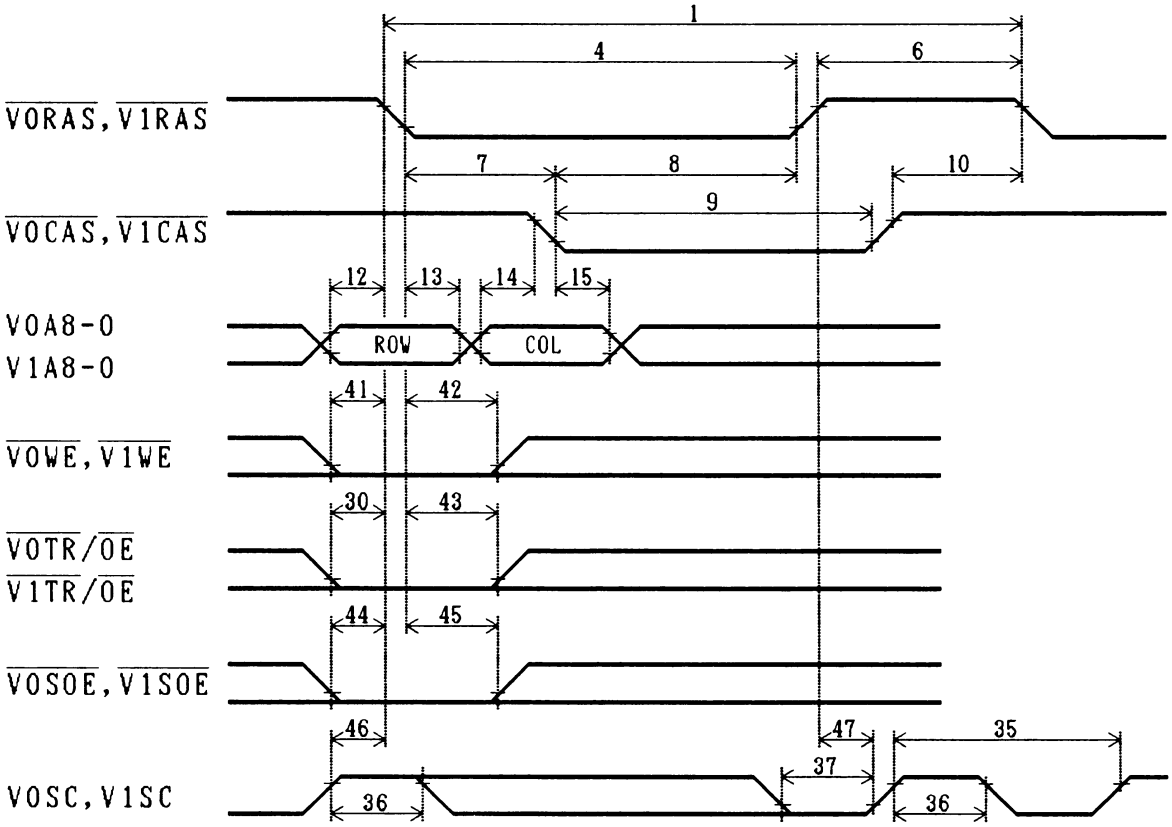
VRAM CAS BEFORE RAS REFRESH CYCLE



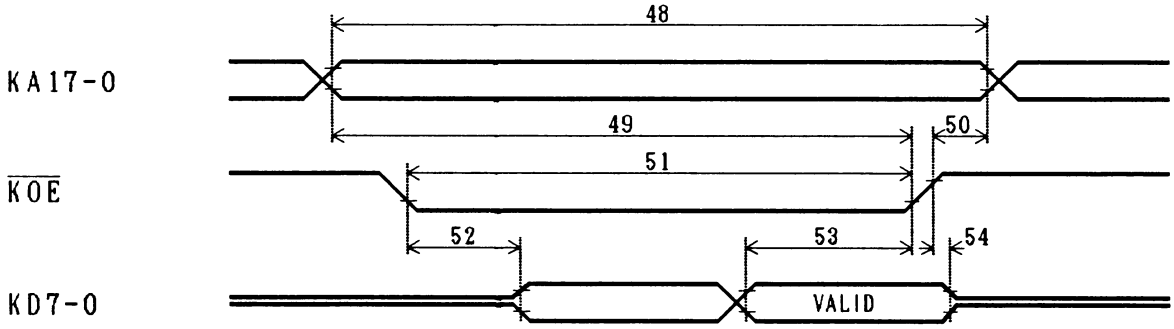
VRAM READ TRANSFER CYCLE



VRAM PSEUDO WRITE TRANSFER CYCLE



VRAM WRITE TRANSFER CYCLE



KANJI-ROM READ CYCLE

13.3.9 Color bus, synchronous signal output timing

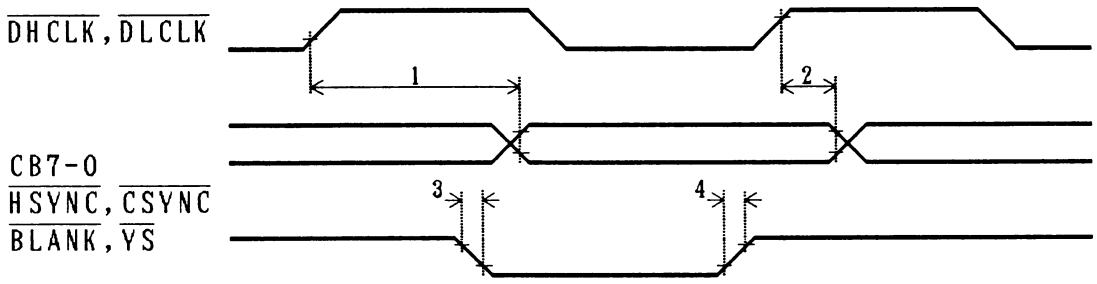
No.	Symbol	Item	Condition	Min.	Max.	Unit
1	tdCB	Color bus, synchronous signal output delay time	CL= 50PF		TC+20	ns
2	thCB	Color bus, synchronous signal output hold time		TC-20		
3	tfSYNC	Color bus, synchronous signal output fall time			10	
4	trSYNC	Color bus, synchronous signal output rise time			10	

13.3.10 RGB signal AC characteristics

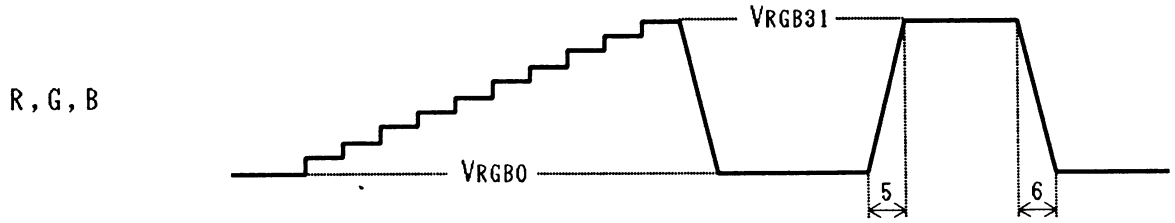
No.	Signal	Item	Condition	Min.	Typ.	Max.	Unit
5	trRGB	R,G,B signal output fall time	RL=470Ω		20		ns
6	tfRGB	R,G,B signal output rise time	CL= 50PF		20		

13.3.11 RGB signal output level

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
VRGB31	Maximum output voltage	RL=470Ω CL= 50PF		2.8		V
VRGB0	Minimum output voltage			1.7		
Vp-p	VRGB31-VRGB0 potential difference			1.1		
DRGB	Vp-p deviation				5	%



COLOR BUS,SYNC OUTPUT TIMING



R,G,B OUTPUT

13.3.12 Horizontal synchronous signal, display data timing

When horizontal synchronous signal, display data timing (NTSC, PAL) SM=0

No.	Item	Time	
		When using 21MHz	When using 14MHz
1	Horizontal cycle	63.70 μS	63.70 μS
2	Horizontal display period	47.68 μS	53.64 μS
3	Right border period	2.61 μS	0 μS
4	Right retrace line erase period	1.49 μS	1.40 μS
5	Horizontal synchronous pulse width	4.66 μS	4.75 μS
6	Left retrace line erase period	4.66 μS	3.91 μS
7	Left border period	2.61 μS	0 μS

When horizontal synchronous signal, display data time (NTSC, PAL) SM=1

No.	Item	Time	
		When using 21MHz	When using 14MHz
1	Horizontal cycle	63.56 μS	63.56 μS
2	Horizontal display period	47.68 μS	53.64 μS
3	Right border period	2.61 μS	0 μS
4	Right retrace line erase period	1.49 μS	1.40 μS
5	Horizontal synchronous pulse width	4.66 μS	4.75 μS
6	Left retrace line erase period	4.52 μS	3.77 μS
7	Left border period	2.61 μS	0 μS

Horizontal synchronous signal, display data timing (high scan)

No.	Item	Time	
		400 LINES	480 LINES
—	Dot clock frequency	21.477 MHz	25.175 MHz
1	Horizontal cycle	39.48 μS	31.78 μS
2	Horizontal display period	29.80 μS	25.42 μS
4	Right retrace line erase period	2.98 μS	0.64 μS
5	Horizontal synchronous pulse width	2.98 μS	3.81 μS
6	Left retrace line erase period	3.72 μS	1.91 μS

13.3.13 Vertical synchronous signal, display data timing

Vertical synchronous signal, display data timing (NTSC)

No.	Item	Non-interlace		Interlace	
		SM1=0	SM1=1	1st field	2nd field
8	Vertical cycle	262 H	263 H	262.5 H	262.5 H
9	Vertical display period	212 H	212 H	212 H	212 H
10	Bottom border period	14 H	14 H	14 H	14 H
11	Bottom retrace line erase period	4 H	4 H	4.5 H	4 H
12	Vertical synchronous pulse width	3 H	3 H	3 H	3 H
13	Top retrace line erase period	15 H	16 H	15 H	15.5 H
14	Top border period	14 H	14 H	14 H	14 H

※) The border period becomes the display period during over-scan.

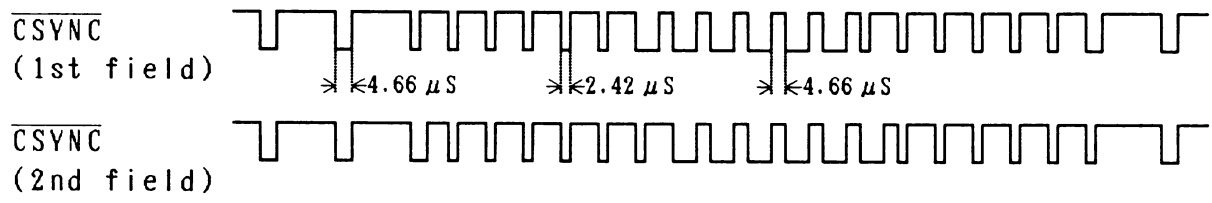
Vertical synchronous signal, display data timing (PAL)

No.	Item	Non-interlace	Interlace	
			1st field	2nd field
8	Vertical cycle	313 H	312.5 H	312.5 H
9	Vertical display period	212 H	212 H	212 H
10	Bottom border period	37 H	37 H	37 H
11	Bottom retrace line erase period	5 H	5.5 H	5 H
12	Vertical synchronous pulse width	3 H	3 H	3 H
13	Top retrace line erase period	15 H	14 H	14.5 H
14	Top border period	41 H	41 H	41 H

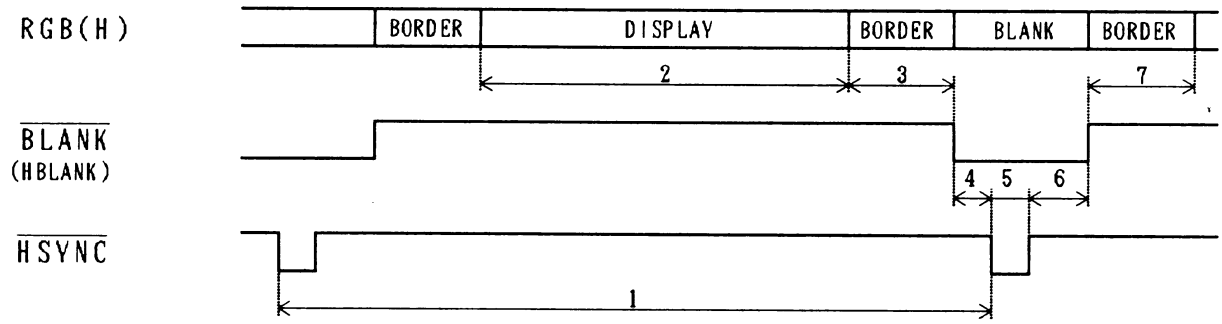
※) The border period becomes the display period during over-scan.

Vertical synchronous signal, display data timing (High scan)

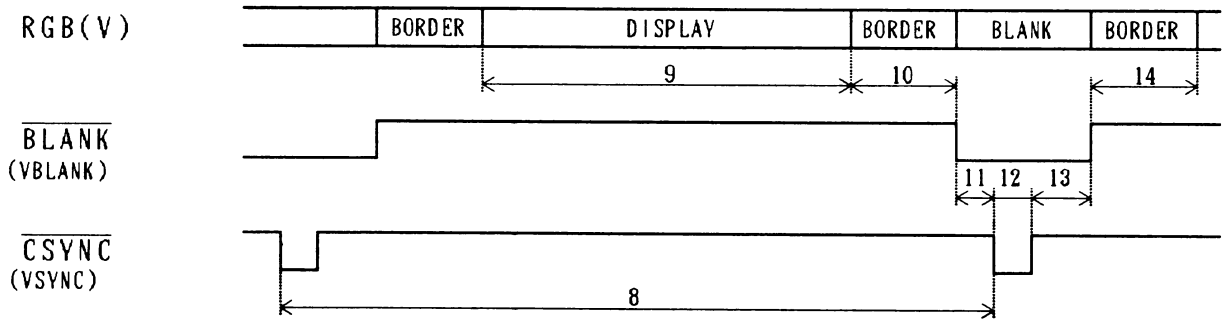
No.	Item	400LINES	480LINES
8	Vertical cycle	440 H	525 H
9	Vertical display period	400 H	480 H
11	Bottom retrace line erase period	7 H	10 H
12	Vertical synchronous pulse width	8 H	2 H
13	Top retrace line erase period	25 H	33 H



CSYNC OUTPUT TIMING (V-BLANKING)



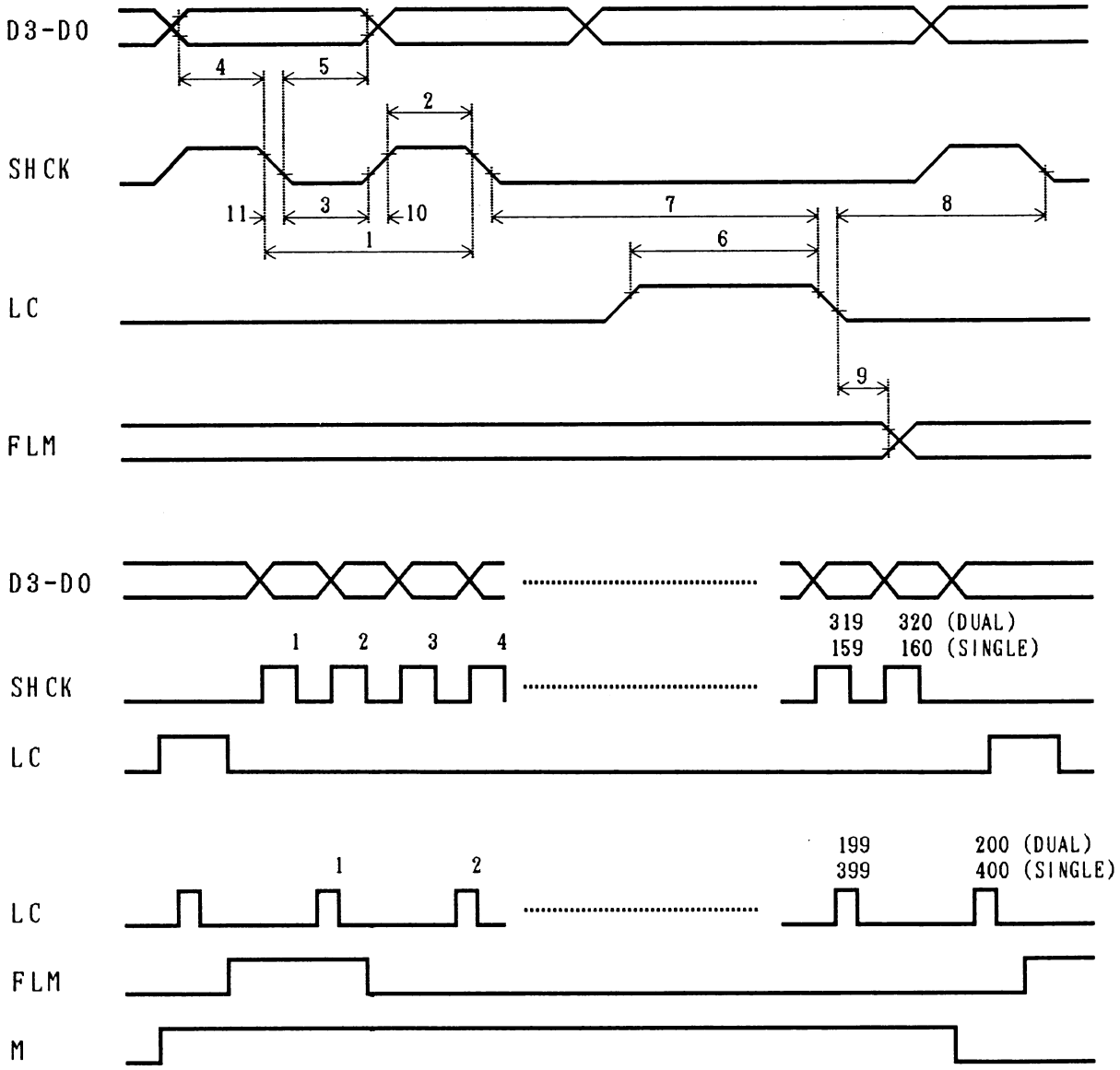
H DISPLAY TIMING



V DISPLAY TIMING

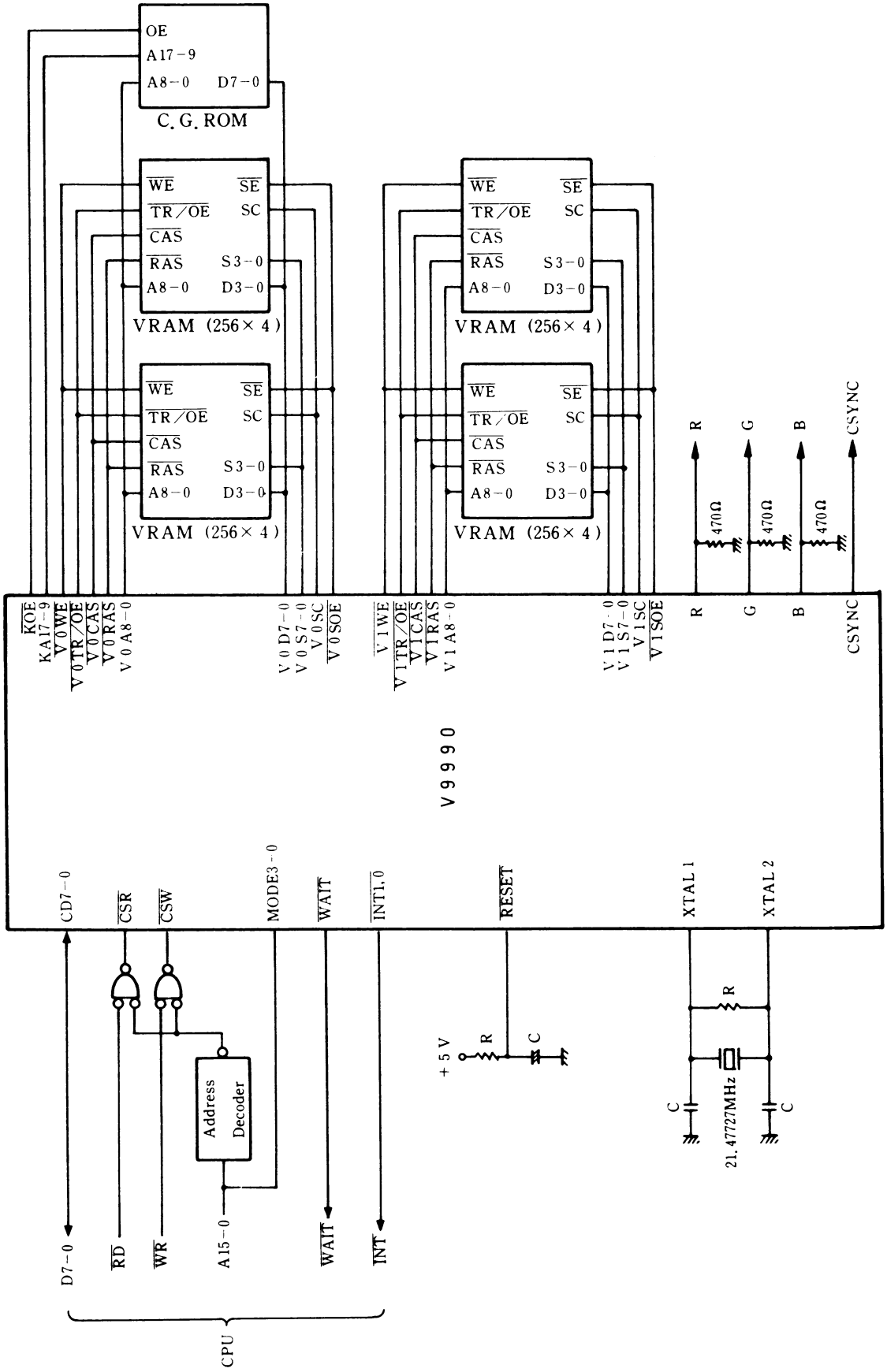
13.3.14 Panel interface timing

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	tcSCK	SHCK clock cycle	CL= 50PF		4TC		ns
2	twhSCK	SHCK high level pulse width		2TC-10	2TC		
3	twlSCK	SHCK low level pulse width		2TC-10	2TC		
4	tsD	Data set-up time		2TC-20	2TC		
5	thD	Data hold time		2TC-20	2TC		
6	twLC	LC pulse width		4TC-10	4TC		
7	tdSCLC	SHCK—LC delay time (400LINES)			125TC		
7	tdSCLC	SHCK—LC delay time (480LINES)			77TC		
8	tdLCSC	LC—SHCK delay time			87TC		
9	thFLM	FLM hold time		4TC-20	4TC		
10	tr	Clock rise time				10	
11	tf	Clock fall time				10	



PANEL INTERFACE TIMING

14 EXAMPLE OF SYSTEM CONFIGURATION



15 EXAMPLE OF SAMPLE SOFTWARE

The content of this page is a file called "V9990. inc", which is used in the example of the program hereafter.

Commands and application examples

```
vdp       equu      0e0h
;
;         VDP   commands
;
c_abort           equ       00000000b
c_lmmc            equ       00010000b
c_lmmv            equ       00100000b
c_lmcm            equ       00110000b
c_lmmm            equ       01000000b
c_cmmc            equ       01010000b
c_cmmk            equ       01100000b
c_cmmm            equ       01110000b
c_bmxl            equ       10000000b
c_bmlx            equ       10010000b
c_bmll            equ       10100000b
c_line            equ       10110000b
c_srch            equ       11000000b
c_point           equ       11010000b
c_pset            equ       11100000b
c_advance         equ       11110000b

;
;         Macro to set register number to be accessed by later
;         'outreg' and 'inreg'
;
setreg    macro     val
          ifdif     <val>,<a>
          ld        a,val
          endif
          out       (vdp+4),a
          endm
;
;         Macro to output value to a register
;
outreg    macro     val
          ifdif     <val>,<a>
          ld        a,val
          endif
          out       (vdp+3),a
          endm
;
;         Macro to input value from a register
;
inreg     macro
          in        a,(vdp+3)
          endm

sx:       defs      2
sy:       defs      2
dx:       defs      2
dy:       defs      2
nx:       defs      2
ny:       defs      2
argu:     defs      1
logop:    defs      1
mask0:    defs      1
mask1:    defs      1
color:    defs      4
cmd:      defs      1
```

```
        .z80

        include v9990.inc

outcmd  macro   command,reg
        ld      a,command
        ld      (cmd),a
        ld      hl,0ffffh
        ld      (mask0),hl
        call    wait_end
        setreg  reg
        ld      hl,cmd-(52-reg)
        ld      b,53-reg
        ld      c,vdp+3
        otir
        endm

pset:
        ld      hl,100
        ld      (dx),hl
        ld      hl,200
        ld      (dy),hl
        ld      hl,12345
        ld      (color),hl
        ld      a,1100b
        ld      (logop),a
        outcmd  c_pset,36
        ret

wait_end:
        in      a,(vdp+5)
        rrca
        jr      c,wait_end
        ret

        end
```

```
        .z80
        include V9990.inc
;
;       Initialize V9990                                        Initialization of V9990
init:

        xor     a                       ; set MCS
        out     (vdp+7),a
        setreg  6
        outreg  10000011b               ; set B1, X image = 256,16 bit/dot
        outreg  10000000b               ; set non-interlace
        outreg  10000010b               ; enable display, VRAM = 512KByte
        ret

;
;       Move BC byte from memory HL to VRAM A:DE                Memory transfer
;
ldirvm:
        push    af
        setreg  0
        outreg  e                       ; set A07..A00
        outreg  d                       ; set A15..A08
        pop     af
        outreg  a                       ; set A18..A16
        ld      a,b                     ; set higher byte of length
        ld      b,c                     ; set lower byte of length
        inc     b                       ; is lower byte 0?
        dec     b
        jr      z,ldirvm_go             ; yes
        inc     a                       ; modify higher byte
ldirvm_go:
        ld      c,vdp
ldirvm_loop:
        otir
        dec     a
        jr      nz,ldirvm_loop
        ret

;
;       Set screen mode                                         Screen mode setting
;
;               A = 0   P1
;                   1   P2
;                   2   B1
;                   3   B2
;                   4   B3
;                   5   B4
;                   6   B5
;                   7   B6
;
screen:
        ld      e,a
        ld      d,0
        ld      l,e
        ld      h,d
        add     hl,hl                   ; x3
        add     hl,de
        ld      de,screen_table
        add     hl,de
        ld      a,(hl)                  ; Set 'system control port'
        inc     hl
        out     (vdp+7),a
        setreg  6+01000000b             ; Set 'screen mode register 0'
        inreg
```

```
        and     00001111b
        or      (hl)
        inc     hl
        outreg  a
        inreg                           ; Set 'screen mode register 1'
        and     10111110b
        or      (hl)
        outreg  a
        ret

screen_table:
;               v vvvv        v     v
        defb    0,00000000b,00000000b       ; p1
        defb    0,01010000b,00000000b       ; p2
        defb    0,10000000b,00000000b       ; b1
        defb    1,10010000b,00000000b       ; b2
        defb    0,10010000b,00000000b       ; b3
        defb    1,10100000b,00000000b       ; b4
        defb    0,10110000b,00000001b       ; b5
        defb    0,10110000b,01000001b       ; b6

;
;       Set bits/pixel
;
;               A = 0     2bit/pixel
;                   1     4bit/pixel
;                   2     8bit/pixel
;                   3    16bit/pixel
;
colors:
        ld      b,a
        setreg  6+11000000b
        inreg
        and     11111100b
        or      b
        outreg  a
        ret

;
;     Set  number of dots in the image space
;
;               A = 0     256 dot
;                   1     512 dot
;                   2    1024 dot
;                   3    2048 dot
;
images:
        add     a,a
        add     a,a
        ld      b,a
        setreg  6+11000000b
        inreg
        and     11110011b
        or      b
        outreg  a
        ret

;
;       Initialize palette
;
init_palette:
        setreg  13
        outreg  00000000b           ; enable palette
                                    ; disable YJK/YUV with attribute
                                    ; enable auto increment of R#14
                                    ; set palette offset to 0
        outreg  0
```

Bit/pixel setting

Setting dot number in image space

Initialization of color palette

```
        ld      hl,palette_data
        ld      c,vdp+1
        ld      b,64*3
        otir
        ret

;
;               R   G   B
;
palette_data:
        defb    4*0,4*0,4*0
        defb    4*0,4*0,4*0
        defb    4*1,4*6,4*1
        defb    4*3,4*7,4*3
        defb    4*1,4*1,4*7
        defb    4*2,4*3,4*7
        defb    4*5,4*1,4*1
        defb    4*2,4*6,4*7
        defb    4*7,4*1,4*1
        defb    4*7,4*3,4*3
        defb    4*6,4*6,4*1
        defb    4*6,4*6,4*4
        defb    4*1,4*4,4*1
        defb    4*6,4*2,4*5
        defb    4*5,4*5,4*5
        defb    4*7,4*7,4*7

        defb    3*0,3*0,3*0
        defb    3*0,3*0,3*0
        defb    3*1,3*6,3*1
        defb    3*3,3*7,3*3
        defb    3*1,3*1,3*7
        defb    3*2,3*3,3*7
        defb    3*5,3*1,3*1
        defb    3*2,3*6,3*7
        defb    3*7,3*1,3*1
        defb    3*7,3*3,3*3
        defb    3*6,3*6,3*1
        defb    3*6,3*6,3*4
        defb    3*1,3*4,3*1
        defb    3*6,3*2,3*5
        defb    3*5,3*5,3*5
        defb    3*7,3*7,3*7

        defb    2*0,2*0,2*0
        defb    2*0,2*0,2*0
        defb    2*1,2*6,2*1
        defb    2*3,2*7,2*3
        defb    2*1,2*1,2*7
        defb    2*2,2*3,2*7
        defb    2*5,2*1,2*1
        defb    2*2,2*6,2*7
        defb    2*7,2*1,2*1
        defb    2*7,2*3,2*3
        defb    2*6,2*6,2*1
        defb    2*6,2*6,2*4
        defb    2*1,2*4,2*1
        defb    2*6,2*2,2*5
        defb    2*5,2*5,2*5
        defb    2*7,2*7,2*7

        defb    1*0,1*0,1*0
        defb    1*0,1*0,1*0
        defb    1*1,1*6,1*1
        defb    1*3,1*7,1*3
        defb    1*1,1*1,1*7
```

```
        defb    1*2,1*3,1*7
        defb    1*5,1*1,1*1
        defb    1*2,1*6,1*7
        defb    1*7,1*1,1*1
        defb    1*7,1*3,1*3
        defb    1*6,1*6,1*1
        defb    1*6,1*6,1*4
        defb    1*1,1*4,1*1
        defb    1*6,1*2,1*5
        defb    1*5,1*5,1*5
        defb    1*7,1*7,1*7

;
;       Wait until VSYNC
;
wait_vsync:
        in      a,(vdp+5)
        and     01000000b
        jr      nz,wait_vsync     ; still in VSYNC
wait_vsyncl:
        in      a,(vdp+5)
        and     01000000b
        jr      z,wait_vsyncl     ; not in VSYNC
        ret

        end
```

WAIT till Vsync

16 V9990 EVALUATION BOARD

16.1 V9990 evaluation board

The evaluation board can be operated on 3 systems as listed below.

- PC-98 system
- MSX system
- IBM-PC system

It consists of a V9990 main board, an interface board for each of the above systems, and interface cable that connects these two boards, allowing selection to individual application.

Installation is as simple as to set switches on the interface board and to insert in into the slot. The main board is so designed that it can be installed to the outside of the system to facilitate function check and system development.

16.2 Connectors on main board

CN1·····Digitizing connector (for analog system)

Pin No.	Name	Pin No.	Name
1	$\overline{YS}$	2	+12V
3	R	4	
5	G	6	-12V
7	B	8	
9	DCLK	10	A-GND
11	VRESET	12	
13	HSYNC	14	
15	CSYNC	16	
17	A-GND	18	
19	V-OUT	20	

CN2·····VIDEO OUT (RCA)

CN3·····Analog RGB OUT (Multi 21 pin)

CN4·····Panel connector

Pin No.	Name	Pin No.	Name
1	M	2	FLM
3	LC	4	SCK
5	D0	6	D1
7	D2	8	D3
9	+5V	10	D-GND

CN5……Microcomputer interface connector

Pin No.	Name	Pin No.	Name
1		2	GND
3		4	CD0
5		6	CD1
7		8	CD2
9		10	CD3
11		12	CD4
13		14	CD5
15		16	CD6
17		18	CD7
19		20	
21	GND	22	MOD0
23		24	MOD1
25		26	MOD2
27		28	MOD3
29		30	
31		32	$\overline{CSW}$
33		34	$\overline{CSR}$
35		36	$\overline{WAIT}$
37		38	$\overline{INT0}$
39		40	$\overline{INT1}$
41		42	$\overline{RESET}$
43	+12V	44	+12V
45	−12V	46	−12V
47	+5V	48	+5V
49		50	

CN6……Digitizing connector (for digital system)

Pin No.	Name	Pin No.	Name
1	C0	2	C8
3	C1	4	C9
5	C2	6	C10
7	C3	8	C11
9	C4	10	C12
11	C5	12	C13
13	C6	14	C14
15	C7	16	C15
17	D-GND	18	D-GND
19		20	
21		22	MCLK
23	+5V	24	+5V
25		26	

16.3 Switches on interface board

●Interface board for PC-98, interface board for IBM-PC

- SW1
- SW2

Port address setting (ON side … "L", OFF side … "H")

- SW3 − 1 : Unused
  - 2 : $\overline{INT1}$ ON/OFF
  - 3 : $\overline{INT0}$ ON/OFF
  - 4 : $\overline{WAIT}$ ON/OFF

●Interface board for MSX

- SW1 : Port address setting (ON side … "L", OFF side … "H")
- SW2 − 1 : $\overline{WAIT}$ ON/OFF
  - 2 : $\overline{INT0}$ ON/OFF
  - 3 : $\overline{INT1}$ ON/OFF
  - 4 : Unused

17 DISPLAY FUNCTION FOR YUV, YJK FORM DATA

	b7	b6	b5	b4	b3	b2	b1	b0
R#13	PLTM1	PLTM0	YAE					

・PLTM1 PLTM0 Selection of color palette mode

1	1	: YUV mode
1	0	: YJK mode
0	1	: 256 color mode
0	0	: Palette mode

・YAE Selection of YJK,YUV and RGB mixing mode (effective when in YUV,YJK modes)

1	: YJK,YUV image and RGB image displayed as mixed.
0	: Only YJK,YUV image displayed.

1) YAE 0 : without attribute

	C7	C6	C5	C4	C3	C2	C1	C0
1dot	Y1					VL		
1dot	Y2					VH		
1dot	Y3					UL		
1dot	Y4					UH		

	C7	C6	C5	C4	C3	C2	C1	C0
1dot	Y1					KL		
1dot	Y2					KH		
1dot	Y3					JL		
1dot	Y4					JH		

represents color data for 1dot and 2^{17}colors can be specified.

YUV,YJKfrom data are divided into groups each of which consist of continuous 4dot as follows.

Y1・VL(KL)・VH(KH)・UL(JL)・UH(JH) : Color data for the first dot.
Y2・VL(KL)・VH(KH)・UL(JL)・UH(JH) : Color data for the second dot.
Y3・VL(KL)・VH(KH)・UL(JL)・UH(JH) : Color data for the third dot.
Y4・VL(KL)・VH(KH)・UL(JL)・UH(JH) : Color data for the fourth dot.

2) YAE 1 : with attribute

	C7	C6	C5	C4	C3	C2	C1	C0
1dot	Y1				A	VL		
1dot	Y2				A	VH		
1dot	Y3				A	UL		
1dot	Y4				A	UH		

	C7	C6	C5	C4	C3	C2	C1	C0
1dot	Y1				A	KL		
1dot	Y2				A	KH		
1dot	Y3				A	JL		
1dot	Y4				A	JH		

A:Attribute

(1)WhenA=0

Just like when YAE="0", represent color data for 1dot and 2^{16}colors can be specified.
(Bit"A"Is ignored.)

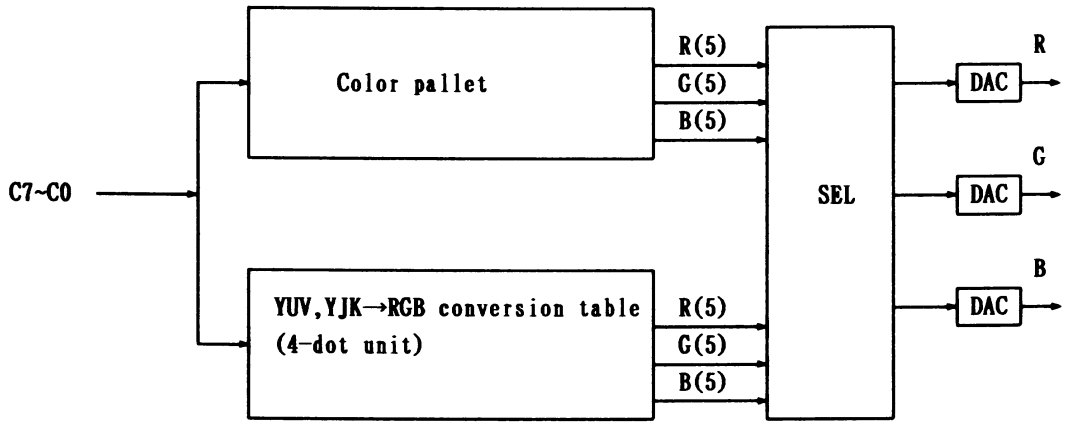
(2)WhenA=1

Each of Y1,Y2,Y3 and Y4 becomes a color code and is output by RGB through the color pallet.
(16 colors)
In this case,VL(KL)・VH(KH)・UL(JL)・UH(JH) data are ignored.

3) Combination of PLTM1,0 and YAE

PLTM1	PLTM0	YAE	VRAM data
0	0	*	Through color pallet
0	1	*	Direct RGB (G:3bit, R:3bit, B:2bit)
1	0	0	Through YUV,YJK→RGB conversion table
1	1		
1	0	1	A=0··· Through YUV,YJK→RGB conversion table A=1··· through color pallet
1	1		

Either "0" or "1" can be used for *.



4) Conversion formula between YUV,YJK and RGB

(1) Conversion from YUV to RGB

$$R = Y + U$$
$$G = \frac{5}{4}Y - \frac{U}{2} - \frac{V}{4}$$
$$B = Y + V$$

(2) Conversion from RGB to YUV

$$Y = \frac{G}{2} + \frac{R}{4} + \frac{B}{8}$$
$$U = R - Y$$
$$V = B - Y$$

(3) Conversion from YJK to RGB

$$R = Y + J$$
$$G = Y + K$$
$$B = \frac{5}{4}Y - \frac{J}{2} - \frac{K}{4}$$

(4) Conversion from RGB to YJK

$$Y = \frac{B}{2} + \frac{R}{4} + \frac{G}{8}$$
$$J = R - Y$$
$$K = G - Y$$

The specifications of this product are subject to improvement changes without prior notice.

AGENCY

YAMAHA CORPORATION

Address inquiries to:
Semi-conductor Sales Department

- Head Office 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-01
  Electronic Equipment business section
  Tel. 0539-62-4918 Fax. 0539-62-5054
- Tokyo Office 3-4, Surugadai Kanda, Chiyoda-ku, Tokyo, 101
  Ryumeikan Bldg. 4F
  Tel. 03-3255-4481 Fax. 03-3255-4488
- Osaka Office 3-12-9, Minami Senba, Chuo-ku, Osaka City, Osaka, 542
  Shinsaibashi Plaza Bldg. 4F
  Tel. 06-252-7980 Fax. 06-252-5615
- U.S.A. Office YAMAHA Systems Technology.
  981 Ridder Park Drive San Jose, CA95131
  Tel. 408-437-3133 Fax. 408-437-8791

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