EE511 Final Project

In the final project, you will design a 5-stage pipelined processor that is compatible with Cortex-M0. You only need to implement the functions that you did in your midterm project. Implement everything in "CortexM0.v". You can use the template for test programs that was distributed for the midterm project. Use *.hex file for the simulation. The instruction set simulator you made in the midterm project will be useful when you debug the processor.

Additionally, you have to submit the block diagram of the datapath of your processor. You can use any program to draw it, but convert it to .pdf file when you submit.

Please do not create additional files. Also, do not include $display command in your final files.

- **Deadline: 11/31 (Thu) 23:59**
- **E-mail Address**
  - sjlee@ics.kaist.ac.kr
  - E-mail Title: Final {Your student ID}
  - For example, Final 20191234
- **Attachment: Final 20191234.zip**
  - CortexM0.v
  - Block diagram of the datapath, Datapath 20191234.pdf