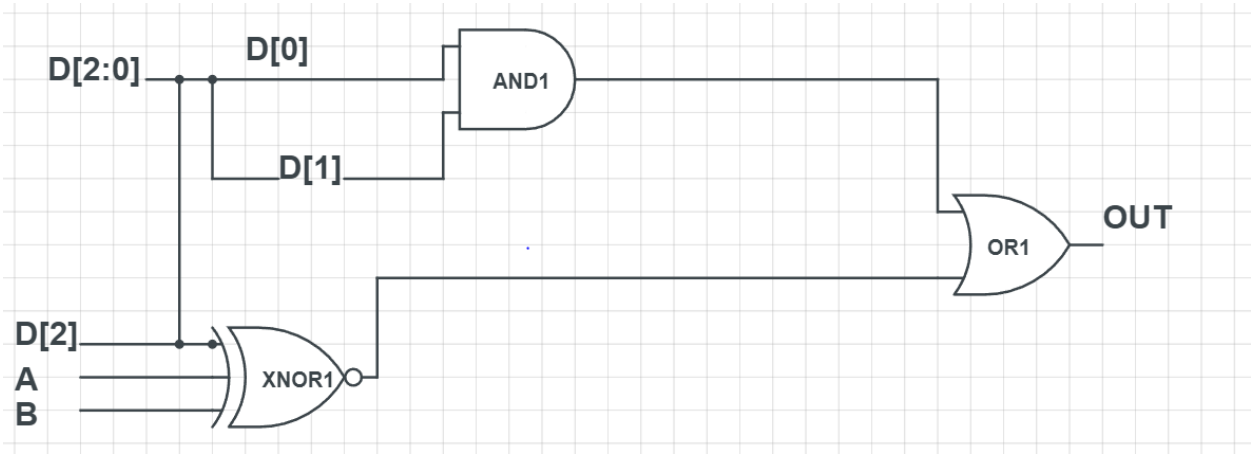
Assignment 1

Deliverables:

1. Verilog codes for each Design and the top module.

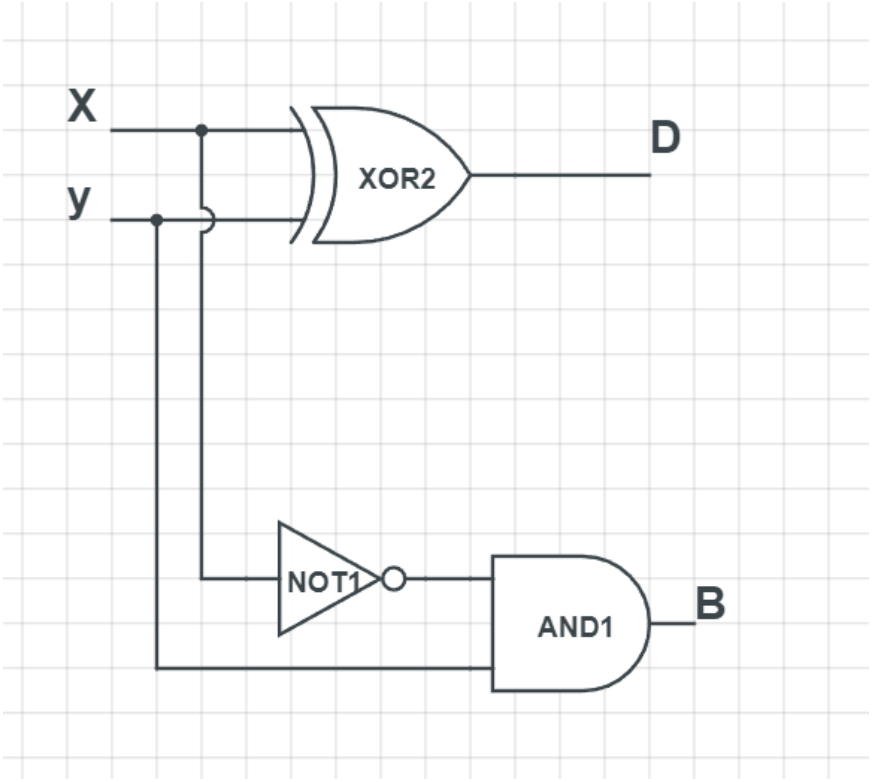
2. Snippets from Model sim simulation wave and results for all possible inputs in the design.

Q1 : Design the following circuit using Verilog

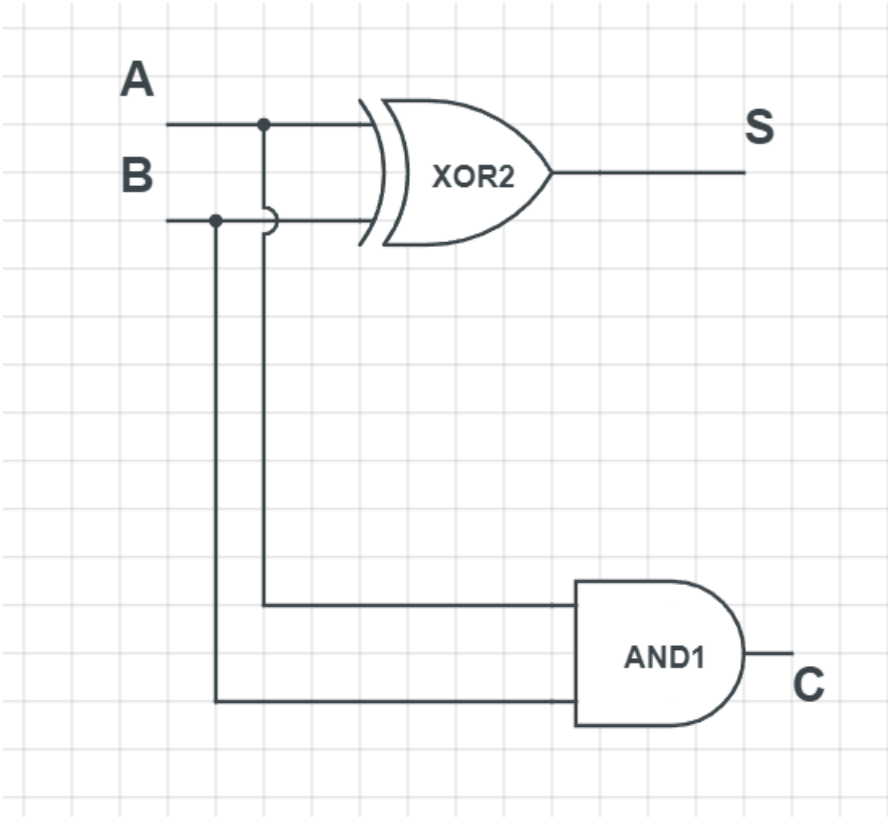


Q2 :

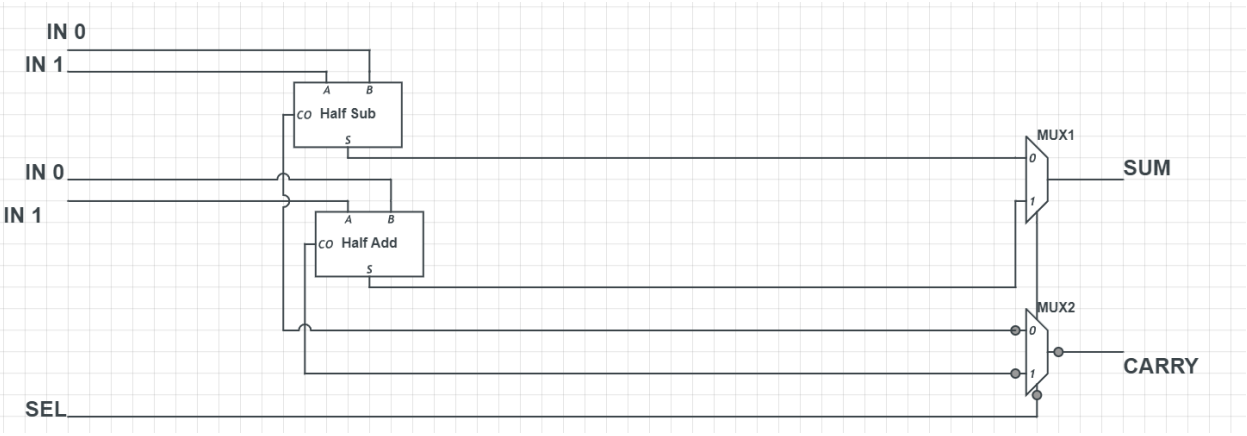
1- Design a half subtractor using gate level modeling style



2- Design a half adder using gate level modeling



3- Design this top module and Instantiate the mux written in the session, half adder and half subtractor in your design



<u>The top module has 3 inputs IN0 , IN1 , SEL and 2 outputs SUM , CARRY</u>