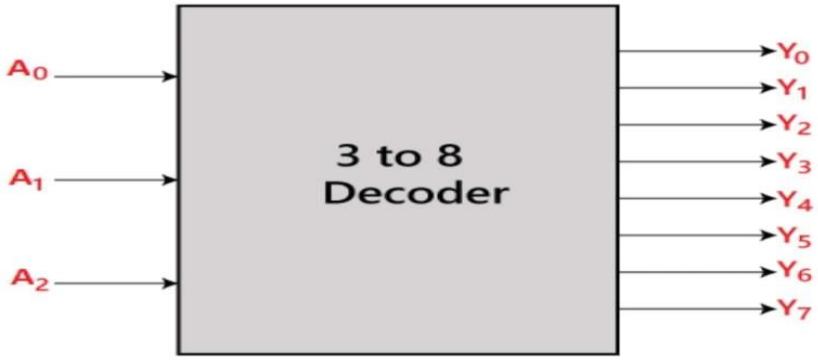
# Assignment 2

**Design the following circuits using Verilog and create a randomized testbench.**

Q1: Design this 3x8 Decoder with enable signal.




## Truth Table:

| Enable | INPUTS | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| E | $A_2$ | $A_1$ | $A_0$ | $Y_7$ | $Y_6$ | $Y_5$ | $Y_4$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Q2: We have 3 inputs N bits (A , B , C) and 2N bits output (out1, out 2)  since N is a parameter = 5.

**You should compare between three numbers and assign the outputs according to the table below:**

| Input | Out1 | Out2 |
|---|---|---|
| The largest number And two other inputs | Sign extension of the largest number | Concatenate of the other two inputs |
| The three inputs are equal | Out1= shift left by 2 of the input | Out2= shift right by 2 of the input |
| Default | Out1=0 | Out2=0 |

***Do we really want to write default case or we covered all possibilities ? Justify your answer.***

## *Sign extension explanation:*

Is to check the most significant bit if it was zero then the output will be extended by zeros else will be extended by ones.