TCA9548A 支持复位的低压 8 通道 I^{2}C 开关

1 特性

- 8 选 1 双向转换开关
- 与 I^{2}C 总线和系统管理总线 (SMBus) 兼容
- 低电平有效复位输入
- 三个地址引脚，在 I^{2}C 总线上最多支持八个 TCA9548A 器件
- 以任意组合通过 I^{2}C 总线实现通道选择
- 加电时取消选定所有开关通道
- 低 R_{ON} 开关
- 支持 1.8V，2.5V，3.3V 和 5V 总线间的电压电平转换
- 加电时无毛刺脉冲
- 支持热插入
- 低待机电流
- 工作电源电压范围为 1.65V 至 5.5V
- 5V 耐压输入
- 0 至 400kHz 时钟频率
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - ±2000V 人体放电模式 (A114-A)
  - 200V 机器放电模式 (A115-A)
  - ±1000V 组件充电模式 (C101)

2 应用范围

- 服务器
- 路由器（电信交换设备）
- 工厂自动化
- 具有 I^{2}C 从地址冲突（例如，存在多个完全相同的温度传感器）的产品

3 说明

TCA9548A 器件配有八个可通过 I^{2}C 总线控制的双向转换开关。串行时钟/串行数据 (SCL/SDA) 上行对可扩展为 8 个下行对或通道。根据可编程控制寄存器的内容，可选择任一单独 SCn/SDn 通道或者通道组合。

发生超时或其他不当操作时，系统主控器可通过将 $\overline{\text{RESET}}$ 输入置为低电平来复位 TCA9548A。同样，加电复位即可取消选中所有通道并初始化 I^{2}C/SMBus 状态机。将 $\overline{\text{RESET}}$ 置为有效也可实现复位和初始化，并且无需将部件断电。

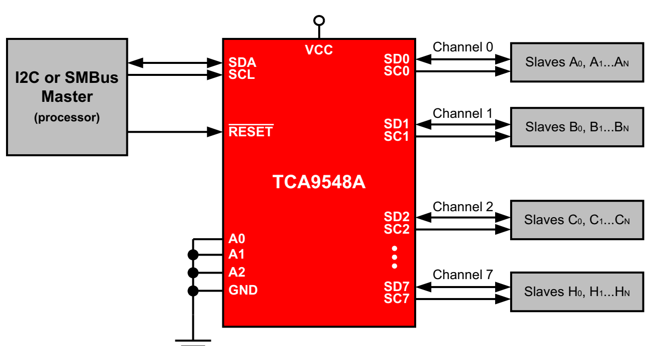
开关上有导通栅极，这样 VCC 引脚便可用于限制通过 TCA9548A 的最大高电压。限制最大高电压允许在每个通道对上使用不同的总线电压，以便 1.8V，2.5V 或 3.3V 部件可以在没有任何额外保护的情况下与 5V 部件通信。对于每个通道，外部上拉电阻器将总线电压上拉至所需的电压水平。所有 I/O 引脚为 5V 耐压。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA9548A	TSSOP (24)	7.80mm × 4.40mm
	VQFN (24)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化的应用示意图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (January 2015) to Revision E	Page
• Updated Pin Functions table.	3
• Added new I^2C Sections and read/write description	14

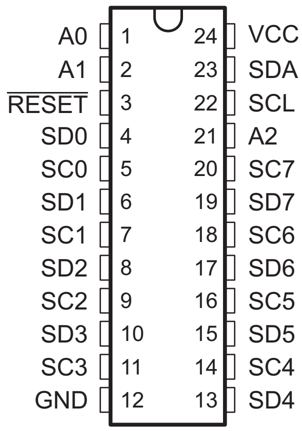
Changes from Revision C (November 2013) to Revision D	Page
• 已添加 *引脚配置和功能部分*，*ESD 额定值表*，*特性 描述 部分*，*器件功能模式*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分*	1
• Updated Typical Application schematic.	19

Changes from Revision B (November 2013) to Revision C	Page
• Updated V_{POR} and I_{CC} standby specification.	5

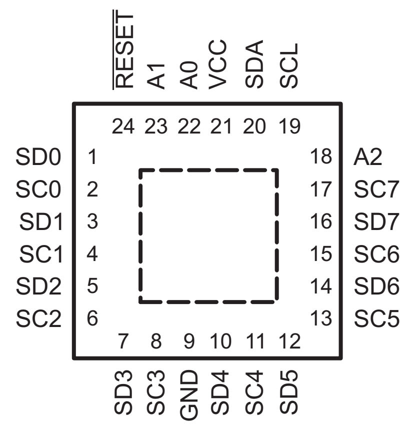
Changes from Revision A (July 2012) to Revision B	Page
• 更新了文档格式。	1
• 已删除订购信息。	1

5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP (PW)	QFN (RGE)		
A0	1	22	Input	Address input 0. Connect directly to V_{CC} or ground.
A1	2	23	Input	Address input 1. Connect directly to V_{CC} or ground.
$\overline{\text{RESET}}$	3	24	Input	Active-low reset input. Connect to V_{CC} or V_{DPUM} (1) through a pull-up resistor, if not used.
SD0	4	1	I/O	Serial data 0. Connect to V_{DPU0} (1) through a pull-up resistor.
SC0	5	2	I/O	Serial clock 0. Connect to V_{DPU0} (1) through a pull-up resistor.
SD1	6	3	I/O	Serial data 1. Connect to V_{DPU1} (1) through a pull-up resistor.
SC1	7	4	I/O	Serial clock 1. Connect to V_{DPU1} (1) through a pull-up resistor.
SD2	8	5	I/O	Serial data 2. Connect to V_{DPU2} (1) through a pull-up resistor.
SC2	9	6	I/O	Serial clock 2. Connect to V_{DPU2} (1) through a pull-up resistor.
SD3	10	7	I/O	Serial data 3. Connect to V_{DPU3} (1) through a pull-up resistor.
SC3	11	8	I/O	Serial clock 3. Connect to V_{DPU3} (1) through a pull-up resistor.
GND	12	9	Ground	Ground
SD4	13	10	I/O	Serial data 4. Connect to V_{DPU4} (1) through a pull-up resistor.
SC4	14	11	I/O	Serial clock 4. Connect to V_{DPU4} (1) through a pull-up resistor.
SD5	15	12	I/O	Serial data 5. Connect to V_{DPU5} (1) through a pull-up resistor.
SC5	16	13	I/O	Serial clock 5. Connect to V_{DPU5} (1) through a pull-up resistor.
SD6	17	14	I/O	Serial data 6. Connect to V_{DPU6} (1) through a pull-up resistor.
SC6	18	15	I/O	Serial clock 6. Connect to V_{DPU6} (1) through a pull-up resistor.
SD7	19	16	I/O	Serial data 7. Connect to V_{DPU7} (1) through a pull-up resistor.
SC7	20	17	I/O	Serial clock 7. Connect to V_{DPU7} (1) through a pull-up resistor.
A2	21	18	Input	Address input 2. Connect directly to V_{CC} or ground.
SCL	22	19	I/O	Serial clock bus. Connect to V_{DPUM} (1) through a pull-up resistor.
SDA	23	20	I/O	Serial data bus. Connect to V_{DPUM} (1) through a pull-up resistor.
VCC	24	21	Power	Supply voltage

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage and V_{DPU0}-V_{DPU7} are the slave channel reference voltages.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage(2)	–0.5	7	V
I_I	Input current	–20	20	mA
I_O	Output current	–25		mA
I_{CC}	Supply current	–100	100	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	6	V
		A2–A0, $\overline{\text{RESET}}$	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A2–A0, $\overline{\text{RESET}}$	–0.5	$0.3 \times V_{CC}$	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TCA9548A		UNIT
		PW (TSSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	57.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	62.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.7	34.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	34.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics[1]

V_{CC} = 2.3 V to 3.6 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP[2]	MAX	UNIT
V_{PORR}	Power-on reset voltage, V_{CC} rising		No load, $V_I = V_{CC}$ or GND[3]			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling[4]		No load, $V_I = V_{CC}$ or GND[3]		0.8	1		V
$V_{o(sw)}$	Switch output voltage		$V_{i(sw)} = V_{CC}$, I_{SWout} = –100 µA	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1		2	
				1.8 V		1.1		
				1.65 V to 1.95 V	0.9		1.25	
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 5.5 V	3	6		mA
			V_{OL} = 0.6 V		6	9		
I_I	SCL, SDA		$V_I = V_{CC}$ or GND[3]	1.65 V to 5.5 V	–1		1	µA
	SC7–SC0, SD7–SD0				–1		1	
	A2–A0				–1		1	
	$\overline{\text{RESET}}$				–1		1	
I_{CC}	Operating mode	f_{SCL} = 400 kHz	$V_I = V_{CC}$ or GND[3], I_O = 0	5.5 V		50	80	µA
				3.6 V		20	35	
				2.7 V		11	20	
				1.65 V		6	10	
		f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND[3], I_O = 0	5.5 V		9	30	
				3.6 V		6	15	
				2.7 V		4	8	
				1.65 V		2	4	
	Standby mode	Low inputs	V_I = GND[3], I_O = 0	5.5 V		0.2	2	
				3.6 V		0.1	2	
				2.7 V		0.1	1	
				1.65 V		0.1	1	
		High inputs	$V_I = V_{CC}$, I_O = 0	5.5 V		0.2	2	
				3.6 V		0.1	2	
				2.7 V		0.1	1	
				1.65 V		0.1	1	
ΔI_{CC}	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND[3]	1.65 V to 5.5 V		3	20	µA
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND[3]			3	20	
C_i	A2–A0		$V_I = V_{CC}$ or GND[3]	1.65 V to 5.5 V		4	5	pF
	$\overline{\text{RESET}}$					4	5	
	SCL		$V_I = V_{CC}$ or GND[3], Switch OFF			20	28	
$C_{io(off)}$[5]	SDA		$V_I = V_{CC}$ or GND[3], Switch OFF	1.65 V to 5.5 V		20	28	pF
	SC7–SC0, SD7–SD0					5.5	7.5	

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.
(2) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.
(3) $\overline{\text{RESET}} = V_{CC}$ (held high) when all other input voltages, V_I = GND.
(4) The power-on reset circuit resets the I^2C bus logic with $V_{CC} < V_{PORF}$.
(5) $C_{io(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

Electrical Characteristics(1) (continued)

V_{CC} = 2.3 V to 3.6 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(2)	MAX	UNIT
R_{ON}	Switch-on resistance	V_O = 0.4 V, I_O = 15 mA	4.5 V to 5.5 V	4	10	20	Ω
			3 V to 3.6 V	5	12	30	
		V_O = 0.4 V, I_O = 10 mA	2.3 V to 2.7 V	7	15	45	
			1.65 V to 1.95 V	10	25	70	

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		μs
t_{scl}	I²C clock low time		4.7		1.3		μs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0(1)		0(1)		μs
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (2)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (2)	300	ns
t_{ocf}	I²C output (SDn) fall time (10-pF to 400-pF bus)			300	$20 + 0.1C_b$ (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		μs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		μs
t_{sth}	I²C start or repeated start condition hold		4		0.6		μs
t_{sps}	I²C stop condition setup		4		0.6		μs
$t_{vdL(Data)}$	Valid-data time (high to low)(3)	SCL low to SDA output low valid		1		1	μs
$t_{vdH(Data)}$	Valid-data time (low to high)(3)	SCL low to SDA output high valid		0.6		0.6	μs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	μs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see Figure 6)

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \le 100$ pF (unless otherwise noted) (see Figure 5)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{rst} (2)	$\overline{\text{RESET}}$ time (SDA clear)		$\overline{\text{RESET}}$	SDA		500	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

6.8 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{W(L)}$	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

6.9 Typical Characteristics

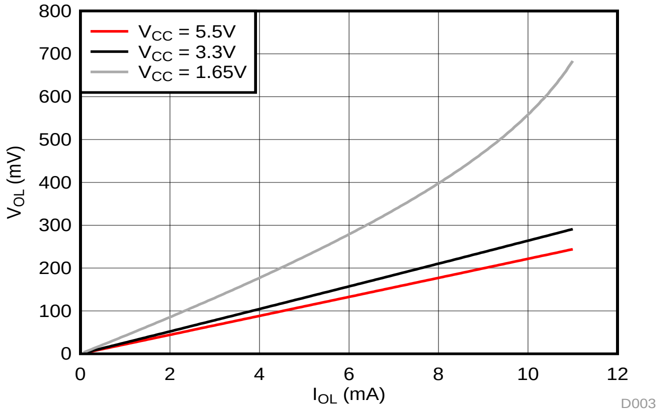


Figure 1. SDA Output Low Voltage (V_{OL}) vs Load Current (I_{OL}) at Three V_{CC} Levels

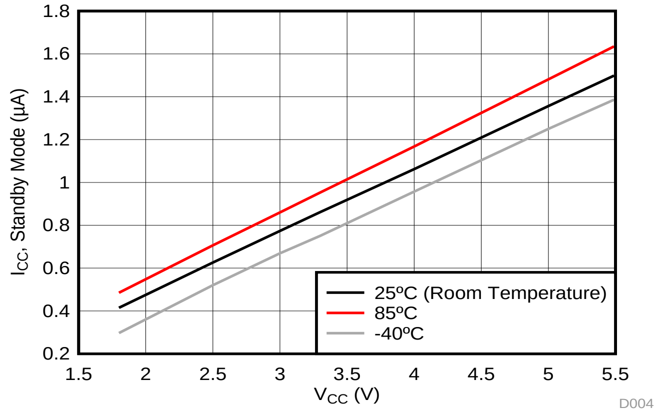


Figure 2. Standby Current (I_{CC}) vs Supply Voltage (V_{CC}) at Three Temperature Points

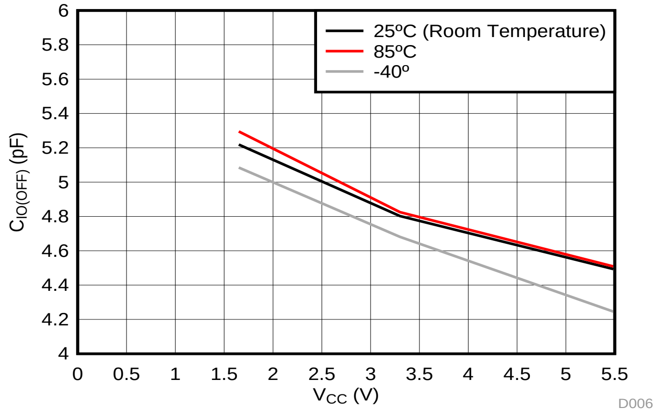


Figure 3. Slave Channel (SCn/SDn) Capacitance ($C_{io(OFF)}$) vs. Supply Voltage (V_{CC}) at Three Temperature Points

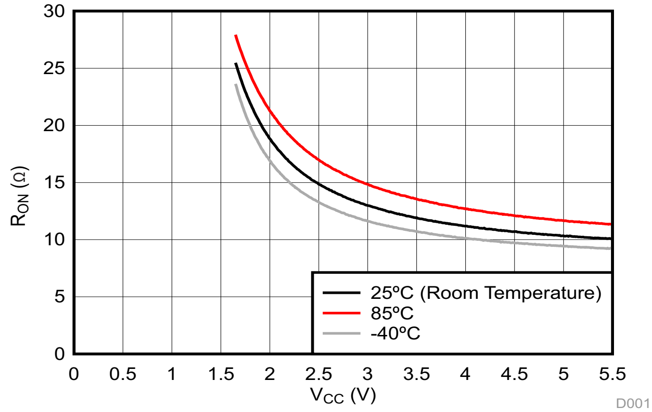
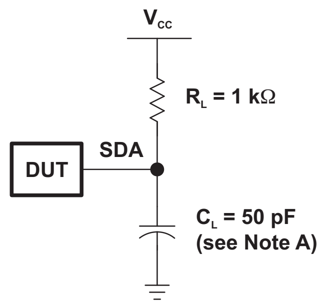
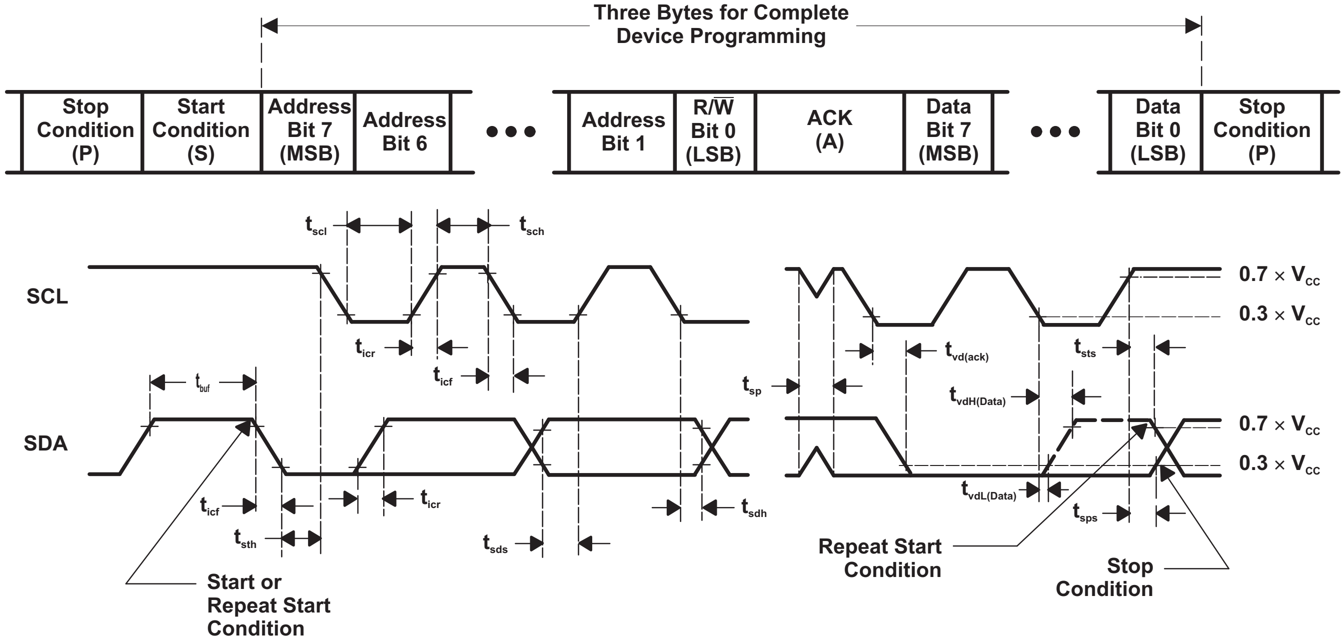


Figure 4. ON-Resistance (R_{ON}) vs Supply Voltage (V_{CC}) at Three Temperatures

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

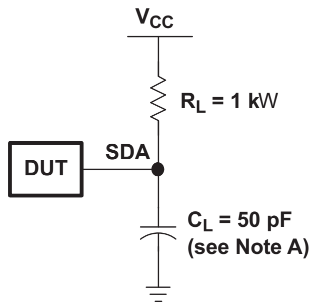
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

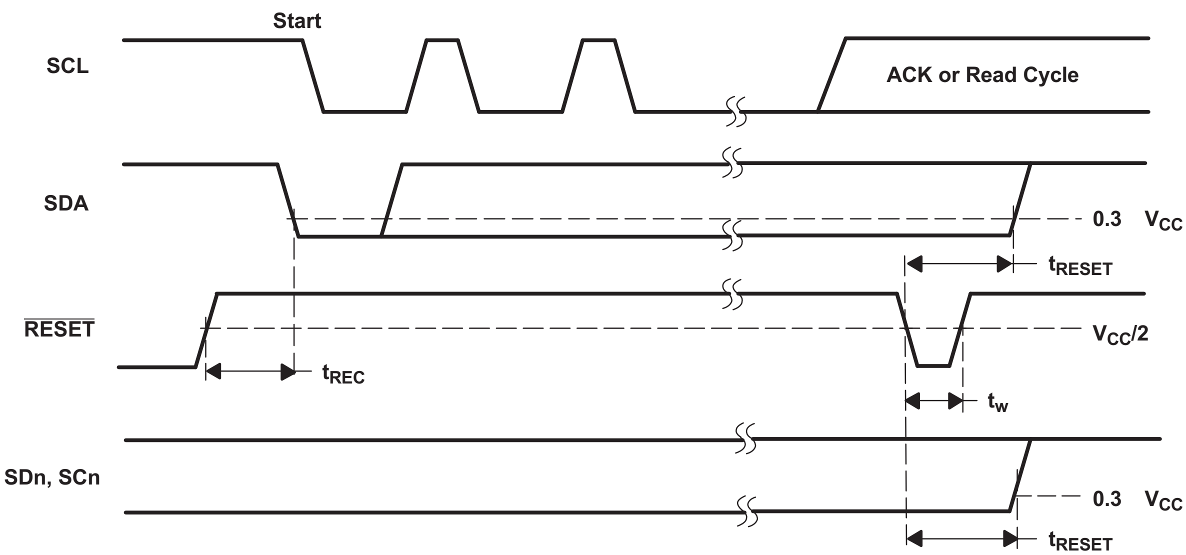
C. Not all parameters and waveforms are applicable to all devices.

Figure 5. I^2C Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



SDA LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. I/Os are configured as inputs.

D. Not all parameters and waveforms are applicable to all devices.

Figure 6. Reset Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

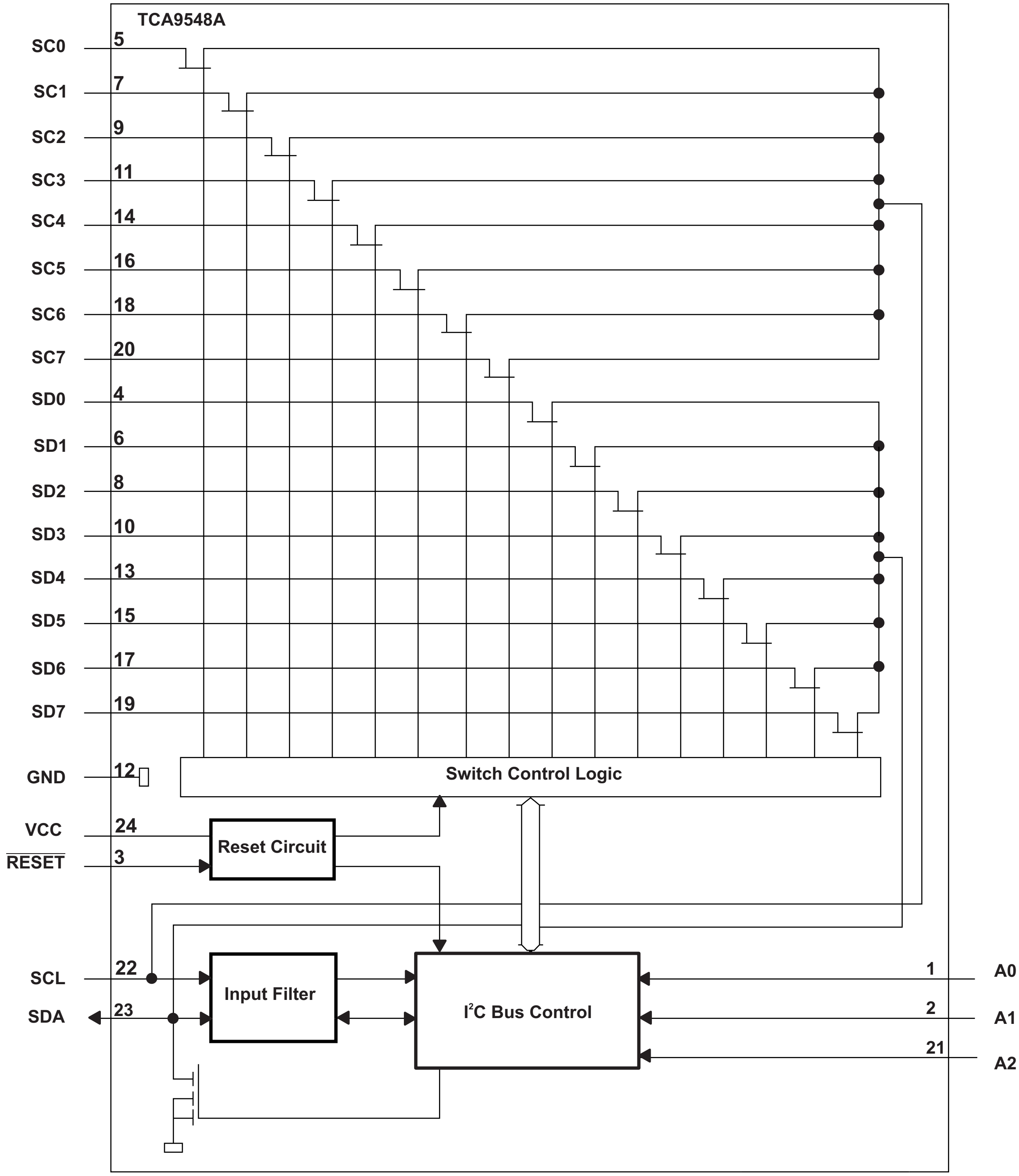
The TCA9548A is an 8-channel, bidirectional translating I^2C switch. The master SCL/SDA signal pair is directed to eight channels of slave devices, SC0/SD0-SC7/SD7. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the TCA9548A to recover should one of the downstream I^2C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Both the $\overline{RESET}$ function and a POR will cause all channels to be deselected.

The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0, A1, and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The TCA9548A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

8.2 Functional Block Diagram



8.3 Feature Description

The TCA9548A is an 8-channel, bidirectional translating switch for I^{2}C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9548A features I^{2}C control using a single 8-bit control register in which each bit controls the enabling and disabling of one of the corresponding 8 switch channels for I^{2}C data flow. Depending on the application, voltage translation of the I^{2}C bus can also be achieved using the TCA9548A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^{2}C bus enters a fault state, the TCA9548A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL}, the TCA9548A resets its registers and I^{2}C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

8.4.2 Power-On Reset

When power is applied to the VCC pin, an internal power-on reset holds the TCA9548A in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released, and the TCA9548A registers and I^{2}C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{PORF} to reset the device.

8.5 Programming

8.5.1 I^{2}C Interface

The TCA9548A has a standard bidirectional I^{2}C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^{2}C bus has a specific device address to differentiate between other slave devices that are on the same I^{2}C bus. Many slave devices will require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical I^{2}C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^{2}C lines. (For further details, refer to *I^{2}C Pull-up Resistor Calculation* (SLVA689).) Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

The following is the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   – Master-transmitter sends a START condition and addresses the slave-receiver.
   – Master-transmitter sends data to slave-receiver.
   – Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   – Master-receiver sends a START condition and addresses the slave-transmitter.
   – Master-receiver sends the requested register to read to slave-transmitter.
   – Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

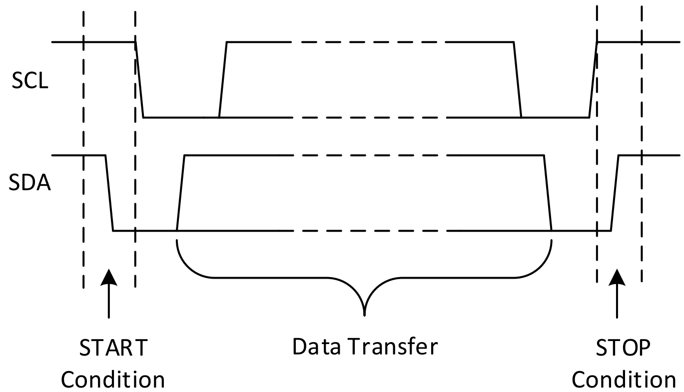


Figure 7. Definition of Start and Stop Conditions

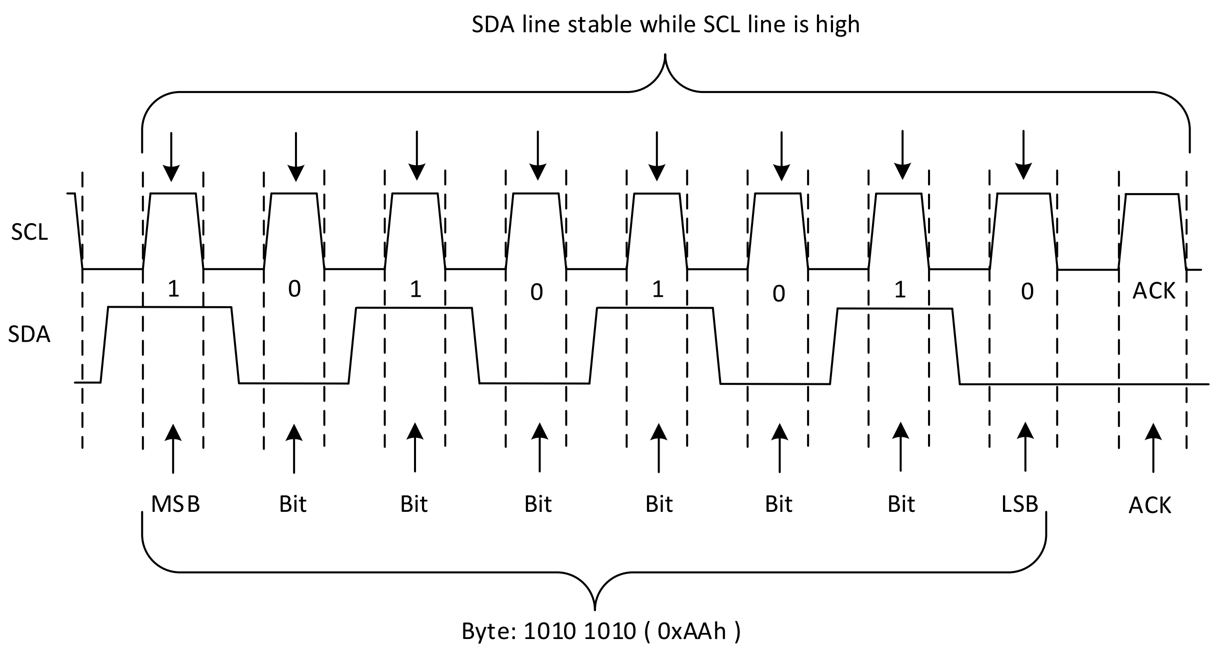


Figure 8. Bit Transfer

8.5.2 Device Address

Figure 9 shows the address byte of the TCA9548A.

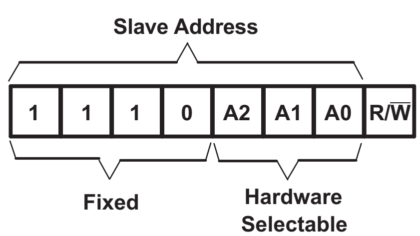


Figure 9. TCA9548A Address

Programming (continued)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Table 1. Address Reference

INPUTS			I2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

8.5.3 Bus Transactions

Data must be sent to and received from the slave devices, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

While it is common to have registers in I^{2}C slaves, note that not all slave devices will have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the slave address, instead of addressing a register. The TCA9548A is example of a single-register device, which is controlled via I^{2}C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the master merely writes the register data after the slave address, skipping the register number.

8.5.3.1 Writes

To write on the I^{2}C bus, the master will send a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. The slave will acknowledge, letting the master know it is ready. After this, the master will start sending the control register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master will terminate the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what will be in the register.

Figure 10 shows an example of writing a single byte to a slave register.

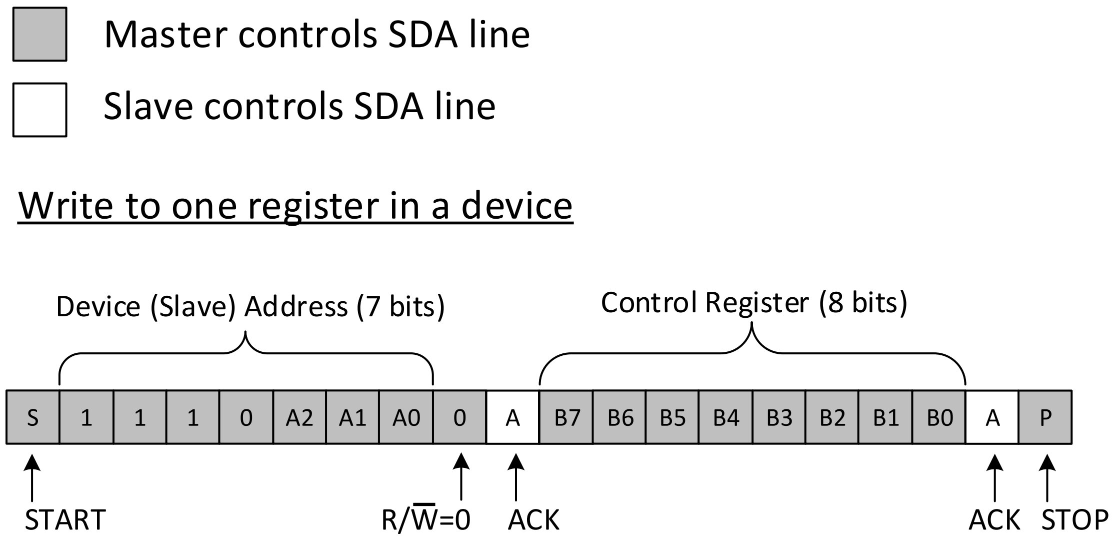


Figure 10. Write to Register

8.5.3.2 *Reads*

Reading from a slave is very similar to writing, but the master will send a START condition, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). The slave will acknowledge the read request, and the master will release the SDA bus but will continue supplying the clock to the slave. During this part of the transaction, the master will become the master-receiver, and the slave will become the slave-transmitter.

The master will continue to send out the clock pulses, but will release the SDA line so that the slave can transmit data. At the end of every byte of data, the master will send an ACK to the slave, letting the slave know that it is ready for more data. Once the master has received the number of bytes it is expecting, it will send a NACK, signaling to the slave to halt communications and release the bus. The master will follow this up with a STOP condition.

Figure 11 shows an example of reading a single byte from a slave register.

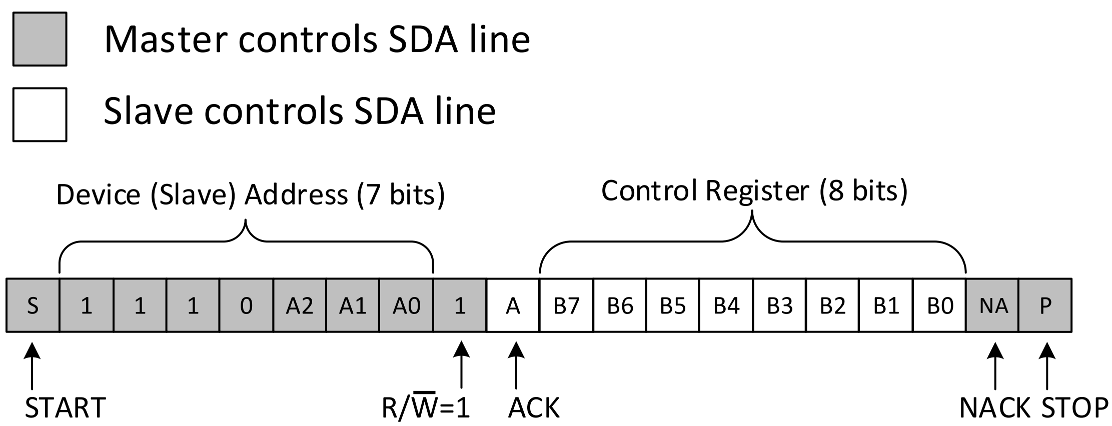


Figure 11. Read from Control Register

8.5.4 Control Register

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9548A (see Figure 12). This register can be written and read via the I^2C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the TCA9548A, it saves the last byte received.

Channel Selection Bits (Read/Write)

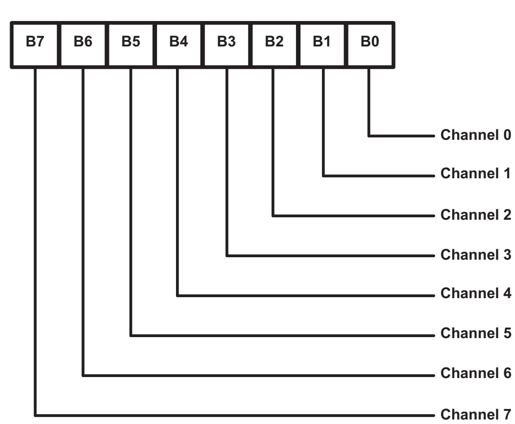


Figure 12. Control Register

Table 2. Command Byte Definition

CONTROL REGISTER BITS								COMMAND
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

8.5.5 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL}, the TCA9548A resets its registers and I^2C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

8.5.6 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA9548A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the TCA9548A registers and I^2C state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{POR} and then back up to the operating voltage for a power-reset cycle.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

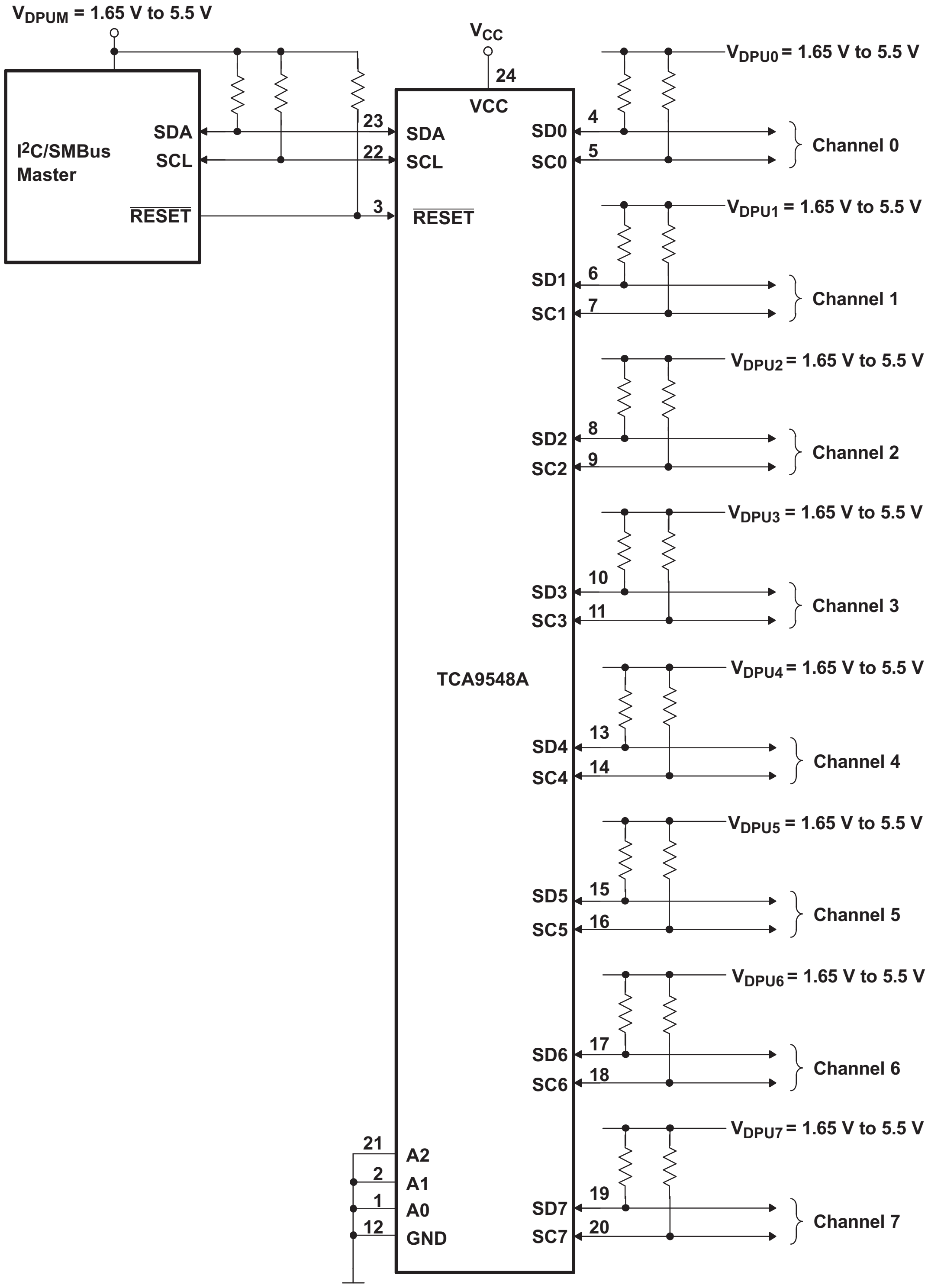
Applications of the TCA9548A will contain an I^2C (or SMBus) master device and up to eight I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (see *Design Requirements* and *Detailed Design Procedure*).

9.2 Typical Application

Figure 13 shows an application in which the TCA9548A can be used.

Typical Application (continued)



A. Pin numbers shown are for the PW package.

Figure 13. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

A typical application of the TCA9548A will contain one or more data pull-up voltages, V_{DPUX}, one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU7}). In the event where the master device and all slave devices operate at the same voltage, then V_{DPUM} = V_{DPUX} = VCC. In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate V_{CC} voltage.

The A0, A1, and A2 pins are hardware selectable to control the slave address of the TCA9548A. These pins may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the TCA9548A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 14 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in *Electrical Characteristics*). In order for the TCA9548A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 14, $V_{pass(max)}$ is 2.7 V when the TCA9548A supply voltage is 4 V or lower, so the TCA9548A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 13).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \qquad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \qquad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9548A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

Typical Application (continued)

9.2.3 Application Curves

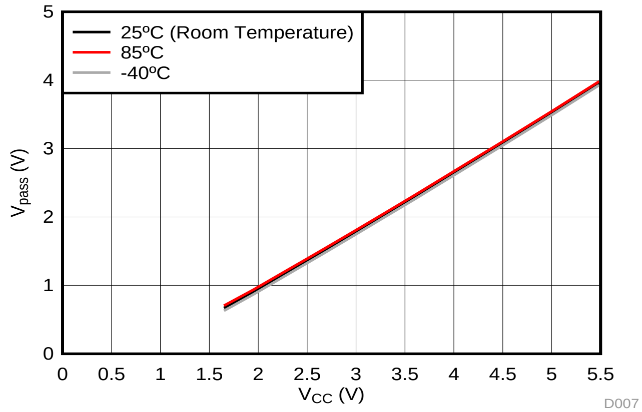
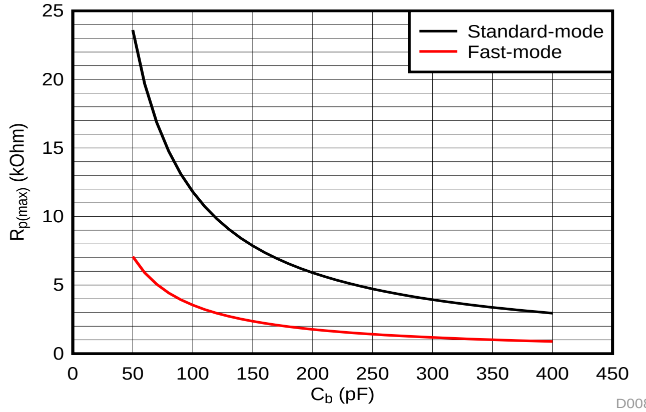


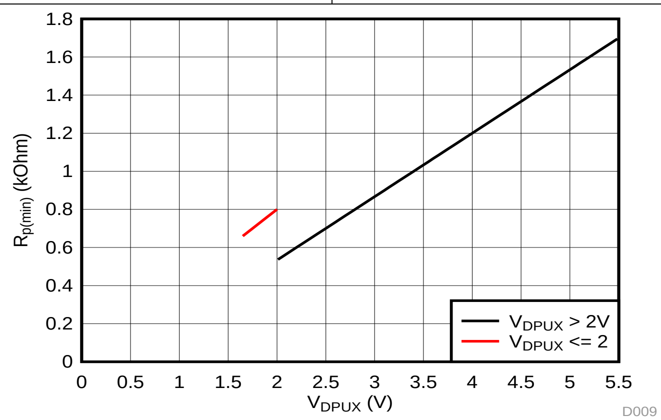
Figure 14. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 15. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 16. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

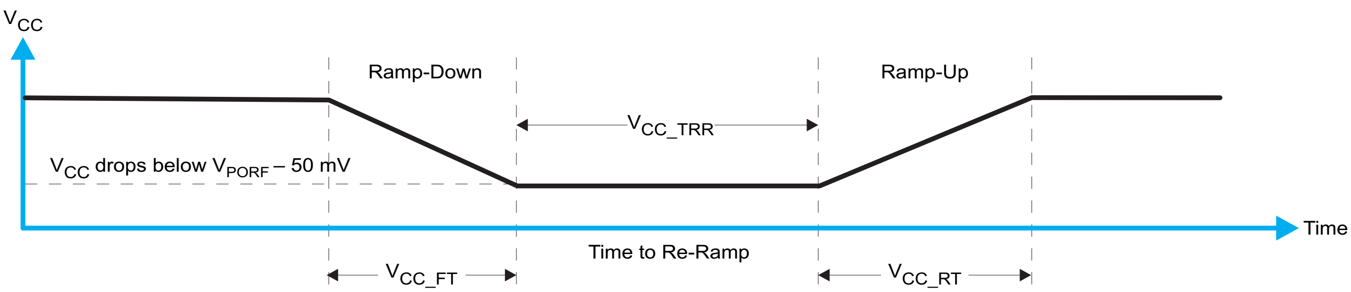
10 Power Supply Recommendations

The operating power-supply voltage range of the TCA9548A is 1.65 V to 5.5 V applied at the VCC pin. When the TCA9548A is powered on for the first time or anytime the device must be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I^2C bus logic is initialized properly.

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9548A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 17.



V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Figure 17. Power-On Reset Waveform

Table 3 specifies the performance of the power-on reset feature for TCA9548A for both types of power-on reset.

Table 3. Recommended Supply Sequencing and Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall time	See Figure 17	1		100	ms
V_{CC_RT}	Rise time	See Figure 17	0.1		100	ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops below $V_{PORF(min)}$ – 50 mV or when V_{CC} drops to GND)	See Figure 17	40			μs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 μs	See Figure 18			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CC\_GH} = 0.5 \times V_{CC}$	See Figure 18			10	μs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 18 and Table 3 provide more information on how to measure these specifications.

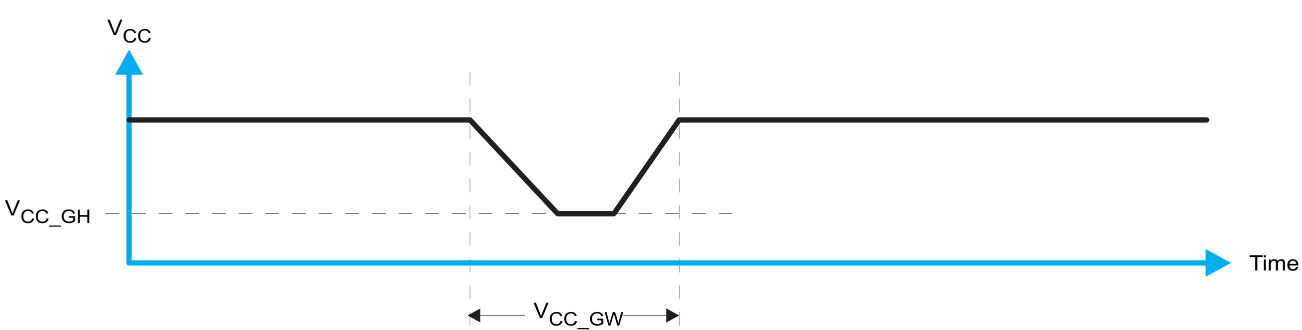


Figure 18. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 19 and Table 3 provide more details on this specification.

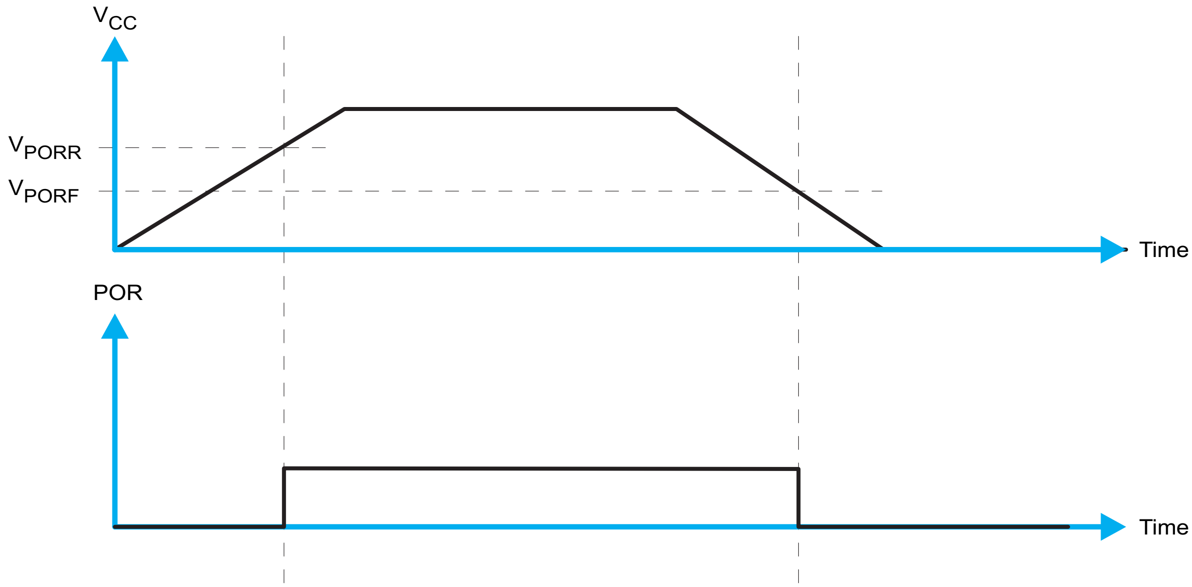


Figure 19. V_{POR}

11 Layout

11.1 Layout Guidelines

For PCB layout of the TCA9548A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM} and V_{DPU0}-V_{DPU7}, may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn and SDn) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example

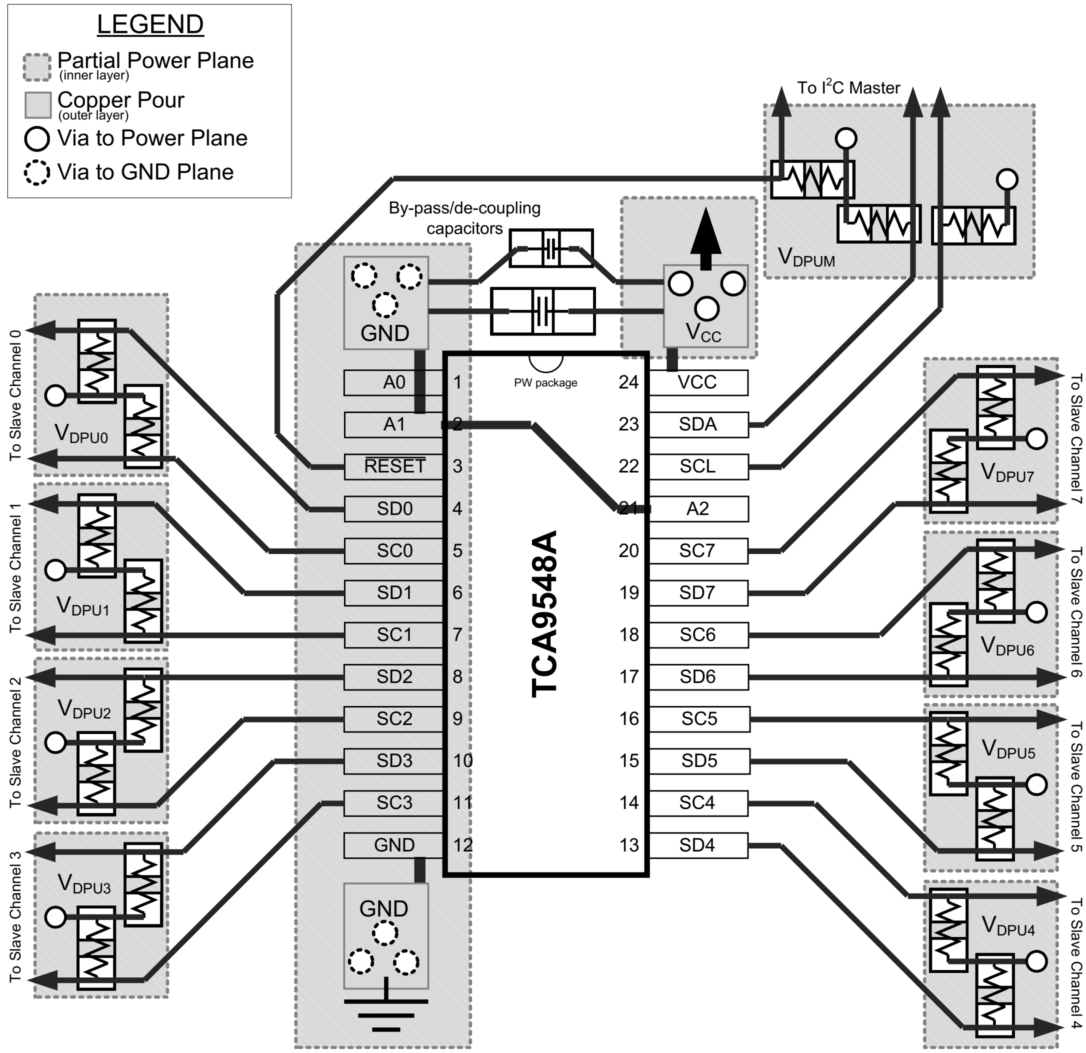


Figure 20. Layout Schematic

12 器件和文档支持

12.1 社区资源

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9548AMRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A	Samples
TCA9548APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW548A	Samples
TCA9548ARGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW548A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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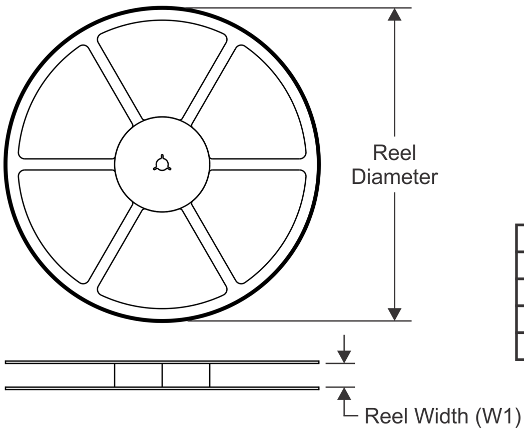
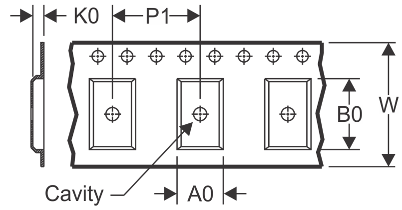
TAPE AND REEL INFORMATION

REEL DIMENSIONS

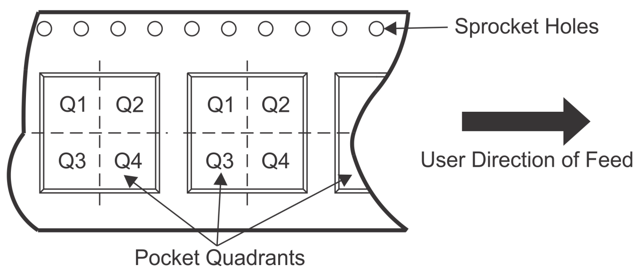


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

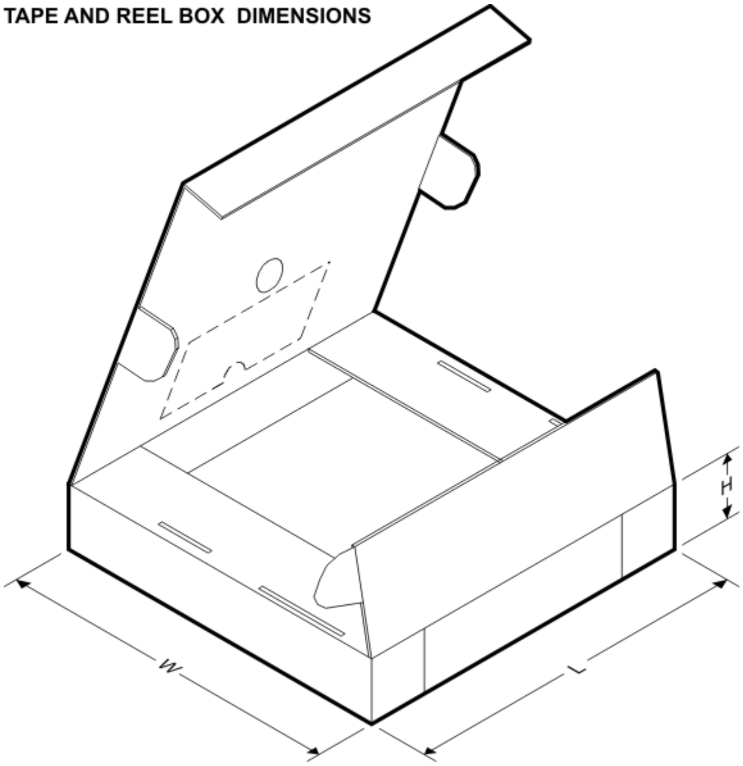
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9548AMRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1
TCA9548APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9548ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

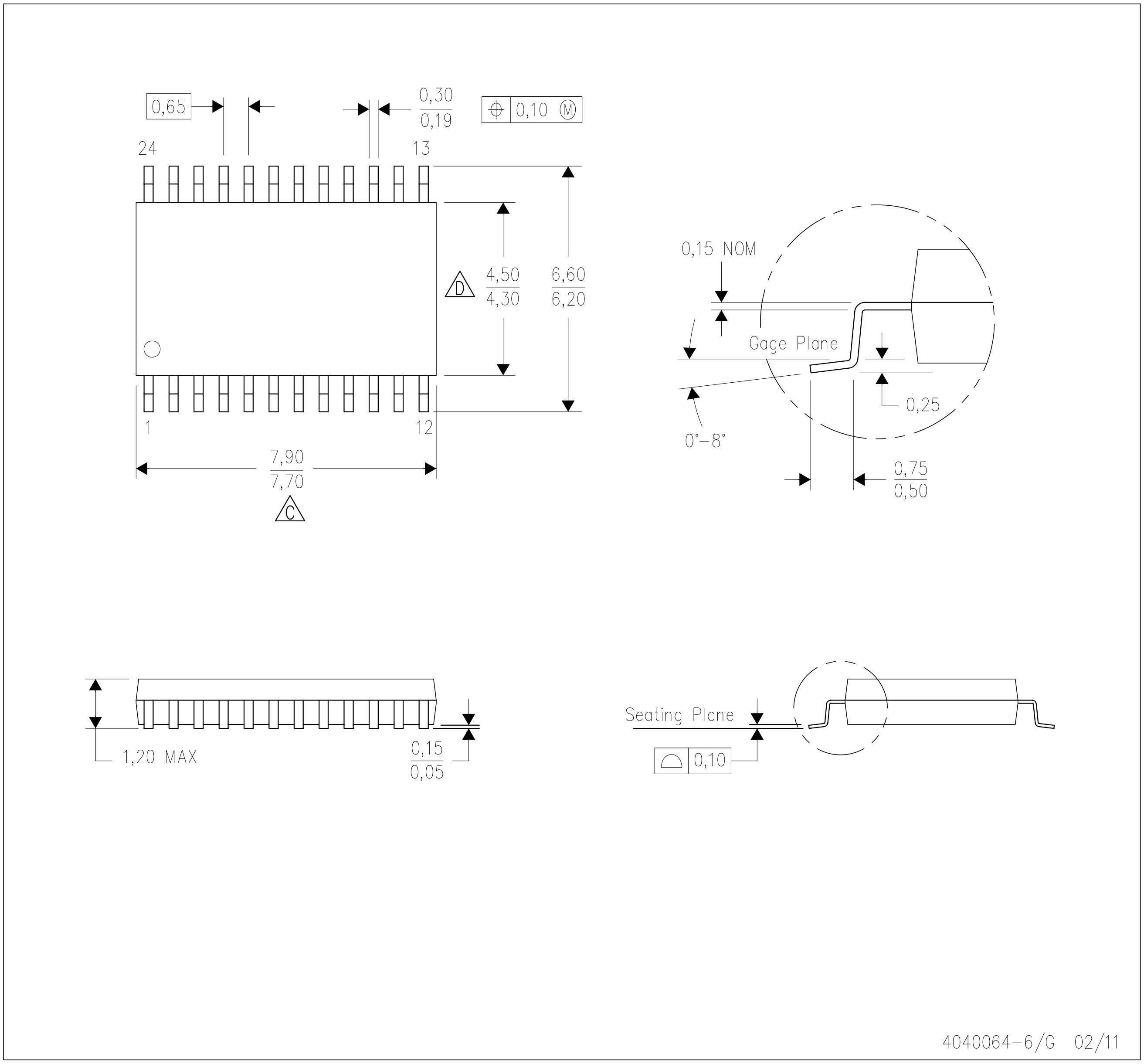
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

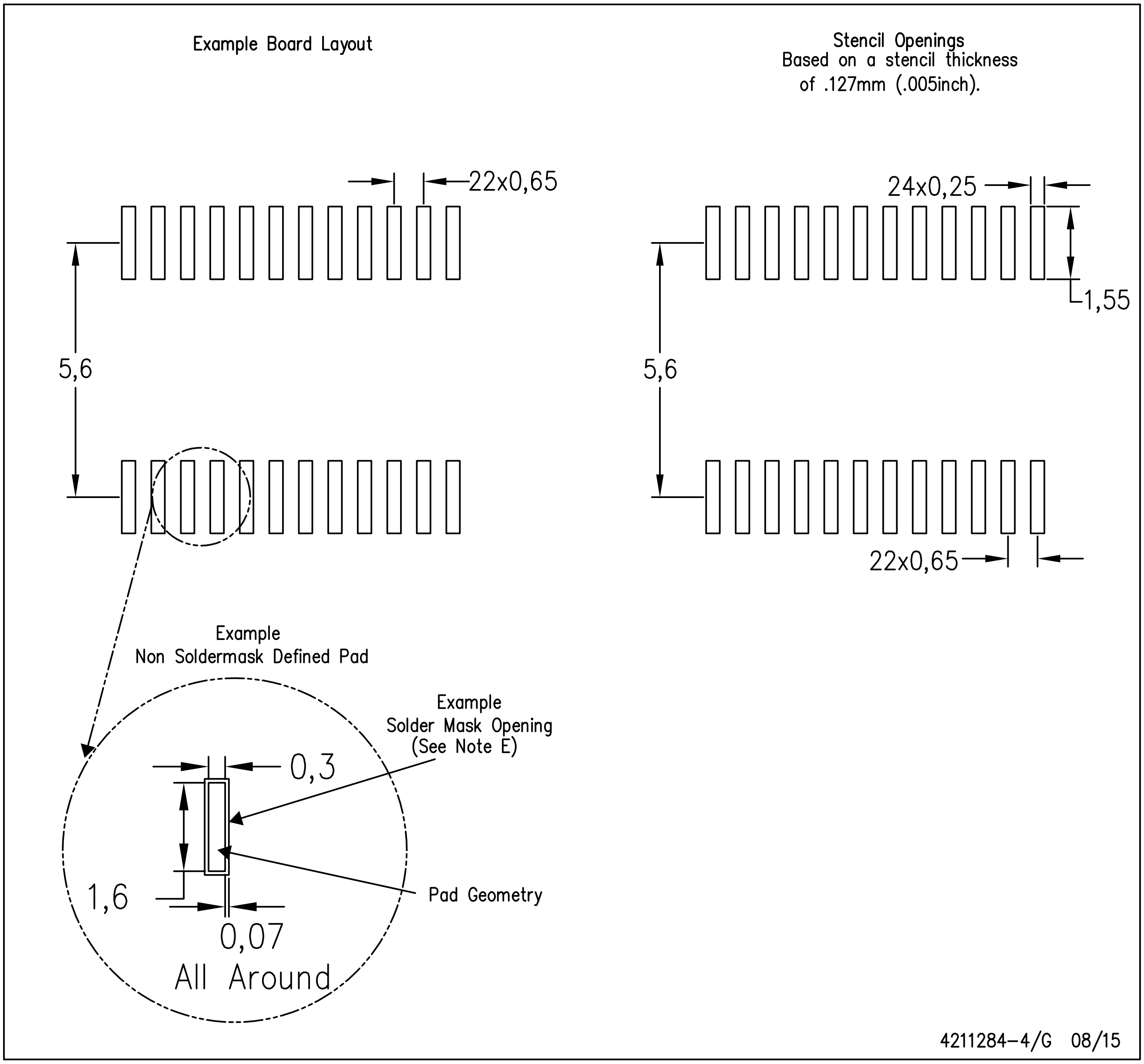
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9548AMRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TCA9548APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
TCA9548ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

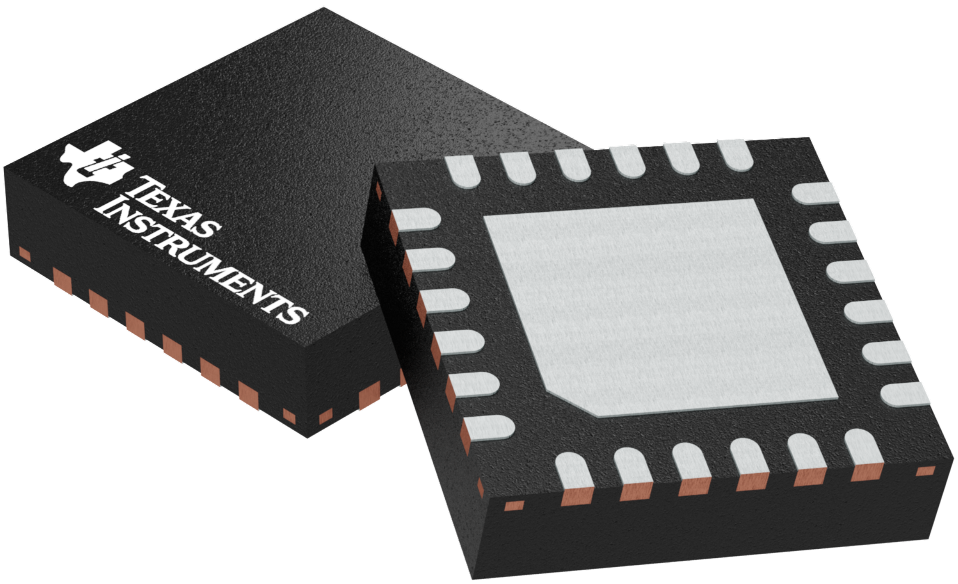
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

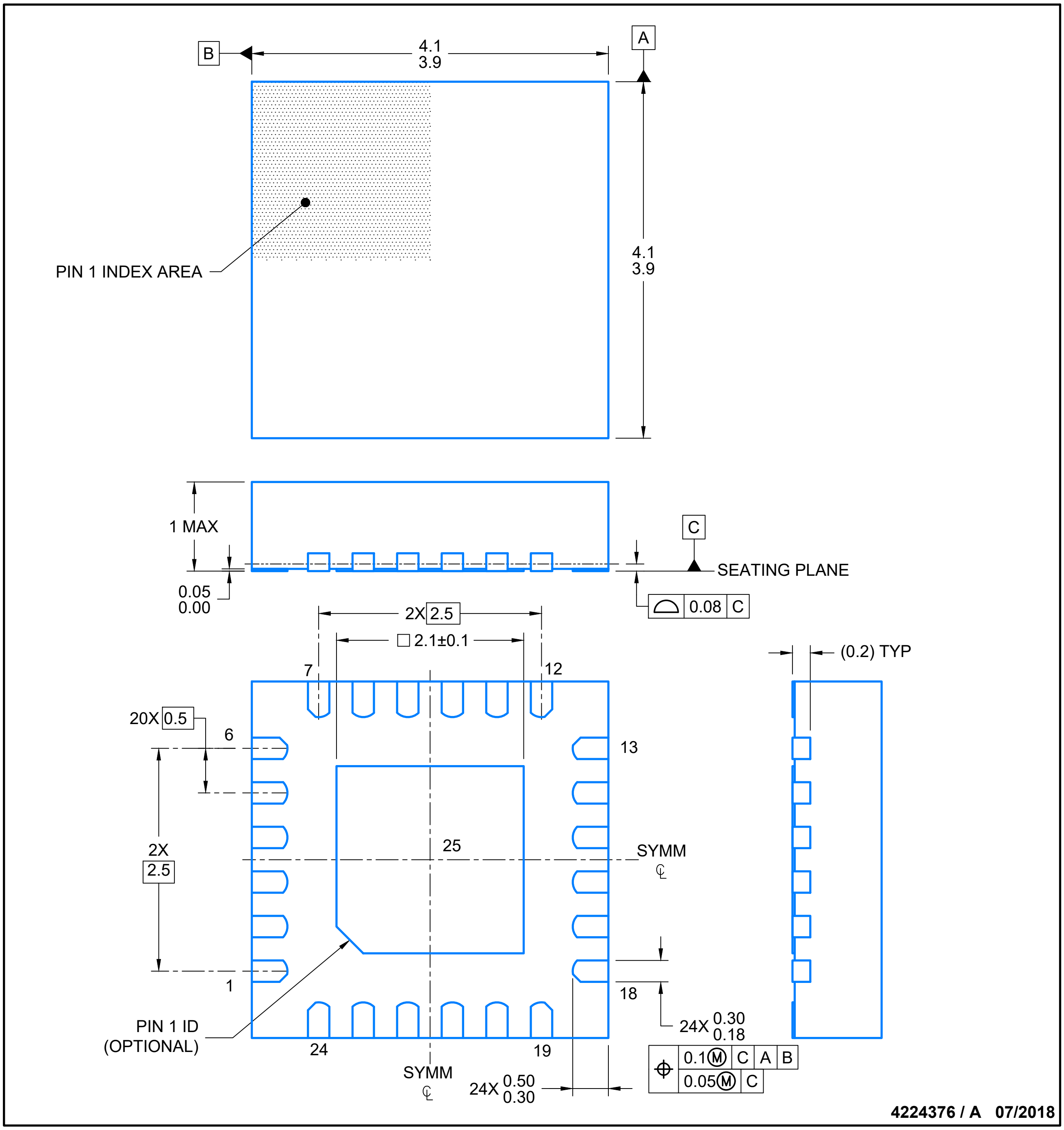
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



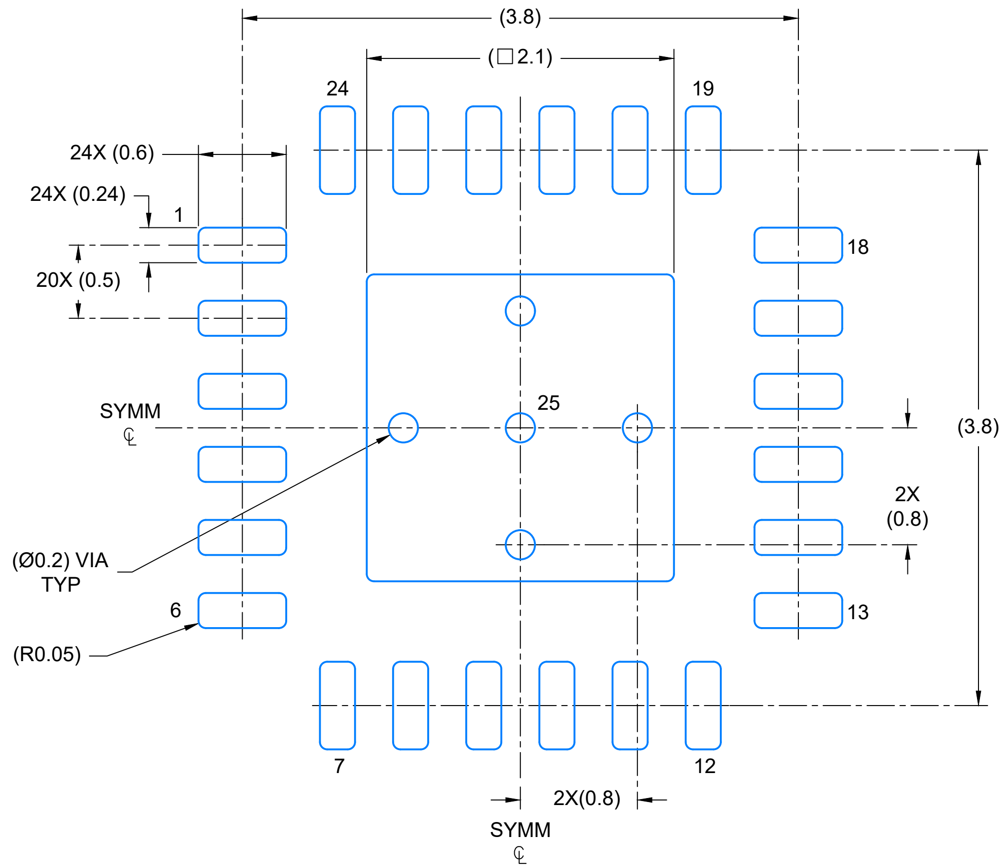
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

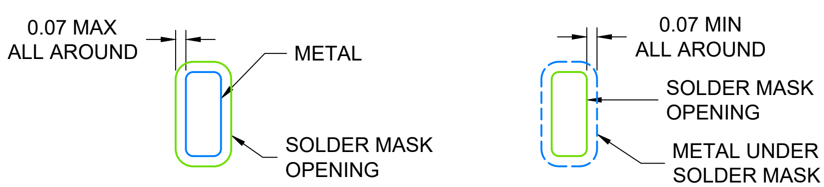


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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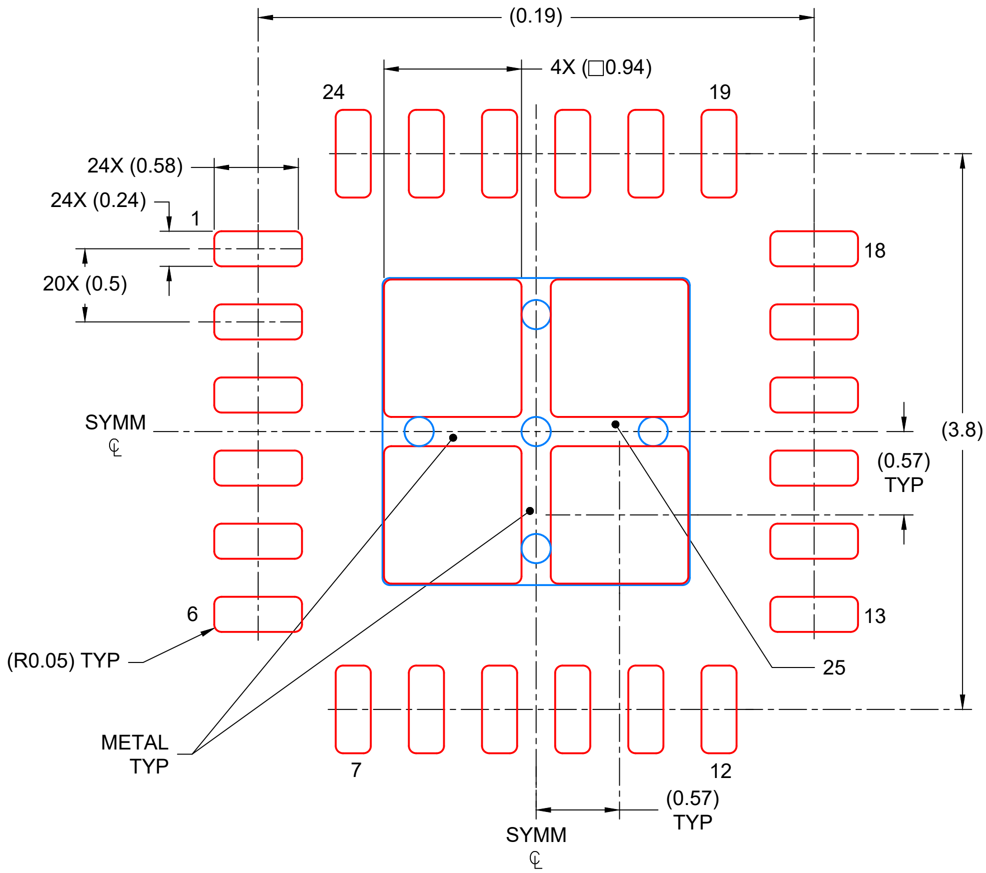
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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