交通灯状态机程序：

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.ALL;

USE IEEE.std\_logic\_arith.ALL;

ENTITY traffic\_light\_dianlian IS

PORT(clk:IN std\_logic;

reset:IN std\_logic;

rl,gl,yl:OUT std\_logic;

counter\_time:OUT std\_logic\_vector(3 DOWNTO 0));

END ENTITY;

ARCHITECTURE nan OF traffic\_light\_dianlian\_32 IS

SIGNAL mtime:integer RANGE 0 TO 9;

BEGIN

PROCESS(clk,reset)

TYPE state\_type IS(R,G,Y);

VARIABLE state:state\_type;

BEGIN

IF reset='1'

THEN state:=R;

rl<='1';

gl<='0';

yl<='0';

mtime<=9;

counter\_time<=conv\_std\_logic\_vector(mtime,4);

ELSIF clk'event and clk='1' THEN

CASE state IS

WHEN R=>rl<='1';gl<='0'; yl<='0';

mtime<=mtime-1;

counter\_time<=conv\_std\_logic\_vector(mtime,4);

IF(mtime=1)THEN state:=G; mtime<=6;

ELSE state:=R;

END IF;

WHEN G=>gl<='1'; rl<='0';yl<='0';

mtime<=mtime-1;

counter\_time<=conv\_std\_logic\_vector(mtime,4);

IF(mtime=1)THEN state:=Y; mtime<=3;

ELSE state:=G;

END IF;

WHEN Y=>yl<='1'; gl<='0'; rl<='0';

mtime<=mtime-1;

counter\_time<=conv\_std\_logic\_vector(mtime,4);

IF(mtime=1)THEN state:=R; mtime<=9;

ELSE state:=Y;

END IF;

END CASE;

END IF;

END PROCESS;

END nan;

数码管显示：

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.ALL;

ENTITY led IS

PORT(counter\_time:IN std\_logic\_vector(3 DOWNTO 0);

EN:IN std\_logic;

seven\_seg\_input:OUT std\_logic\_vector(7 DOWNTO 0));

END led;

ARCHITECTURE led\_arch OF led IS

SIGNAL counter\_time\_input:std\_logic\_vector(4 DOWNTO 0);

SIGNAL seven\_seg\_input\_reg:std\_logic\_vector(7 DOWNTO 0);

BEGIN

counter\_time\_input<=EN&counter\_time;

display:PROCESS(counter\_time\_input,seven\_seg\_input\_reg)

BEGIN

CASE counter\_time\_input IS

WHEN"00000"=>seven\_seg\_input\_reg<="00000010";

WHEN"00001"=>seven\_seg\_input\_reg<="10011110";

WHEN"00010"=>seven\_seg\_input\_reg<="00100100";

WHEN"00011"=>seven\_seg\_input\_reg<="00001100";

WHEN"00100"=>seven\_seg\_input\_reg<="10011000";

WHEN"00101"=>seven\_seg\_input\_reg<="01001000";

WHEN"00110"=>seven\_seg\_input\_reg<="01000000";

WHEN"00111"=>seven\_seg\_input\_reg<="00011110";

WHEN"01000"=>seven\_seg\_input\_reg<="00000000";

WHEN"01001"=>seven\_seg\_input\_reg<="00001000";

WHEN OTHERS=>seven\_seg\_input\_reg<="11111111";

END CASE;

seven\_seg\_input<=seven\_seg\_input\_reg;

END PROCESS;

END led\_arch;

分频器：

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.ALL;

ENTITY frequencies IS

PORT(clk:IN std\_logic;

q:OUT std\_logic);

END frequencies;

ARCHITECTURE behav OF frequencies IS

BEGIN

PROCESS(clk)

VARIABLE time:integer RANGE 0 TO 50000000;

BEGIN

IF rising\_edge(clk) THEN

time:=time+1;

IF time<=25000000 THEN

q<='1';

ELSE IF time<50000000 THEN

q<='0';

else

time:=0;

END IF;

END IF;

END IF;

END PROCESS;

END BEHAV;