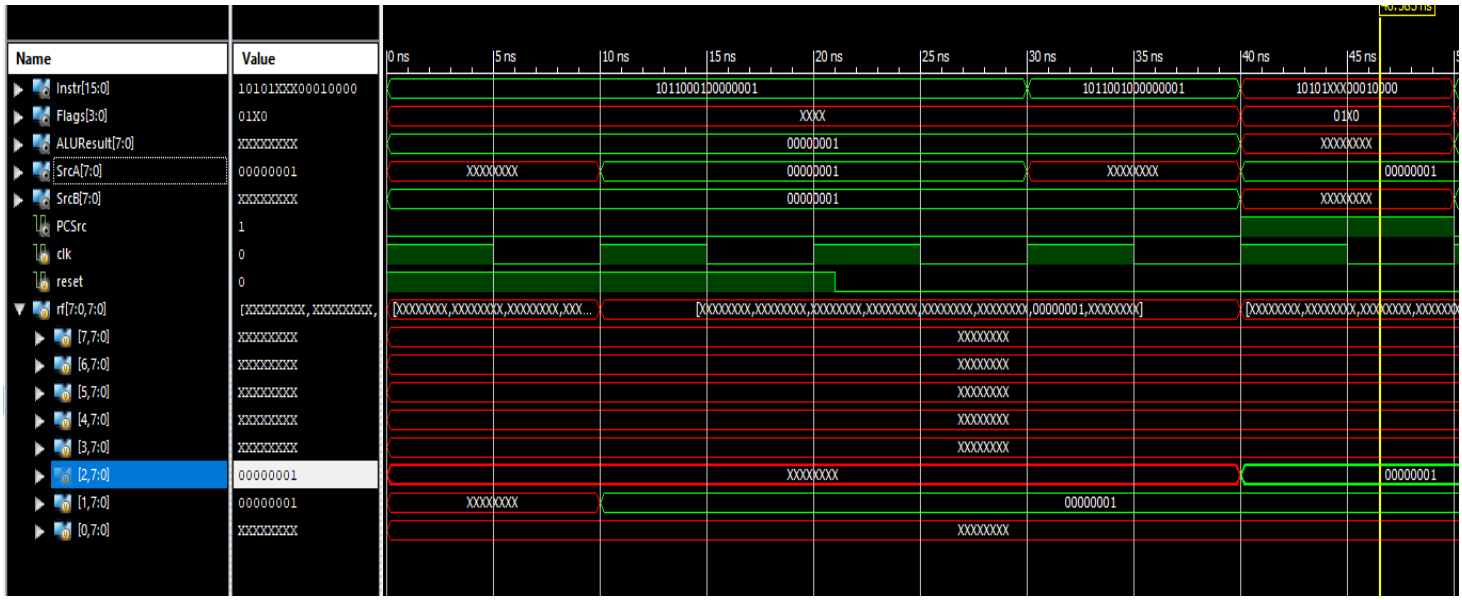
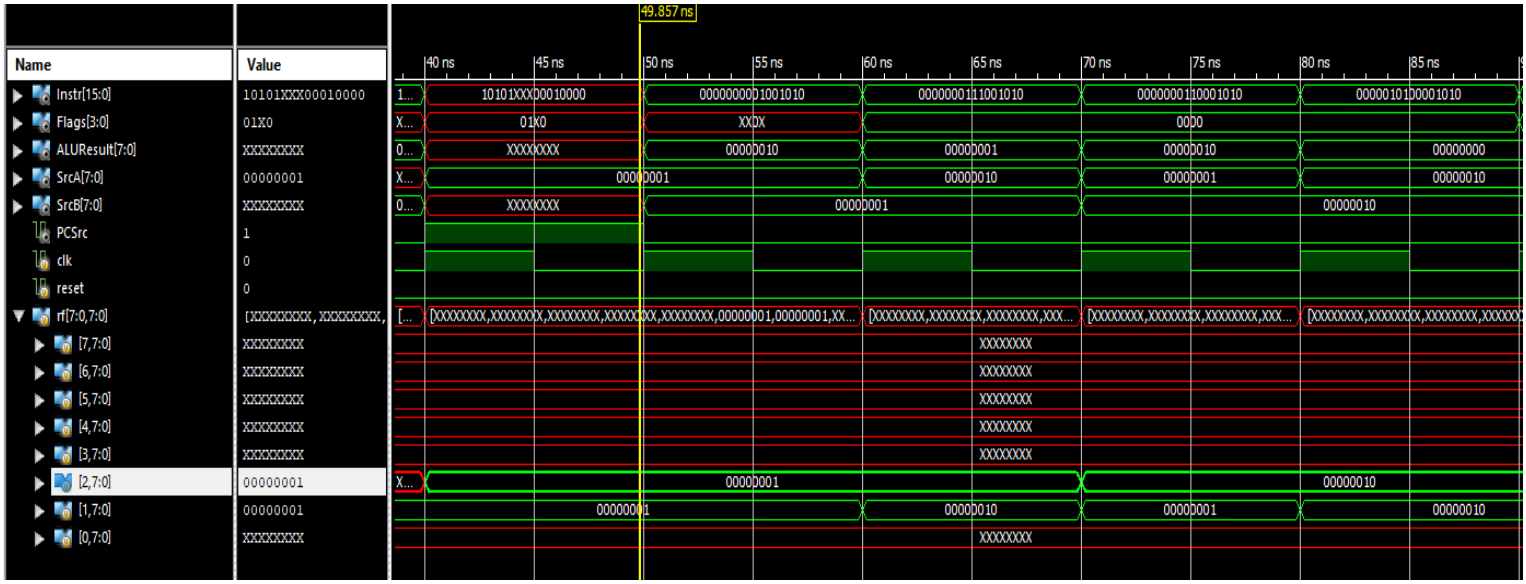
آزمایش شماره ۴ CPU

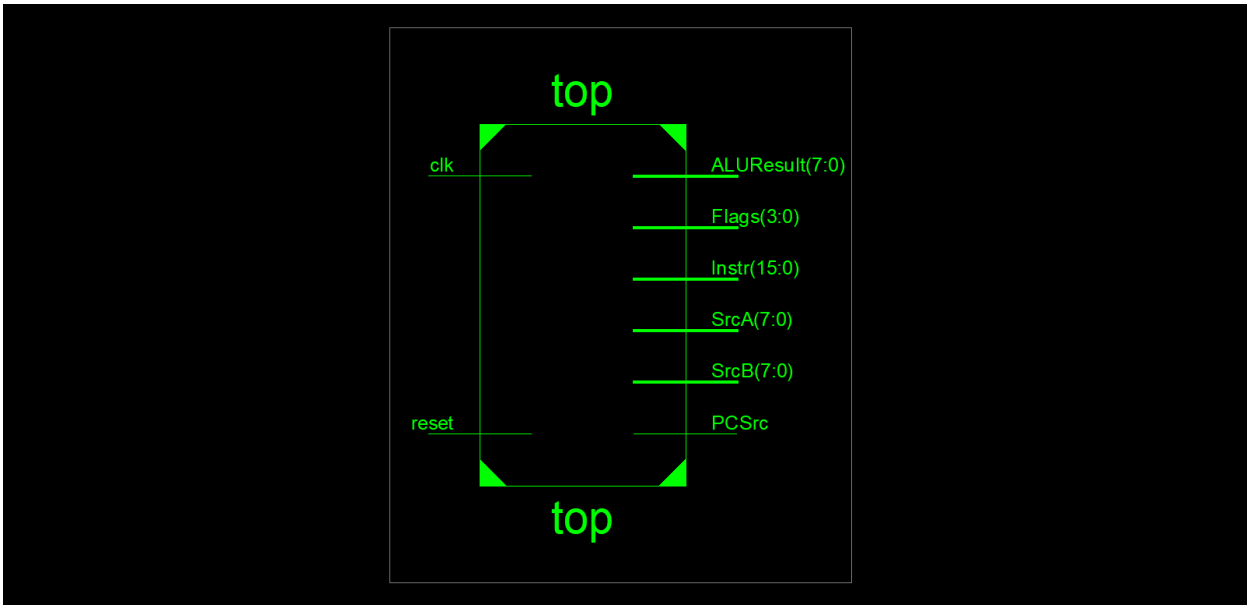
پارسا فدایی خدمت و درین رستمی گروه۲

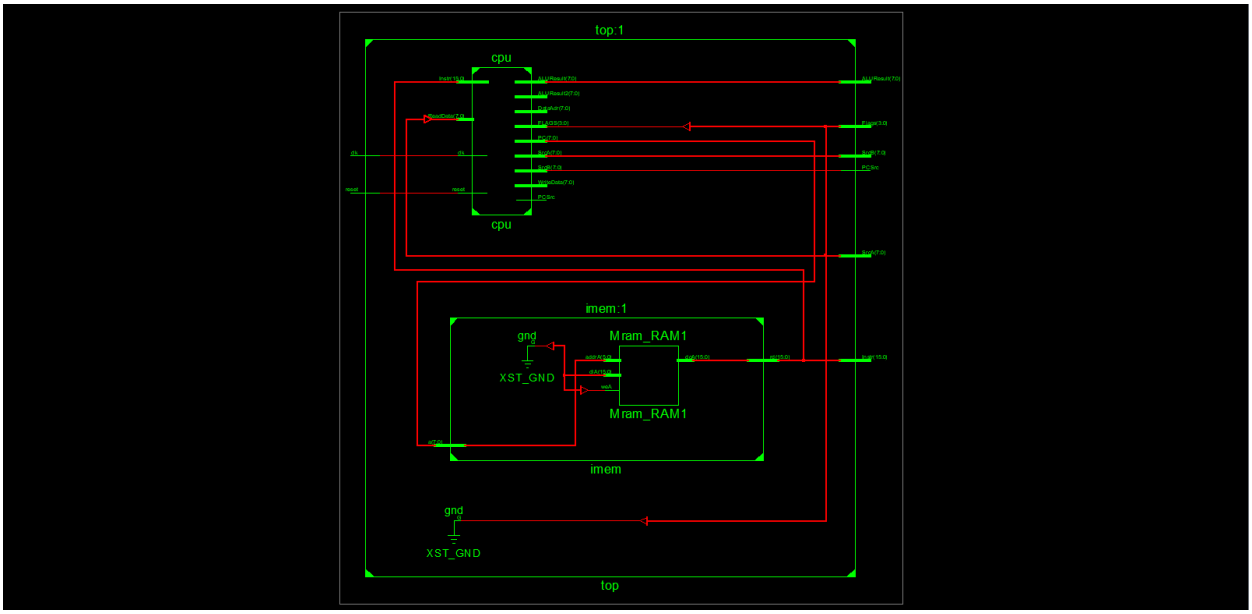
نتیجه ی شبیه سازی :

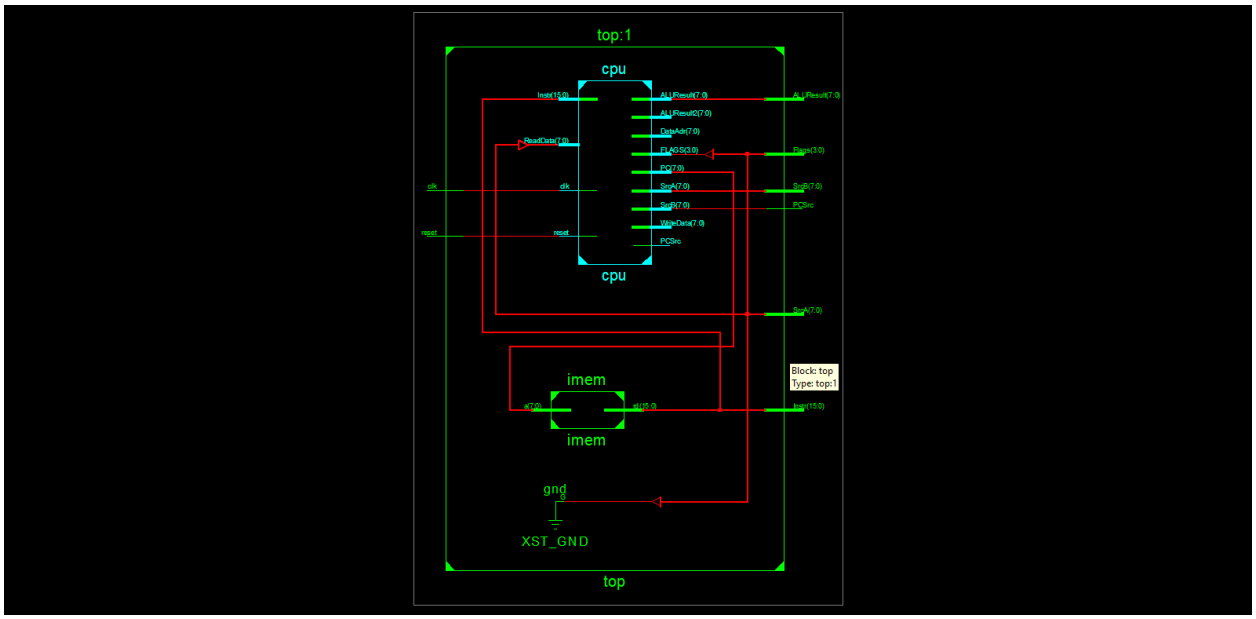


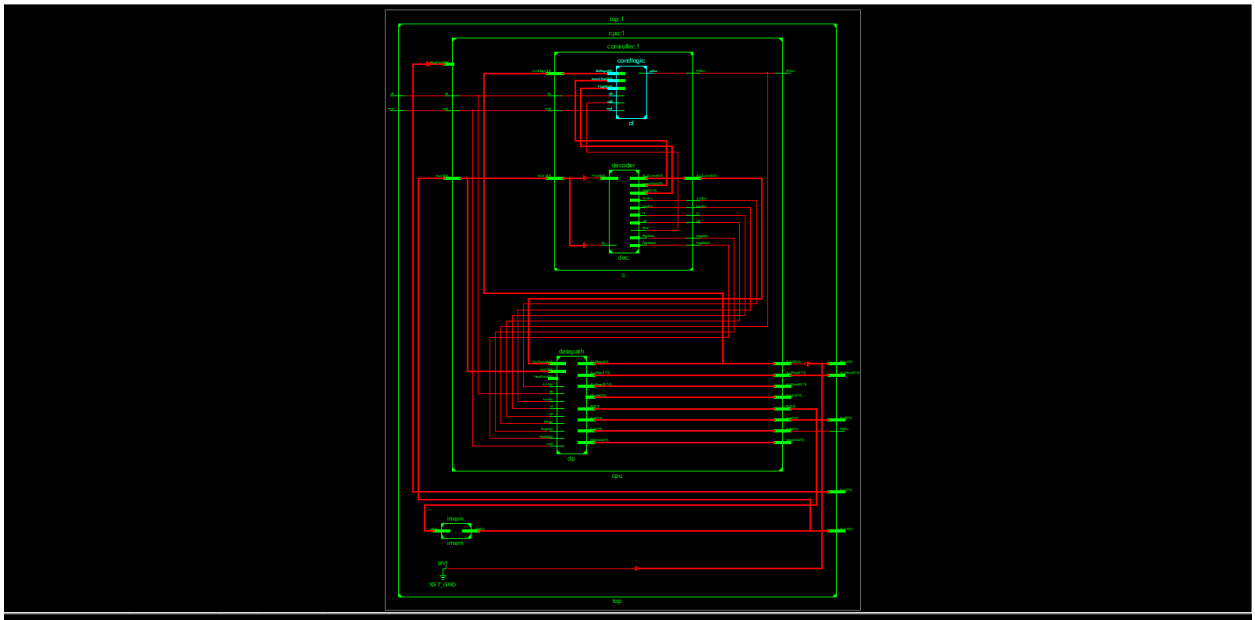


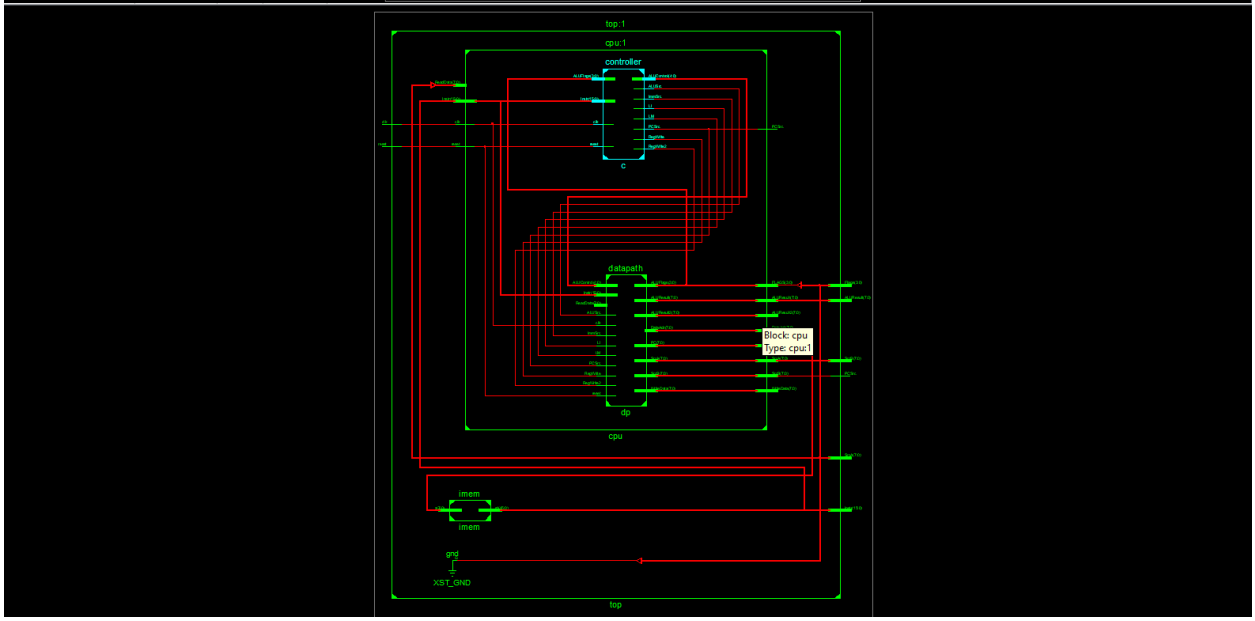
RTL SCHEMATIC:

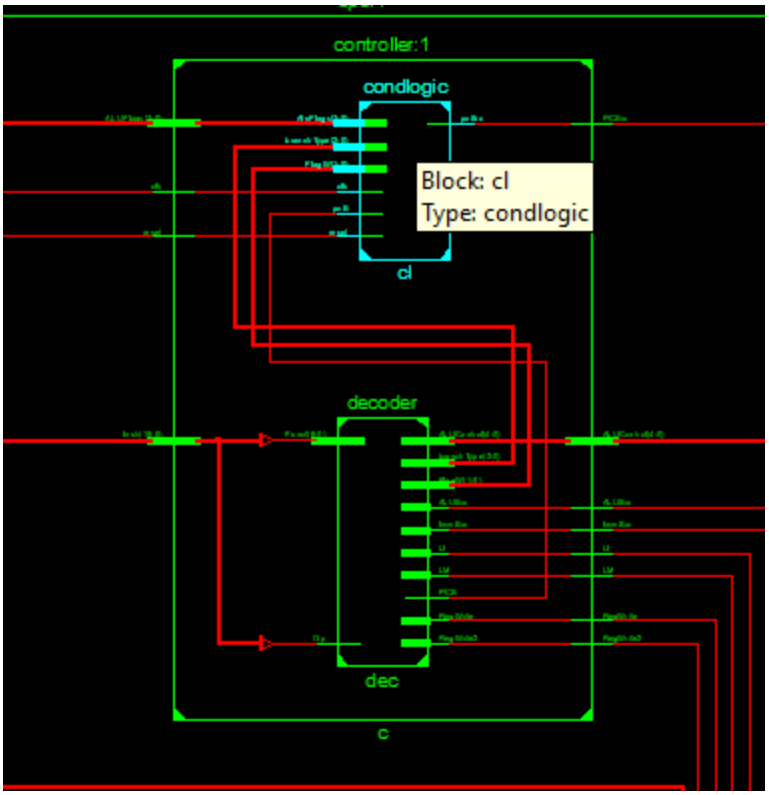


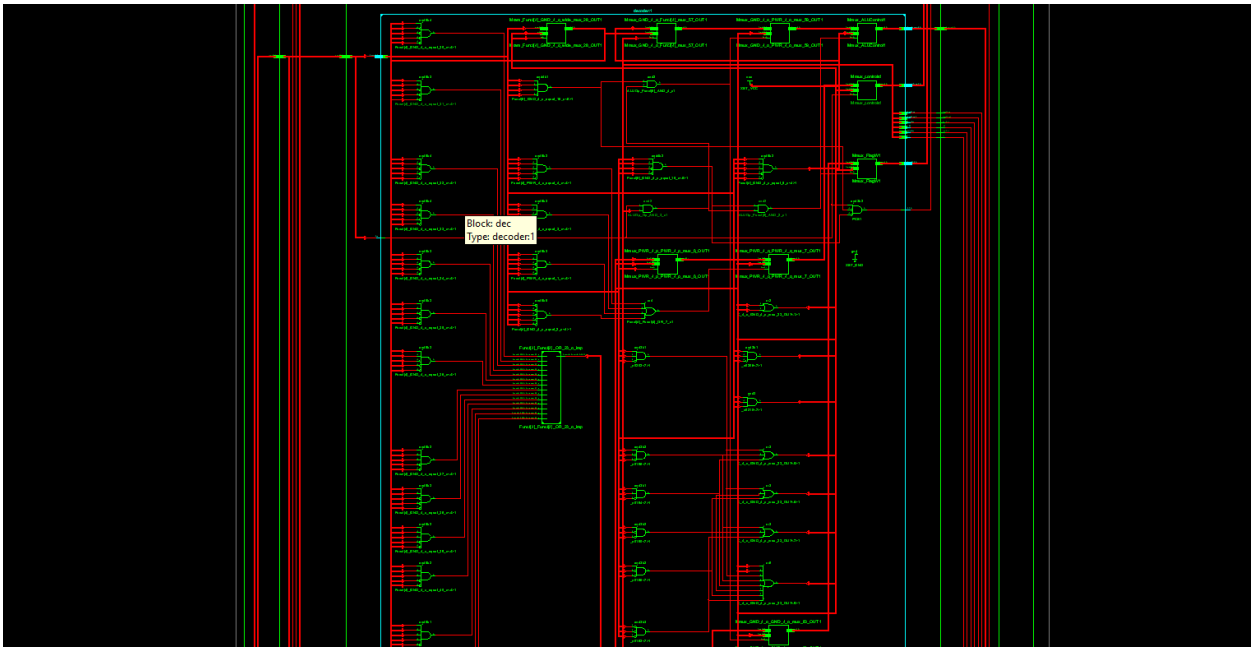

top:1
cpu
cpu
imem:1
gnd
XST_GND
Mram_RAM1
Mram_RAM1
imem
gnd
XST_GND
top

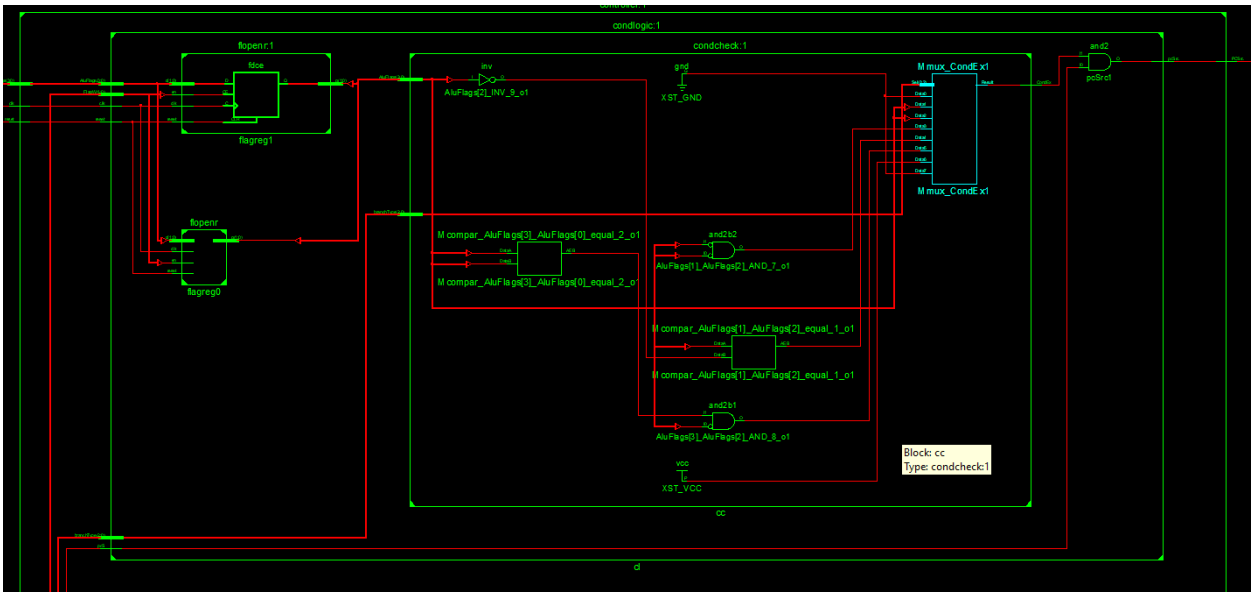

top:1
cpu
Inst(15:0)
ALUResult(7:0)
ALUResult2(7:0)
DataAdr(7:0)
FLAGS(3:0)
PC(7:0)
SrcA(7:0)
SrcB(7:0)
WriteData(7:0)
PCSrc
ReadData(7:0)
clk
reset
cpu
imem
imem
gnd
XST_GND
top
Block: top
Type: top:1

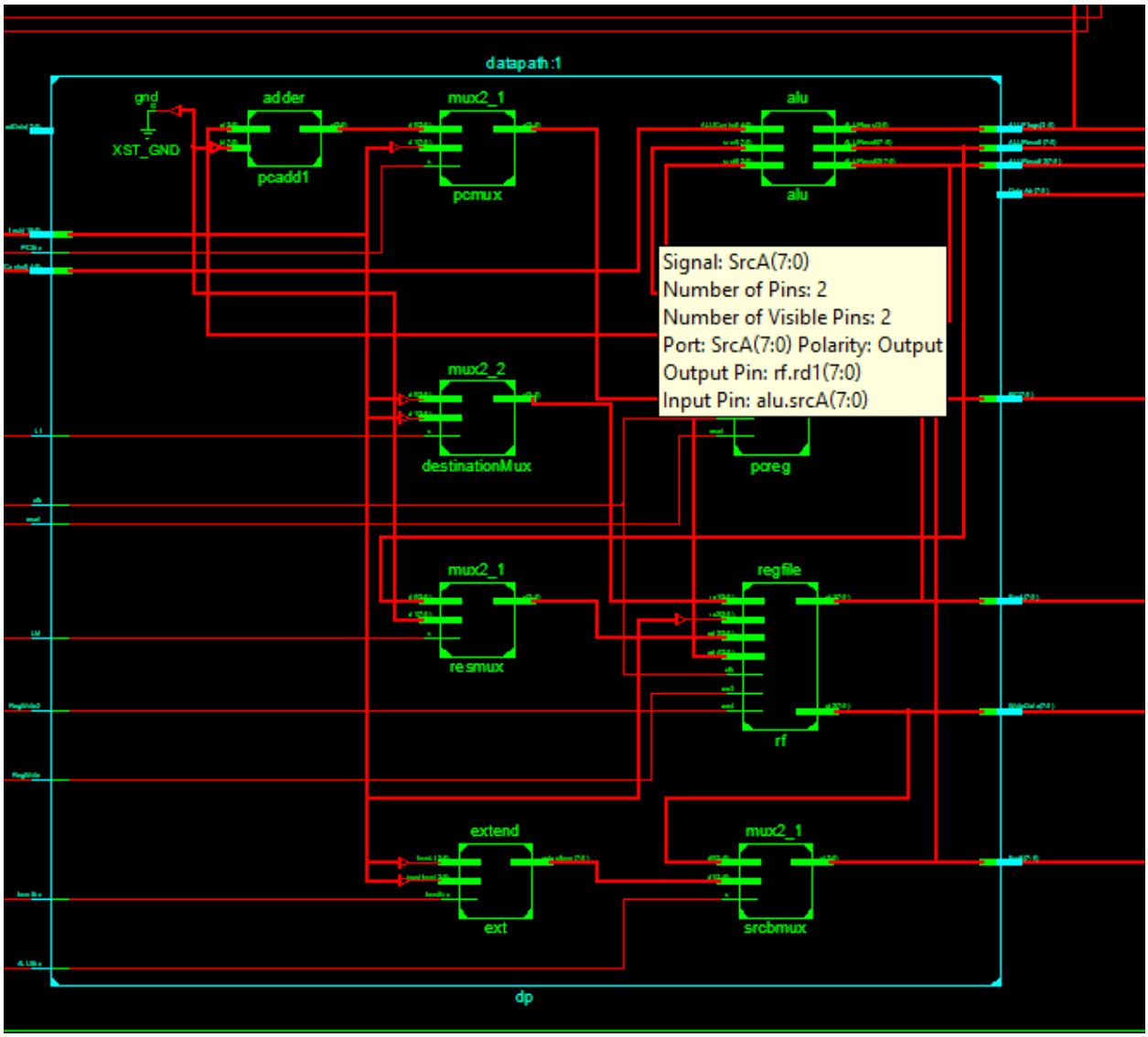

top:1
cpu:1
controller:1
condlogic
c
decoder
dec
c
datapath
dp
cpu
imem
imem
gnd
XST_GND
top


top:1
cpu:1
controller
c
datapath
Block: cpu
Type: cpu:1
dp
cpu
imem
imem
gnd
XST_GND
top

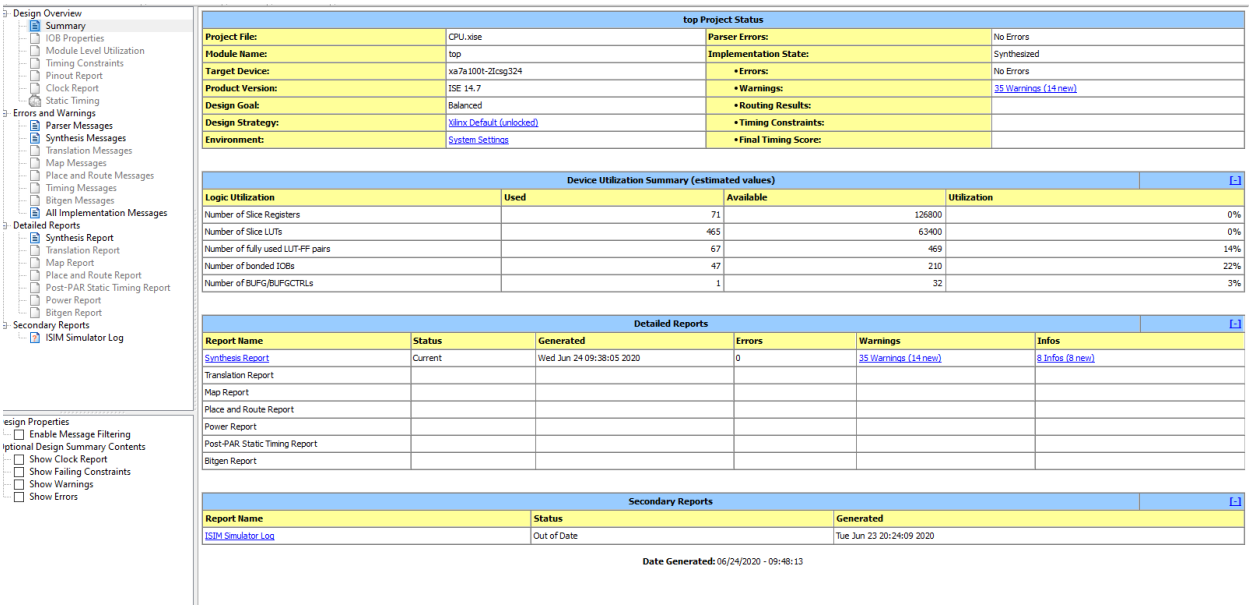

controller:1
condlogic
Block: cl
Type: condlogic
cl
decoder
dec
c


Block: dec
Type: decoder:1


condlogic:1
flopenr:1
fdce
flagreg1
condcheck:1
inv
AluFlags[2]_INV_9_o1
gnd
XST_GND
Mmux_CondEx1
and2
pcSrc1
flopenr
flagreg0
Mcompar_AluFlags[3]_AluFlags[0]_equal_2_o1
Mcompar_AluFlags[3]_AluFlags[0]_equal_2_o1
and2b2
AluFlags[1]_AluFlags[2]_AND_7_o1
Mcompar_AluFlags[1]_AluFlags[2]_equal_1_o1
Mcompar_AluFlags[1]_AluFlags[2]_equal_1_o1
and2b1
AluFlags[3]_AluFlags[2]_AND_8_o1
vcc
XST_VCC
Block: cc
Type: condcheck:1
cc
cl


datapath:1
gnd
XST_GND
adder
pcadd1
mux2_1
pcmux
alu
alu
Signal: SrcA(7:0)
Number of Pins: 2
Number of Visible Pins: 2
Port: SrcA(7:0) Polarity: Output
Output Pin: rf.rd1(7:0)
Input Pin: alu.srcA(7:0)
mux2_2
destinationMux
pcreg
mux2_1
resmux
regfile
rf
extend
ext
mux2_1
srcbmux
dp

گزارش:



- Design Overview
  - Summary
  - IOB Properties
  - Module Level Utilization
  - Timing Constraints
  - Pinout Report
  - Clock Report
  - Static Timing
- Errors and Warnings
  - Parser Messages
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Implementation Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Post-PAR Static Timing Report
  - Power Report
  - Bitgen Report
- Secondary Reports
  - ISIM Simulator Log

esign Properties
- Enable Message Filtering

ptional Design Summary Contents
- Show Clock Report
- Show Failing Constraints
- Show Warnings
- Show Errors

top Project Status

Project File:	CPU.xise	**Parser Errors:**	No Errors
Module Name:	top	**Implementation State:**	Synthesized
Target Device:	xa7a100t-2lcsg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	35 Warnings (14 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	71	126800	0%
Number of Slice LUTs	465	63400	0%
Number of fully used LUT-FF pairs	67	469	14%
Number of bonded IOBs	47	210	22%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports [-]

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed Jun 24 09:38:05 2020	0	35 Warnings (14 new)	8 Infos (8 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]

Report Name	Status	Generated
ISIM Simulator Log	Out of Date	Tue Jun 23 20:24:09 2020

Date Generated: 06/24/2020 - 09:48:13

دستورات داخل memfile.dat:

1. LR R1,1 1011000100000001
2. LR R2,1 1011001000000001
3. JMP,1000 10101xxx00010000
4. SAL R1,2 0000001011001010
5. ADD R1 , R2 0000000001001010
6. XCHNG R1,R2 0000000111001010
7. MOV R1,R2 0000000110001010
8. CMP R1,R2 0000010100001010
9. SUB R2,R1 0000000011001010
10. NON 0000000000000000
11. ROL R1, 1 0000001101010001

TECH SCHEMATIC: