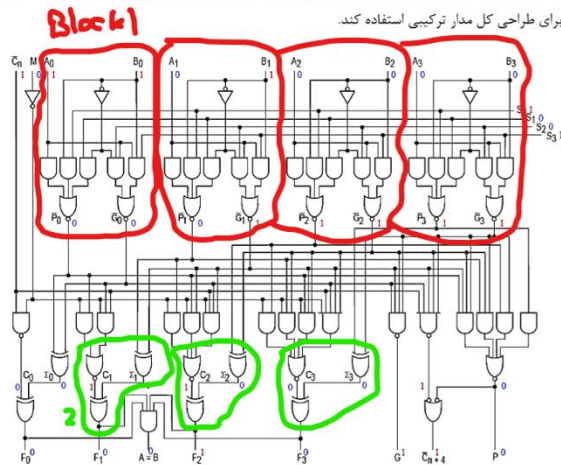


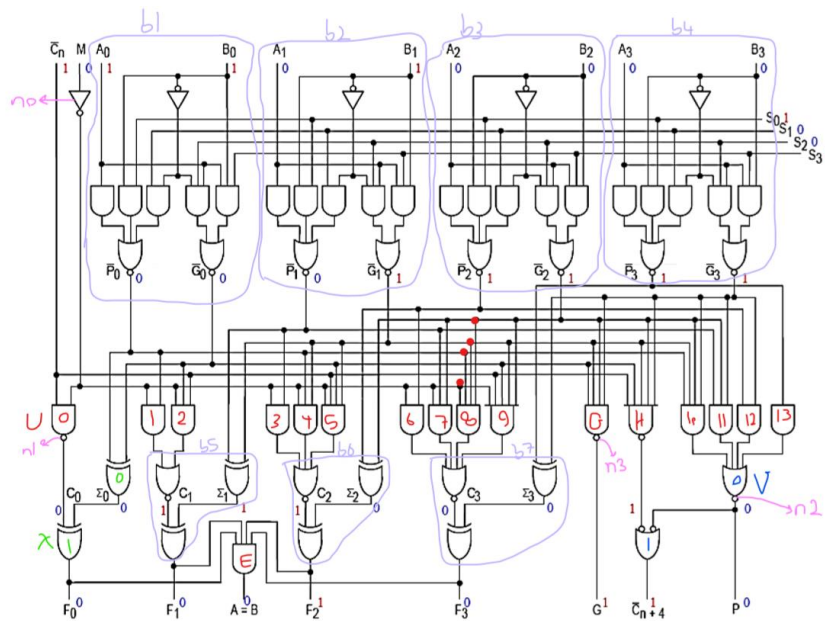
## ماژول های Block1 و Block2 استفاده شده برای طراحی مدار:

نشان دهند. با توجه به اینکه مدار دارای زیربخش‌های مشابهی است، دانشجو می‌تواند از آن بخش‌ها نمونه‌ای تهیه کند و در ماژول اصلی از آن برای طراحی کل مدار ترکیبی استفاده کند.



شکل (۱): شماتیک واحد محاسبه و منطق ۷۴۱۸۱ با نمونه‌ای از ورودی و خروجی‌های محاسبه شده

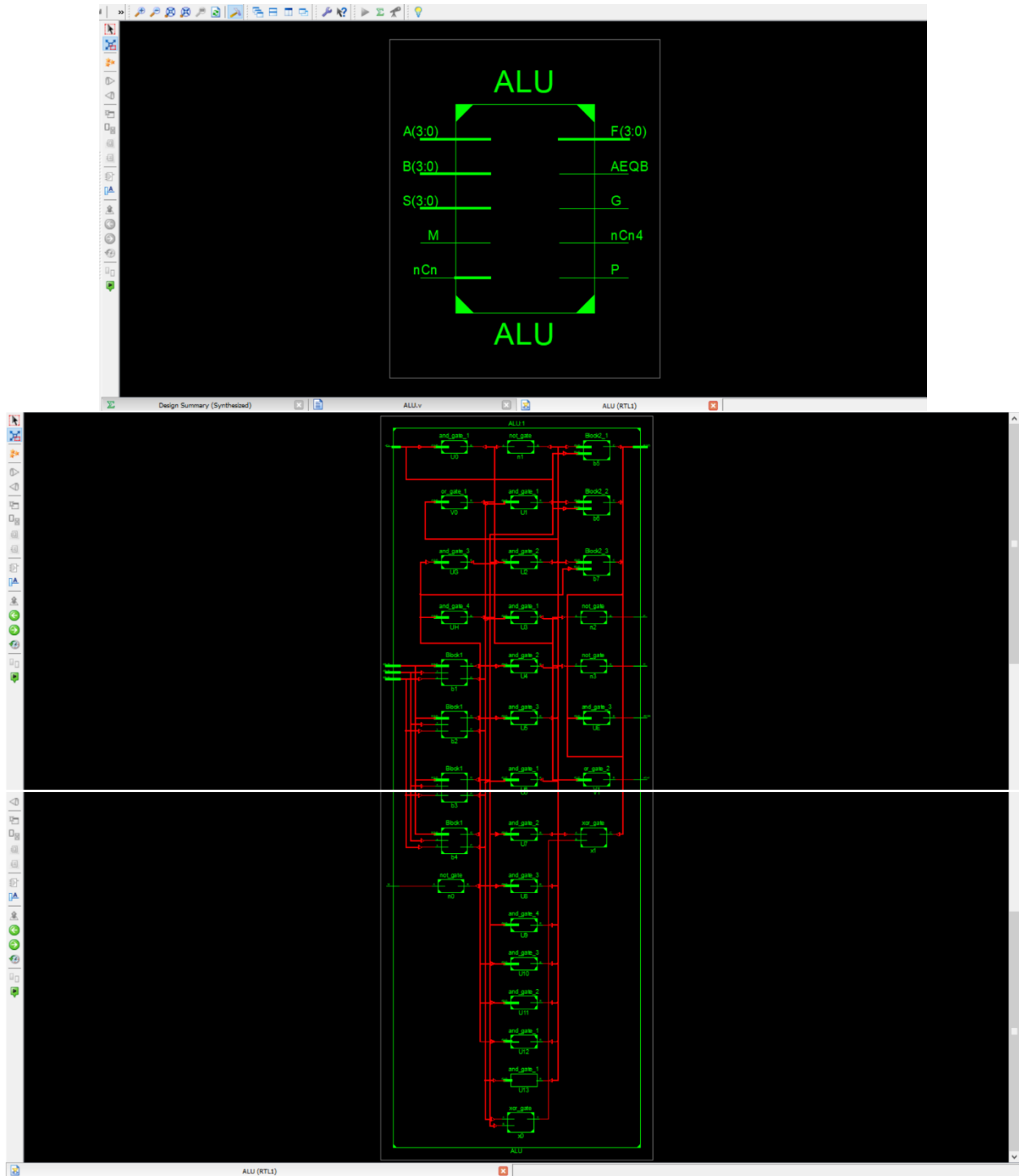
## نامگذاری ماژول ها در ماژول اصلی:



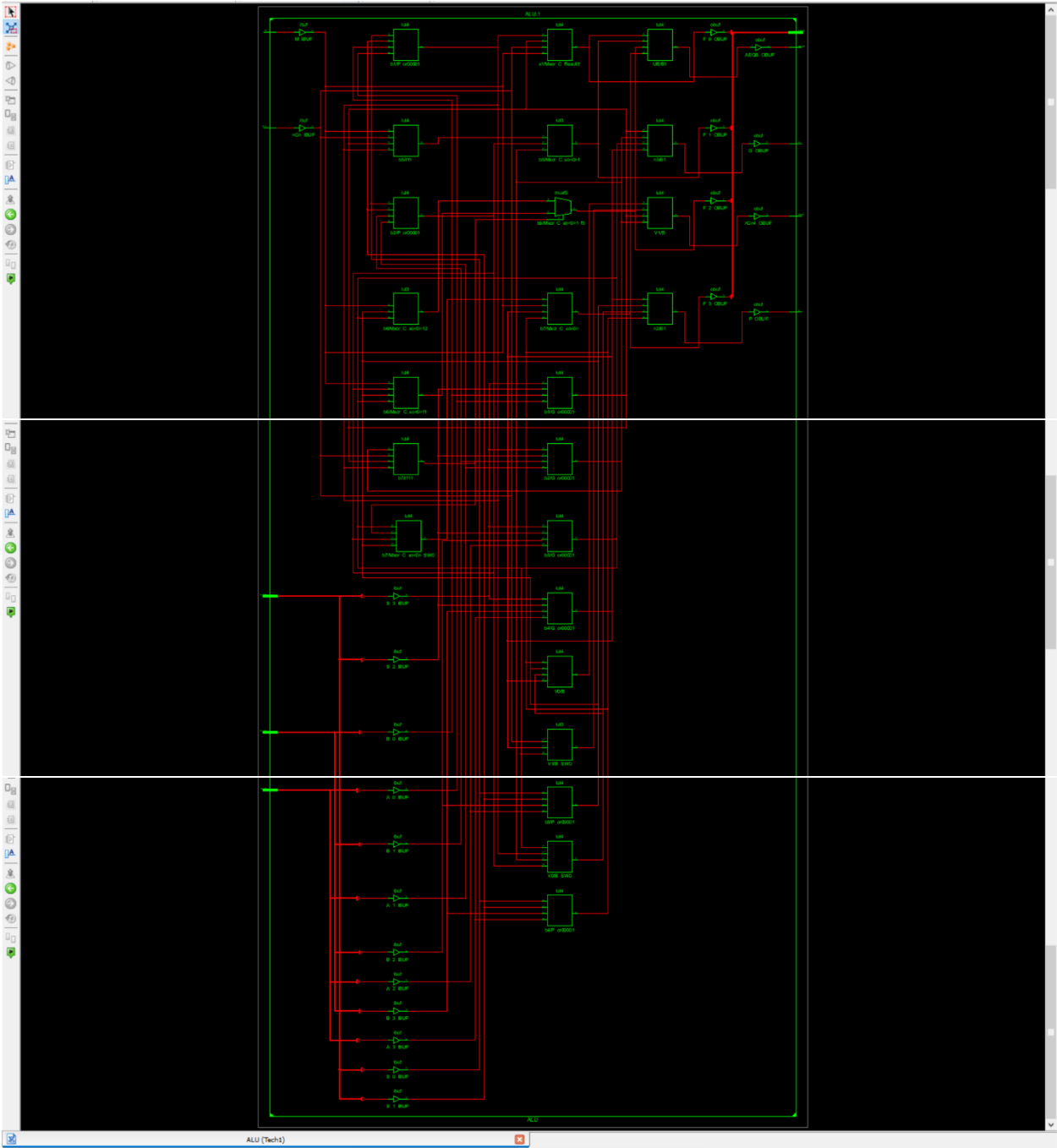
سنتز و پیاده سازی روی FPGA :

شماتیک:

RTL Schematic:



Technology Schematic:



## جزئیات چند LUT :

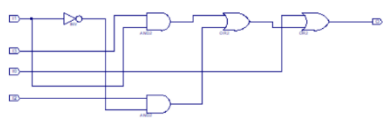
ISE Schematic Viewer (P.20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

**LUT4\_FEB4**  
INIT = FEB4

Schematic Equation TruthTable Karnaugh Map



OK Help

ALU [Tech1]

View by Category

Design Objects of Top Level Block

Properties of Instance: b1/P\_or00001

ISE Schematic Viewer (P.20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

**LUT4\_FEB4**  
INIT = FEB4

Schematic Equation TruthTable Karnaugh Map

I3	I2	I1	I0	O
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

OK Help

ALU [Tech1]

View by Category

Design Objects of Top Level Block

Properties of Instance: b1/P\_or00001

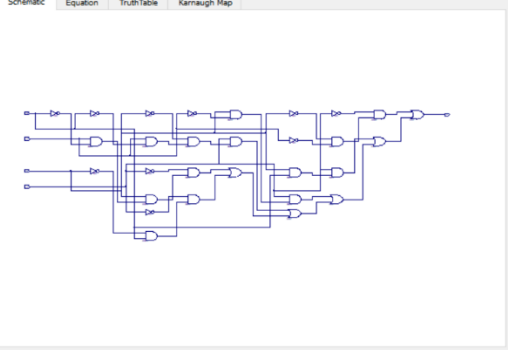
ISE Schematic Viewer (P20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

**LUT4\_B44B**  
INTT = B44B

Schematic Equation TruthTable Karnaugh Map



OK Help

ALU [Tech1]

View by Category

Design Objects of Top Level Block

Properties of Instance: x1/Hxor\_C\_Result1

ISE Schematic Viewer (P20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

**LUT4\_B44B**  
INTT = B44B

Schematic Equation TruthTable Karnaugh Map

I3	I2	I1	I0	O
0	0	0	0	1
0	0	0	1	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

OK Help

ALU [Tech1]

View by Category

Design Objects of Top Level Block

Properties of Instance: x1/Hxor\_C\_Result1

ISE Schematic Viewer (P20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

LUT4\_8000  
INSET = 8000

Schematic Equation TruthTable Karnaugh Map

OK Help

ALU (Tech1)

View by Category

Design Objects of Top Level Block

Properties of Instance: UE/B1

ISE Schematic Viewer (P20131013) - [ALU (Tech1)]

File Edit View Window Layout Help

LUT Dialog

LUT4\_8000  
INSET = 8000

Schematic Equation TruthTable Karnaugh Map

I3	I2	I1	I0	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

OK Help

ALU (Tech1)

View by Category

Design Objects of Top Level Block

Properties of Instance: UE/B1

## سنجش تاخیر مدار ترکیبی:

### Summary:

The screenshot displays the Xilinx Vivado IDE interface. The left pane shows the Design Hierarchy with the ALU module selected. The top-right pane shows the Design Summary (Implemented) report, which includes the following sections:

- Project File:** ALU.v, ALU.v
- Module Name:** ALU
- Target Device:** xc3s100e-5vq100
- Product Version:** ISE 14.7
- Design Goal:** Balanced
- Design Strategy:** Xilinx Default (unlocked)
- Environment:** System Settings
- Parser Errors:** No Errors
- Implementation State:** Placed and Routed
- Errors:** No Errors
- Warnings:** 2 Warnings (0 new)
- Routing Results:** All Signals Completely Routed
- Timing Constraints:** 0
- Final Timing Score:** 0 (Timing Report)

The **Device Utilization Summary** section provides the following data:

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	23	1,820	1%	
Number of occupied Slices	13	960	1%	
Number of Slices containing only related logic	13	13	100%	
Number of Slices containing unrelated logic	0	13	0%	
Total Number of 4 input LUTs	23	1,820	1%	
Number of bonded IOBs	22	66	33%	
Average Fanout of Non-Clock Nets	2.72			

The **Performance Summary** section shows:

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

The **Detailed Reports** section lists the following reports:

Report Name	Status	Generated	Errors	Warnings	Infos
ALU.v					

### Post-PAR Static Timing Report:

#### Data Sheet report:

All values displayed in nanoseconds (ns)

#### Pad to Pad

Source Pad | Destination Pad | Delay |

A<0>	AEQB	10.615
A<0>	F<0>	6.736
A<0>	F<1>	8.728
A<0>	F<2>	8.913
A<0>	F<3>	9.991
A<0>	G	6.991
A<0>	P	8.851
A<0>	nCn4	8.796
A<1>	AEQB	10.513

A<1>	F<1>	7.565
A<1>	F<2>	8.811
A<1>	F<3>	9.889
A<1>	G	7.348
A<1>	P	9.021
A<1>	nCn4	8.966
A<2>	AEQB	10.034
A<2>	F<2>	9.037
A<2>	F<3>	9.170
A<2>	G	7.401
A<2>	P	9.434
A<2>	nCn4	9.379
A<3>	AEQB	8.650
A<3>	F<3>	8.026
A<3>	G	7.009
A<3>	P	7.495
A<3>	nCn4	8.167
B<0>	AEQB	11.138
B<0>	F<0>	7.259
B<0>	F<1>	8.998
B<0>	F<2>	9.436
B<0>	F<3>	10.514
B<0>	G	7.514
B<0>	P	9.121
B<0>	nCn4	9.066
B<1>	AEQB	10.808
B<1>	F<1>	8.029
B<1>	F<2>	9.106
B<1>	F<3>	10.184



B<1>	G	7.643
B<1>	P	9.316
B<1>	nCn4	9.261
B<2>	AEQB	9.711
B<2>	F<2>	8.714
B<2>	F<3>	8.847
B<2>	G	7.078
B<2>	P	9.111
B<2>	nCn4	9.056
B<3>	AEQB	9.082
B<3>	F<3>	8.458
B<3>	G	7.446
B<3>	P	7.927
B<3>	nCn4	8.599
M	AEQB	8.360
M	F<0>	6.299
M	F<1>	6.926
M	F<2>	7.363
M	F<3>	6.384
S<0>	AEQB	10.436
S<0>	F<0>	6.653
S<0>	F<1>	8.645
S<0>	F<2>	8.734
S<0>	F<3>	9.812
S<0>	P	8.817
S<0>	nCn4	8.762
S<1>	AEQB	10.518
S<1>	F<0>	6.735
S<1>	F<1>	8.727

S<1>	F<2>	8.816
S<1>	F<3>	9.894
S<1>	P	8.850
S<1>	nCn4	8.795
S<2>	AEQB	10.492
S<2>	F<0>	6.583
S<2>	F<1>	8.285
S<2>	F<2>	8.790
S<2>	F<3>	9.868
S<2>	G	7.602
S<2>	P	9.000
S<2>	nCn4	8.945
S<3>	AEQB	10.743
S<3>	F<0>	6.864
S<3>	F<1>	8.566
S<3>	F<2>	9.041
S<3>	F<3>	10.119
S<3>	G	7.538
S<3>	P	9.211
S<3>	nCn4	9.156
nCn	AEQB	8.961
nCn	F<0>	6.267
nCn	F<1>	6.934
nCn	F<2>	7.259
nCn	F<3>	8.337
nCn	nCn4	7.544

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# شبیه سازی:

