Rethinking Memory Profiling and Migration for Multi-Tiered Large Memory Systems

Jie Ren¹, Dong Xu¹, Ivy Peng³, Junhee Ryu², Kwangsik Shin², Daewoo Kim², and Dong Li¹

¹University of California, Merced ²Sk Hynix ³KTH Royal Institute of Technology

Abstract

Multi-terabyte large memory systems are often characterized by more than two memory tiers with different latency and bandwidth. Multi-tiered large memory systems call for rethinking of memory profiling and migration because of the unique problems unseen in the traditional memory systems with smaller capacity and fewer tiers. We develop MTM, an application-transparent page management system based on three principles: (1) connecting the control of profiling overhead with the profiling mechanism for high-quality profiling; (2) building a universal page migration policy on the complex multi-tiered memory for high performance; and (3) introducing huge page awareness. We evaluate MTM using common big-data applications with realistic working sets (hundreds of GB to 1 TB). MTM outperforms seven state-of-the-art solutions by up to 42% (17% on average).

1. Introduction

The memory hierarchy is adding more tiers and becoming more heterogeneous to cope with performance and capacity demands from applications. Multi-tier memory systems that started from multi-socket non-uniform memory access (NUMA) architecture is now a de-facto solution for building scalable and cost-effective memory systems. For instance, the Amazon EC2 High Memory Instance has three DRAM-based memory tiers built upon eight NUMA nodes [19]. Recently, the commercial availability of new memory technologies, such as high-bandwidth memory (HBM) and compute express link (CXL) [1], is adding a new dimension to memory systems. As a result, a multi-tier memory system can easily exceed two memory tiers. Top tiers feature lower memory latency or higher bandwidth but smaller capacity, while bottom tiers feature higher capacity but lower bandwidth and longer latency. When high-density memory is in use, e.g., Intel's Optane DC PM [45], a multi-tier large memory system could enable high-performance, terabyte-scale graph analysis [10, 13, 40], in-memory database services [3, 6, 51], and scientific simulations [36, 49] on a single machine in a cost-effective way.

Most of the page management systems for multi-tier heterogeneous memory (HM) [2, 20, 22, 27, 32, 35, 41] consist of three components – a profiling mechanism, a migration policy, and a migration mechanism. A profiling mechanism is critical for identifying performance-critical data in applications and is often realized through tracking page accesses.

A migration policy chooses candidate pages to be moved to top tiers. Finally, the effectiveness of a page management solution directly depends on whether its migration mechanism can move pages across tiers at low overhead. The emergence of multi-tiered large memory systems calls for rethinking of memory profiling and migration to address unique problems unseen in traditional single- or two-tier systems with smaller capacity.

Problems. The large memory capacity brings challenges to memory profiling. Linux and existing memory profiling mechanisms [9] manipulate specific bits in page table entries (PTEs) to track memory accesses at a per-page granularity. This profiling method has the benefit of application-transparency, but is not scalable on a large memory system. Our evaluation shows that tracking millions of pages could take several seconds – too slow to respond to time-changing access patterns, and causes 20% slowdown in TPC-C against VoltDB [47]. The most recent solution DAMON [37, 38, 44] dynamically forms memory regions out of the virtual memory space mostly based on spatial locality, and profiles a single page per region. The total number of regions is constrained, such that the profiling overhead is controlled. DAMON has been adopted by Linux [44], and solves the profiling overhead problem faced by the large memory system, but its profiling quality can be out of control (shown in Section 3): DAMON can miss more than 50% of frequently-accessed pages and is slow to respond to the variance of memory access patterns.

The limitation in profiling quality comes from (1) the rigid control over profiling overhead and (2) the ad-hoc formation of memory regions. Memory profiling relies on PTE scans. Given a large memory system with a certain constraint on profiling overhead, the PTE scan for memory profiling can only happen certain times. Deciding the distribution of those PTE scans in the memory regions is critical for effective profiling. Strictly enforcing one PTE scan per region (to profile one page), as in DAMON, breaks the functionality of the profiling mechanism and compromises profiling quality. Furthermore, the ad-hoc formation of memory regions (such as sometimes splitting each memory region to two) takes a long time to find pages with the similar memory access patterns to form memory regions for profiling, delaying page migration.

In addition, rich memory heterogeneity brings challenges to page migration. Existing solutions, such as tiered-AutoNUMA [22] for multi-tiered memory are built upon an

abstraction extended from the traditional NUMA systems, where page migration occurs between two neighboring tiers with the awareness of no more than two NUMA distances. However, such an abstraction limits multi-tiered memory systems, because migrating pages from the lowest to the top tier, at tier-by-tier steps, has to make multiple migration decisions to reach the destination tier, which takes multiple seconds and fails to timely migrate pages for high performance.

Furthermore, Linux and existing solutions do not consider the implications of huge pages on memory profiling and migrations. Using huge pages is common in the large memory systems to reduce TLB misses and avoid long traverse of page tables. The transparent huge page mechanism (THP) in Linux mixes huge pages and 4KB pages, which brings complexity to form memory regions for profiling. THP also calls for a support of effective migration of huge pages.

Solutions. We argue that the following principles must be upheld to address the above problems.

- Connecting the control of profiling overhead with the profiling mechanism to enable high-quality profiling;
- Building a universal page migration policy on the complex multi-tiered memory hierarchy for high performance;
- Introducing huge page awareness.

In this paper, we contribute a page management system called MTM (standing for *Multi-Tiered* memory *M*anagement) that realizes the above principles on large multi-tier memory.

MTM decouples the control of profiling overhead from the number of memory regions, but connects it directly with the number of PTE scans (the profiling mechanism). Hence, profiling quality and overhead can be distributed proportionally according to the variation of both spatial and temporal locality. More PTE scans or page profiling can be enforced for a memory region where there is large variation hence demanding more fine-grained profiling. Also, the splitting of memory regions based on the variation is able to be guided rather than randomly happened as in DAMON.

To avoid the slow formation of memory regions, MTM uses performance counters to guide PTE scans in the largest memory tier. Only memory regions identified by performance counters due to memory events are subject to be profiled with higher accuracy and faster promotion to faster memory tiers. The performance counter-guided profiling is event-driven, providing promptness to catch changes in memory access patterns.

MTM breaks the barrier that blocks the construction of a universal page migration policy across tiers. This barrier comes from the limited memory profiling functionality (either at the slowest NUMA node [35] or random selection of hundreds of MB on NUMA nodes [9, 21, 23, 28, 35]). MTM uses the overhead-controlled, high-quality profiling to establish a *global* view of all memory regions in all tiers and consider all NUMA distances to decide page migration. In particular, MTM enables a "fast promotion and slow demotion" policy for high performance. Hot (frequently-accessed) pages identified in all lower tiers are ranked and directly promoted to the top

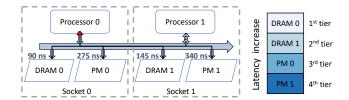


Figure 1: An example of multi-tiered memory system.

tier, minimizing data movement through tiers. When a page is migrated out of the top tier to accommodate hot pages, the page is moved to the next lower tier with available space. This policy needs no apriori knowledge of the number of memory tiers in a system and makes the best usage of fast tiers.

MTM also features a fast migration mechanism, which is critical for realizing the migration policy in practice. This mechanism dynamically chooses from an asynchronous page copy-based scheme and a synchronous page migration scheme, based on the read/write pattern of the migrated page, to minimize migration time.

Finally, page migration and profiling in MTM fully supports huge pages and THP, embodied as page alignment during splitting and merging of memory regions and effective support of huge page migration.

Evaluation. We rigorously evaluated MTM against seven state-of-the-art solutions, including two state-of-the-art solutions (AutoTiering [27] and HeMem [41]), an existing solution in Linux (tiered-AutoNUMA [9]), a hardware-based solution (Optane Memory Mode), and first-touch NUMA. MTM is also compared against two kernel-based page migration solutions (the ones in Linux and Nimble [50]). MTM outperforms Memory Mode, first-touch NUMA, tiered-AutoNUMA, AutoTiering, AutoNUMA and HeMem by 20%, 22%, 24%, 25% and 24%. MTM outperforms the Linux and Nimble migration approaches by 40% and 36% for read-intensive workloads, and performs similarly for write-intensive workloads.

2. Background and Related Work

We introduce memory organization in multi-tiered largememory systems. In such a system, each processor has its local memory as a fast memory tier, and has memory expansion or other processor's local memory as a tier of slow memory. The memory expansion may be based on CXL interconnect and appear as CPU-less memory nodes. Figure 1 shows an example of such a system which is an Intel Optane-based system with two sockets and four memory components (i.e., DRAM 0-1 and PM 0-1). Two PM components appear as CPU-less memory nodes in Linux. Each process has its local DRAM as a fast memory tier, and has two PM components and a remote DRAM as three tiers of slow memory. Another example of such a system can be found from Microsoft Azure [31].

2.1. Large Memory Systems

Given emerging large memory systems, there is a pressing need of studying effectiveness and scalability of system software and hardware to support them. We review related works.

Software support for page management. Recent work manages large memory systems based on an existing NUMA balancing [32] solution in Linux. Tiered-AutoNUMA [22] periodically profiles 256MB memory pages. Tiered-AutoNUMA balances memory access between CPU-attached memory nodes, and then balance memory accesses between CPUattached memory node and CPU-less memory node based on page hotness. As a result, a hot page takes a long time to migrate to the fastest memory for high performance. Auto Tiering [27] is a state-of-the-art solution. It uses the same profiling method as Tiered-AutoNUMA, and introduces flexible page migration across memory tiers. However, it does not have a systematic migration strategy guided by page hotness. HeMem [41] is a state-of-the-art solution for two-tiered PM-based HM. HeMem only uses performance counters to identify hot pages and fails to explore more than two tiers.

Hardware-managed memory caching. Some large memory systems use fast memory as a hardware-managed cache to slow memory. For example, in Intel's Optane PM, DRAM can work as a hardware-managed cache to PM in the *Memory Mode*. However, this solution results in data duplication, wasting fast memory capacity. It also causes serious write amplification when there are memory cache misses [4].

2.2. Two-Tiered Heterogeneous Memory

HM combines the best properties of memory technologies optimized for performance, capacity, and cost, but complicate memory management. There are application-transparent solutions that measure data reuse and migrate data for performance [2, 11, 12, 18, 25, 26, 29, 33, 41, 50]. However, they can cause uncontrolled profiling overhead or low profiling quality, and are not designed for more than two memory tiers.

There are application-specific solutions that leverage application domain knowledge to reduce profiling overhead, prefetch pages from slow memory to fast memory, and avoid slow-memory accesses. Those solutions include big data analysis frameworks (e.g., Spark [48]), machine learning applications [17, 42, 43], scientific computing [36, 39, 49], and graph analysis [10, 13, 40]. These solutions show better performance than the application-transparent, system-level solutions, but require extensive domain knowledge and application modifications. MTM is an application-transparent solution.

2.3. Huge Page Support in Linux

Linux supports fixed-sized huge pages, e.g., 2MB and 1GB, on x86 architectures. While it is possible to manage huge pages explicitly within applications using specific APIs, Transparent Huge Pages (THP) is the most common approach to use huge pages, because it requires no application modifications. When THP is enabled, the kernel automatically uses huge pages to satisfy large memory allocation with page alignment. Also, a kernel daemon (khugepaged) runs periodically to detect if contiguous 4KB pages can be promoted into a huge page

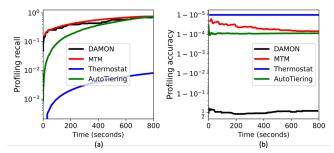


Figure 2: Comparison of different memory profiling methods in terms of their effectiveness of identifying hot pages.

or vice versa, mostly based on access recency and frequency. THP is swappable by splitting a huge page into basic 4KB pages before swapping out. Thus, when existing works reuse the Linux default page swapping routines to migrate pages to a slower memory tier [28, 35], the huge page cannot arrive at the slower memory tier unless it is split into 4KB pages because of access recency and frequency (not because of migration).

3. Motivation

High accuracy, low overhead profiling mechanism is key for managing multi-tiered large memory. We study the profiling methods in state-of-the-art works (Thermostat [2], AutoTiering [27], Linux's DAMON [38, 44]) and summarize their overhead and accuracy tradeoff as follows. AutoTiering randomly chooses 256 MB pages for profiling to detect hot pages. Both Thermostats and DAMON maintain a list of memory regions and randomly choose one page per region for profiling. Thermostats keeps all memory regions in a fixed size while DAMON dynamically splits and merges memory regions to improve profiling quality – they control profiling overhead by changing the number of memory regions.

We compare the profiling methods in these works with MTM by running the GUPS [14] benchmark with a 512GB working set on the four-tier memory system in Figure 1. We know a priori page hotness in each profiling interval during execution. Figure 2 reports profiling *recall* (i.e., the ratio of the number of correctly detected hot pages to the number of hot pages identified by priori knowledge) and profiling *precision* (i.e., the ratio of the number of correctly detected hot pages to the number of total detected hot pages including mis-identified hot pages).

Under the same profiling overhead (5%), Thermostat and AutoTiering take long time to reach high recall (i.e., slower to identify hot pages in Figure 2.a), because their randomness in page sampling and the formation of memory regions cause uncontrolled profiling quality. DAMON takes shorter time in Figure 2.a, but about 50% of hot pages detected by DAMON are not hot (see Figure 2.b), because of its ad-hoc design of forming regions and slow response to the variance of memory access patterns. Due to low profiling quality, DAMON, Thermostat, and AutoTiering perform 15% worse than MTM.

We rethink memory profiling support for multi-tiered large

memory based on the latest Linux support (i.e., DAMON). DAMON splits a process's virtual memory space into memory regions. In each profiling interval, it randomly profiles one 4KB page per memory region to capture spatial locality. The control of profiling overhead is achieved through a user-defined maximum number of memory regions for profiling. DAMON merges two neighbor memory regions if they have similar profiling results in an interval, and splits *each* region into two randomly-sized regions to improve profiling quality if fewer than half of the maximum number of regions exist.

We identify five limitations to be addressed.

- 1. The control of profiling overhead is not directly connected with the profiling mechanism (i.e., scanning PTEs), but connected with the number of memory regions and only one random page in a region is profiled. This constraint compromises profiling quality.
- 2. Splitting memory regions is ad-hoc. Splitting each region into two can lead to useless profiling when the new regions after splitting have the similar memory access patterns.
- 3. The process of forming memory regions can be slow to capture access patterns, because of the time constraint in the profiling intervals. This is problematic in large memory systems (e.g., multi-terabyte capacity) with many memory regions to split and merge.
- 4. Temporal locality is not considered well.
- 5. Lack of support for profiling huge pages.

4. Overview

MTM is designed to control the profiling overhead by considering the total number of PTE scans in all memory regions (Section 5.3). Like DAMON in Linux, MTM partitions the virtual address space of a process into memory regions for profiling and dynamically merges and splits them. However, MTM has the freedom to perform PTE scan multiple times for a page or multiple pages in a memory region in a profiling interval (Section 5.2). Having such flexibility provides opportunities to re-distribute sampling quotas between memory regions under a fixed profiling overhead to improve profiling quality, addressing Limitations 1 and 2. MTM uses performance counter-assisted PTE scanning to quickly detect changes in access patterns and address Limitation 3 (Section 5.5).

MTM decide page migration between tiers based on a "global view" of all memory regions (Section 6). By calculating the exponential moving average of page hotness collected from all profiling intervals, MTM learns the distribution of hot memory regions in *all* memory tiers, addressing Limitation 4.

Guided by the new profiling techniques, MTM introduces the "fast promotion and slow demotion" policy (Section 6.2). Also, when migrating pages, MTM uses an asynchronous page-copy mechanism that overlaps page copying with application execution. This mechanism reduces the overhead of page copy, but come with the time cost of *extra* page copy, because when a page is updated during copying, the page has to be copied again. The traditional, synchronous page-copy mechanism

does not need extra page copy, but completely exposes the overhead of page copy into the critical path. Hence, MTM uses a hybrid approach that takes advantage of both mechanisms, and selects one based on whether page modification happens during migration (Section 7).

To support huge pages, MTM enables page profiling at the huge page level instead of 4KB-page level using the page table information; memory merging and splitting are carefully managed to be aligned with the huge page size, such that the huge page semantics is not broken (Section 5.4). Also, MTM lifts the constraint in existing work that huge pages cannot move across distant memory tiers and support huge-page migration based on the existing support of 4KB-page migration (Section 7.3).

In summary, MTM has (1) an adaptive profiling mechanism with high profiling quality and constrained overhead; (2) a page-migration strategy using a global view to make informed decisions; and (3) a page-migration mechanism adapting data copy schemes based on page access patterns.

5. Adaptive Memory Profiling

MTM tracks page accesses using PTE reserved bits and PTE scan. Each PTE maintains an access bit, indicating its access status. The access bit is initially set to 0, but changed to 1 by the memory management unit (MMU) when the corresponding page is accessed. By repeatedly scanning PTE to check the value of the access bit and resetting the access bit to 0 if found to be 1, page accesses can be monitored. This mechanism is commonly used in Linux and existing works [18, 38].

Scanning all PTEs to track memory accesses to each page is prohibitively expensive for large memory. For example, scanning a five-level page table for 1.5 TB memory in 2MB pages on an Optane-based platform (hardware details in Table 1) with helper threads takes more than one second – infeasible to capture workload behaviors online. Thus, page sampling is often used to avoid such high overhead. However, large memory systems have large numbers of pages and the profiling quality with unguided, random sampling [2, 20, 23, 27, 38] could lead to poor performance. MTM systematically forms memory regions to address this problem.

5.1. Formation of Memory Regions

A memory region is a contiguous address space mapped by a last-level page directory entry (PDE) by default. This indicates that in a typical five-level page table, the memory region has a default size of 2MB. During program execution, whenever a last-level PDE is set as valid by the OS, the corresponding memory region is subject to profiling.

Multiple scans of PTEs. In a profiling interval, the access bit of the PTE corresponding to a sampled page is scanned multiple times. The total number of scans per PTE per profiling interval is subject to a constant, *num_scans*.

We use the multi-scan method, instead of single-scan to reduce skewness of profiling results. In a profiling interval, a single-scan method can only detect whether a page is accessed or not, but cannot accurately capture the number of accesses. Although aggregating memory accesses across multiple profiling intervals could alleviate this problem, the skewness of profiling results can be accumulated over time (see Section 6.1), leading to sub-optimal migration decisions. Using the multiscan method avoids this problem.

At the end of a profiling interval, the average number of accesses to all sampled pages in a memory region is used to indicate the *hotness* of that memory region. Based on the results, MTM may merge or split memory regions. Note that the formation of memory regions through merging and splitting is based on "logical" memory regions and there is no change to PTE during the formation.

Merge memory regions. MTM actively looks for opportunities to merge contiguous memory regions at the end of a profiling interval. Two contiguous regions are merged, if their difference in the hotness in the most recent profiling interval is smaller than a threshold τ_1 .

Split a memory region. MTM checks whether a memory region should be split to keep pages in a region to have similar hotness. When the maximum difference in the number of accesses among all sampled pages in a region exceeds a threshold τ_2 , the region is split into two equally-sized ones.

Selection of τ_1 **and** τ_2 . τ_1 and τ_2 define the minimum and maximum differences in the number of memory accesses among sampled pages in a memory region. τ_1 and τ_2 fall into $[0, num_scans]$. To avoid frequent merging/splitting and balance between them, τ_1 and τ_2 evenly split the range of $[0, num_scans]$, i.e., $\tau_1 = 1/3 * num_scans$ and $\tau_2 = 2/3 * num_scans$ by default. τ_1 can be dynamically fine-tuned to enforce the limit on profiling overhead, discussed in Section 5.3.

5.2. Adaptive Page Sampling

Because the profiling overhead control is decoupled from the number of memory regions and relies on PTE scans, MTM can adapt the number of sampled pages in a region to improve profiling quality. Since each sampled page has the same number of PTE scans per profiling interval, the control of PTE scans is implemented by the control of page samples (see Section 5.3).

Initial page sampling. MTM differentiates the slowest tier from other tiers in each profiling interval. The slowest tier relies on performance counters to identify memory regions with memory accesses. Only those memory regions are subject to be profiled with PTE scan-based profiling. Each memory region in the slowest memory tier for profiling has only one page profiled. This page is the one captured by performance counters. All other memory tiers profile all memory regions and each region initially has a random page profiled.

After merging two memory regions, the total number of page samples in the two regions is reduced by half under the constraint that the new region has at least one sample. This reduction saves the profiling overhead for the two regions, and allows other memory regions to have more samples without

exceeding the overhead constraint.

The saved page sample quota after merging memory regions is re-distributed to other memory regions. First, MTM distributes sample quota to the memory regions whose hotness indication shows the largest variance in the last two profiling intervals among all memory regions. Having a large variance of hotness indication in two profiling intervals indicates the memory access pattern change. Adding more page samples for profiling in this case is useful to improve profiling quality.

To efficiently find memory regions with the largest variance of hotness indication among all regions, MTM keeps track of top-five largest variances and the corresponding regions when analyzing profiling results. We choose "five" empirically to make it lightweight. Whenever a new profiling result for a region is available, MTM checks the top-five records and updates them if needed. After the merging, the saved page-sample quota is re-distributed to those top-five regions.

After splitting a memory region into two new regions, the page sample quota in the original region is evenly split into the two regions. Therefore, splitting does not change the number of total PTE scans. Splitting memory regions brings two benefits. First, the hotness indication, which is the *average* number of accesses to all sampled pages in a memory region, provides better indication of memory accesses to the new, smaller memory regions, hence providing better guidance on page migration. Second, migration is more effective, because using the smaller memory region avoids unnecessary data movement coming with the larger region.

5.3. Profiling Overhead Control

MTM supports the user to define a profiling overhead constraint. MTM respects this overhead constraint while maximizing profiling quality, by dynamically changing the number of memory regions and distributing page-sample quotas between the regions. The overhead constraint is a percentage of program execution time without profiling and migration. For example, in our evaluation section, this overhead constraint is 5%. Given the length of a profiling interval (*t_{mi}*), profiling overhead constraint, overhead of scanning one PTE (*one_scan_overhead*), and the number of scans per PTE (*num_scans*), the total number of page samples in all memory regions that can be profiled in a profiling interval, denoted as *num_ps*, is calculated in Equation 1.

$$num_ps = \frac{t_{mi} \times profiling_overhead_constraint}{one_scan_overhead \times num_scans}$$
 (1)

 t_{mi} can be set by the user, as in existing works [2, 18, 38]. $one_scan_overhead$ is measured offline. As MTM merges or splits memory regions, the total number of page samples in all memory regions remains equal to num_ps to respect the profiling overhead constraint.

The total number of memory regions needs to be smaller than *num_ps* so that each memory region has at least one page sample. When the total number of memory regions is too large, MTM temporarily increases τ_1 (the threshold to merge regions, and keeps $\tau_2 > \tau_1$) to merge memory regions more aggressively. τ_1 is gradually increased across profiling intervals, until the number of memory regions is no larger than $num_p s$, and then τ_1 is reset to the original value.

Another approach to enforce the profiling overhead constraint is to change the number of scans per page sample (i.e., num_scans). However, we do not use this approach, because of its significant impact on profiling quality. Changing num_scans leads to a change of profiling results in all memory regions. For example, in our evaluation, when changing num_scans from 2 to 3, MTM changes the migration decision for at least 20% of memory regions. We set num_scans as a constant "3". Our empirical study shows that using a value larger than 3 leads to no obvious change (less than 5%) in the migration decision.

Memory consumption overhead. For each memory region, MTM stores its hotness as an integer. Given a terabyte-scale memory, this yields an overhead in hundreds of MBs. In our 1.5 TB memory platform, the memory overhead to store profiling results is no larger than 600MB.

5.4. Support of Huge Pages

When MTM selects a page for profiling, this selection is huge page-aware. In particular, in the beginning of the profiling interval, MTM checks whether the selected page for profiling is a huge page or not by checking its PTE. If it is, then any access to the huge page is captured by scanning its PTE. This method is different from the existing huge page-aware solution (Thermostat). Thermostat randomly selects a basic 4KB page out of the huge page to approximate the number of memory accesses to the huge page, losing profiling quality. Also, if the huge page is mprotected, 4KB-based profiling in Thermostat cannot happen. MTM does not have these limitations.

The formation of memory regions is also huge page-aware. When splitting a memory region, MTM checks if the split happens in the middle of a huge page. If so, the split will be slightly adjusted to be aligned with the huge page boundary. Without such handling, a huge page can be profiled in two subregions, wasting PTE scans, and also suffer from conflicting migration decisions. Furthermore, the two subregions after the adjustment may not be equally-sized, increasing the risk of memory fragmentation after migration. However, in practice, given the large size of the memory region (at the scale of MBs), the size difference between the two subregions is small (often less than 10KB) without increasing memory fragmentation.

5.5. Performance Counter-Assisted PTE Scanning

After the initial page sampling (Section 5.2), the slowest memory tier continues to use performance counters to assist PTE scanning. In particular, at the beginning of a profiling interval, the performance counters are enabled for a short time (10% of the profiling internal) to collect memory accesses and identify huge page-sized memory regions where the memory accesses

happen. Those memory regions are compared with the existing memory regions in the slowest memory tier. If they are the same, then the existing regions continue to use PTE scans. If not, then the memory regions identified by the performance counters are subject to be profiled, and the existing memory regions not identified by the performance counters are not profiled in the current profiling interval.

Compared with DAMON, using performance counters can save multiple profiling intervals to identify hot pages, because DAMON uses a time-interval-based approach to capture hot pages by chance, while MTM uses an event-driven approach: once a memory region is accessed, it is immediately subject for high-quality profiling to confirm its hotness. Different from Dancing [7] that also uses the hybrid performance counter/PTE scan, MTM selectively apply the hybrid approach (i.e. only in the slowest memory tier with the largest capacity) and the interaction between the counters and PTE scans are driven by the needs of fast responses (not gaining better visibility to memory accesses as Dancing). Note that using performance counters alone without PTE scan is not enough to provide high-quality profiling, shown in our comparison with HeMem (Section 9.1), because its full randomness misses hot pages.

6. Page Migration Strategy

A page migration strategy decides (1) which memory regions to migrate, and (2) given a region to migrate, which memory tier to migrate.

6.1. Which Memory Region to Migrate?

At the end of a profiling interval, MTM promotes some memory regions to the fastest tier, and the total size of migrated regions is a constant N (N=200MB in our evaluation). This is similar to the existing works [20, 23, 27, 34] that periodically migrates a fixed number of pages. If there is no enough free space in the fastest tier, some pages in the fastest tier need to be demoted first to the slower tiers (see Section 6.2).

Select memory regions for promotion. The goal of promotion is to place recent frequently accessed pages into faster tiers. MTM's migration decision is holistic – considering *all* memory regions together regardless of which tiers those memory regions are currently in. MTM uses time-consecutive profiling results based on the exponential moving average (EMA) of hotness indication collected from all profiling intervals. Given a sequence of data points, EMA places a greater weight and significance on the most recent data points. Thus, MTM using EMA considers temporal locality in migration decision and avoids page migration due to the bursty memory access pattern in one profiling interval.

We define EMA of hotness indication as follows. Assume that HI_i is the hotness indication collected at the profiling interval i for a memory region, and the EMA of hotness indication for that memory region at i, denoted as WHI_i , is defined in Equation 2. This equation is a recursive formulation including WHI_i and WHI_{i-1} from the prior interval i-1.

$$WHI_i = \alpha \times HI + (1 - \alpha) \times WHI_{i-1}$$
 (2)

 α indicates the importance of historical information in decision making. In practice, we set α as 0.5. There are two benefits of using EMA. First, the memory consumption is small. There is no need to store all prior profiling results. Second, the computation of EMA is lightweight.

With the EMA of hotness indication in all memory regions, MTM builds a histogram to get the distribution of EMA of all memory regions. The histogram buckets the range of EMA values, and counts how many and what memory regions fall into each bucket. Given the size of pages to migrate to the fastest memory, MTM chooses those memory regions falling into the highest buckets in the histogram to migrate. Building and maintaining the histogram has low overhead: whenever the EMA of hotness indication of a memory region is available, the histogram only needs to be slightly updated accordingly.

6.2. Where to Migrate Memory Regions?

Promotion. As memory regions are promoted to the fastest tier based on the histogram, it is likely that after a profiling interval, there is no region to promote because those regions falling into the highest buckets of the histogram are already in the fastest tier. In that case, memory regions in the lower buckets of the histogram are selected to promote to the second-fastest memory tier. The accumulated size of regions to migrate should always be N. In general, MTM makes the best efforts to promote frequently accessed regions to faster tiers.

Demotion. When a memory tier is a destination of memory promotion but does not have enough space to accommodate memory promotion, some memory regions in that memory tier may need to be demoted to the next lower memory tier with enough memory capacity. Memory regions for demotion are selected based on the histogram – memory regions that are in the lowest buckets of the histogram are demoted to the next lower tier. We use the above slow-demotion strategy to avoid performance loss caused by migrating pages that are still likely to be accessed in near future.

Handling multi-view of tiered memory. If the application managed by MTM has multiple threads, depending on which memory node a thread is close to, different threads can have different views on whether a memory node is fast or slow. For example, in Figure 1, a thread on processor 0 thinks DRAM 0 is a fast memory, while a thread on processor 1 thinks DRAM 0 is a slow memory. We call this, the *multi-view of tiered memory*. The multi-view does not impact profiling results because the page hotness is only related to the number of page accesses, no matter from which thread memory accesses come. However, the multi-view impacts page migration destination.

In MTM, the migration destination of a page is decided using the view of the thread that has the most accesses to that page, because enabling high performance for the most memory accesses gives the best overall performance. To support this design, during the memory profiling, MTM checks

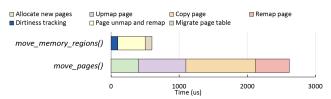


Figure 3: Performance breakdown for migration mechanisms.

where memory accesses come from. This is implemented by leveraging the hint-fault mechanism in Linux [9]. A hint-fault takes 12× longer time than a PTE scan. To amortize this cost, every 12 PTE scans, MTM turns on the hint-fault mechanism to capture one memory access, and includes the amortized cost into *one_scan_overhead* in Equation 1.

7. Adaptive Migration Mechanism

7.1. Performance Analysis of Page Migration Mechanism

Linux provides an API, *move_pages()*, for a privileged process to move a group of 4KB pages from a source memory node (or tier) to a target memory node (or tier). There are four steps in *move_pages()*, and they are performed sequentially: (1) allocate new pages in the target memory node; (2) unmap pages to migrate (including invalidating PTE); (3) copy pages from source to target memory node; (4) map new pages (including updating PTE).

Figure 3 shows the performance of migrating a 2MB memory region from the fastest tier to the slowest tier on the Optane-based platform. Copying pages is the most time-consuming step, taking 40% of total time. One reason for the high overhead is that *move_pages()* moves 4KB-sized pages sequentially. Although recent work [50] enables multi-threaded page copy to fully utilize memory bandwidth, it is still a bottleneck especially when moving a large memory region.

7.2. Adaptive Page Migration Schemes

Asynchronous page copy. We introduce an asynchronous page copy mechanism to reduce page copy overhead. In the asynchronous page copy, the thread that triggers migration (named *main thread*) launches one or more helper threads to run the steps (1) and (3); the main thread runs the steps (2) and (4), and then waits for the helper thread(s) to join. With the asynchronous page copy, it is possible that copying a page happens before invalidating its PTE but the page is modified in the source memory tier after copying the page. In such cases, the page must be copied again to update its copy in the target tier, which is costly. We introduce an adaptive page-migration mechanism to address this limitation.

Adaptive page migration. For read-intensive pages, the asynchronous page copy brings performance benefit. However, for write-intensive pages, due to repeated data copy, it is likely that the asynchronous page copy performs worse than the synchronous. Hence, MTM chooses suitable migration mechanism based on the write intensity of pages. In particular, MTM uses the asynchronous page copy by default. But when-

ever any page in the memory region for migration is written after the asynchronous page copy starts, MTM switches to the synchronous page copy. To track page write, MTM utilizes PTE access bits and page faults, discussed in Section 8.

We implement the above mechanism and introduce a new API called *move_memory_regions()*. In this implementation, tracking page write, performing page map/unmap, and migrating PTEs are still on the critical path, but the time-consuming page copying could be performed off the critical path. Figure 3 presents the performance of *move_memory_regions()* migrating 2MB memory region using the same setting as for *move_pages()*, and excludes the overhead of page copying (and page allocation in the step (1), using asynchronous page allocation). *move_memory_regions()* is 4.37× faster than *move_pages()* in this case. Section 9.4 shows more results.

7.3. Support of Huge Page Migration

MTM enables direct migration of a huge page to a lower memory tier without waiting for it to be split into basic 4KB pages as AutoTiering (a solution supporting multi-tiered memory). In particular, MTM uses *move_memory_regions()* to move a huge page as a whole. In contrast, AutoTiering puts huge pages to the (in)active lists where they are split into 4KB basic pages for profiling and then for migration as needed.

8. Implementation

We implement the adaptive memory profiling as a kernel module that enables performance counters to guide profiling and periodically scans PTEs based on adaptive page sampling. The kernel module takes a process ID as input. For performance counters, it uses Intel processor event-based sampling mode (PEBS) to collect memory accesses into a preallocated buffer, and uses a register interrupt handler to indicate when the buffer is full. MTM uses hardware events MEM_LOAD_RETIRED.LOCAL_PMM and MEM_LOAD_RETIRED.REMOTE_PMM to capture memory accesses. The sampling frequency is set as 200 memory accesses as in production environment [35], which is sufficient to distinguish hot and code pages [41]. In addition, profiling results from PTE scans is saved in a shared memory space, and stored as a table, where each record contains a memory region ID, hotness indication in the current profiling interval, and the EMA of hotness indication of prior intervals. The region ID is generated based on the start address of the memory region.

We implement the page management as a daemon service at the user space. The daemon service executes with the application and calls the kernel module for profiling at the beginning of each profiling interval. At the end of each profiling interval, the service reads collected profiling results from the shared memory space. With overhead control, the profiling module ensures that profiling always finishes within a profiling interval. The service then makes the migration decision and performs migration using *move memory regions()*.

Table 1: Hardware overview of experimental system.

Optane-based Multi-tiered Memory System			
Fast Mem Local Access (1st tier)	latency: 90ns	bw: 95 GB/s	
Fast Mem Remote Access (2nd tier)	latency: 145ns	bw: 35 GB/s	
Slow Mem Local Access (3rd tier)	latency: 275ns	bw: 35 GB/s	
Slow Mem Remote Access (4th tier)	latency: 340ns	bw: 1 GB/s	
Emulated Multi-tiered	d Memory System		
Emulated Multi-tiered Fast Mem Local Access (1st tier)	d Memory System latency: 198ns	bw: 95 GB/s	
Fast Mem Local Access (1st tier)	latency: 198ns	bw: 95 GB/s	

move_memory_regions() takes the same input as Linux move_pages(), but implements the adaptive migration mechanism. It detects page dirtiness during the migration by setting a reserved bit in PTE to trigger a write protection fault when there is write to the memory region. Leveraging a user-space page fault handler, move_memory_regions() tracks writes, and decides whether to stop the asynchronous page copy and switch to the synchronous mechanism.

MTM cannot manage multiple applications co-running in the same machine, because that requires coordination of page migration among applications, which is our future work.

9. Evaluation

Testbed. We evaluate MTM on a two-socket machine. Each socket has Intel Xeon Gold 6252 CPU (24 cores), 756GB Intel Optane DC PM and 96GB DRAM. This machine has four memory tiers (see Figure 1). We also emulate a fourtiered memory system with doubled latency and bandwidth using memhog in Linux. The emulation launched memhog instances in each memory tier to continuously inject memory access traffic. The details of evaluation platforms show in table 1. Unless indicated otherwise, we report results on the Optane-based machine (not the emulation platform). We use madvise for THP [46] and uses 2MB as huge page size by default, which is typical in large memory systems. We set the profiling overhead constraint to 5% and the profiling interval to 10 seconds. This setting is similar to existing works and production environments [2, 18, 35, 38].

Workloads. We use large-memory workloads in Table 2. Their memory footprints are larger than the fastest two tiers, enabling effectively evaluation on all tiers. Unless indicated otherwise, we use eight application threads per workload.

Baselines. Eight state-of-the-art solutions are used.

- Hardware-managed memory caching (HMC) uses the fast memories as hardware-managed cache for slow memories.
 We use Memory Mode in Optane.
- *First-touch NUMA* is a common allocation policy. It allocates pages in a memory tier close to the running task that first touches the pages. It does not migrate pages.
- Tiered-AutoNUMA [22] in Linux and AutoTiering [27].
- *HeMem* [41] is for two-tiered systems. HeMem leverages performance counters alone to find hot pages.
- Thermostat [2] is for two-tiered systems. It allocates all

Table	ე.	Work	loade	for ava	luation.

Workloads	Descriptions	Mem	R/W
GUPS [14]	A measurement of how frequently a computer	512GB	1:1
	can issue updates to randomly generated mem-		
	ory locations.		
VoltDB [47]	A commercial in-memory database with TPC-	300GB	1:1
	C [30] using 5K warehouse.	/1.2TB	
Cassandra [5]	A highly-scalable partitioned row store with	400GB	1:1
	YCSB [8] (using update-heavy benchmark A).		
BFS [40]	A parallel implementation of graph traversing	525GB	read-
	and searching on a graph with 0.9B nodes and		only
	14B edges.		
SSSP [40]	A parallel implementation of finding the	525GB	read-
	shorted path between two vertices on a graph		only
	with 0.9B nodes and 14B edges.		
Spark [52]	A spark program running the TeraSort bench-	350GB	1:1
	mark [15].		

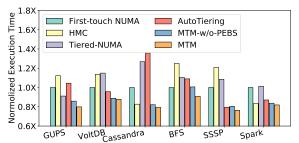


Figure 4: Overall performance (normalized to first-touch NUMA's) using existing solutions and MTM on Optane.

pages in the fast tier and selectively moves them to the slow tier. It cannot support applications with footprint larger than the fast tier. Thus, we do not evaluate its page migration but only evaluate its profiling method.

- *DAMON* [38, 44] is a Linux profiling tool at the memory region granularity. We use it to evaluate profiling quality.
- Nimble [50] is a page migration mechanism using bidirection page copy and parallel page copy. MTM includes the techniques in Nimble but adds adaptive migration. We use Nimble to evaluate our page migration mechanism.

9.1. Overall Performance

Optane-based multi-tiered system. Figure 4 shows that MTM outperforms all baselines. We have five observations.

- (1) MTM outperforms HMC by up to 40% (avg. 19%). HMC incurs write amplification when cache misses occur [16], causing unnecessary data movement and low performance.
- (2) MTM outperforms first-touch NUMA by up to 24% (avg. 17%). Without page migration, first-touch NUMA outperforms HMC on VoltDB and BFS, and outperforms tiered-AutoNUMA on Cassandra and BFS, indicating that page migration is not always helpful. HMC performs worse because of unnecessary page movement. tiered-AutoNUMA has worse performance because it cannot effectively identify hot pages.
- (3) MTM outperforms tiered-AutoNUMA by up to 37% (avg. 23%). Tiered-AutoNUMA provides page migration across all memory tiers. However, tiered-AutoNUMA promotes hot pages slowly, which wastes the opportunity to accelerate application execution in fast memory.

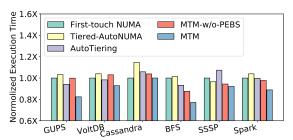


Figure 5: Performance comparison between existing solutions and MTM on the emulated multi-tiered memory system. The performance is normalized by First-touch NUMA performance.

- (4) MTM outperforms AutoTiering by up to 42% (avg. 17%). AutoTiering uses random sampling and opportunistic demotion, failing to effectively identify pages for migration.
- (5) MTM outperforms the solution of disabling performance counter for profiling (MTM-w/o-PEBS in the figure) by up to 10.6%. Lack of efficient methods to detect hot regions in the slowest memory tier, MTM-w/o-PEBS fails to provide high quality profiling result to guide page placement.

Emulated multi-tiered memory system. Figure 5 shows that on the emulated platform, MTM maintains the same performance trend as on the Optane-based testbed – it outperforms first-touch NUMA, tiered-AutoNUMA, AutoTiering and MTM-w/o-PEBS by 19%, 26%, 17%, and 14% respectively. Note that HMC is not evaluated because when HMC is used, fast memory tiers are hidden from software and we cannot inject latency into fast memory.

Performance breakdown. We show the breakdown into application execution time, migration time, and profiling time in Figure 6. The migration time is the overhead exposed on critical path, excluding asynchronous page copying time. We only compare tiered-AutoNUMA, MTM-w/o-PEBS and MTM because they are the only solutions that can leverage all four memory tiers for migration. We add first-touch NUMA as a performance baseline because evaluated solutions use first-touch NUMA for memory allocation. In all cases, the profiling overhead falls within the profiling overhead constraint.

With tiered-AutoNUMA, the time reduction is lower or equal to the overhead of profiling and migration (see VoltDB and Cassandra). Hence, they perform worse than first-touch NUMA without page migration. Compared to tiered-AutoNUMA, MTM spends similar time in profiling but 3.5× faster in migration, reducing the execution time by 21% on average. Compared to AutoTiering, MTM spends similar time in profiling but 25% faster in migration, and reduces the execution time by 19% on average.

Memory bandwidth usage of MTM. We study the impact of memory bandwidth when using MTM. We measure the memory bandwidth with Intel PCM [24] and compare with NUMA first-touch, which does not have page migration. With NUMA first-touch, memory pages are allocated in local DRAM first. Once the local DRAM is full, the remaining pages are allocated in the order of local PM (tier3), remote

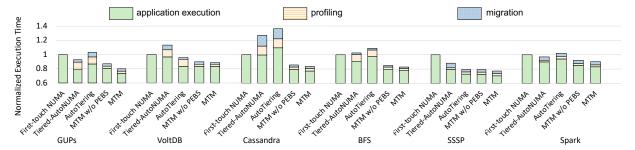


Figure 6: Breakdown of application execution time. Each bar is normalized by the execution time of first-touch NUMA.

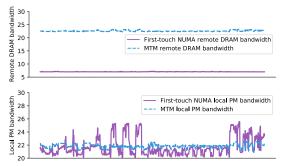


Figure 7: Memory bandwidth utilization with MTM and NUMA first-touch

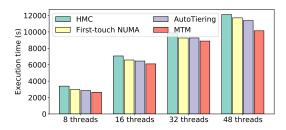


Figure 8: Execution time of VoltDB with different number of client threads.

DRAM (tier2) and remote PM (tier4). Due to space limitation, Figure 7 only shows the bandwidth comparison on remote DRAM (tier2) and local PM (tier3). NUMA first-touch cannot utilize memory bandwidth offered by remote DRAM, while accesses pages on local PM, leading to under-utilization of remote DRAM. MTM is able to utilize memory bandwidth from all tiers.

Scalability of MTM. We evaluate the scalability of MTM with VoltDB by increasing the number of clients. We see the memory consumption increases from 300GB to 1.2TB. We compare the performance of MTM, HMC, first-touch NUMA, and AutoTiering. We evaluate AutoTiering since it has the second-best performance among all we evaluate. Figure 8 shows that MTM consistently outperforms HMC, first-touch NUMA, and AutoTiering by 19%, 10%, and 8% on average.

Evaluation with different THP settings. Figure 9 shows the results using madvise and always as THP setting. We evaluate SSSP, because it has the largest memory consumption among all evaluated applications. The results confirm that MTM consistently outperforms other solutions.

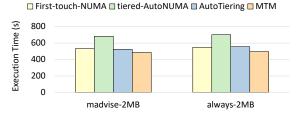


Figure 9: SSSP with MTM and different THP configurations. Table 3: The number of memory accesses when using VoltDB.

# of memory accesses	Tiered-AutoNUMA	AutoTiering	MTM-w/o-PEBS	MTM
tier 1	248M	258M	295M	293M
tier 2	15M	34M	198K	220K
tier 3	60M	30M	9M	10M
tier 4	704K	2.5M	92K	205K

9.2. Adaptive Profiling in MTM

9.2.1. Statistic of Profiling

Number of memory accesses. We count the number of memory accesses in each memory tier when running VoltDB. We only report the results for tiered-AutoNUMA, MTM-w/o-PEBS, and MTM because only they can leverage all four memory tiers for migration. We use Intel Processor Counter Monitor [24] to count the number of memory accesses and exclude memory accesses caused by page migration. This counting method allows us to evaluate the number of memory accesses from the application (not from page migration). Table 3 shows the results where there are eight VoltDB clients residing in one processor, and the view of tiered memory is defined from their view. Table 3 shows that with MTM, the number of memory accesses in the fastest memory tier (tier 1) is 20% and 14% more than with tiered-AutoNUMA and AutoTiering. This indicates that MTM effectively migrates frequently accessed pages to the fast tier for high performance.

Statistics of memory regions. On average, the number of

Table 4: Statistics of forming memory regions using MTM. "MR" and "PI" stand for memory regions and profiling interval.

	# of PI	avg # of MR merged in a PI	avg # of MR splited in a PI	avg # of MR in a PI
GUPS	1000	26.5	20.4	2410
VoltDB	800	53.2	50.6	1274
Cassandra	1600	42.5	63.2	1073
BFS	120	16.7	17.3	2574
SSSP	360	21.3	18.2	2492
Spark	800	35.9	32.5	1852

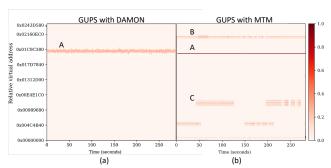


Figure 10: The heatmap of memory accesses in GUPS using (a) DAMON and (b) MTM under the same profiling overhead (5%).

memory regions merged and split in a profiling interval is 3.4% of all memory regions, as reported in Table 4. Compared with DAMON, MTM has less merging/splitting because of performance counter guidance and effective formation of memory regions. For example, GUPS with MTM has 12% less merging and 32% less splitting than with DAMON.

9.2.2. Effectiveness of Adaptive Profiling

Comparison with tiered-AutoNUMA and Thermostat. We study profiling quality and overhead, and compare MTM with two sampling-based profiling methods: one used in tiered-AutoNUMA and AutoTiering, and the other used in Thermostat. We use tiered-AutoNUMA and Thermostat, and replace their migration with MTM's, which excludes the impact of migration on performance, and is fair.

The profiling method in tiered-AutoNUMA randomly chooses a 256MB virtual address space in each profiling interval, and then manipulates the present bit in each PTE in the chosen address space. This method tracks page accesses by counting page faults. The profiling method in Thermostat randomly chooses a 4KB page out of each 2MB memory region for profiling. This method manipulates page protection bits in PTE and leverages protection faults to count accesses.

Figure 11 shows that MTM outperforms tiered-AutoNUMA and Thermostat by 17% and 7%, respectively. The profiling overhead in Thermostat is $6\times$ higher than in tiered-AutoNUMA, because the number of sampled pages for profiling in Thermostat is much larger than that in tiered-AutoNUMA. The profiling overhead in Thermostat is $2.5\times$ higher than in MTM, because manipulating reserved bits in PTE and counting protection faults in Thermostat is more expensive than scanning PTEs in tiered-AutoNUMA and MTM. With tiered-AutoNUMA, the application run time is longer than with MTM by 22%. This indicates that random sampling-based profiling is not as effective as our adaptive profiling.

Comparison with DAMON. We compare DAMON and MTM in terms of profiling quality. We use GUPS that randomly accesses 512GB memory with 24 threads. Specifically, 20% of GUPS' memory footprint is randomly selected as the hotset. Each thread randomly updates the memory 1M times, and 80% of them happens in the hotset. 1M-updates repetitively happens, so that there is variance on hot pages. Using

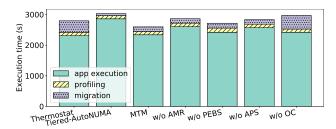


Figure 11: Evaluation of the effectiveness of adaptive memory regions ("AMR"), adaptive page sampling ("APS"), and profiling overhead control ("OC") using VoltDB.

knowledge on GUPS, we know there are three hot data objects: the indexes to access the hotset (labeled as "A"), the hotset information (labeled as "B"), and the hotset (labeled as "C").

Figure 10 shows results. (1) MTM finds C, while DAMON cannot because of its slow response. (2) MTM finds B, but DAMON cannot because its memory regions are initially set based on the virtual memory area tree, which is too coarsegrained to capture B even after splitting regions. (3) DAMON and MTM find A, but the scope of A found by MTM is correctly narrowed down, which reduces unneeded migration.

We further evaluate the following profiling techniques and disable them one by one to examine performance difference.

Effectiveness of adaptive memory regions. We disable adaptive memory regions but respect the profiling overhead constraint. Figure 11 shows the application execution time is 22% longer, although the overhead constraint is met. Such a loss indicates that hot memory regions are not effectively identified without adaptive regions and hence placed in slow memory.

Effectiveness of adaptive page sampling. This technique distributes PTE scans between memory regions by using time-consecutive profiling, which includes information on temporal locality. We disable it and randomly distribute PTE scans between memory regions, and observe 21% performance loss.

Evaluation of profiling overhead control. We set $\tau_1 = \tau_2 = 0$ (i.e., no merging/splitting memory regions) and observe that the profiling time is increased by $3 \times$ in Figure 11.

Evaluation of performance-counter assistance. MTM-w/o-PEBS in Figure 11 does not use performance counters to guide profiling. It performs worse than MTM because PEBS improves profiling quality. For VoltDB, it performs 4% worse. The overhead of PEBS is less than 1%.

9.2.3. Sensitivity Study for Memory Profiling Impacts of profiling overhead. We study the relationship between the profiling overhead and profiling quality. Figure 12 shows the results. We set profiling interval length as 5s, and test a set of profiling overhead targets. As the overhead target increases from 1% to 10%, the application execution time is reduced by 12%. Such performance improvement comes from the improvement of profiling quality when trading profiling overhead (by taking more samples) for profiling quality. However, taking more samples (or using a larger overhead target) does not necessarily lead to better performance. As shown in Figure 12,

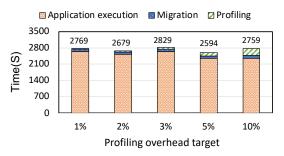


Figure 12: Execution time with various profiling overhead targets. We evaluate voltDB with MTM.

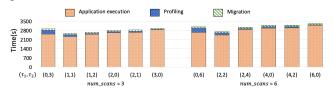


Figure 13: Execution time with various τ_1 and τ_2 . We execute voltDB with MTM.

the application execution time increases by 7% as the profiling overhead target increases from 5% to 10%. We use 5% as the profiling overhead target by default, which universally works well for all applications in our study.

Impacts of profiling thresholds τ_1 and τ_2 . We study the relationship between memory region merging/split thresholds (τ_1 and τ_2) and profiling quality. The increase of τ_1 leads to aggressive merging of memory regions, and the decrease of τ_2 leads to aggressive split of memory regions. We change τ_1 and τ_2 and measure performance. Figure 13 shows the results.

With num_scans is set as 3, $\tau_1 = 1$ and $\tau_2 = 2$ lead to the best performance, outperforming other configurations of τ_1 and τ_2 by at least 7%. The execution time of voltDB increases as τ_1 increases. We observe that more aggressive merging of memory region leads to inaccurate profiling results: In the extreme case, when $tau_1 = num_scans$, there is only one memory region. The inaccurate profiling results leads to bad application performance. Both profiling overhead and execution time increase when τ_2 decreases. With aggressive split of memory regions, MTM uses a long time to capture memory access pattern of the application, which increases profiling overhead and loses profiling quality. We observe the same trend when num_scans is set as 6.

9.3. Sensitivity study for Migration Strategy

Impact of memory promotion threshold α . The memory promotion threshold α is used in Equation 2 to balance the contributions of the historical profiling results and current profiling results. When $\alpha=0$, MTM makes migration decisions only based on the historic profiling result. When $\alpha=1$, MTM ignores historic information. We set α with different values for sensitivty study. Figure 14 demonstrates that different applications have different sensitivity to α . Using both historic

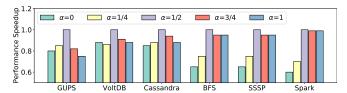


Figure 14: Performance variance when changing α . The performance is normalized by that of the default setting $\alpha = 1/2$.

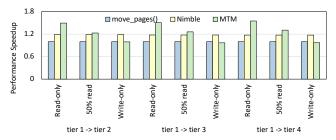


Figure 15: Performance comparison between Nimble, $move_pages()$ and MTM. The performance is normalized by the performance of $move_pages()$.

and current profiling results are generally helpful for most of applications (e.g., GUPS, voltDB, Cassandra, BFS and SSSP). In contrast, Spark is not sensitive to the inclusion of historical profiling results. This may be because of lack of temporal locality in Spark.

9.4. Migration Mechanism in MTM

Effectiveness of Migration Mechanism We use three microbenchmarks to evaluate the migration mechanisms in MTM, Nimble [50], and <code>move_pages()</code> in Linux: sequential read-only, 50% read (i.e., a sequential read followed by an update on an array element), and 100% sequential write on a 1GB array. The array is allocated and touched in a memory tier, and then migrated to another. Figure 15 shows the results. Migrating pages between the tiers 1 and 2, MTM's mechanism performs 40%, 23%, and -0.5% better than <code>move_pages()</code>, and performs 26% 4% and -6% better than Nimble, for the three benchmarks respectively. We see the same trend in other tiers. In general, for read-intensive pages, MTM's mechanism brings large benefit; for write-intensive pages, MTM performs similar to <code>move_pages()</code> and Nimble.

Overhead of user-space page fault handler. The user-space page fault handler is used in $move_memory_regions()$ to track writes and enable asynchronous page copying. We measure its overhead by repeatedly triggering faults. On average, it takes about $40\mu s$ to handle a page fault. Furthermore, we compare the performance of $move_memory_regions()$ without the user-space page fault handler (i.e., disable userfd), with it (but handling all userfd on the critical execution path), and with MTM.

Figure 16 shows the results. We use the same microbenchmarks for evaluation. The read-only microbenchmark does not trigger the user-space page fault handling. In the 50%-read microbenchmark, a part of the overhead of the user-space page

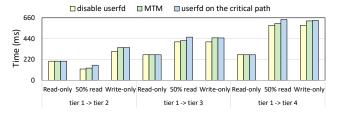


Figure 16: Performance comparison between disabling userfd, MTM and handle userfd on the critical path.

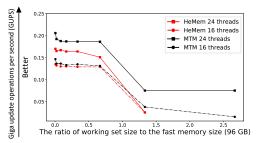


Figure 17: Evaluation of MTM on two-tiered HM and comparison with HeMem.

fault handling can be hidden from the critical path. MTM outperforms "userfd on the critical path" by 6% at most. The overhead of the user-space page fault handling in MTM is 3% on average. In write-only cases, the overhead of the user-space page fault handling are all on the critical path. The overhead of the user-space page fault handling in MTM is 7% on average.

9.5. MTM with two-tiered HM

The evaluation is performed on a single socket with two tiers, using GUPS [14] as in HeMem [41]. Figure 17 reports using 16 and 24 application threads. The results show that when the working set size fits in the fast memory tier (i.e., the ratio in the x axis is smaller than 1.0), MTM performs similarly to HeMem at 16 threads but better at 24 threads. Once the working set size exceeds the fast memory, HeMem fails to sustain performance at 24 threads while MTM still sustains higher performance at 24 threads than 16 threads. MTM performs better because its profiling method can quickly adapt to changes in memory accesses and identify more hot pages.

9.6. MTM with Phase-change Workload

we introduce different execution phases into GUPS. Specifically, we concatenate four GUPS execution blocks into a single workload. Different GUPS blocks have different memory access patterns. This allows us to build a phase-change workload with the apriori knowledge on page hotness.

Figure 18 shows the profiling accuracy of MTM, DAMON and Tiered-AutoNUMA. The results indicate that Tiered-AutoNUMA cannot capture phase changes well. The profiling accuracy of MTM largely outperforms that of Tiered-AutoNUMA by 2.7× on average. DAMON can detect phase changes. However, DAMON shows slow response to phase changes. DAMON takes 3X longer time than MTM to achieve 50% profiling accuracy. This is because DAMON builds mem-

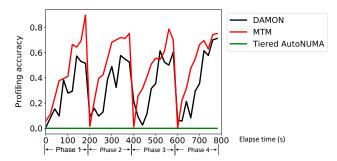


Figure 18: Profiling accuracy with DAMON, MTM and Tiered AutoNUMA. We use phase-change GUPS

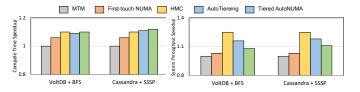


Figure 19: Completion time and system throughput for application co-run. The results are normalized by those of MTM

ory region randomly. In contrast, with assists from PEBS for adaptive profiling, MTM can quickly detect potentially hot memory regions and quickly adjust the memory region size. It achieves 80% accuracy within 50s in each execution phase.

We further compare execution times for different page migration strategies. MTM outperforms NUMA frist-touch, HMC, AutoTiereing, and Tiered AutoNUMA by 15%, 17%, 23%, and 26% respectively.

9.7. MTM with Application Co-runs

We launch two applications simultaneously. We report system throughput (i.e., the number of write bytes caused by workload execution per second) and the completion time of co-applications. We test two co-run workloads, i.e., VoltDB with BFS co-run, and Cassandra with SSSP co-run. Figure 19 shows the result. MTM outperforms NUMA frist-touch, HMC, AutoTiereing, and Tiered AutoNUMA by 6%, 12%, 10%, 11% respectively in terms of average completion time. MTM outperforms NUMA frist-touch, HMC, AutoTiereing, and Tiered AutoNUMA by 3%, 25%, 18%, 11% in system throughput.

Currently, MTM handles application co-run by profiling each application and making page migration decisions independently, which loses a global view of the entire system. We leave the page placement optimization across applications as our future work.

10. Conclusions

Emerging multi-tiered large memory systems calls for rethinking memory profiling and migration for high performance. We present MTM, a page management system customized for large memory systems based on three design principles of improving profiling quality, building a universal page migration policy and huge page awareness. Our extensive evaluation of MTM against multiple state-of-the-art solutions shows that MTM can largely outperform existing solutions by up to 42%.

References

- [1] Compute Express Link Industry Members. https://www.computeexpresslink.org/members, 2021.
- [2] Neha Agarwal and Thomas F. Wenisch. Thermostat: Application-transparent Page Management for Two-tiered Main Memory. In International Conference on Architectural Support for Programming Languages and Operating Systems, 2017.
- [3] Mihnea Andrei, Christian Lemke, Günter Radestock, Robert Schulze, Carsten Thiel, Rolando Blanco, Akanksha Meghlan, Muhammad Sharique, Sebastian Seifert, Surendra Vishnoi, Daniel Booss, Thomas Peh, Ivan Schreter, Werner Thesing, Mehul Wagle, and Thomas Willhalm. Sap hana adoption of non-volatile memory. Proc. VLDB Endow., 10(12), August 2017.
- [4] Julian T. Angeles, Mark Hildebrand, Venkatesh Akella, and Jason Lowe-Power. Investigating Hardware Caches for Terabyte-scale NVDIMMs. In Annual Non-Volatile Memories Workshop, 2021.
- [5] Apache. Open Source NoSQL Database. https://cassandra.apache.org/, 2021.
- [6] Cheng Chen, Jun Yang, Mian Lu, Taize Wang, Zhao Zheng, Yuqiang Chen, Wenyuan Dai, Bingsheng He, Weng-Fai Wong, Guoan Wu, Yuping Zhao, and Andy Rudoff. Optimizing In-Memory Database Engine for AI-Powered Online Decision Augmentation Using Persistent Memory. In *Proceedings of the VLDB Endowment*, 2021.
- [7] Jinyoung Choi, Sergey Blagodurov, and Hung-Wei Tseng. Dancing in the dark: Profiling for tiered memory. In 2021 IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2021.
- [8] Brian F. Cooper, Adam Silberstein, Erwin Tam, Raghu Ramakrishnan, and Russell Sears. Benchmarking Cloud Serving Systems with YCSB. In Proceedings of the 1st ACM Symposium on Cloud Computing, 2010.
- [9] J. Corbet. AutoNUMA: the Other Approach to NUMA Scheduling. http://lwn.net/Articles/488709.
- [10] Laxman Dhulipala, Charles McGuffey, Hongbo Kang, Yan Gu, Guy E. Blelloch, Phillip B. Gibbons, and Julian Shun. Sage: Parallel semi-asymmetric graph algorithms for nvrams. *Proc. VLDB Endow.*, 13(9):1598–1613, May 2020.
- [11] Thaleia Dimitra Doudali, Sergey Blagodurov, Abhinav Vishnu, Sudhanva Gurumurthi, and Ada Gavrilovska. Kleio: A Hybrid Memory Page Scheduler with Machine Intelligence. In *International Symposium on High-Performance Parallel and Distributed Computing*, 2019.
- [12] Thaleia Dimitra Doudali, Daniel Zahka, and Ada Gavrilovska. Cori: Dancing to the right beat of periodic data movements over hybrid memory systems. In 2021 IEEE International Parallel and Distributed Processing Symposium (IPDPS), pages 350–359, 2021.
- [13] Gurbinder Gill, Roshan Dathathri, Loc Hoang, Ramesh Peri, and Keshav Pingali. Single machine graph analytics on massive datasets using intel optane dc persistent memory. *Proc. VLDB Endow.*, 13(8):1304–1318, April 2020.
- [14] GUPS. Giga Updates Per Second. http://icl.cs.utk.edu/ projectsfiles/hpcc/RandomAccess/, 2021.
- [15] Ewan Higgs. Spark-terasort. https://github.com/ehiggs/ spark-terasort, 2018.
- [16] Mark Hildebrand, Julian T. Angeles, Jason Lowe-Power, and Venkatesh Akella. A Case Against Hardware Managed DRAM Caches for NVRAM Based Systems. In IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2021.
- [17] Mark Hildebrand, Jawad Khan, Sanjeev Trika, Jason Lowe-Power, and Venkatesh Akella. AutoTM: Automatic Tensor Movement in Heterogeneous Memory Systems Using Integer Linear Programming. In International Conference on Architectural Support for Programming Languages and Operating Systems, 2020.
- [18] Takahiro Hirofuchi and Ryousei Takano. Raminate: Hypervisor-based virtualization for hybrid main memory systems. In *Proceedings of the* Seventh ACM Symposium on Cloud Computing, 2016.
- [19] Amazon Inc. Amazon EC2 High Memory Instances with 6, 9, and 12 TB of Memory, Perfect for SAP HANA. https://aws.amazon.com/blogs/aws/now-available-amazon-ec2high-memory-instances-with-6-9-and-12-tb-of-memory-perfectforsap-hana/, September 2018.
- [20] Intel. Intel Memory Optimizer. https://github.com/intel/memory-optimizer, 2019.
 [21] Intel Intel Memory Optimizer.
- [21] Intel. Intel Memory Optimizer. https://github.com/intel/ memory-optimizer, 2019.
- [22] Intel. Autonuma: Optimize Memory Placement in Memory Tiering System. https://lwn.net/Articles/803663/, 2020.
- [23] Intel. Intel Memory Tiering. https://lwn.net/Articles/802544/, 2021.

- [24] Intel. Intel Processor Counter Monitor. https://github.com/opcm/pcm, 2021.
- [25] Sudarsun Kannan, Ada Gavrilovska, Vishal Gupta, and Karsten Schwan. HeteroOS: OS Design for Heterogeneous Memory Management in Datacenter. In *International Symposium on Computer* Architecture, 2017.
- [26] Sudarsun Kannan, Yujie Ren, and Abhishek Bhattacharjee. KLOCs: Kernel-Level Object Contexts for HeterogeneousMemory Systems. In International Conference on Architectural Support for Programming Languages and Operating Systems, 2021.
- [27] Jonghyeon Kim, Wonkyo Choe, and Jeongseob Ahn. Exploring the Design Space of Page Management for Multi-Tiered Memory Systems. In USENIX Annual Technical Conference, 2021.
- [28] Jonghyeon Kim, Wonkyo Choe, and Jeongseob Ahn. Exploring the Design Space of Page Management for Multi-Tiered Memory Systems. In 2021 USENIX Annual Technical Conference (USENIX ATC 21), 2021
- [29] Andres Lagar-Cavilla, Junwhan Ahn, Suleiman Souhlal, Neha Agarwal, Radoslaw Burny, Shakeel Butt, Jichuan Chang, Ashwin Chaugule, Nan Deng, Junaid Shahid, Greg Thelen, Kamil Adam Yurtsever, Yu Zhao, and Parthasarathy Ranganathan. Software-defined far memory in warehouse-scale computers. In Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019.
- [30] Scott T. Leutenegger and Daniel Dias. A Modeling Study of the TPC-C Benchmark. In SIGMOD Record, 1993.
- [31] Huaicheng Li, Daniel S. Berger, Stanko Novakovic, Lisa Hsu, Dan Ernst, Pantea Zardoshti, Monish Shah, Ishwar Agarwal, Mark D. Hill, Marcus Fontoura, and Ricardo Bianchini. First-generation Memory Disaggregation for Cloud Platforms, 2022.
- [32] Linux. Automatic NUMA Balancing. https://www.linux-kvm. org/images/7/75/01x07b-NumaAutobalancing.pdf, 2014.
- [33] Lei Liu, Shengjie Yang, Lu Peng, and Xinyu Li. Hierarchical hybrid memory management in os for tiered memory systems. *IEEE Transactions on Parallel and Distributed Systems*, 30(10):2223–2236, 2019
- [34] Hasan Al Maruf and Mosharaf Chowdhury. Effectively prefetching remote memory with leap. In 2020 USENIX Annual Technical Conference (USENIX ATC 20), pages 843–857. USENIX Association, July 2020
- [35] Hasan Al Maruf, Hao Wang, Abhishek Dhanotia, Johannes Weiner, Niket Agarwal, Pallab Bhattacharya, Chris Petersen, Mosharaf Chowdhury, Shobhit Kanaujia, and Prakash Chauhan. TPP: Transparent Page Placement for CXL-Enabled Tiered Memory, 2022.
- [36] Bao Nguyen, Hua Tan, and Xuechen Zhang. Large-scale adaptive mesh simulations through non-volatile byte-addressable memory. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC '17, 2017.
- [37] SeongJae Park, Madhuparna Bhowmik, and Alexandru Uta. DAOS: Data Access-Aware Operating System. In Proceedings of International Symposium on High-Performance Parallel and Distributed Computing (HPDC), 2022.
- [38] SeongJae Park, Yunjae Lee, and Heon Y. Yeom. Profiling dynamic data access patterns with controlled overhead and quality. In *Proceedings* of the 20th International Middleware Conference Industrial Track, Middleware '19, page 1–7, New York, NY, USA, 2019. Association for Computing Machinery.
- [39] I. B. Peng and J. S. Vetter. Siena: Exploring the design space of heterogeneous memory systems. In SC18: International Conference for High Performance Computing, Networking, Storage and Analysis, 2018
- [40] Zhen Peng, Alexander Powell, Bo Wu, Tekin Bicer, and Bin Ren. Graphphi: efficient parallel graph processing on emerging throughputoriented architectures. In Proceedings of the 27th International Conference on Parallel Architectures and Compilation Techniques, pages 1–14, 2018.
- [41] Amanda Raybuck, Tim Stamler, Wei Zhang, Mattan Erez, and Simon Peter. HeMem: Scalable Tiered Memory Management for Big Data Applications and Real NVM. In Proceedings of the ACM SIGOPS 28th Symposium on Operating Systems Principles, 2021.
- [42] Jie Ren, Jiaolin Luo, Kai Wu, Minjia Zhang, Hyeran Jeon, and Dong Li. Sentinel: Efficient Tensor Migration and Allocation on Heterogeneous Memory Systems for Deep Learning. In *International Symposium on High Performance Computer Architecture (HPCA)*, 2021.
- [43] Jie Ren, Minjia Zhang, and Dong Li. HM-ANN: Efficient Billion-Point Nearest Neighbor Search on Heterogeneous Memory. In Conference on Neural Information Processing Systems (NeurIPS), 2020.

- [44] SeongJae Park. DAMON: Data Access Monitor. https://sjp38.github.io/post/damon/.
- [45] Billy Tallis. The Intel Optane Memory (SSD) Preview: 32GB of Kaby Lake Caching. http://www.anandtech.com/show/11210/ the-intel-optane-memory-ssd-review-32gb-of-kaby-lake-caching.
- [46] The Linux Kernel User's and Administrator's Guide. Transparent Hugepage Support. https://www.kernel.org/doc/html/latest/adminguide/mm/transhuge.html.
- [47] voltDB. voltDB. https://www.voltdb.com/, 2021.
- [48] Chenxi Wang, Huimin Cui, Ting Cao, John Zigman, Haris Volos, Onur Mutlu, Fang Lv, Xiaobing Feng, and Guoqing Harry Xu. Panthera: Holistic memory management for big data processing over hybrid memories. In Proceedings of the 40th ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI 2019, 2019.
- [49] Zhen Xie, Wenqian Dong, Jie Liu, Ivy Peng, Yanbao Ma, and Dong Li. MD-HM: Memoization-based Molecular Dynamics Simulations on Big Memory System. In *International Conference on Supercomputing* (ICS), 2021.
- [50] Zi Yan, Daniel Lustig, David Nellans, and Abhishek Bhattacharjee. Nimble Page Management for Tiered Memory Systems. In *International Conference on Architectural Support for Programming Languages and Operating Systems*, 2019.
- [51] Jian Yang, Juno Kim, Morteza Hoseinzadeh, Joseph Izraelevitz, and Steve Swanson. An empirical guide to the behavior and use of scalable persistent memory. In 18th USENIX Conference on File and Storage Technologies (FAST 20), 2020.
- [52] Matei Zaharia, Mosharaf Chowdhury, Tathagata Das, Ankur Dave, Justin Ma, Murphy McCauly, Michael J Franklin, Scott Shenker, and Ion Stoica. Resilient distributed datasets: A fault-tolerant abstraction for in-memory cluster computing. In 9th {USENIX} Symposium on Networked Systems Design and Implementation ({NSDI} 12), pages 15–28, 2012.