Doruk Taneli **LAB1:** 23.02.2018

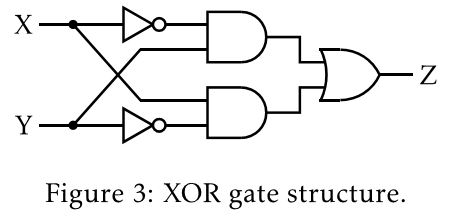
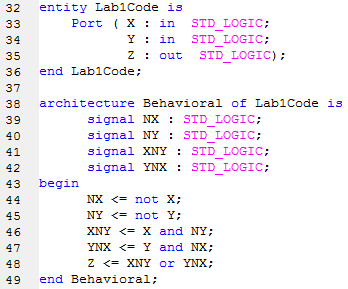
**Getting Familiar with Xilinx ISE Foundation**

**Introduction:**

The aim of this lab is to get familiar with the ISE of the Xilinx design tools by implementing an XOR gate.

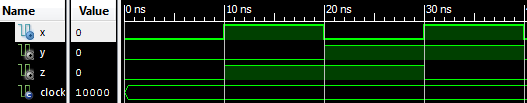
**Methodology:**

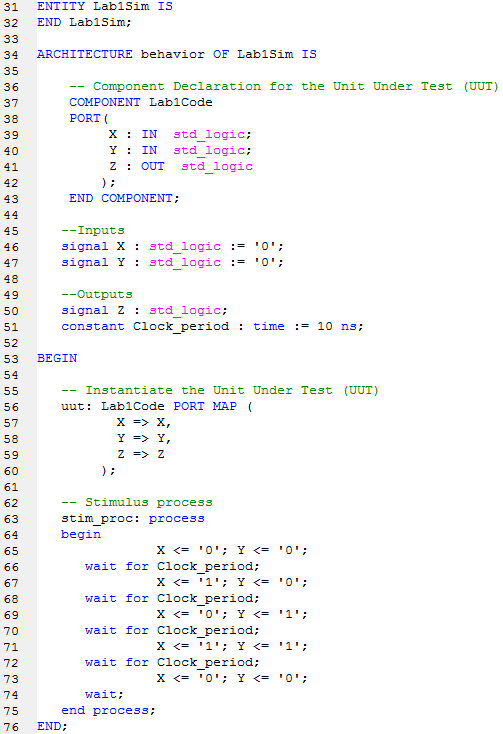
I wrote the code below for the XOR gate in the Figure 3. I implemented the XOR gate using AND, OR, and NOT. The gate takes X and Y as inputs and gives Z as an output. Z returns true only if one of the input is true.



**Experimental Results:**

I mapped X and Y to switches on FPGA board and Z to a LED. The design worked correctly as an XOR gate on the FPGA board. There are 22=4 possible input combinations so 4 test cases are enough. The code and the results of the simulation is shown below.





**Discussion and Conclusion:**

In this lab, I learned how to use Xilinx ISE and Prometheus. I successfully implemented and simulated XOR gate and loaded the bit file to the FPGA board. The things I learned in this lab should greatly help me in the future labs.