Doruk Taneli **LAB5:** 28.04.2018

**Design and Implementation of a Simple**

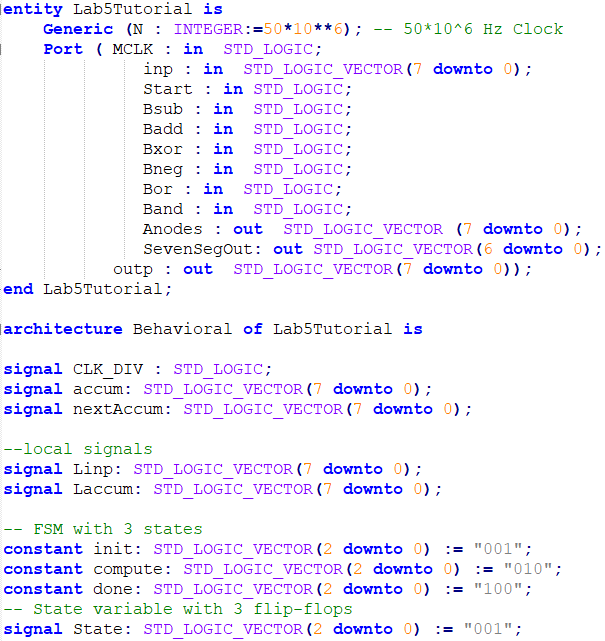
**Digital Accumulator Calculator**

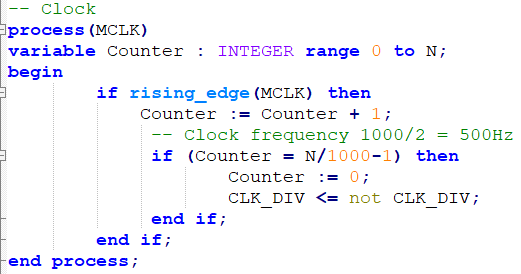
**Introduction:**

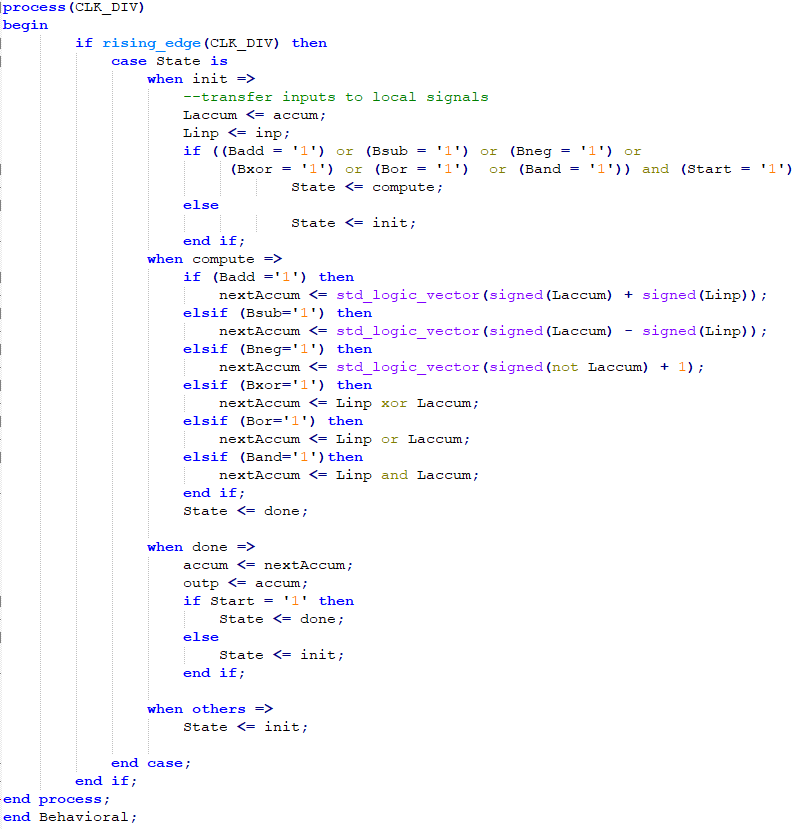
The aim of this lab is to design and implement a digital accumulator calculator as a synchronous sequential circuit.

**Methodology:**

I used the clock given in the example code and used the same states system with the example code. To prevent the digital accumulator from doing multiple calculations in one button press, I used a start switch that needs to be push down and up again before every calculation. Below is the VHDL code.







**Experimental Results:**

I mapped the LEDs, switches and the buttons as instructed in the Laboratory Manual and it performed correctly as expected on the FPGA board.

**Discussion and Conclusion:**

In this lab, I learned how to use states in VHDL which I think will greatly help me in the Lab Project.