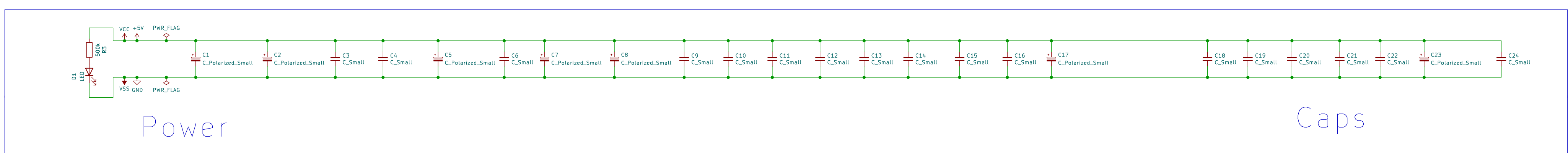
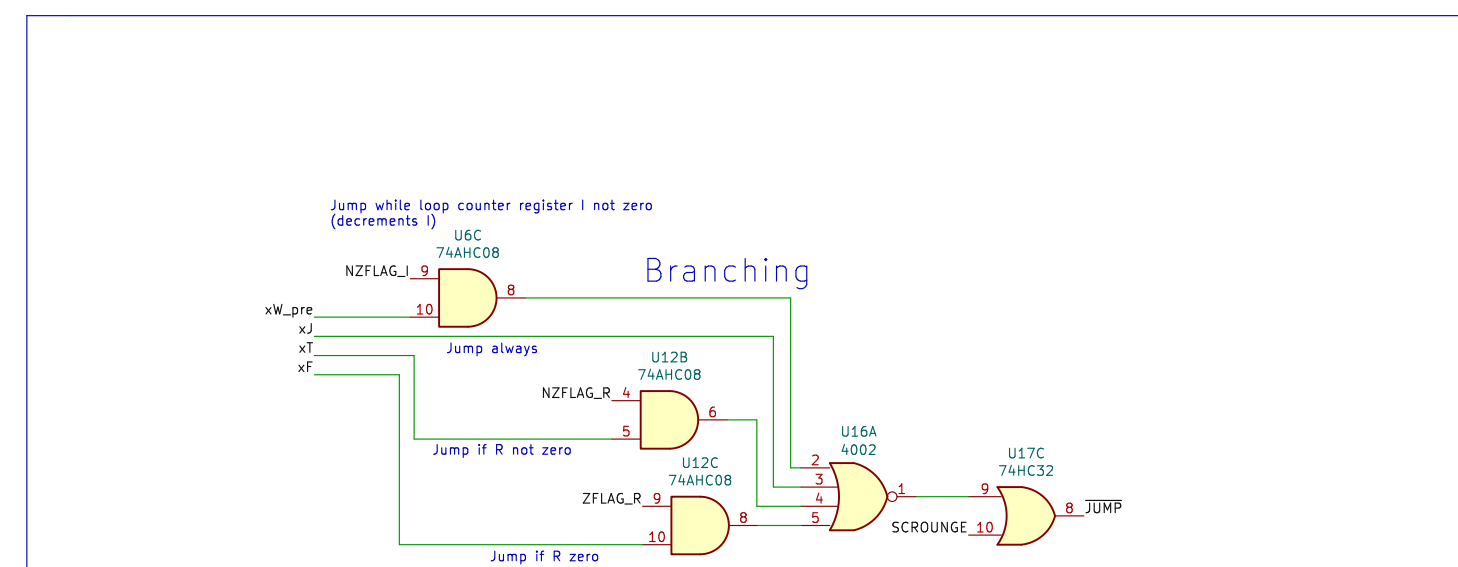


# Sonne-8 Microcontroller Reference Schematics Rev. Myth/LOX



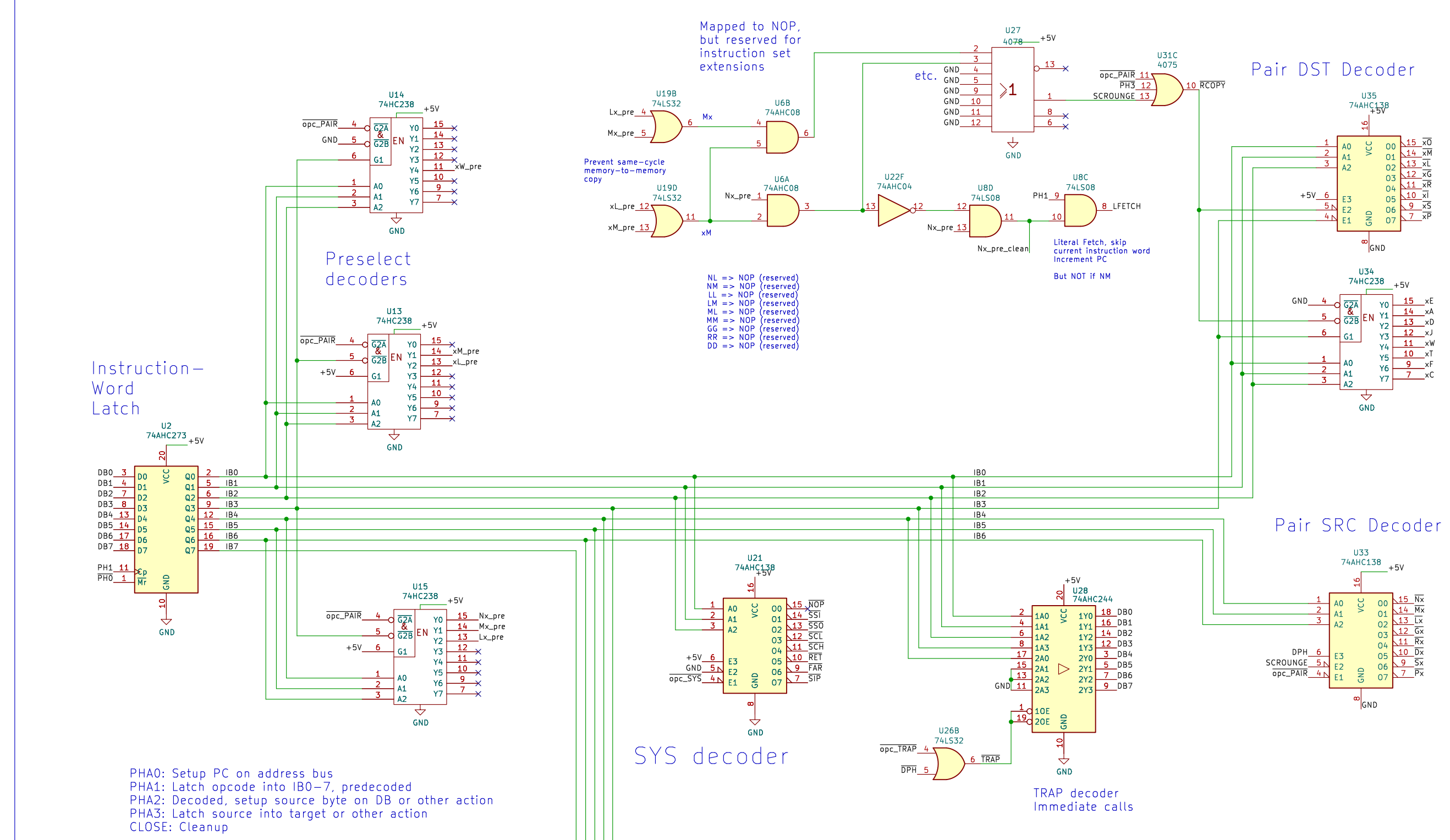
Caps



## Instruction Decoder

Scrounger

Remap 'Scrounger' 66, RR, II etc and impracticable opcodes such as NM

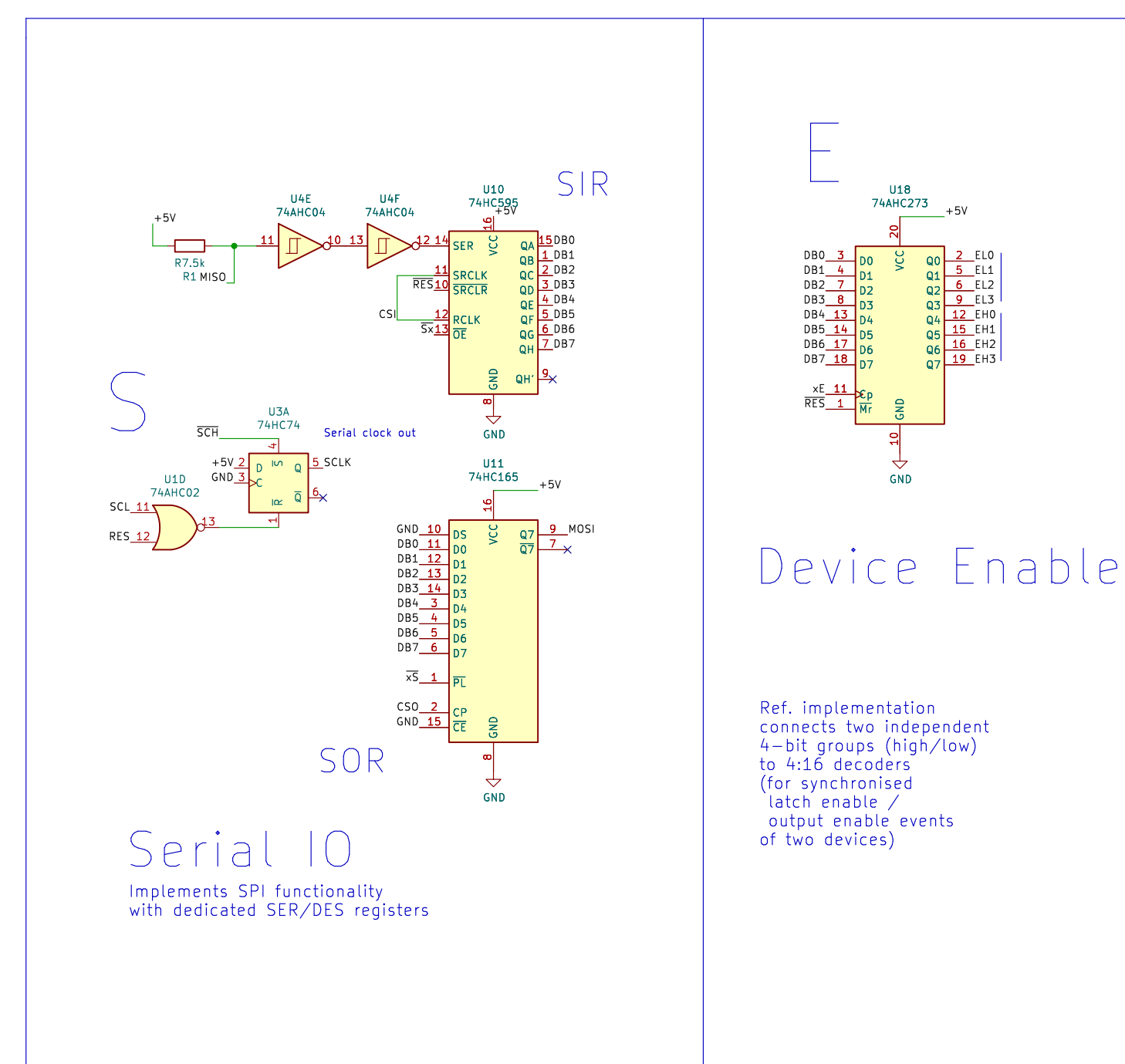
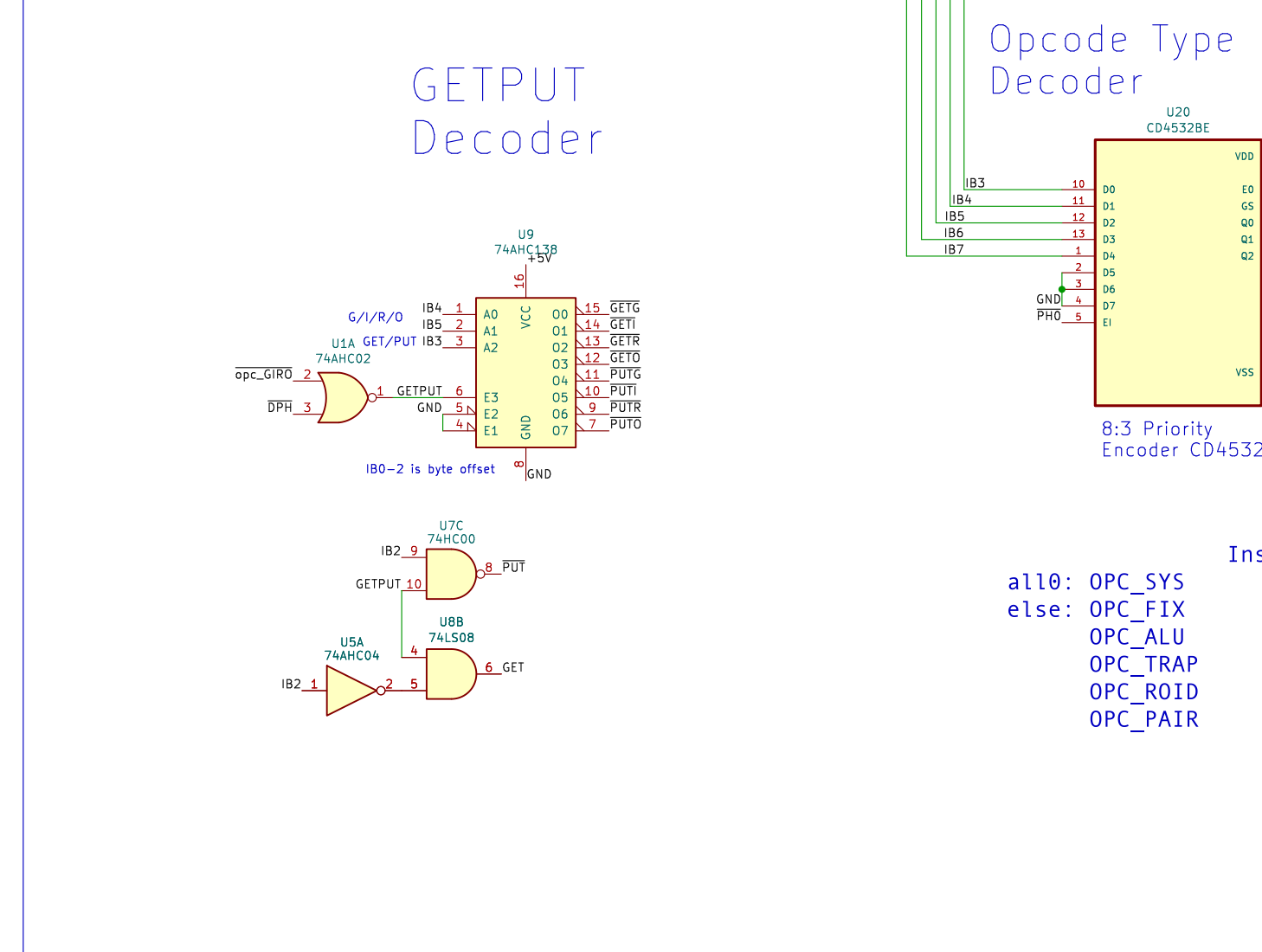


SYS decoder

Opcode Type Decoder

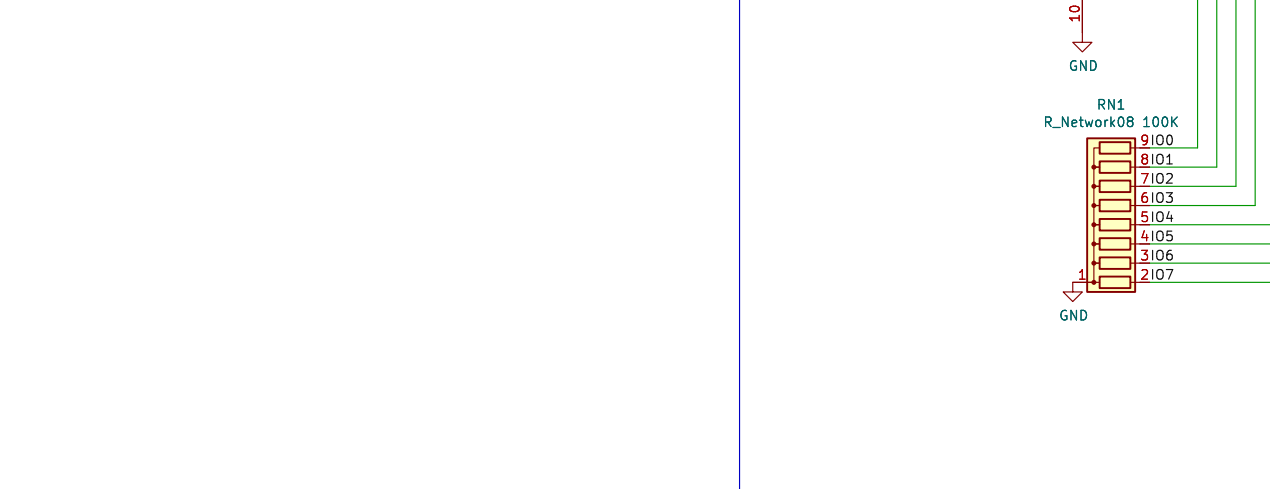
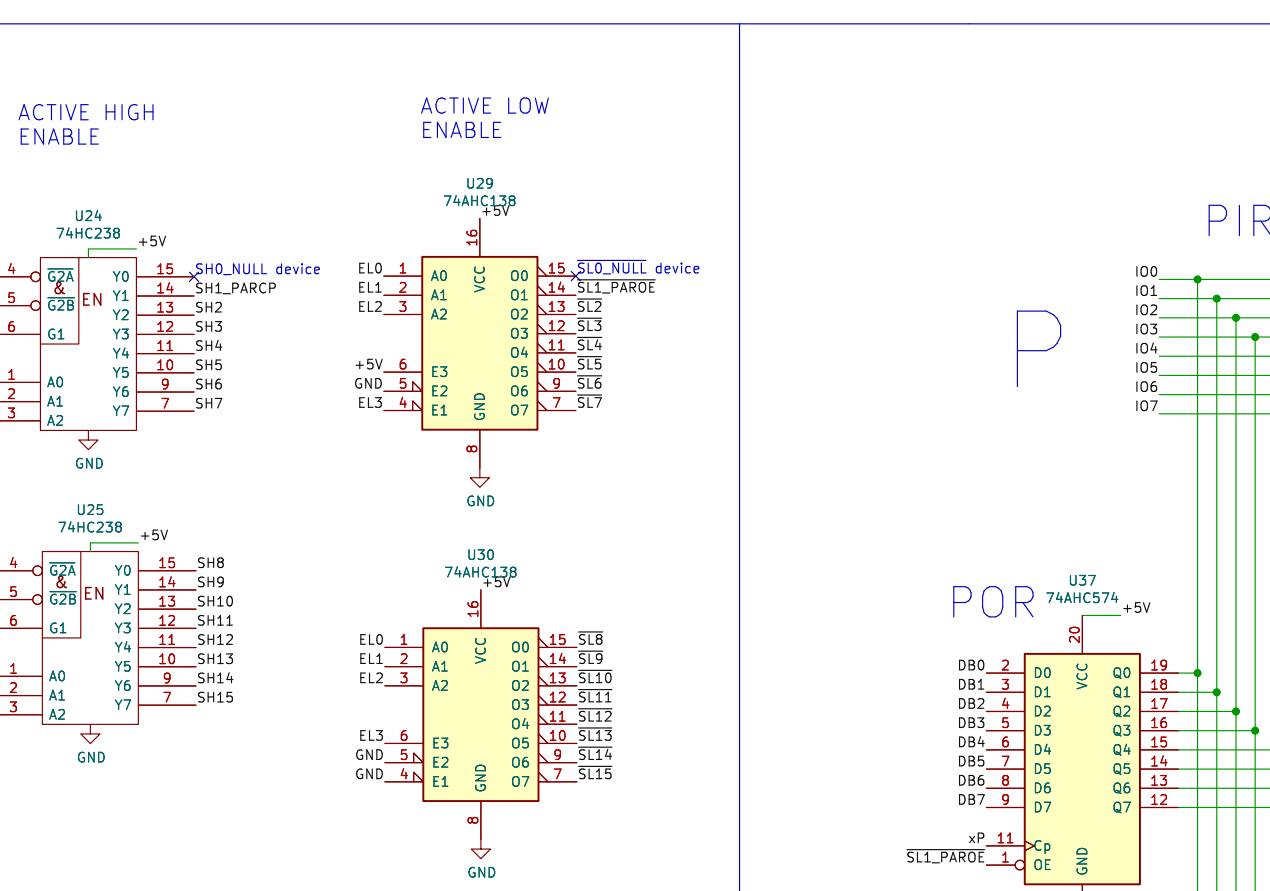
Instruction byte:  
a10: OPC\_SYS  
else: OPC\_FIX  
OPC\_AIU  
OPC\_TRAP  
OPC\_R0ID  
OPC\_PAIR

00000 xxx See table 0 SYS decoder  
00001 xxx b2: extended sign bit b0-LSB  
0001x xxx See table 0 ALU  
001xx xxx b4: MSB b3-0: LSB (remaining bits set 1)  
01xxx xxx db-2 OFFS b3: GET/PUT b4-5: REG(R0ID)  
1xxxx xxx DEST SRC

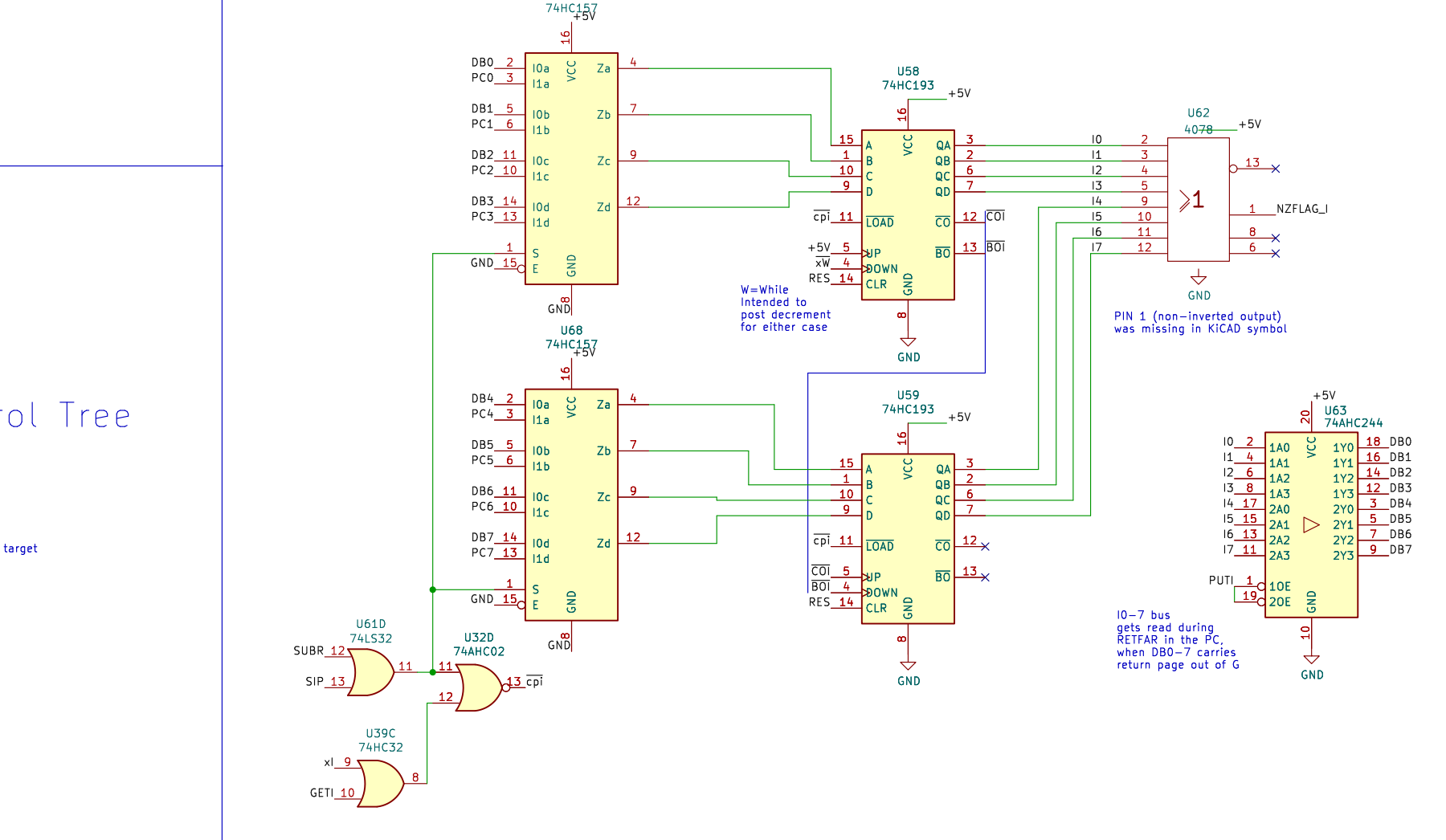


Device Enable

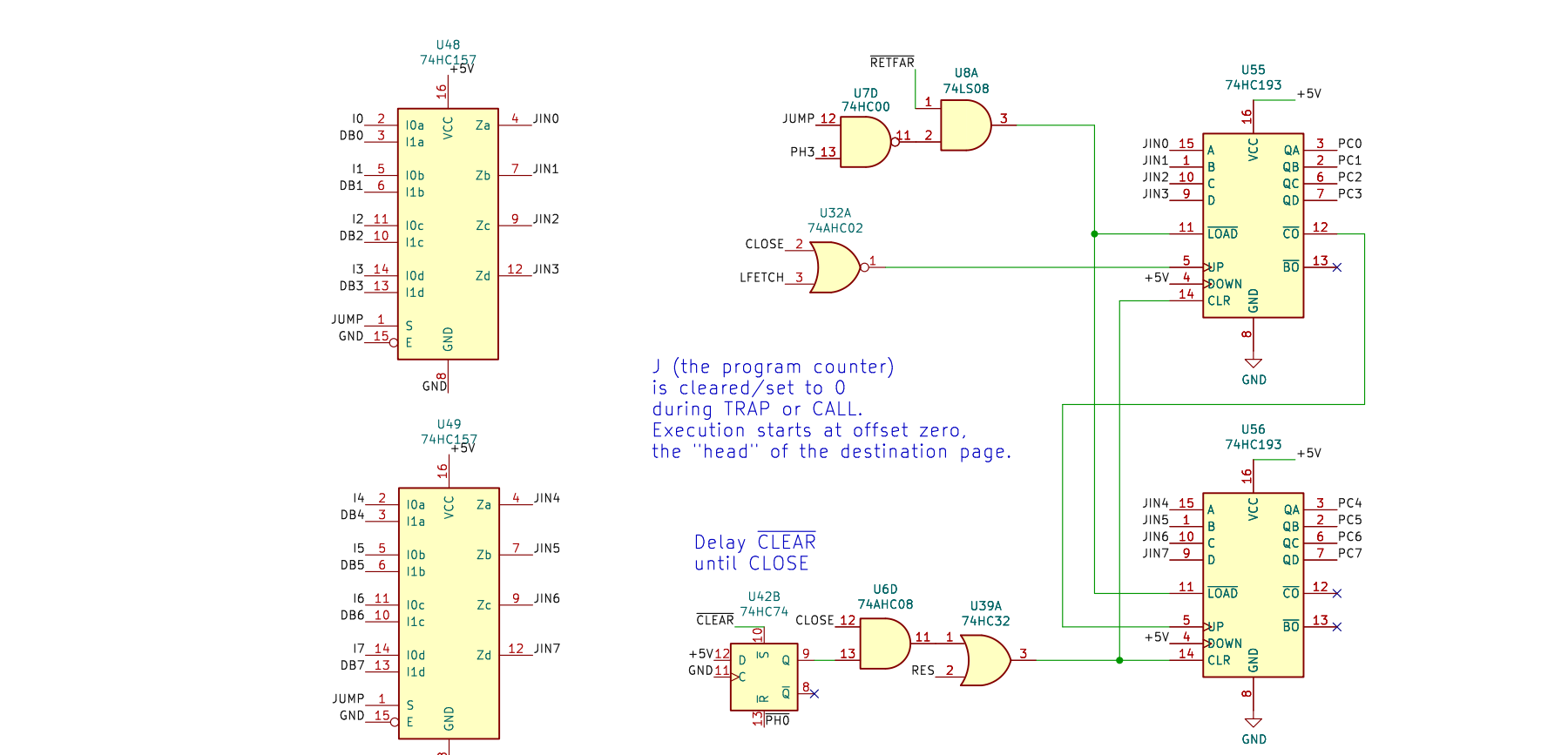
Ref. implementation connects two independent 5-bit decoders (high/low) to 4-16 decoders (for synchronised latch enable / output enable events of two devices)



## I (INNER Loop Register)



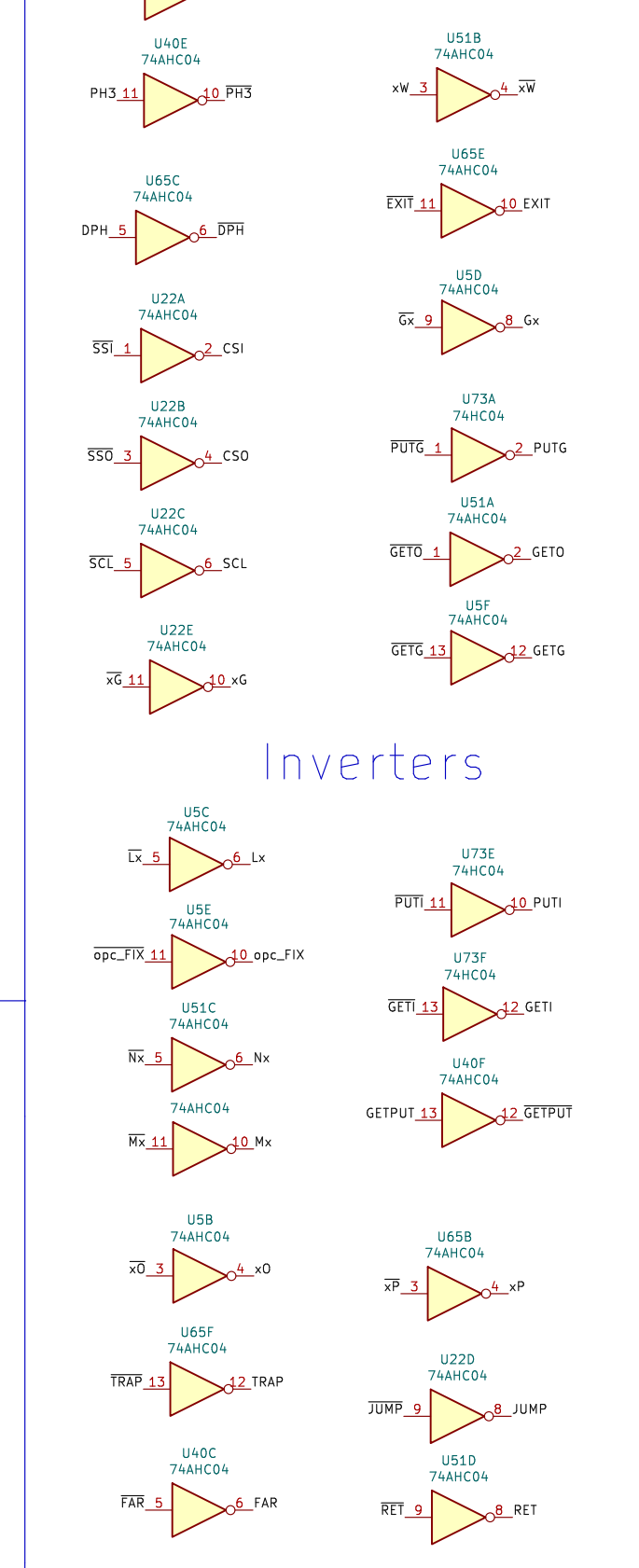
## (PC Program Counter)



## (CODE) Page index



## Inverters



## (LOCAL) Page index (Stack Pointer)



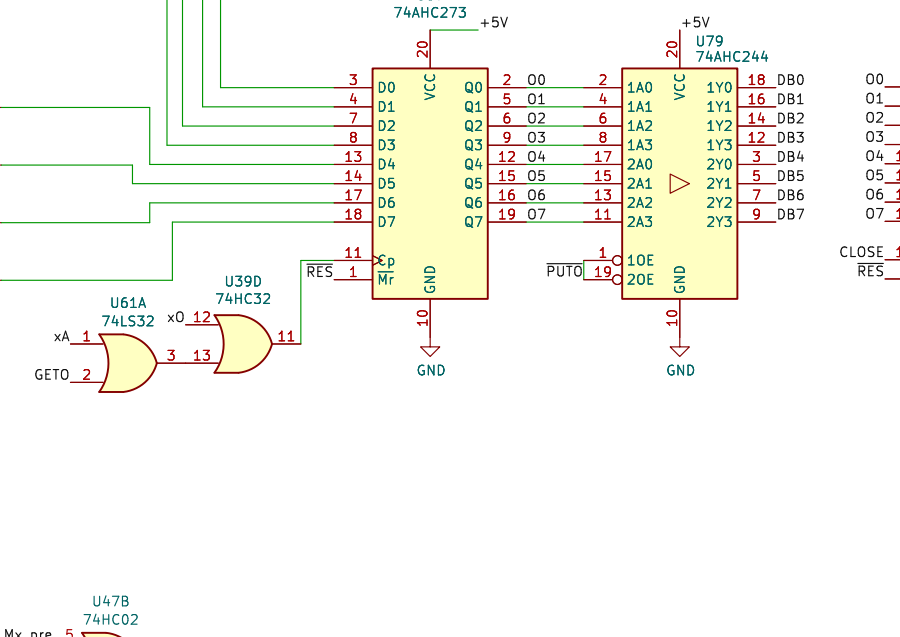
## R-Fix

Hard-coded: R bit 0-2 all 0 replace by 4  
0000 => 0100 +4 R0 (R PLUS 4)  
0001 => 1 P1  
0010 => 2 P2  
0011 => 3 P3  
1000 => 4 R4 (R MINUS 4)  
1001 => 3 R3  
1110 => 2 R2  
1111 => 1 R1  
Else sign extend bit 2

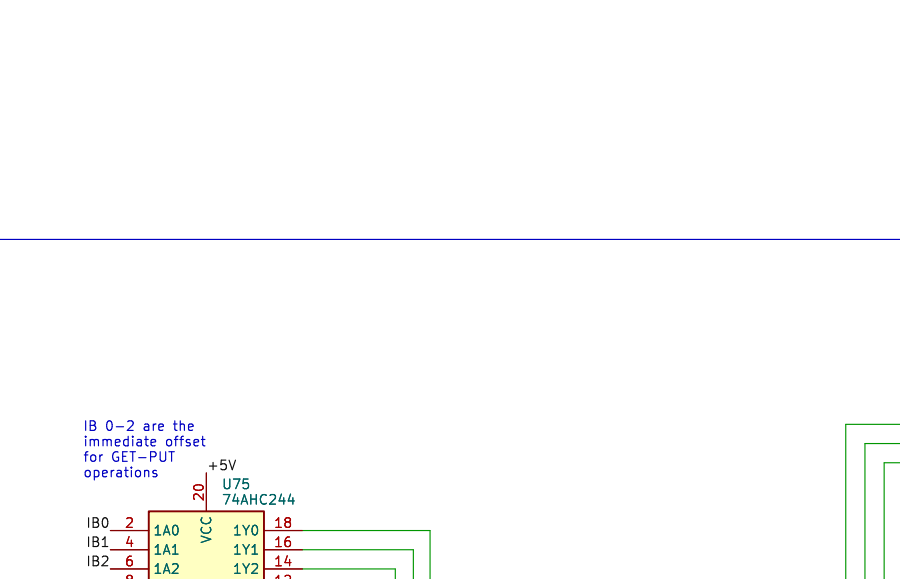
## R(result) Register

Zero detection

## (OFFSET) Operand Register



## (DATA) Page index

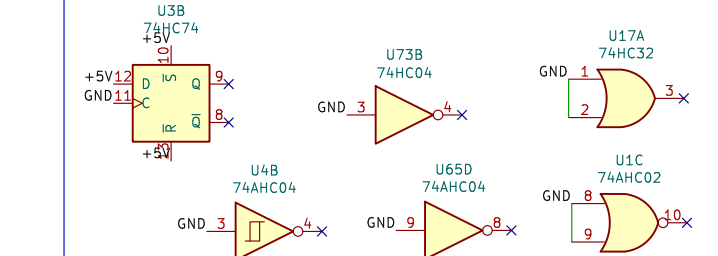


## Low Storage

16K

Memory M

## Spare Units



## Glue Logic

