Myth micro-controller manual

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This document explains the design of a toy 8-bit micro-controller and its programming environment. The homepage for this project is:

`https://github.com/Dosflange/Myth`

1. Serial Communication

The Serial Peripheral Interface (SPI) protocol can be implemented using the device enable register E, serial registers SIR and SOR, and instructions SCL, SCH, SSI, and SSO.

Device Selection

Before communicating with a specific device connected to the serial bus, the corresponding bit pattern representing the device must be set in the E register.

Data Transmission

To transmit data to the selected device, the processor writes the data to be sent into the SOR (Serial Output) register. The SSO (Serial Shift Out) instruction is then used, which clocks the serial output shift register and produces a data bit on the MOSI line. Using the instruction sequence SCL SCH SCL (Serial Clock Low/High), a positive edge clock pulse is generated. As each bit is shifted out, it is sent to the selected device through the serial bus. The passive device processes the transmitted bit and the cycle repeats.

Data Reception

To receive data from an external device, the SSI (Serial Shift In) instruction is used. It clocks

the serial input shift register, allowing the processor to receive one bit of data at a time from the selected device via the MISO line. The received data can then be read from the S register. Clocking is done as for "Data Transmission".

CPOL (Clock Polarity)

The CPOL parameter determines the idle state of the clock signal. The Myth controller provides signals SCL (Serial Clock Low) and SCH (Serial Clock High) instructions which can be used to control the clock signal's state. To configure CPOL=0 (clock idles low), execute SCL to set the clock signal low during the idle state. To configure CPOL=1 (clock idles high), execute SCH to set the clock signal high during the idle state.

CPHA (Clock Phase)

The CPHA parameter determines the edge of the clock signal where data is captured or changed. The Myth controller provides instructions SSI (Serial shift in) and SSO (Serial shift out) to control data transfer on each clock transition. To configure CPHA=0 (data captured on the leading edge), execute SSI before the clock transition to capture the incoming data. To configure CPHA=1 (data captured on the trailing edge), execute SSI after the clock transition to capture the incoming data. Similarly, to transmit data on the leading or trailing edge, execute SSO before or after the clock transition, respectively.

Device Deselection

After data transmission is complete, the selected device needs to be deselected to allow other devices to communicate on the bus. This is done by clearing the bit pattern corresponding to the device in the E register.