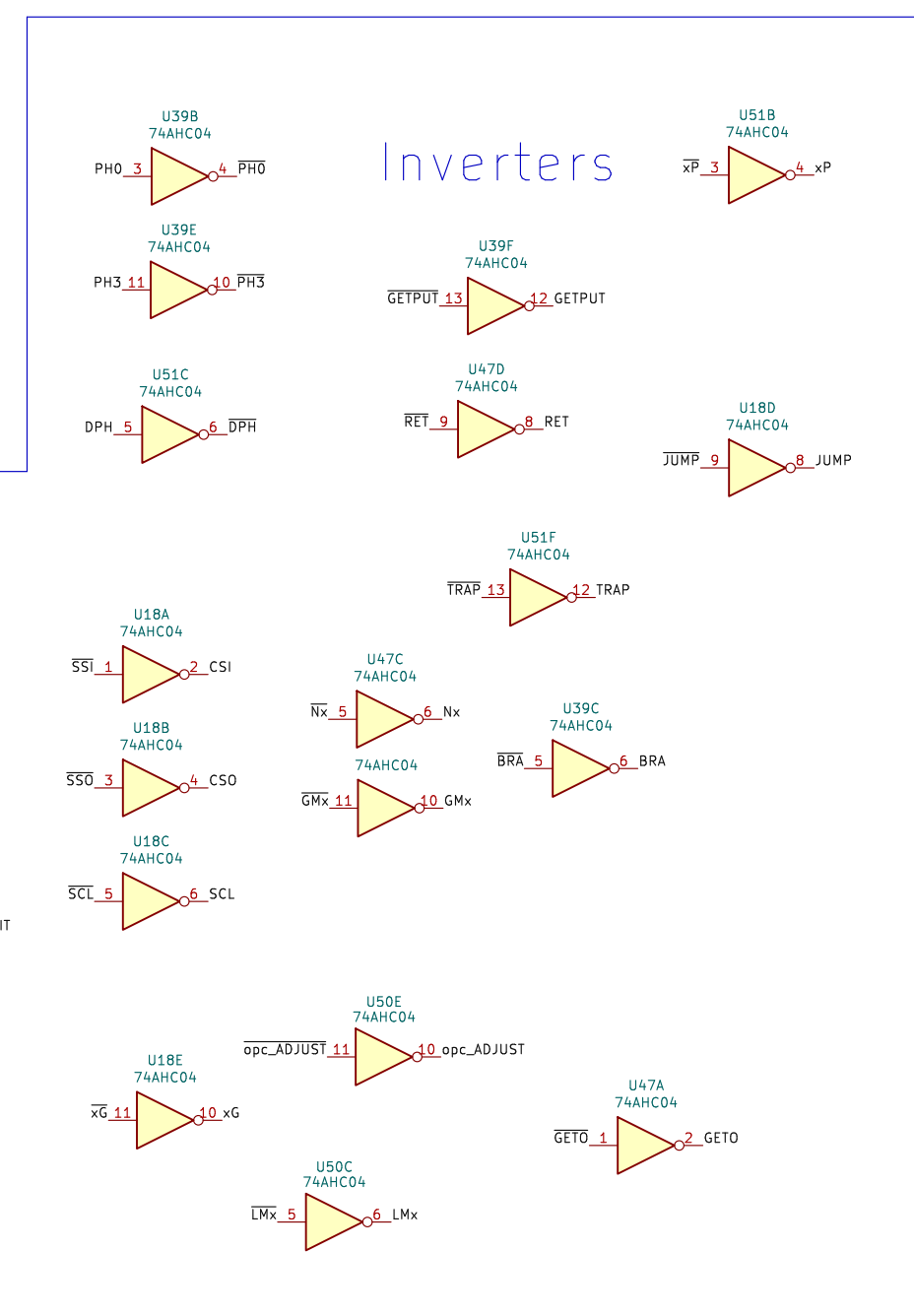
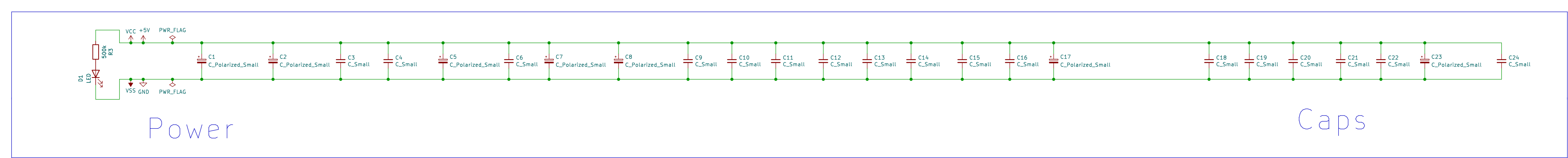


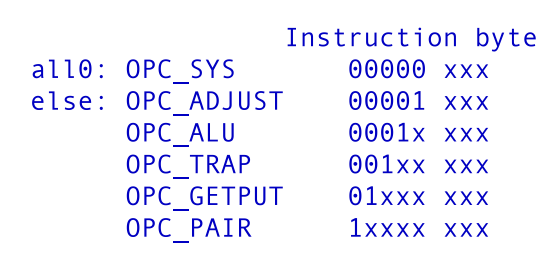
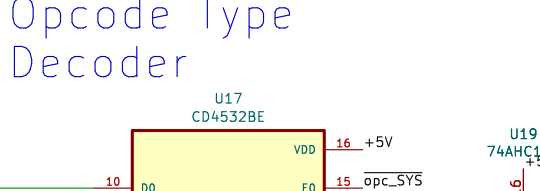
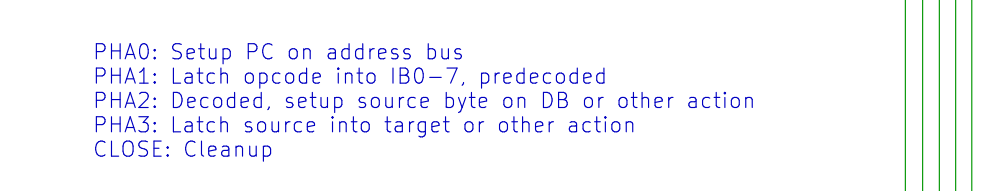
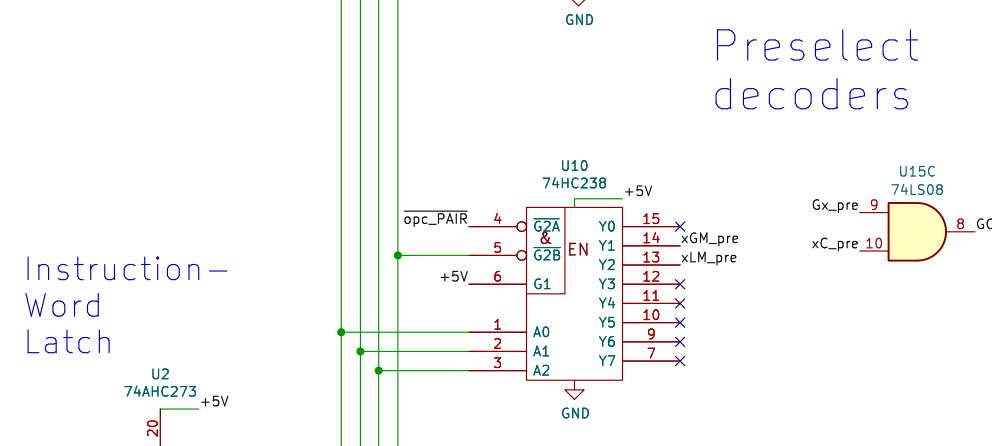
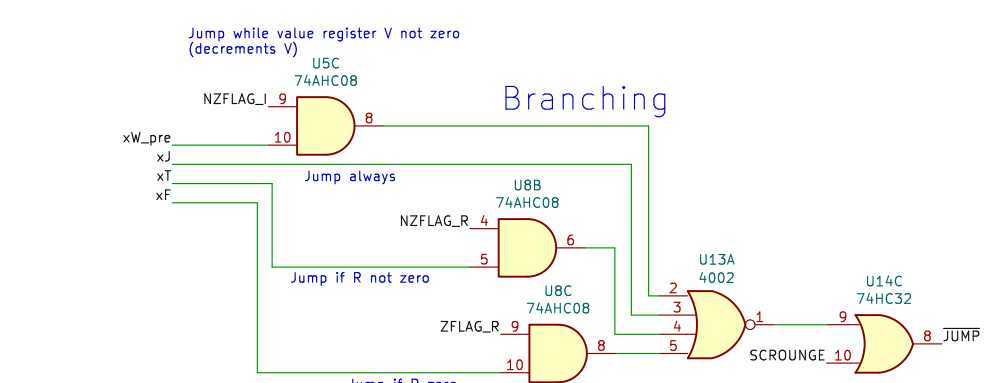
# Myth Microcontroller Reference Schematics



## Instruction Decoder

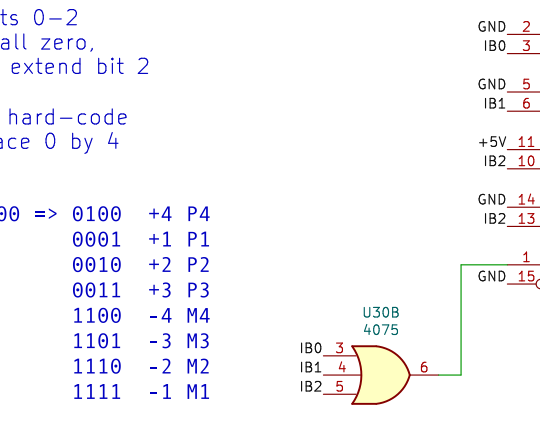
Scrounger

Remap MM, RR, DD etc. and impracticable opcodes such as NM. Currently NOP, reserved for instruction set extension.

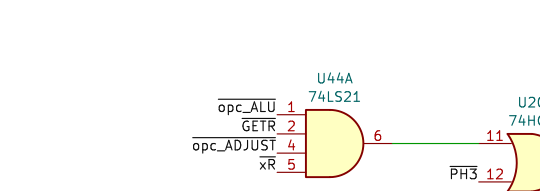


Control Tree

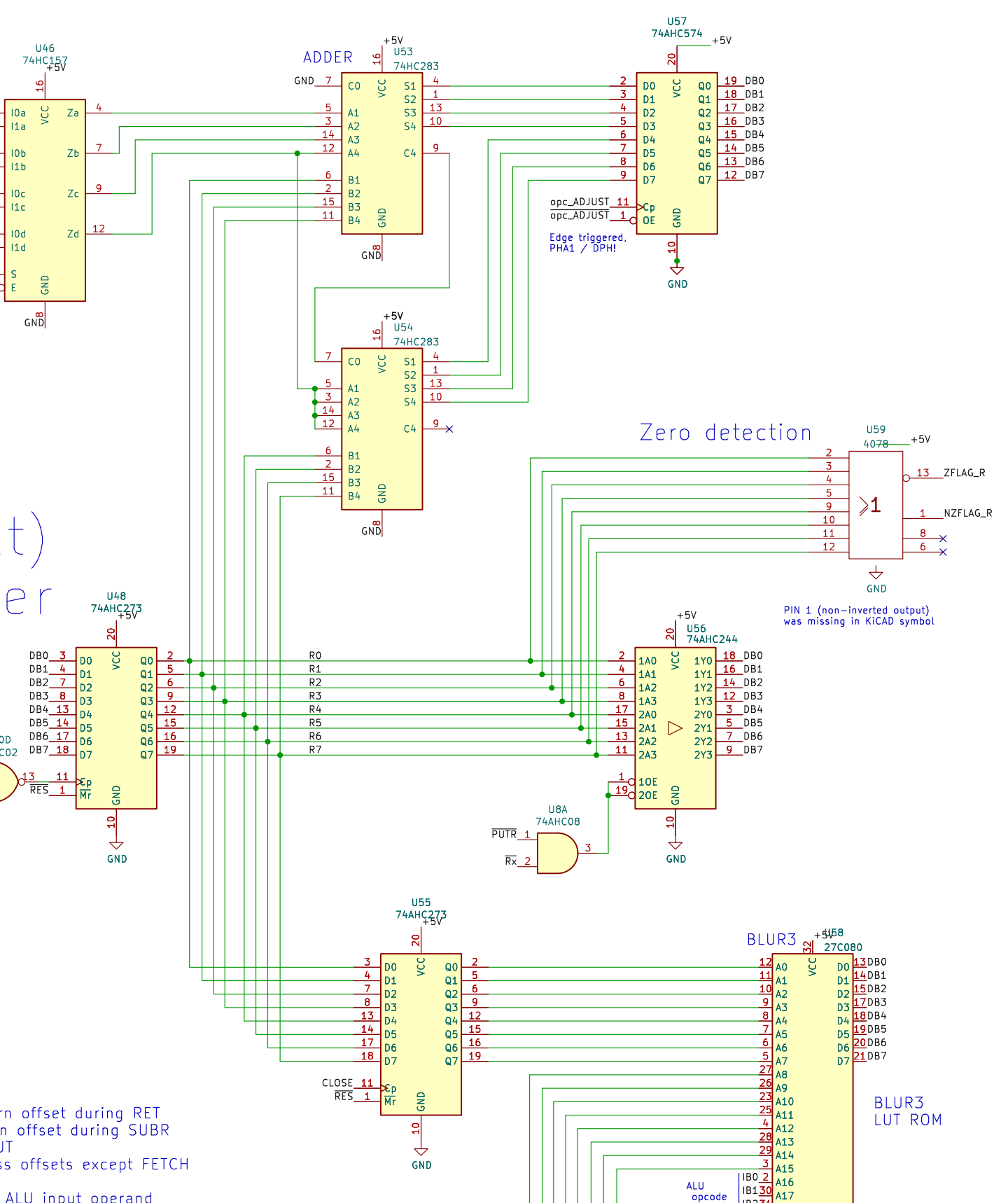
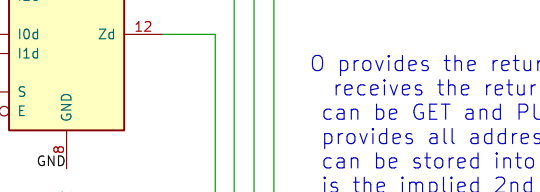
R Adjust



R(esult) Register

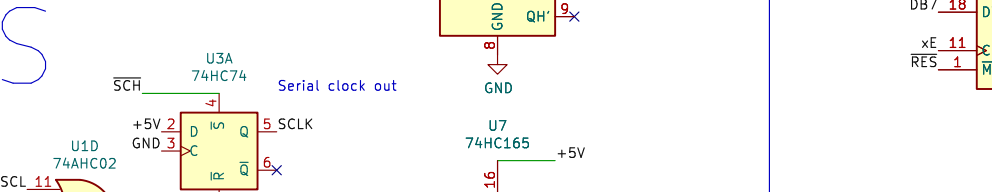
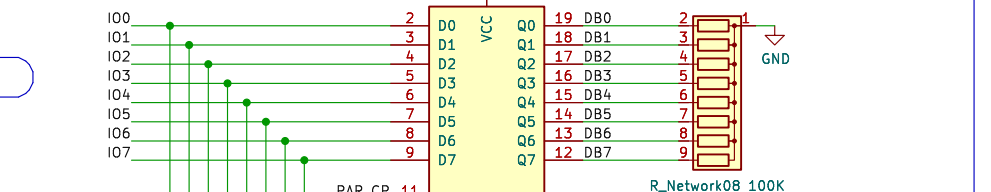
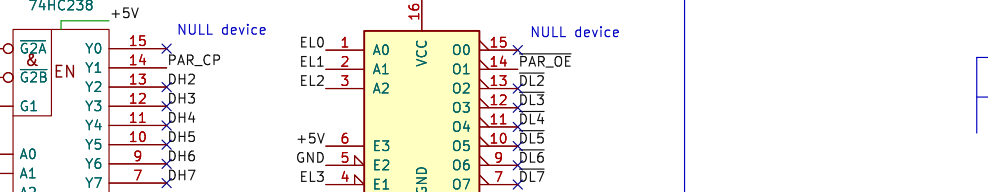
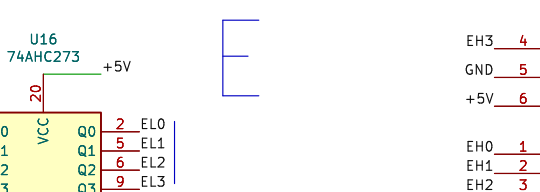
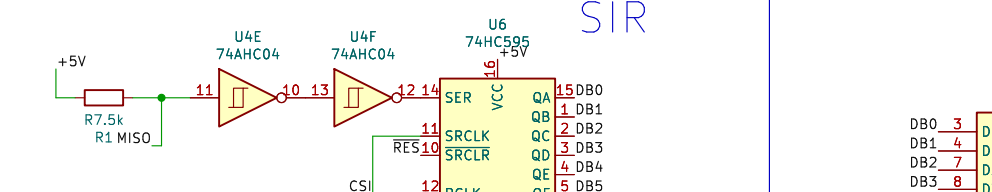
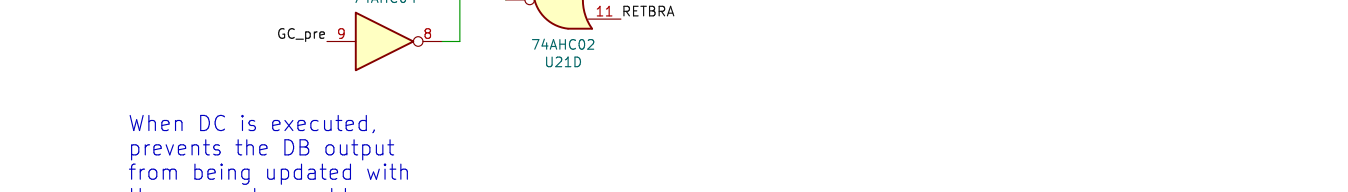
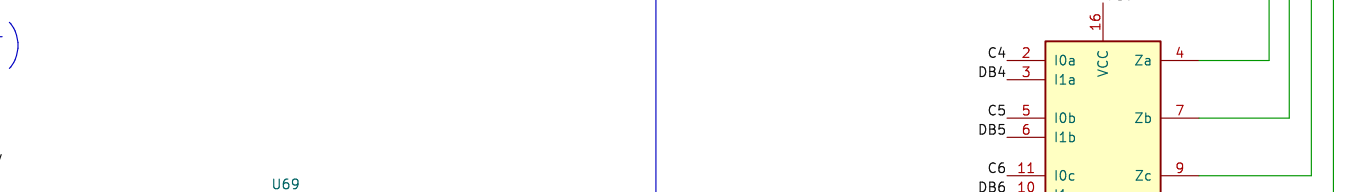
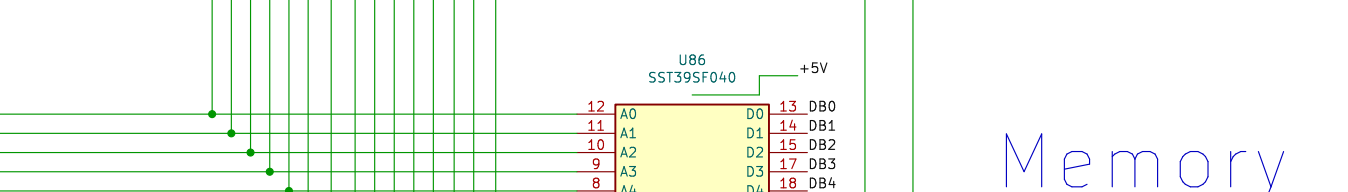
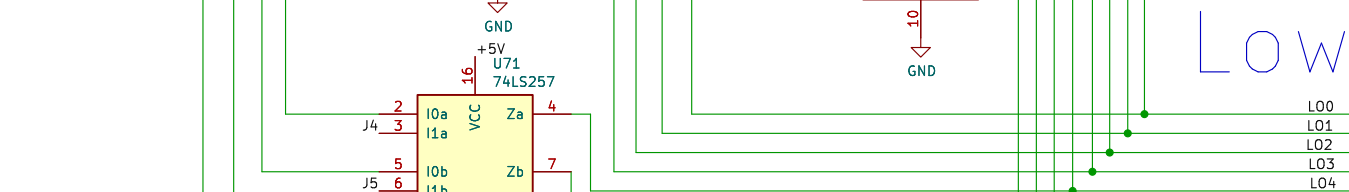


O (OFFSET) Operand Register



ALU

## Storage



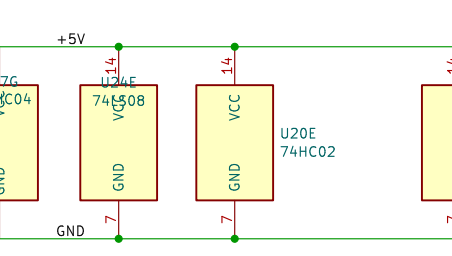
## Device Enable

Original 0 selects a NULL DEVICE. Ref. implementation connects two independent 4-bit groups (high/low) to 4-bit encoders (for simultaneous latch enable / output enable of two separate devices).

Parallel IO

Implement an 8-bit parallel tri-state interface bus with dedicated in/out ports

## Glue Logic



## Spare Units

