Myth Microcontroller Reference Schematics

"VLSI" Footprint

IO0-7 bus tri-state
internal pull-down

RTS request

Internal data bus header

Clock Phases

~8MHz

Power

Caps

Instruction Decoder

Branching

Jump while loop counter register ! not zero (decrements !)

Jump always

Jump if R not zero

Jump if R zero

Scrounger

Remap ("scrounge") GG, RR, II etc,
and impracticable opcodes such as NM

Most mapped to NOP,
but reserved for
instruction set
extensions

etc

Prevent same-cycle
memory-to-memory
copy

NL => 01A (0 1 ADD)
NM => 01B (0 1 SUBTRACT)
IO => NOP (reserved)
JO => NOP (reserved)
KO => NOP (reserved)
LO => NOP (reserved)
II => NOP (reserved)

Control Tree

Clear Program Counter
applied during CLOSE

EXIT: Register branch target
CLOSE: Load into C

Pair DST Decoder

Literal fetch, skip
current instruction word
increment PC

But NOT IR NM

Pair SRC Decoder

Preselect decoders

Instruction-Word Latch

SYS decoder

Opcode Type Decoder

8:3 Priority
Encoder CD4532

Instruction byte:

all0: OPC_SYS	00000 xxx	See table @ SYS decoder
else: OPC_ADJUST	00001 xxx	b2:extended sign bit b1-0 LSB
OPC_ALU	0001x xxx	b4:MSB b3-0:LSB (remaining bits set 1)
OPC_TRAP	001xx xxx	b0-2 OFFS b3:GP B4-5:REG(RODG)
OPC_GETPUT	01xxx xxx	DEST SRC
OPC_PAIR	1xxxx xxx	

TRAP decoder
Immediate calls

(PC Program Counter)

J (the program counter)
is cleared/set to 0
during TRAP or CALL.
Execution starts at offset zero,
the "head" of the destination page.

Delay CLEAR
until CLOSE

G (GLOBAL)

Load DB value (xG)
or DB + I (xA = "ADD")

Inverters

R Adjust

If bits 0-2
not all zero,
sign extend bit 2

Else hard-code
replace 0 by 4

0000 => 0100 =4 R4A (R 4 ADD)
0001 =1 R1A
0010 =2 R2A
0011 =3 R3A
1100 =4 R4S (R 4 SUBTRACT)
1101 =3 R3S
1110 =2 R2S
1111 =1 R1S

R(esult) Register

All delayed
by PHA2

Zero detection

Pin 1 (non-inverted output)
was missing in KiCAD symbol

ALU

O (OFFSET) Operand Register

When DC is executed,
prevents the DB output
from being updated with
the new return address
page index, before the
instruction is done.

D (DATA) Page index

Storage

Memory M

Low

C (CODE) Page index

L (LOCAL) Page index (Stack Pointer)

FRO-7 bus
Frame/Record

Automatic call stack
CALL: Enter stack frame
RET: Resume previous frame

I (INNER Loop Register)

W=while
intended to be
post decrement

Serial IO

Implements SPI functionality
with dedicated SER/DES registers

Device Enable

Ordinal 0
selects a
NULL DEVICE

Ref. Implementation
connects two independent
4-bit groups (high/low)
to 4:16 encoders
(for simultaneous
latch enable /
output enable
of two separate devices)

Parallel IO

Implement an 8-bit parallel tri-state
interface bus with dedicated in/Out ports

Glue Logic

Spare Units

PHA0: Setup PC on address bus
PHA1: Latch opcode into IR0-7, predecoded
PHA2: Decoded, setup source byte on DB or other action
PHA3: Latch source into target or other action
CLOSE: Cleanup

Rev. Step LDX ("Frozen")
Project homepage: https://github.com/Doxflange/Myth
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File: sonne-8.kicad_sch

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