Sonne Microcontroller
Reference Schematics
rev. Myth
Clock
Phases
"VLSI" Footprint
Power
Caps
Inverters
O(rigin)
Register
Instruction
Decoder
Branching
Scrounger
Control Tree
Pair DST Decoder
Preselect
decoders
Instruction-
Word
Latch
Pair SRC Decoder
SYS decoder
Opcode Type
Decoder
GETPUT
Decoder
8:3 Priority
Encoder CD4532
Instruction byte:
all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_ADJUST 00001 xxx b2:extended sign bit b1-0 LSB
OPC_ALU 0001x xxx See table @ ALU
OPC_TRAP 001xx xxx b4:MSB b3-0:LSB (remaining bits set 1)
OPC_GETPUT 01xxx xxx b5-4:OFFS b3:GL b2:GP B1-0:ABRV
OPC_PAIR 1xxxx xxx DEST SRC
A
B
ALU
R Adjust
R(esult)
Register
All delayed
to PHA3
BLUR3 LUT
ROM layout:
16 maps
@256x256
0 IDA ("Identity A" / F:=A)
1 IDB ("Identity B" / F:=B)
2 OCA ("Ones Complement A" / F:=~A)
3 OCB ("Ones Complement B" / F:=~B)
4 SLA ("Shift left A" / F:=A<<1)
5 SLB ("Shift left B" / F:=B<<1)
6 SRA ("Shift right A" / F:=A>>1)
7 SRB ("Shift right B" / F:=B>>1)
8 AND (F:=A&B)
9 IOR (F:=A|B)
10 EOR (F:=A^B)
11 ADD ("Add" / F:=A+B, bits 0-7)
12 CYB ("Carry Bit" / F:= Carry, 9th bit of A+B) 00h or 01h
13 ALB ("Flag: A less than B" / F:= (A<B)? 0xEF:0
14 AEB ("Flag: A equals B" / F:= (A==B)? 0xEF:0
15 AGB ("Flag: A greater than B" / F:= (A>B)? 0xEF:0
Storage
Low
High
Memory
M
16K
7-BIT
Page index
(Implied address
offset for xMx)
(GorL = GLOBAL or LOCAL,
including GETPUT)
I (INNER Loop Register)
L(ocal) page index
Stack Pointer
L
Delay EXIT
until CLOSE
C
C(ode) page index
D
D(ata) page index
Glue Logic
S
SIR
SOR
Serial IO
Implements SPI functionality
with dedicated SER/DES registers
E
Device Enable
P
PIR
POR
Parallel IO
Implement an 8-bit parallel tri-state
interface bus with dedicated In/Out ports
Spare Units
Project homepage: https://github.com/Dosflange/Sonne
Author: Michael Mangelsdorf
Contact: mim@ok-schalter.de
Sheet: /
File: sonne-controller.kicad_sch
Title: Sonne-8 Micro-Controller
Size: A0
Date: 2024-08-12
Rev: Myth
KiCad E.D.A. 8.0.4
Id: 1/1