

Sonne Microcontroller Reference Schematics rev. Myth



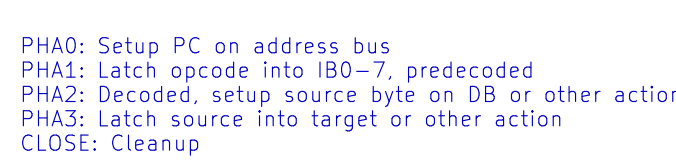
Caps



Instruction Decoder

Scrounger

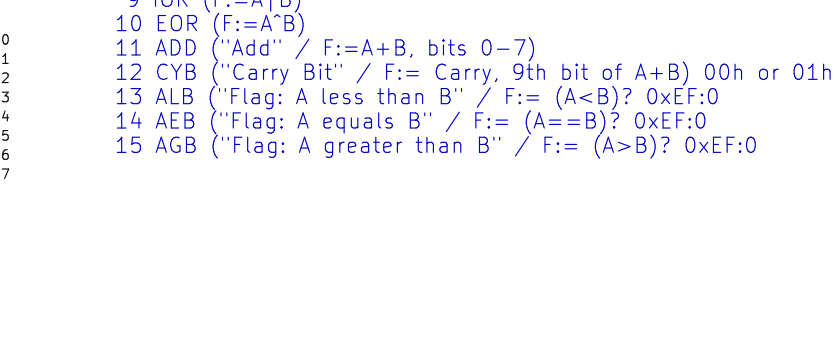
All NOP, but reserved for instruction set extension, except NM



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Instruction byte:
all0: OPC_SYS      00000 xxx   See table 0 SYS decoder
else: OPC_ADJUST   00001 xxx   b2:extended sign bit b1-0: LSB
      OPC_ALU      0001x xxx   See table 0 ALU
      OPC_TRAP     001xx xxx   b4:MSB b3-0: LSB (remaining bits set 1)
      OPC_GETPUT   01xxx xxx   b5-4:OFFS b3:GL b2:GP B1-0:ABRV
      OPC_PAIR     1xxxx xxx   DEST SRC5

```



O(rigin)
Register

0

Memory

M

High



Serial IO

Implements SPI functionality
with dedicated SER/DES registers



Device Enable

Ref. Implementation
connects two independent
4-bit groups (high/low)
to 4:16 encoders
(for simultaneous
latch enable /
output enable
of two separate devices)



Implement an 8-bit parallel tri-state interface bus with dedicated In/Out ports.

Should implement a "force tristate" pin

