Sonne-8 Microcontroller Reference Schematics Rev. Myth/LOX

"VLSI" Footprint

IO0-7 bus tri-state internal pull-down

Internal data bus header

Clock Phases

8MHz

Power

Caps

I (INNER Loop Register)

Control Tree

Instruction Decoder

Branching

Jump always

Jump if R not zero

Jump if R zero

Scrounger

Remap ("scrounge") GG, RR, II etc, and impracticable opcodes such as NM

Mapped to NOP, but reserved for instruction set extensions

Pair DST Decoder

Pair SRC Decoder

Preselect decoders

SYS decoder

TRAP decoder
Immediate calls

Opcode Type Decoder

B:3 Priority Encoder CD4532

Instruction byte:

all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_FIX 00001 xxx b2:extended sign bit b1-0 LSB
OPC_ALU 0001x xxx See table @ ALU
OPC_TRAP 001xx xxx b4:MSB b3-0:LSB (remaining bits set 1)
OPC_ROID 01xxx xxx b0-2 OFFS b3:GET/PUT B4-5:REG(ROID)
OPC_PAIR 1xxxx xxx DEST SRC

PHA0: Setup PC on address bus
PHA1: Latch opcode into IB0-7, predecoded
PHA2: Decoded, setup source byte on DB or other action
PHA3: Latch source into target or other action
CLOSE: Cleanup

(PC Program Counter)

J (the program counter) is cleared/set to 0 during TRAP or CALL. Execution starts at offset zero, the "head" of the destination page.

Delay CLEAR until CLOSE

R-Fix

Hard-coded:
If bits 0-2 all 0
replace by 4

0000 => 0100 +4 P4 (R PLUS 4)
0001 +1 P1
0010 +2 P2
0011 +3 P3
1100 -4 M4 (R MINUS 4)
1101 -3 M3
1110 -2 M2
1111 -1 M1

Else sign extend bit 2

R(esult) Register

ALU

Zero detection

ALU operations

B AND (R:=R&O)
9 IOR (R:=R|O)
10 EOR (R:=R^O)
11 ADD (Add' / R:=R+O, bits 0-7)
12 CAR (Carry Bit' / R:= Carry, 9th bit of R+O) 00h or 01h
13 RLO (Flag: R less than 0' / R:= (R<0)? 0xFF:0
14 REQ (Flag: R equals 0' / R:= (R==0)? 0xFF:0
15 RGO (Flag: R greater than 0' / R:= (R>0)? 0xFF:0

BLUR3 LUT ROM layout:

16 maps @256x256

O (OFFSET) Operand Register

xA adds DB val to O and carries over into O

D (DATA) Page index

C (CODE) Page index

Delay the EXIT signal so that Code Page updates at CLOSE

L (LOCAL) Page index (Stack Pointer)

FRO-7 bus Frame/Record

Automatic call stack
CALL: Enter stack frame
RET: Resume previous frame

G (GLOBAL)

Low Memory M

Storage

16K

IB 0-2 are the immediate offset for GET/PUT operations

S

Serial IO

Implements SPI functionality with dedicated SER/OES registers

E

Device Enable

Ref. implementation connects two independent 4-bit groups (high/low) to 4:16 decoders (for synchronised latch enable / output enable events of two devices)

P

PIR

POR

Parallel IO

Implement an 8-bit parallel tri-state interface bus with dedicated In/Out ports

Glue Logic

Spare Units

Rev. Step LOX ("Frozen")
Project homepage: https://github.com/Doxflange/Myth
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Sheet: /
File: myth.kicad_sch

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