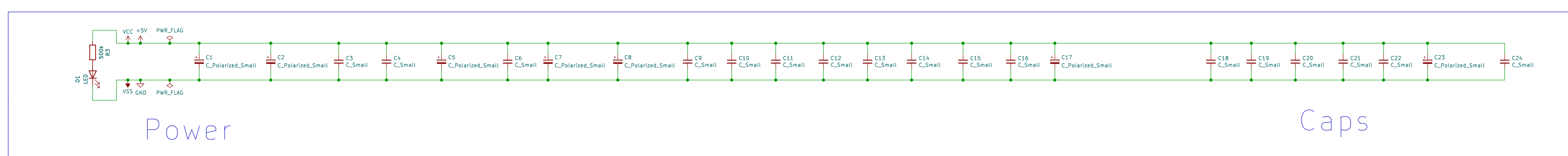
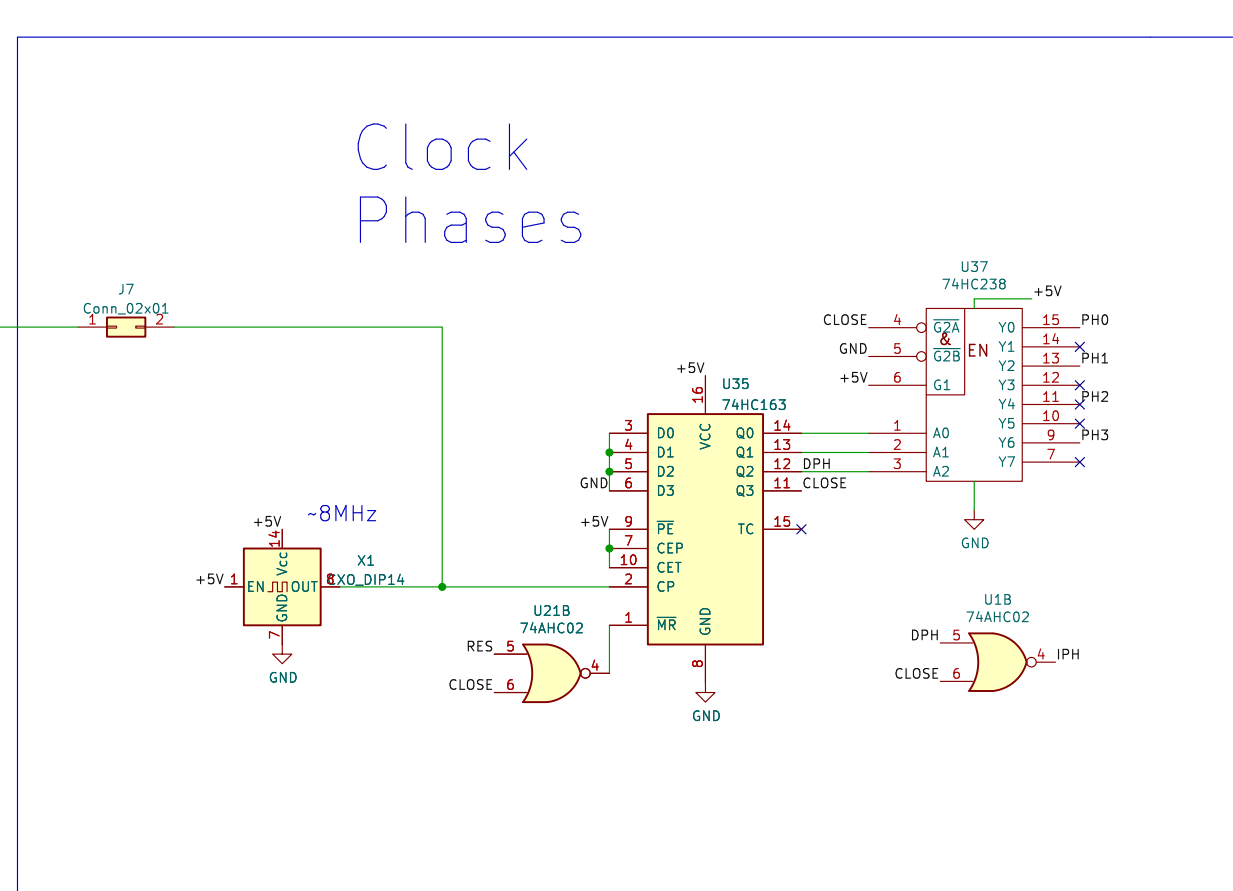
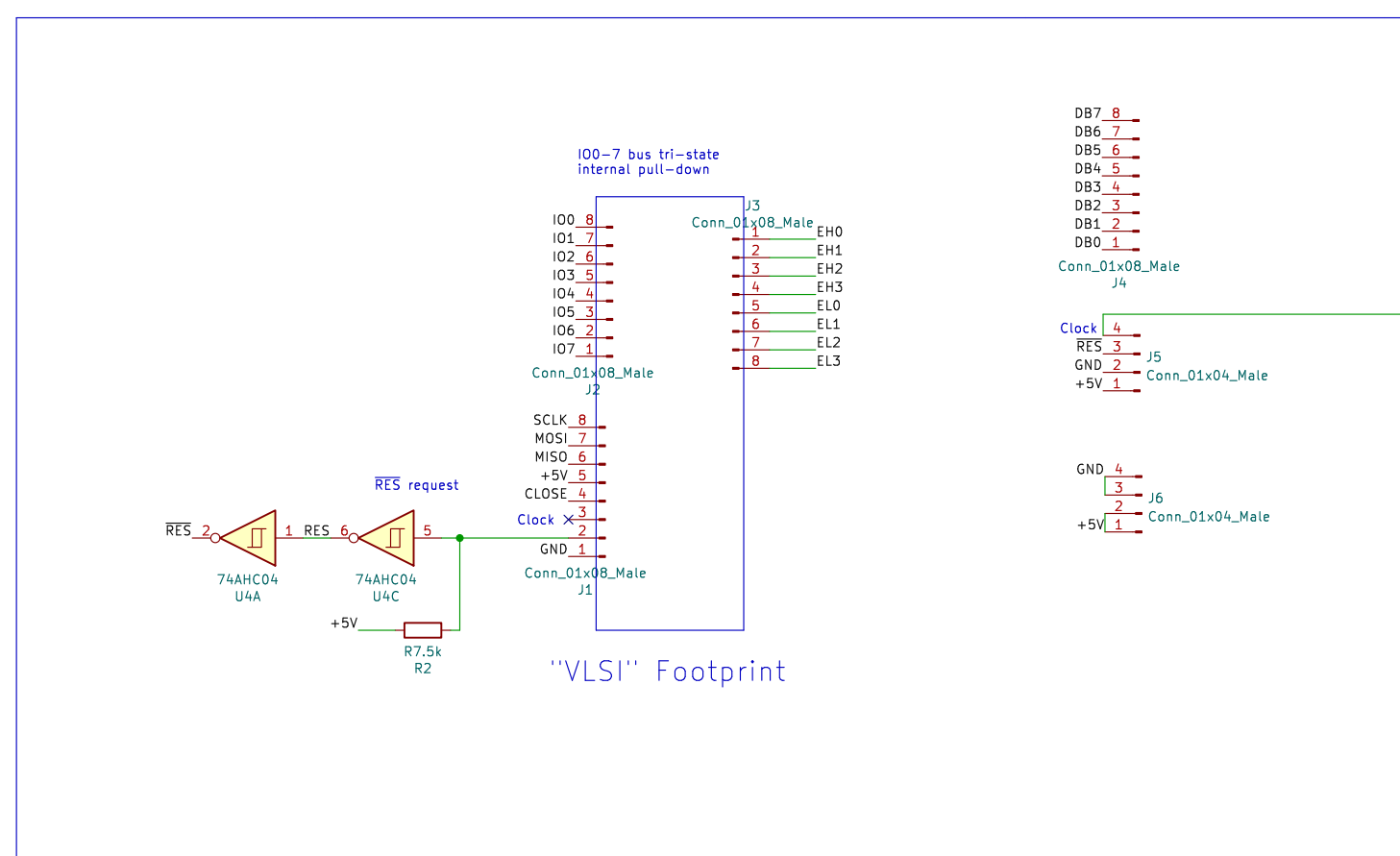
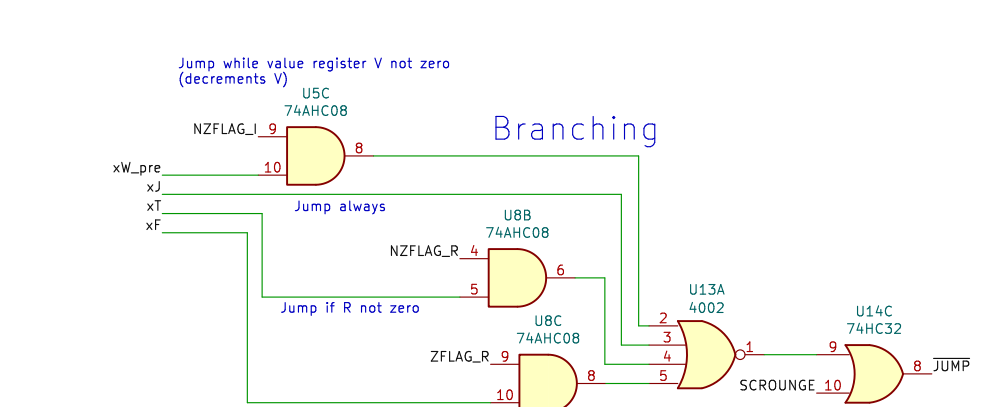


Myth Microcontroller Reference Schematics



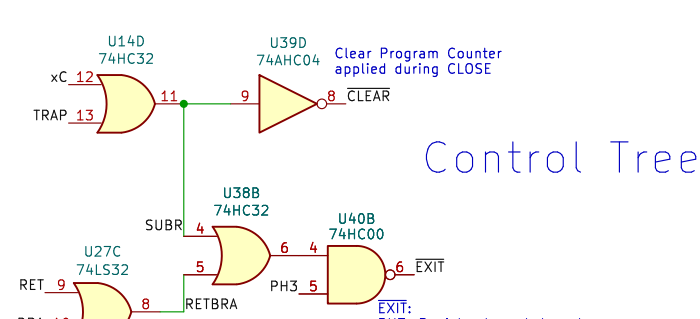
Instruction Decoder



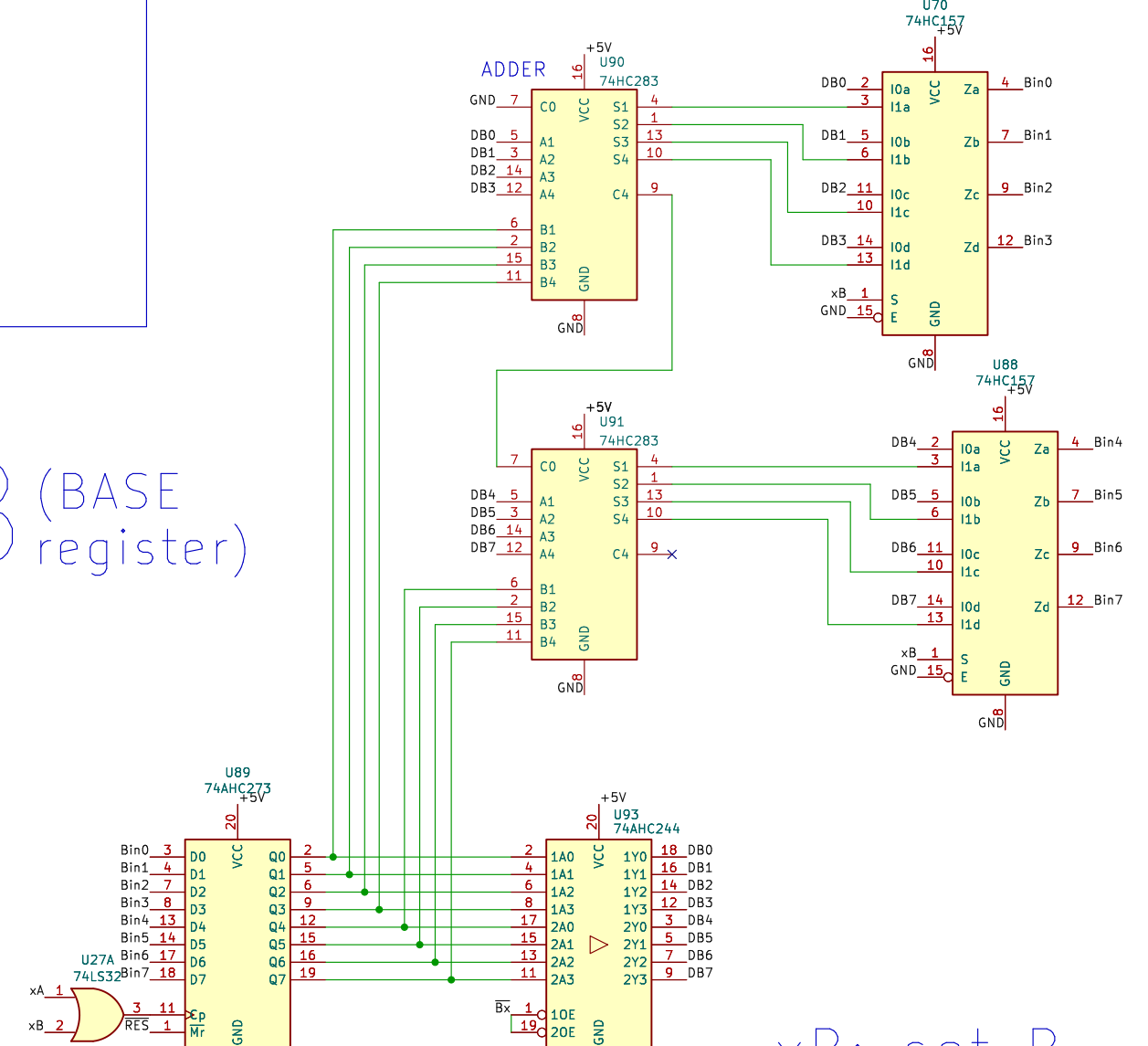
Scrounger

Currently NOP, reserved for instruction set extension

Control Tree

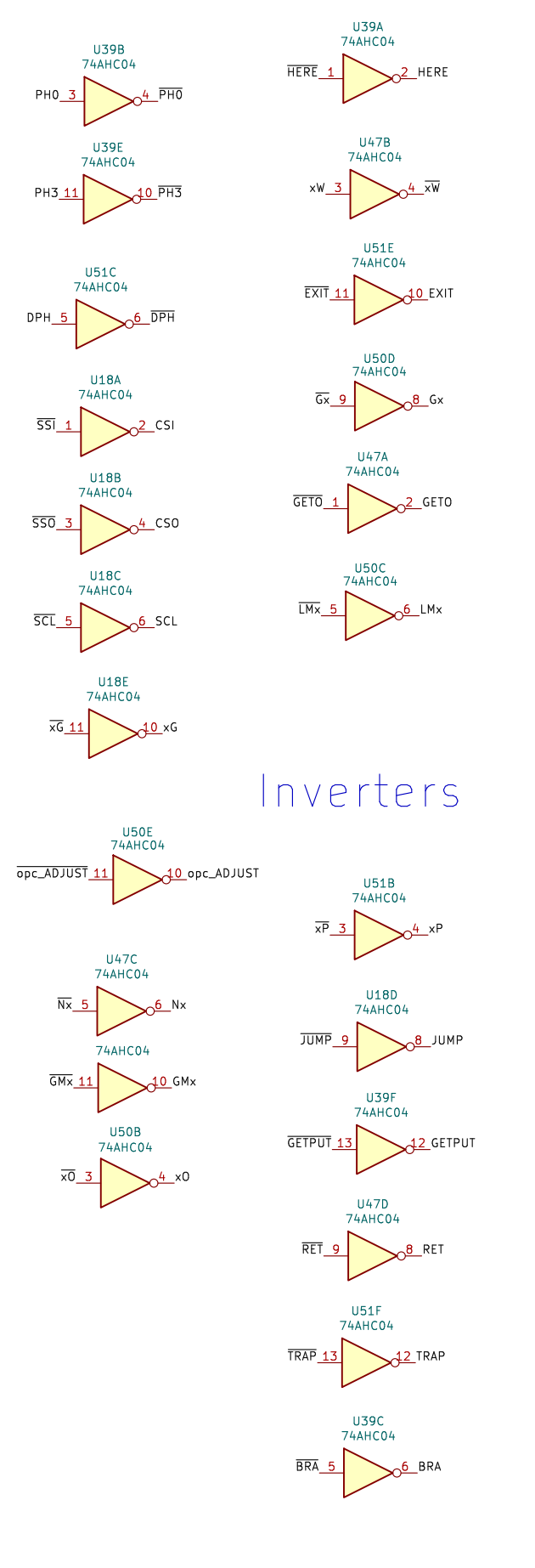


B (BASE register)



xB: set B
xA: add to B

Inverters

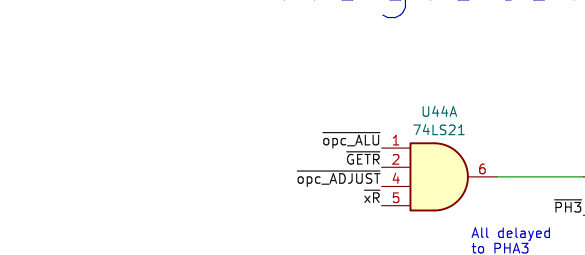


R Adjust

If bits 0-2 not all zero, sign extend bit 2. Else hard-code replace 0 by 4.

0000 => 0100 +4 P4
0001 => +1 P1
0010 => +2 P2
0011 => +3 P3
0100 => +4 P4
0101 => +5 P5
0110 => +6 P6
0111 => +7 P7
1000 => +8 P8
1001 => +9 P9
1010 => +10 P10
1011 => +11 P11
1100 => +12 P12
1101 => +13 P13
1110 => +14 P14
1111 => +15 P15

R(result) Register



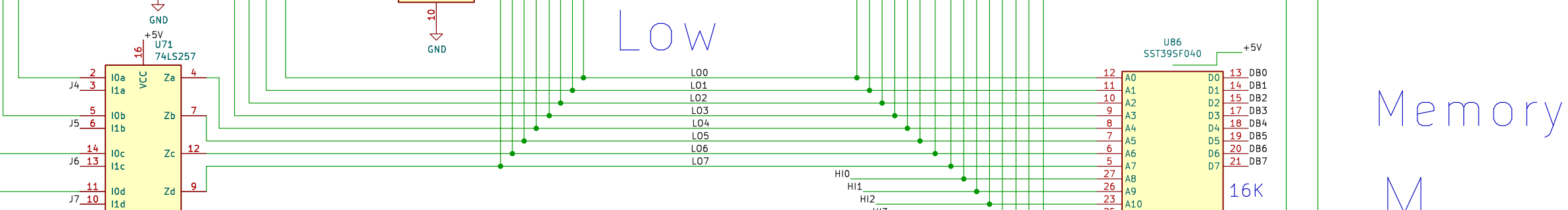
ALU

0 provides the return offset during RET receives the return offset during SUBR can be GET and PUT provides all address offsets except FETCH can be stored into is the implied 2nd ALU input operand

O (OFFSET) Operand Register

0 OR (Identity R / R=0)
1 OR (Identity O / R=0)
2 OR (Ones Complement R / R=~R)
3 OR (Ones Complement O / R=~O)
4 SLR (Shift left New / R=<<1)
5 SLR (Shift left Old / R=<<1)
6 SRR (Shift right New / R=>>1)
7 SRR (Shift right Old / R=>>1)
8 AND (R=R&O)
9 OR (R=R|O)
10 XOR (R=R^O)
11 ADD (Add / R=R+O, bits 0-7)
12 CAR (Carry Bit / R= Carry 5th bit of R+O 00h or 01h)
13 RLO (Flag: R less than O / R=(R<O)? 0xFF:0)
14 RCO (Flag: R equals O / R=(R==O)? 0xFF:0)
15 RGO (Flag: R greater than O / R=(R>O)? 0xFF:0)

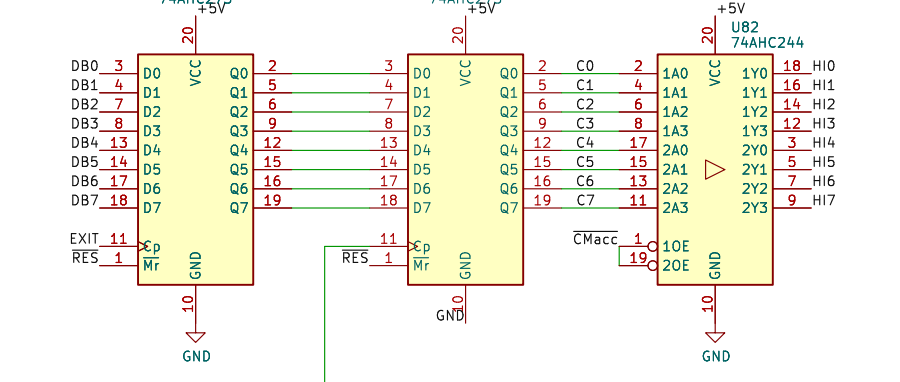
Memory M



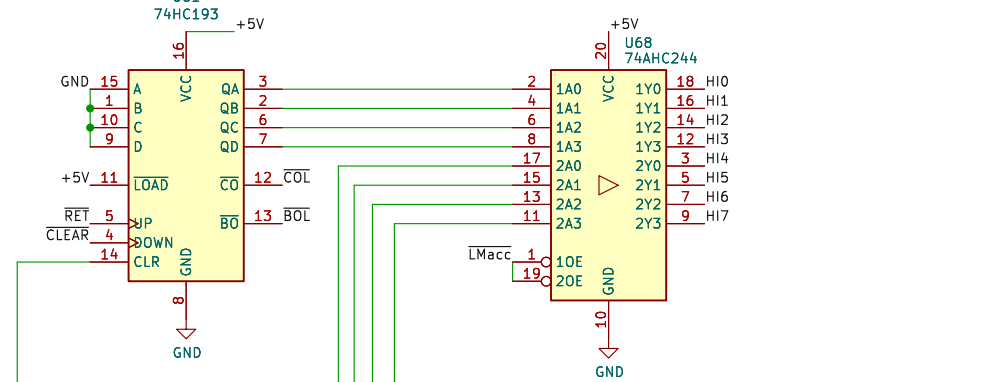
Storage



C (CODE) Page index

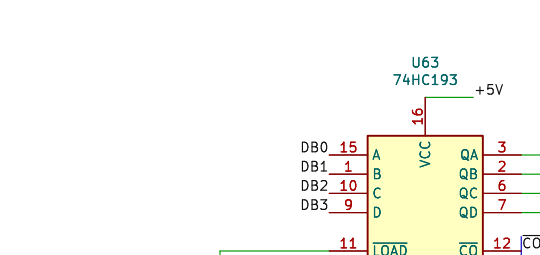


L (LOCAL) Page index (Stack Pointer)

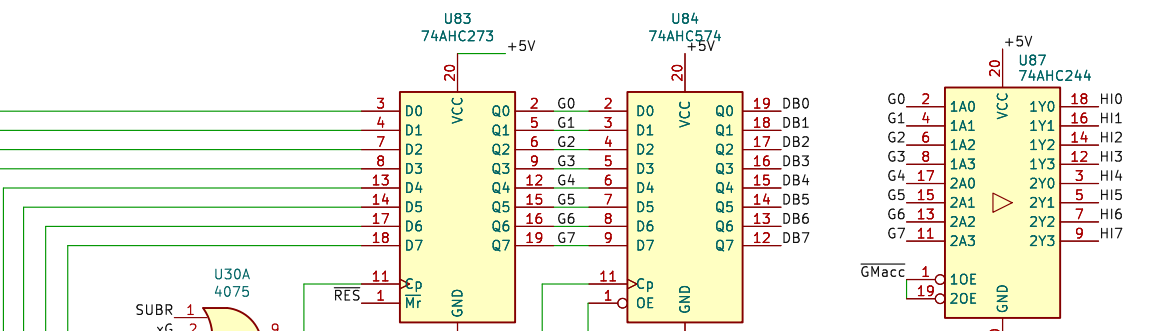


Automatic call stack CALL: Enter stack frame RET: Resume previous frame

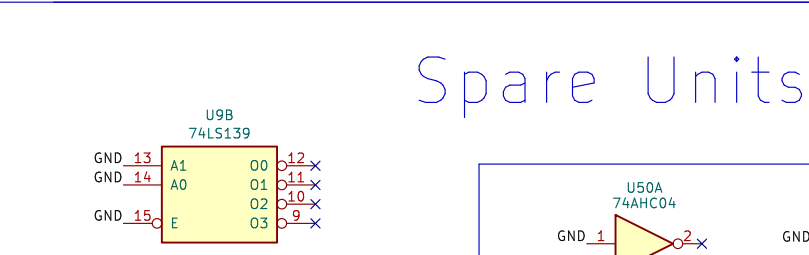
I (INNER Loop Register)



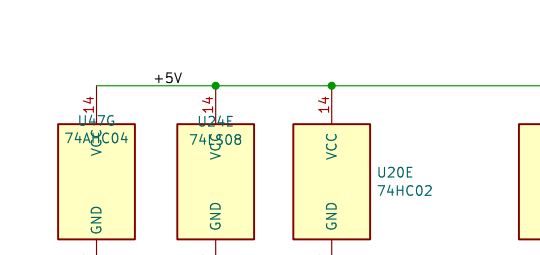
G (GLOBAL) Page index



Spare Units

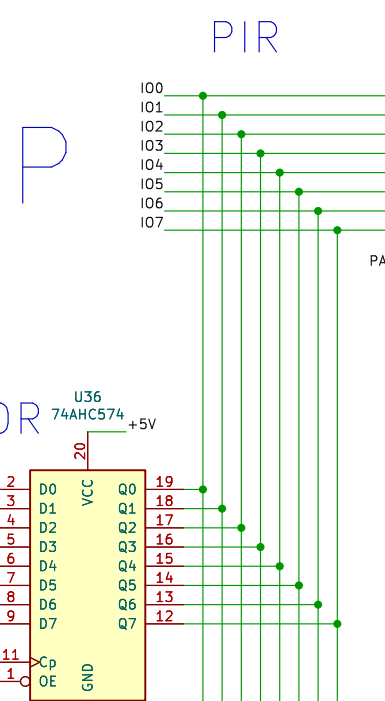


Glue Logic



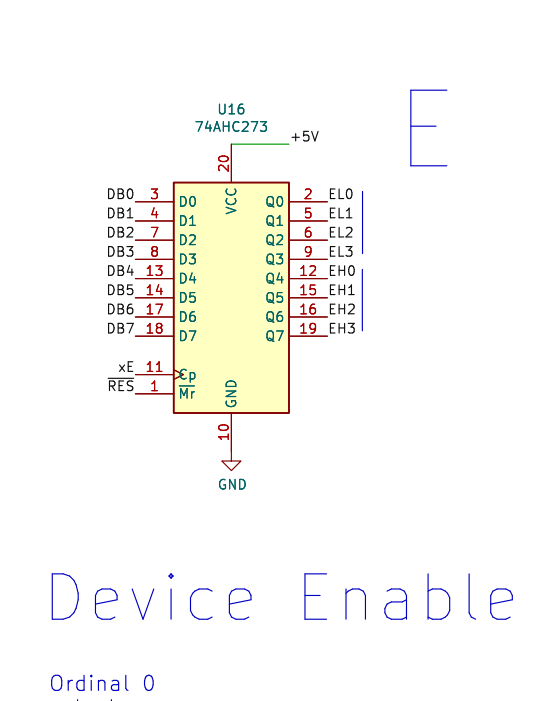
Parallel IO

Implement an 8-bit parallel tri-state interface bus with dedicated in/out ports



Device Enable

Ordinal 0 selects a NULL DEVICE
Ref. implementation connects two independent 4-bit groups (high/low) to 4-bit encoders (for simultaneous latch enable / output enable of two separate devices)



Serial IO

Implements SPI functionality with dedicated SER/DES registers

