Myth Microcontroller Reference Schematics

Power

Caps

Clock Phases

"VLSI" Footprint

Branching

Instruction Decoder

Scrounger

Remap MM, RR, DD etc.
and impracticable opcodes such as NM

Currently NOP,
reserved for
instruction set
extension

Control Tree

Inverters

(Relative addressing)

J (JUMP) register (Program Counter)

J (the program counter)
is cleared/set to 0
during TRAP or CALL.
Execution starts at offset zero,
the "head" of the destination page.

Delay CLEAR
until CLOSE

Preselect decoders

Instruction-Word Latch

Pair DST Decoder

Pair SRC Decoder

SYS decoder

R Adjust

If bits 0-2
not all zero,
sign extend bit 2

Else hard-code
replace 0 by 4

```
0000 => 0100 +4 P4
0001 +1 P1
0010 +2 P2
0011 +3 P3
1100 -4 M4
1101 -3 M3
1110 -2 M2
1111 -1 M1
```

R(esult) Register

Zero detection

PIN 5 (non-inverted output)
was missing in KICAD symbol

ADDER

Storage

Low Memory M

IB 3-5 are the
immediate offset
for LOAD/STORE
operations.

IB7 switches
between RAM and ROM

C (CODE) Page index

Select Program Memory
during Code Phase (INC)
and Interal Tests

Delay EXIT
until CLOSE

L (LOCAL) Page index (Stack Pointer)

FRO-7 bus
Frame/Record

Automatic call stack
CALL: Enter stack frame
RET: Resume previous frame

ALU

O (OFFSET) Operand Register

O provides the return offset during RET
receives the return offset during SUBR
can be GET and PUT
provides all address offsets except FETCH
can be stored into
is the implied 2nd ALU input operand

BLUR3 LUT ROM

BLUR3 LUT
ROM layout:

16 maps
@256x256

```
0 IDN ("Identity New" / New:=New)
1 IDO ("Identity Old" / New:=Old)
2 OCR ("Ones Complement New" / New:=~New)
3 OCA ("Ones Complement Old" / New:=~Old)
4 SLR ("Shift left New" / New:=New<<1)
5 SLA ("Shift left Old" / New:=Old<<1)
6 SRR ("Shift right New" / New:=New>>1)
7 SRA ("Shift right Old" / New:=Old>>1)

8 AND (New:=New&Old)
9 IOR (New:=New|Old)
10 EOR (New:=New^Old)
11 ADD (Add' / New:=New+Old, bits 0-7)
12 CAR ("Carry Bit" / New:= Carry, 9th bit of New+Old) 00h or 01h
13 NLO ("Flag: New less than Old" / New:= (New<Old)? 0xFF:0
14 NEO ("Flag: New equals Old" / New:= (New==Old)? 0xFF:0
15 NGO ("Flag: New greater than Old" / New:= (New>Old)? 0xFF:0
```

I (INNER Loop Register)

w=Write
Interpret to be
post decrement

When DC is executed,
prevents the DB output
from being updated with
the new return address
page index, before the
instruction is done.

G (GLOBAL) Page index

GETPUT Decoder

Opcode Type Decoder

B:3 Priority
Encoder CD4532

TRAP decoder
Immediate jump
to code pages
240..255 (RAM)
112-127 (ROM)

Instruction byte:

```
all0: OPC_SYS      00000 xxx    See table @ SYS decoder
else: OPC_ADJUST   00001 xxx    b2:extended sign bit b1-0 LSB
      OPC_ALU      0001x xxx    See table @ ALU
      OPC_TRAP     001xx xxx    b4:MSB b3-0:LSB (remaining bits set 1)
      OPC_GETPUT   01xxx xxx    b5-3 OFFS b2:GL b1:GP B0:RD
      OPC_PAIR     1xxxx xxx    DEST SRC
```

Serial IO

Implements SPI functionality
with dedicated SER/DES registers

Device Enable

Ordinal 0
selects a
NULL DEVICE

Ref. implementation
connects two independent
4-bit groups (high/low)
to 4:16 encoders
(for simultaneous
latch enable /
output enable
of two separate devices)

Parallel IO

Implement an 8-bit parallel tri-state
interface bus with dedicated In/Out ports

Glue Logic

Spare Units

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