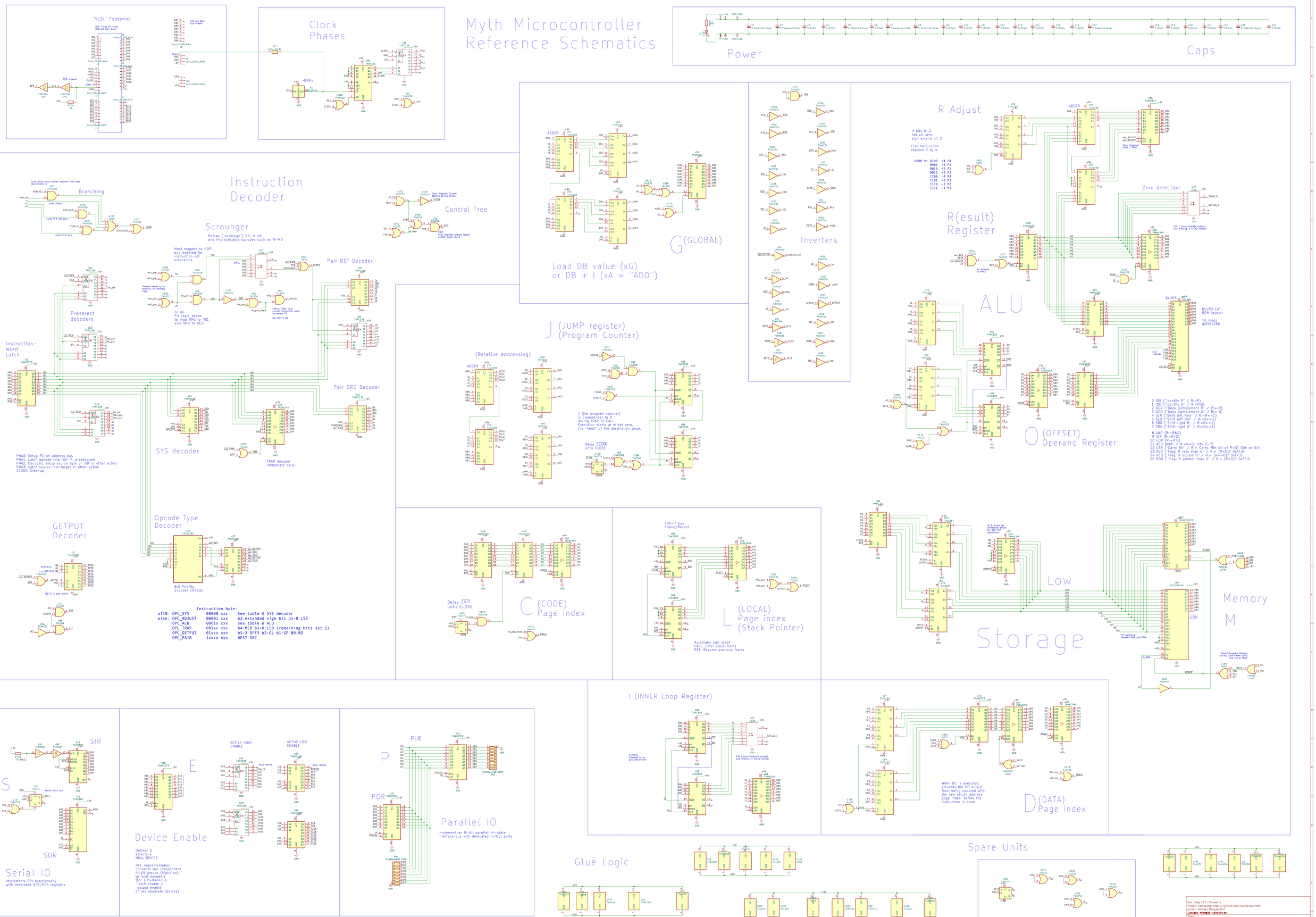
Myth Microcontroller
Reference Schematics
"VLSI" Footprint
Clock
Phases
Power
Caps
Instruction
Decoder
Branching
Scrounger
Control Tree
Preselect
decoders
Instruction-
Word
Latch
Pair DST Decoder
Pair SRC Decoder
SYS decoder
TRAP decoder
Immediate calls
Opcode Type
Decoder
GETPUT
Decoder
G (GLOBAL)
Load DB value (xG)
or DB + 1 (xA = "ADD")
J (JUMP register)
(Program Counter)
(Relative addressing)
Inverters
R Adjust
R(esult)
Register
ALU
O (OFFSET)
Operand Register
C (CODE)
Page index
L (LOCAL)
Page index
(Stack Pointer)
Storage
Low
Memory
M
I (INNER Loop Register)
D (DATA)
Page index
S
SIR
SOR
Serial IO
E
Device Enable
P
PIR
POR
Parallel IO
Glue Logic
Spare Units