
Sonne-8 Microcontroller
Reference Schematics
Rev. Myth/LOX
"VLSI" Footprint
IO0-7 bus tri-state internal pull-down
Internal data bus header
Clock Phases
~8MHz
Power
Caps
Instruction Decoder
Jump while loop counter register I not zero (decrements I)
Branching
Jump always
Jump if R not zero
Jump if R zero
Control Tree
Clear Program Counter applied during CLOSE
EXIT:
PH3: Register branch target
CLOSE: Load into C
Scrounger
Remap ("scrounge") GG, RR, II etc. and impracticable opcodes such as NM
Mapped to NOP, but reserved for instruction set extensions
Prevent same-cycle memory-to-memory copy
Literal Fetch, skip current instruction word increment PC
But NOT if NM
NL => NOP (reserved)
NM => NOP (reserved)
LL => NOP (reserved)
LM => NOP (reserved)
ML => NOP (reserved)
MM => NOP (reserved)
DD => NOP (reserved)
RR => NOP (reserved)
II => NOP (reserved)
Pair DST Decoder
Preselect decoders
Instruction-Word Latch
Pair SRC Decoder
SYS decoder
TRAP decoder
Immediate calls
PHA0: Setup PC on address bus
PHA1: Latch opcode into IB0-7, predecoded
PHA2: Decoded, setup source byte on DB or other action
PHA3: Latch source into target or other action
CLOSE: Cleanup
GETPUT Decoder
IB0-2 is byte offset
Opcode Type Decoder
8:3 Priority Encoder CD4532
Instruction byte:
all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_FIX 00001 xxx b2:extended sign bit b1-0 LSB
OPC_ALU 0001x xxx See table @ ALU
OPC_TRAP 001xx xxx b4:MSB b3-0:LSB (remaining bits set 1)
OPC_GIRO 01xxx xxx b0-2 OFFS b3:GET/PUT B4-5:REG(GIRO)
OPC_PAIR 1xxxx xxx DEST SRC
I (INNER Loop Register)
W=While intended to post decrement for either case
PIN 1 (non-inverted output) was missing in KiCAD symbol
I0-7 bus gets read during FAR into the PC, when DB0-7 carries return page out of G
Inverters
Relative Addressing
(PC Program Counter)
J (the program counter) is cleared/set to 0 during TRAP or CALL. Execution starts at offset zero, the "head" of the destination page.
Delay SUBR until CLOSE
R-Fix
Hard-coded:
if bits 0-2 all 0
replace by 4
0000 => 0100 +4 P4 (R PLUS 4)
0001 +1 P1
0010 +2 P2
0011 +3 P3
1100 -4 M4 (R MINUS 4)
1101 -3 M3
1110 -2 M2
1111 -1 M1
Else sign extend bit 2
Edge triggered, PHA1 / DPH!
R(esult) Register
Zero detection
All delayed to PHA3
ALU
BLUR3 LUT ROM layout:
16 maps @256x256
O (OFFSET) Operand Register
xA adds DB val to O and carries over into D
ALU Instructions
0 CLR ("Clear" / R:=0)
1 IDO ("Identity O" / R:=Old)
2 OCR ("Ones Complement R" / R:=-R)
3 OCO ("Ones Complement O" / R:=-O)
4 SLR ("Shift left New" / R:=R<<1)
5 SLO ("Shift left Old" / R:=O<<1)
6 SRR ("Shift right R" / R:=R>>1)
7 SRO ("Shift right O" / R:=O>>1)
8 AND (R:=R&O)
9 IOR (R:=R|O)
10 EOR (R:=R^O)
11 ADD ("Add" / R:=R+O, bits 0-7)
12 CAR ("Carry Bit" / R:= Carry, 9th bit of R+O) 00h or 01h
13 RLO ("Flag: R less than O" / R:= (R<O)? 0xFF:0
14 REO ("Flag: R equals O" / R:= (R==O)? 0xFF:0
15 RGO ("Flag: R greater than O" / R:= (R>O)? 0xFF:0
Implementation Semantics:
CALL/TRAP: I <= PC, Co <= C, decrement L, PC <= 0, C <= DB0-7
RET: C <= L7, PC <= I, increment L
COR: C <= D, PC <= I
NEW: L7 <= Co
xB does PC-relative in-page branching
D (DATA) Page Index
FR0-7 bus Frame/Record
L (LOCAL) Page index (Stack Pointer)
C (CODE) Page index
Delay the EXIT signal so that Code Page updates at CLOSE
573 Level triggered
Co
Force ENTER/LEAVE/FAR ref L7 ("Owner")
IB 0-2 are the immediate offset for GET-PUT operations
Low
Memory M
16K
HI7 switches between RAM and ROM
Select Program Memory during Code Phase (IPH) and literal fetch
Output L7
Storage
S
SIR
Serial clock out
SOR
Serial IO
Implements SPI functionality with dedicated SER/DES registers
E
ACTIVE HIGH ENABLE
ACTIVE LOW ENABLE
Device Enable
Ref. implementation connects two independent 4-bit groups (high/low) to 4:16 decoders (for synchronised latch enable / output enable events of two devices)
P
PIR
POR
Parallel IO
Implement an 8-bit parallel tri-state interface bus with dedicated In/Out ports
Glue Logic
Spare Units
Rev. Step LOX ("Frozen")
Project homepage: https://github.com/Dosflange/Myth
Author: Michael Mangelsdorf
Contact: mim@ok-schalter.de
Sheet: /
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