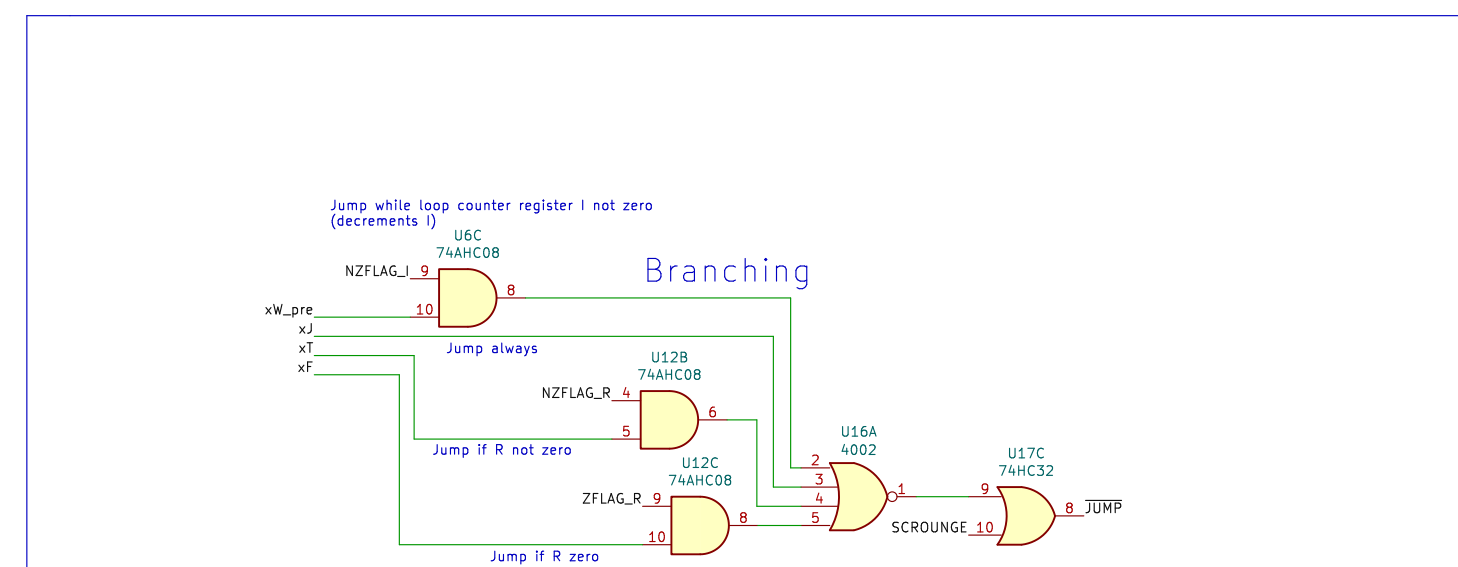
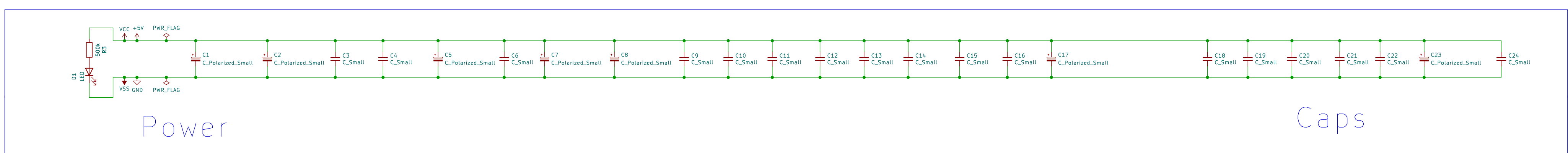


Sonne-8 Microcontroller Reference Schematics

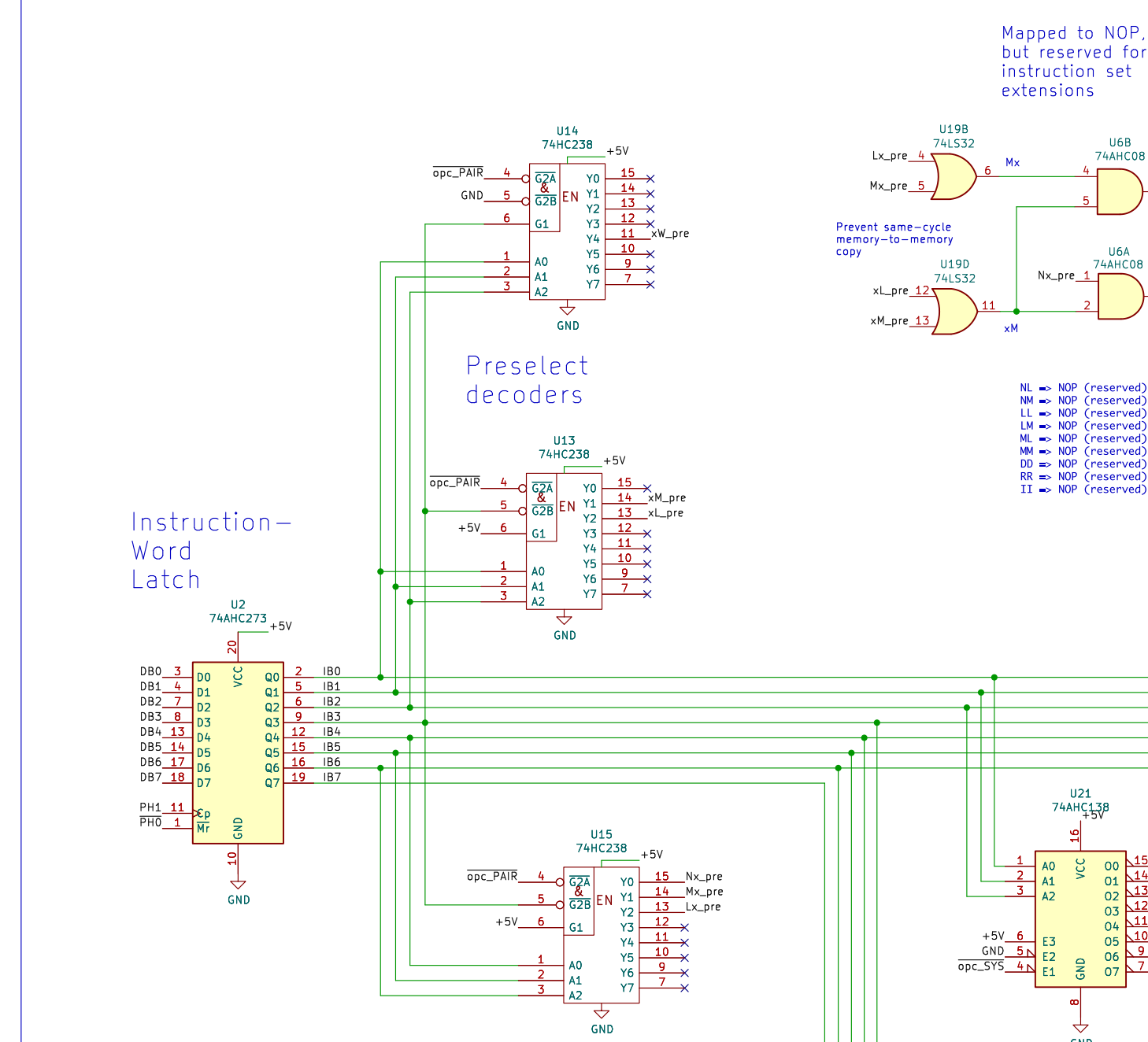
Rev. Myth/LOX



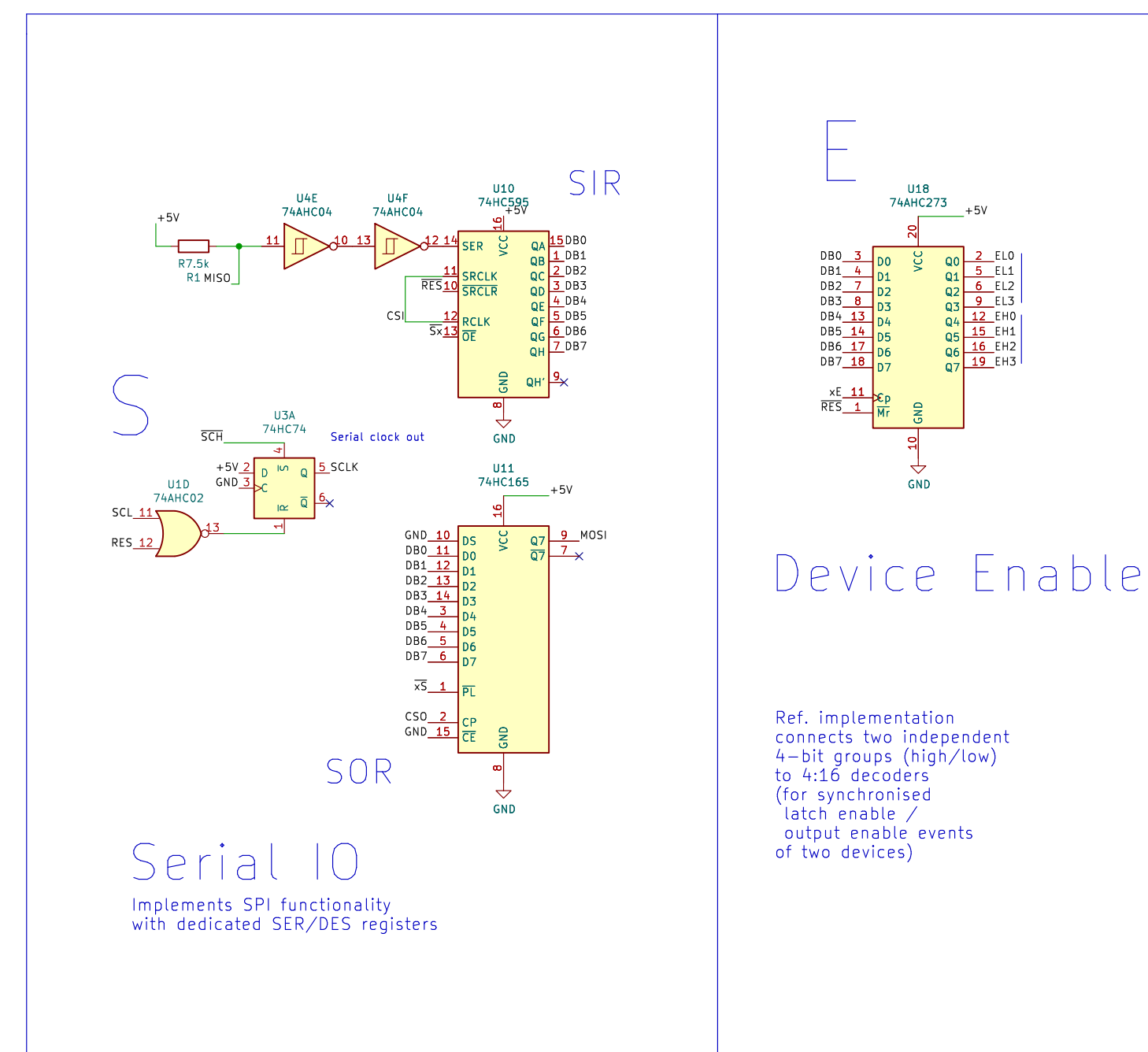
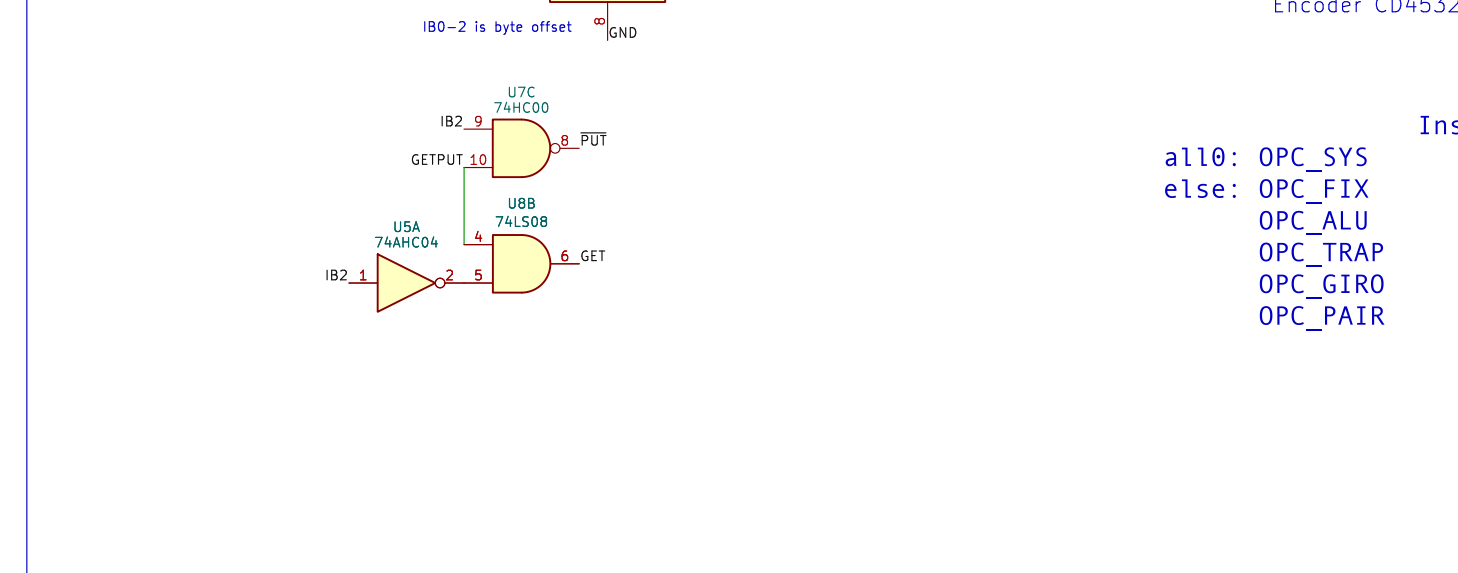
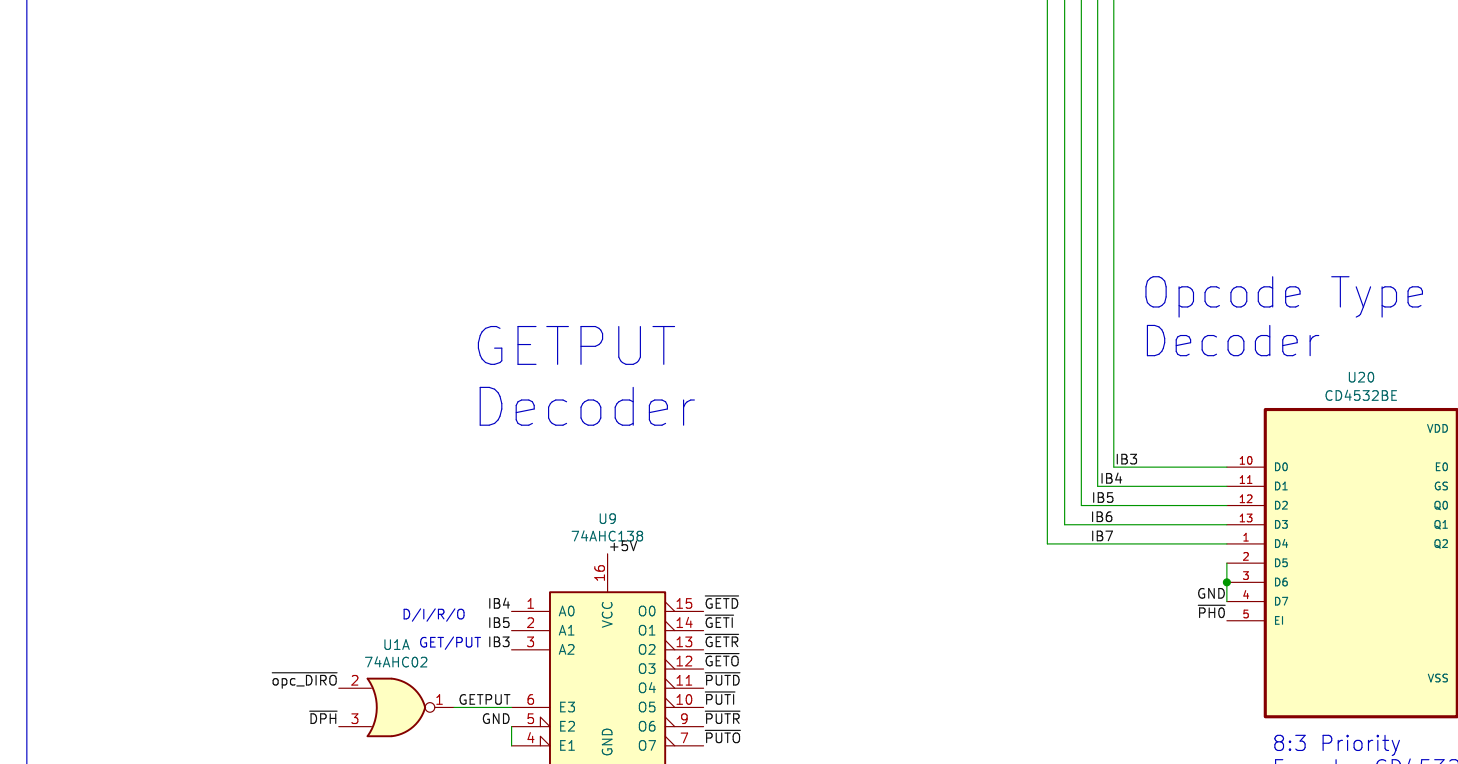
Instruction Decoder

Scrounger

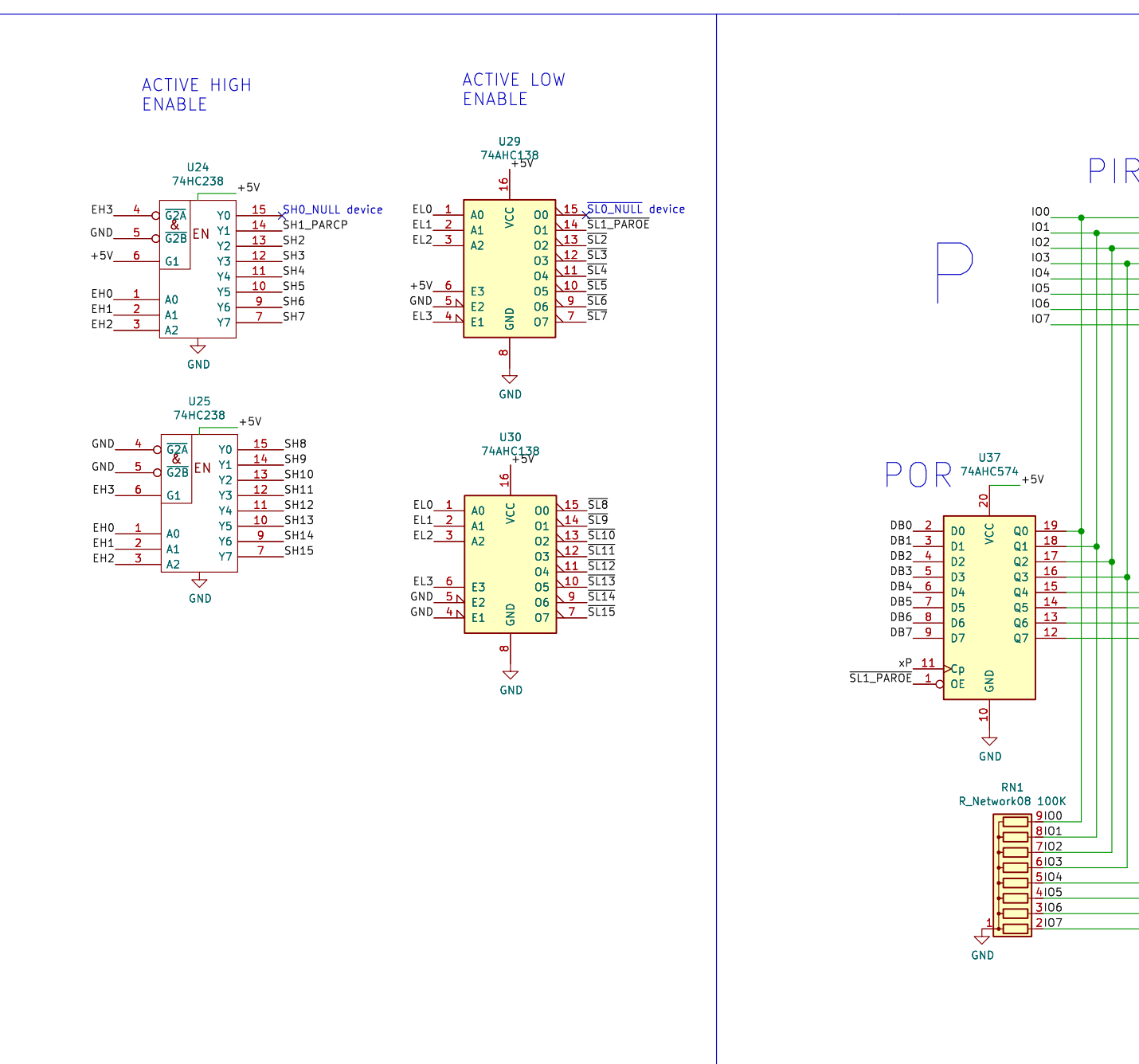
Remap "scrounger" 66, RR, II etc. and impracticable opcodes such as NM



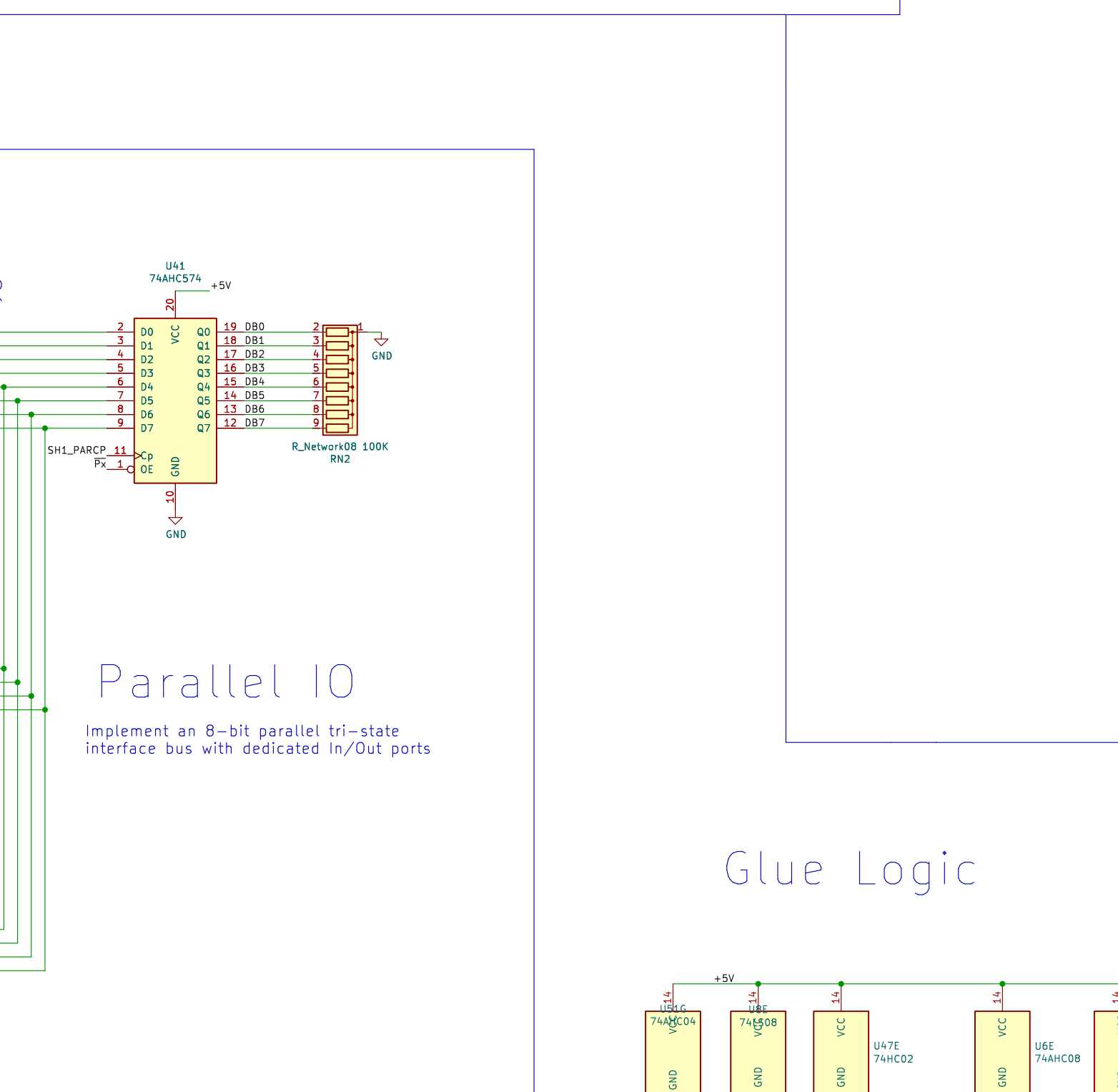
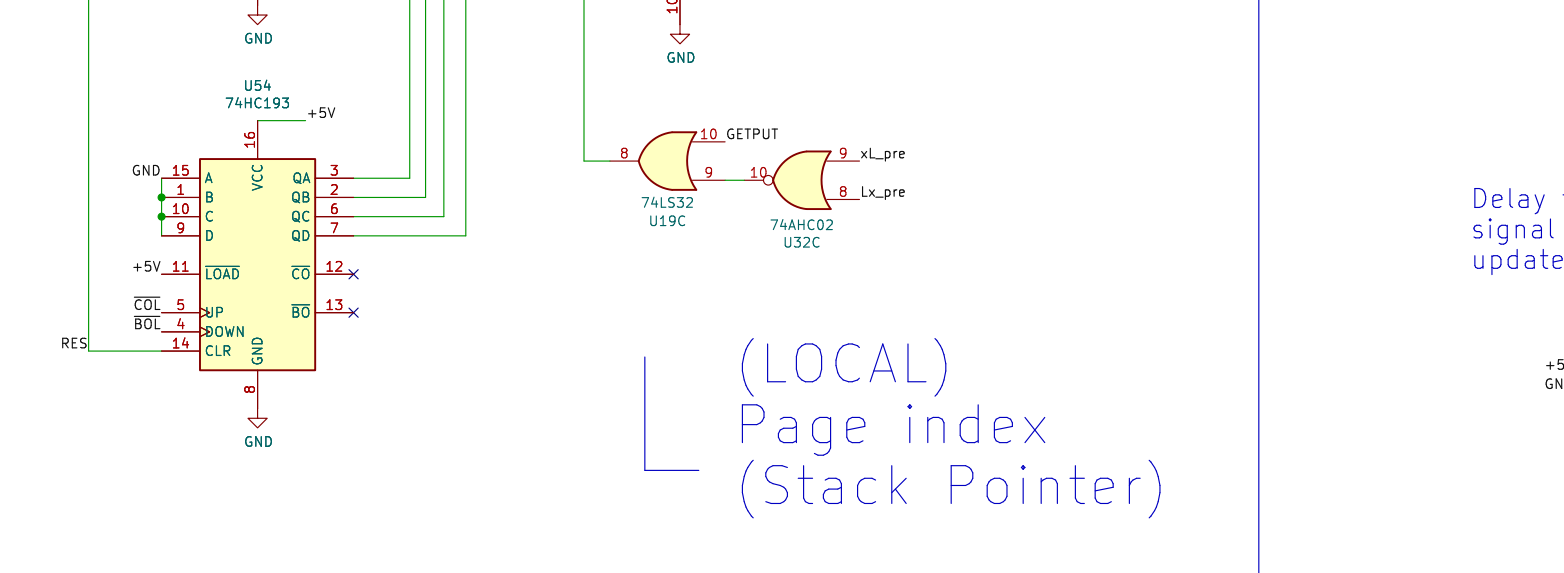
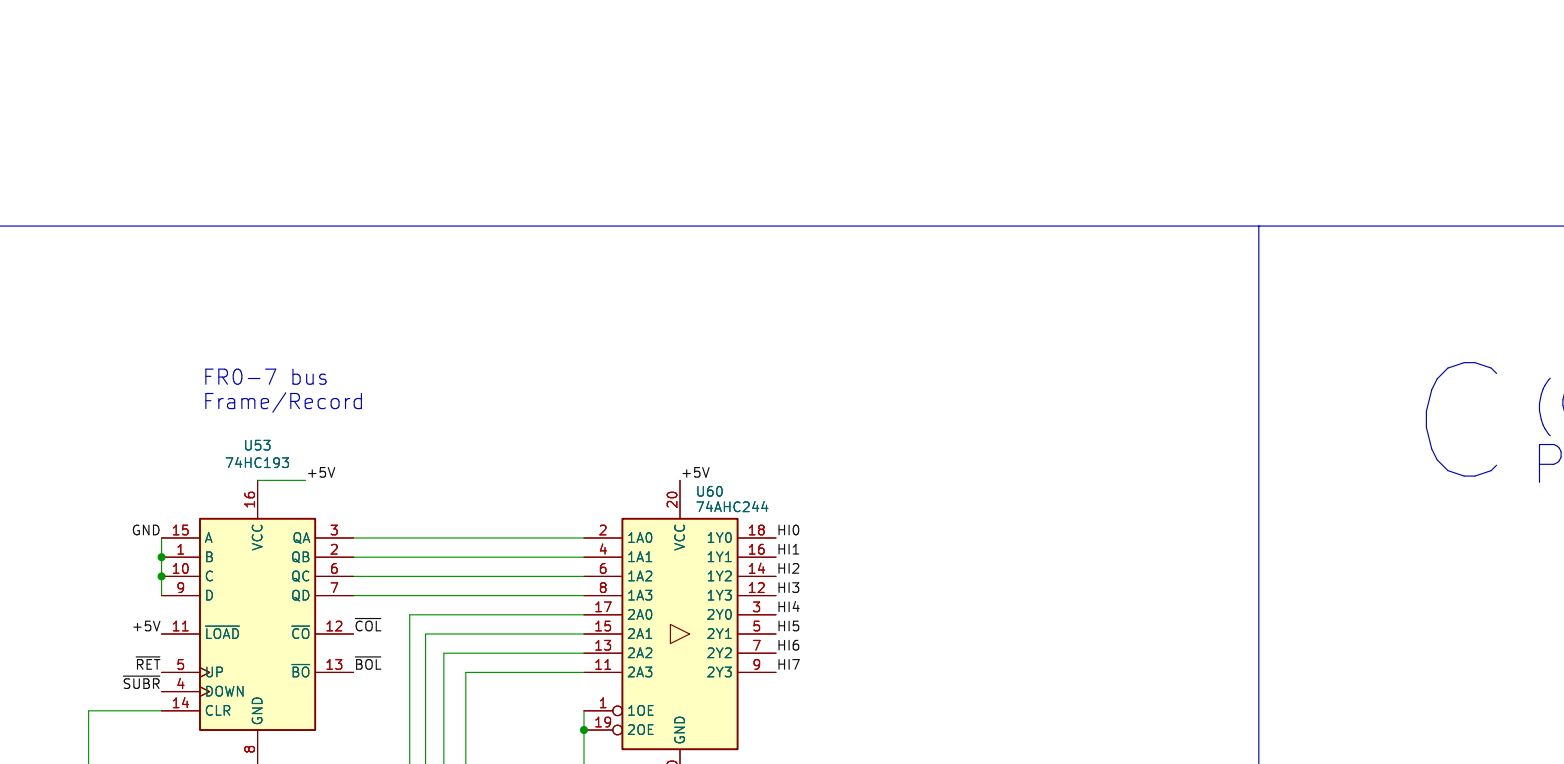
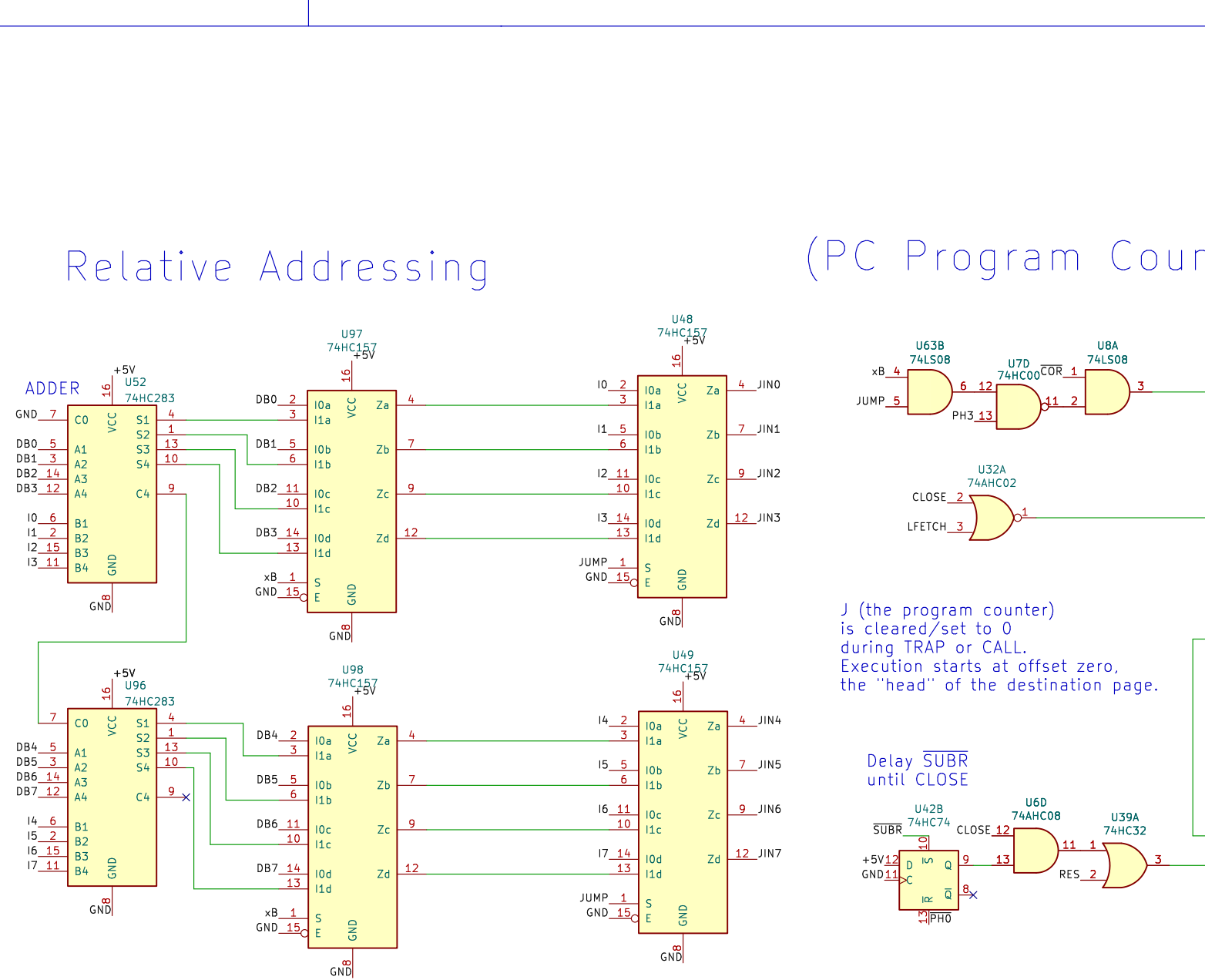
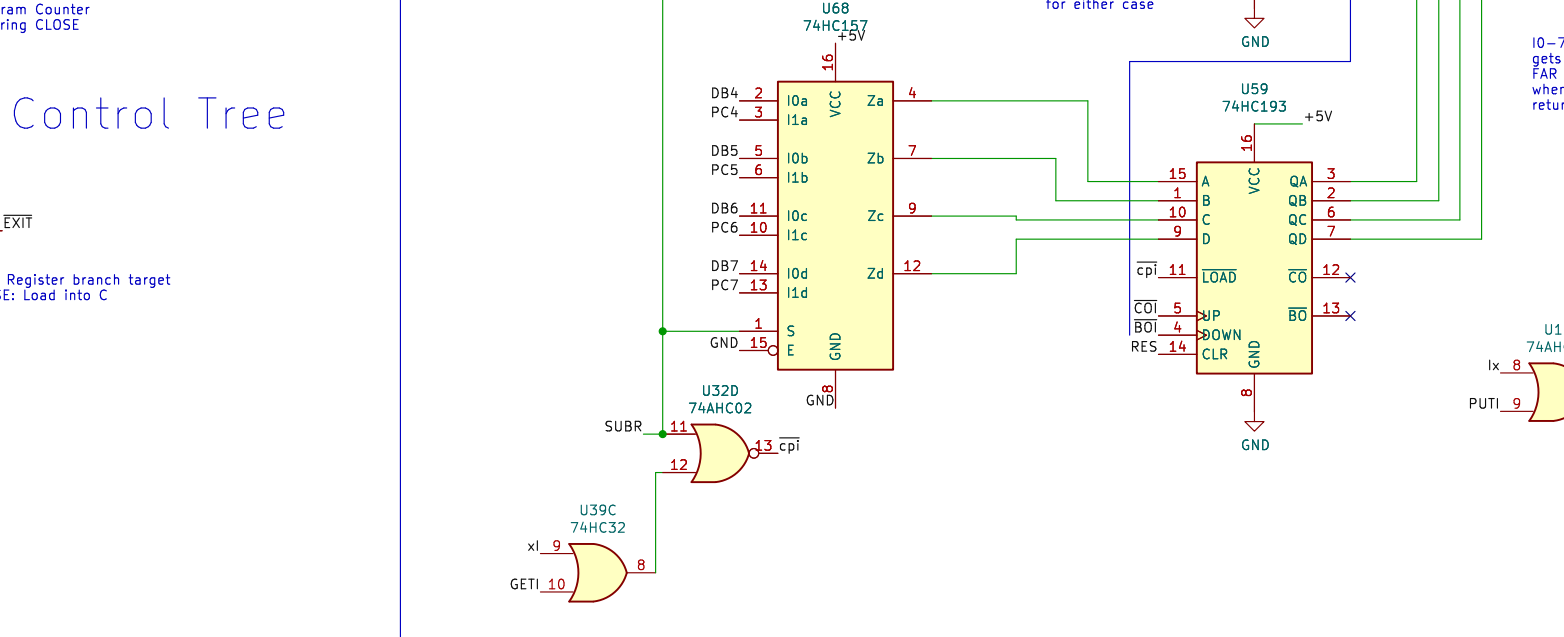
PHA0: Setup PC on address bus
PHA1: Latch opcode into IB0-7, predecoded
PHA2: Decode setup source/dest on IB or other action
PHA3: Latch source into target or other action
CLOSE: Cleanup



Implements SPI functionality with dedicated SER/DES registers



Ref. implementation connects two independent 4-bit groups (high/low) to 4:16 decoders (for synchronous latch enable / output enable events of two devices)



Implement an 8-bit parallel tri-state interface bus with dedicated in/out ports

