Myth Microcontroller Reference Schematics

Power

Caps

Clock Phases

~8MHz

"VLSI" Footprint

IO0-7 bus tri-state
internal pull-down

RES request

Instruction Decoder

Branching

Jump while value register V not zero
(decrements V)

Jump always

Jump if R not zero

Jump if R zero

Scrounger

Remap MM, RR, DD etc.
and impracticable opcodes such as NM

Currently NOP,
reserved for
instruction set
extension

Etc.

Control Tree

Clear Program Counter
applied during CLOSE

Exit Register branch target
CLOSE: Load into C

Pair DST Decoder

Pair SRC Decoder

Preselect decoders

Instruction-Word Latch

SYS decoder

TRAP decoder
Immediate calls

Opcode Type Decoder

Instruction byte:

```
all0: OPC_SYS     00000 xxx    See table @ SYS decoder
else: OPC_ADJUST  00001 xxx    b2:extended sign bit b1-0 LSB
      OPC_ALU     0001x xxx    See table @ ALU
      OPC_TRAP    001xx xxx    b4:MSB b3-0:LSB (remaining bits set 1)
      OPC_GETPUT  01xxx xxx    b5-3 OFFS b2:GL b1:GP B0:RO
      OPC_PAIR    1xxxx xxx    DEST SRC
```

8:3 Priority
Encoder CD4532

GETPUT Decoder

GETPUT
R/O

B (BASE register)

ADDER

xB: set B
xA: add to B

Inverters

J (JUMP register) (Program Counter)

(Relative addressing)

J (the program counter)
is cleared/set to 0
during TRAP or CALL.
Execution starts at offset zero.
the 'head' of the destination page.

Delay CLEAR
until CLOSE

C (CODE) Page index

Delay EXIT
until CLOSE

L (LOCAL) Page index (Stack Pointer)

FRO-7 bus
Frame/Record

Automatic call stack
CALL: Enter stack frame
RET: Resume previous frame

R Adjust

If bits 0-2
not all zero,
sign extend bit 2

Else hard-code
replace 0 by 4

```
0000 => 0100  +4 P4
0001  +1 P1
0010  +2 P2
0011  +3 P3
1100  -4 M4
1101  -3 M3
1110  -2 M2
1111  -1 M1
```

R(esult) Register

All delayed
by PHA2

ALU

O provides the return offset during RET
receives the return offset during SUBR
can be GET and PUT
provides all address offsets except FETCH
can be stored into
is the implied 2nd ALU input operand

When DC is executed,
prevents the DB output
from being updated with
the new return address
page index, before the
instruction is done.

O (OFFSET) Operand Register

0 IDR ("identity R" / R:=R)
1 IDO ("identity O" / R:=Old)
2 OCR ("Ones Complement R" / R:=-R)
3 OCO ("Ones Complement O" / R:=-O)
4 SLR ("Shift left New" / R:=R<<1)
5 SLO ("Shift left Old" / R:=O<<1)
6 SRR ("Shift right R" / R:=R>>1)
7 SRO ("Shift right O" / R:=O>>1)

8 AND (R:=R&O)
9 IOR (R:=R|O)
10 EOR (R:=R^O)
11 ADD (Add" / R:=R+O, bits 0-7)
12 CAR ("Carry Bit" / R:= Carry, 9th bit of R+O) 00h or 01h
13 RLO ("Flag: R less than O" / R:= (R<O)? 0xFF:0
14 REQ ("Flag: R equals O" / R:= (R==O)? 0xFF:0
15 RGO ("Flag: R greater than O" / R:= (R>O)? 0xFF:0

Storage

Memory M

I (INNER Loop Register)

G (GLOBAL) Page index

S SIR

Serial clock out

E SOR

Serial IO

Implements SPI functionality
with dedicated SER/DES registers

Device Enable

Ordinal 0
selects a
NULL DEVICE

Ref. implementation
connects two independent
4-bit groups (high/low)
to 4x16 encoders
(for simultaneous
latch enable
output enable
of two separate devices)

ACTIVE HIGH ENABLE

ACTIVE LOW ENABLE

NULL device

P POR

Parallel IO

Implement an 8-bit parallel tri-state
interface bus with dedicated In/Out ports

Glue Logic

Spare Units

Project homepage: https://github.com/Doxflange/Myth
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File: myth.kicad_sch

Title: Sonne-8 Micro-Controller

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