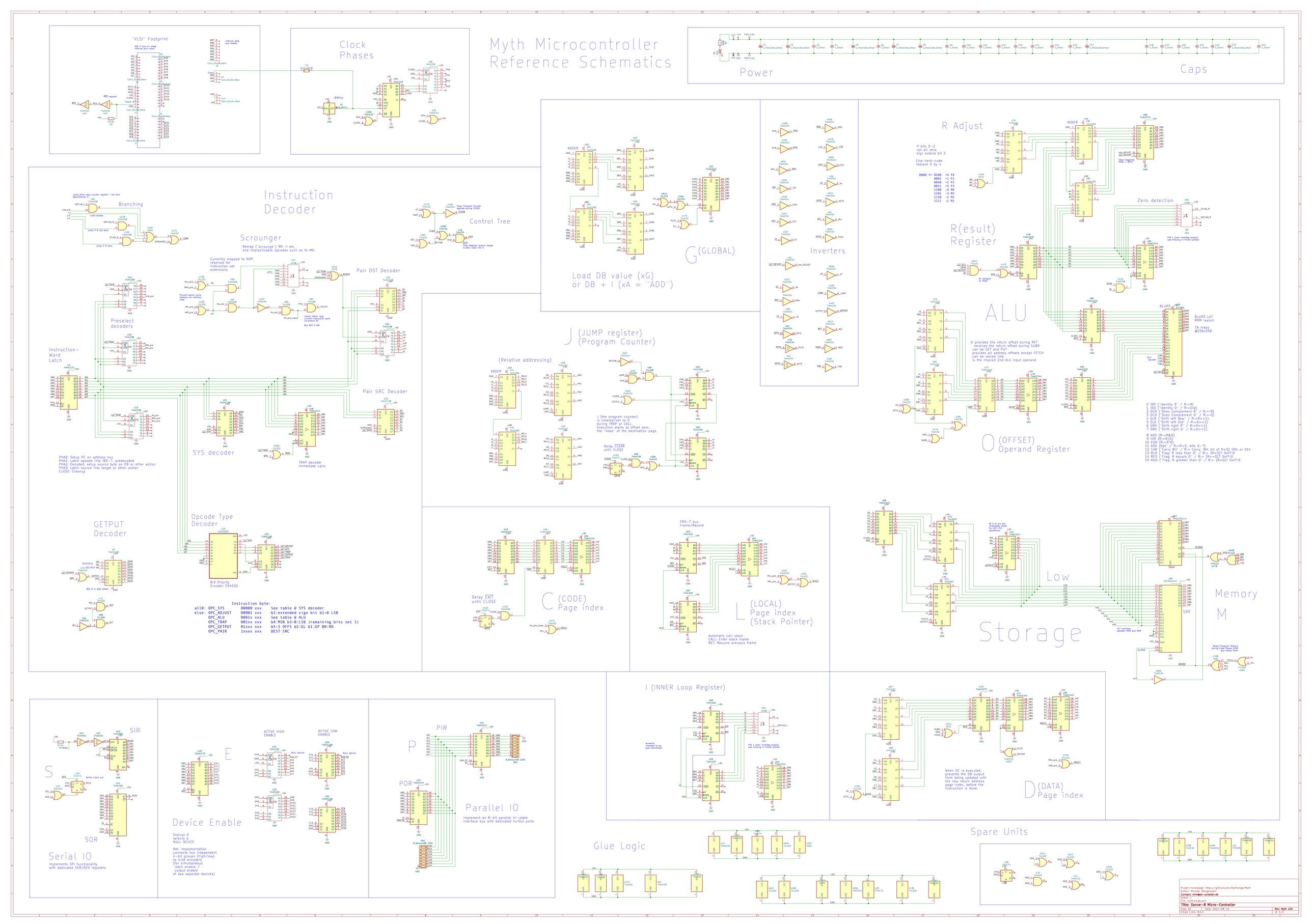
Myth Microcontroller Reference Schematics
"VLSI" Footprint
Clock Phases
Power
Caps
Instruction Decoder
Branching
Scrounger
Control Tree
Preselect decoders
Instruction-Word Latch
Pair DST Decoder
Pair SRC Decoder
SYS decoder
TRAP decoder Immediate calls
GETPUT Decoder
Opcode Type Decoder
G (GLOBAL)
Load DB value (xG) or DB + 1 (xA = "ADD")
Inverters
J (JUMP register) (Program Counter)
(Relative addressing)
R Adjust
R(esult) Register
ALU
O (OFFSET) Operand Register
Zero detection
Low Storage
Memory M
C (CODE) Page index
L (LOCAL) Page index (Stack Pointer)
I (INNER Loop Register)
D (DATA) Page index
S SIR
SOR
Serial IO
E
Device Enable
P
PIR
POR
Parallel IO
Glue Logic
Spare Units
Project homepage: https://github.com/Doollange/Myth
Author: Michael Mangelsdorf
Contact: mimesk-schaller.de
Sheet: /
File: myth.kicad_sch
Title: Sonne-8 Micro-Controller
Size: A0 | Date: 2024-08-21 | Rev: Myth LGX
KiCad E.D.A. 8.0.4 | Id: 1/1