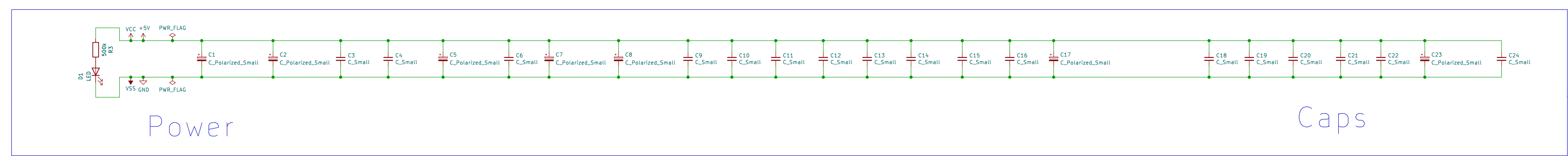
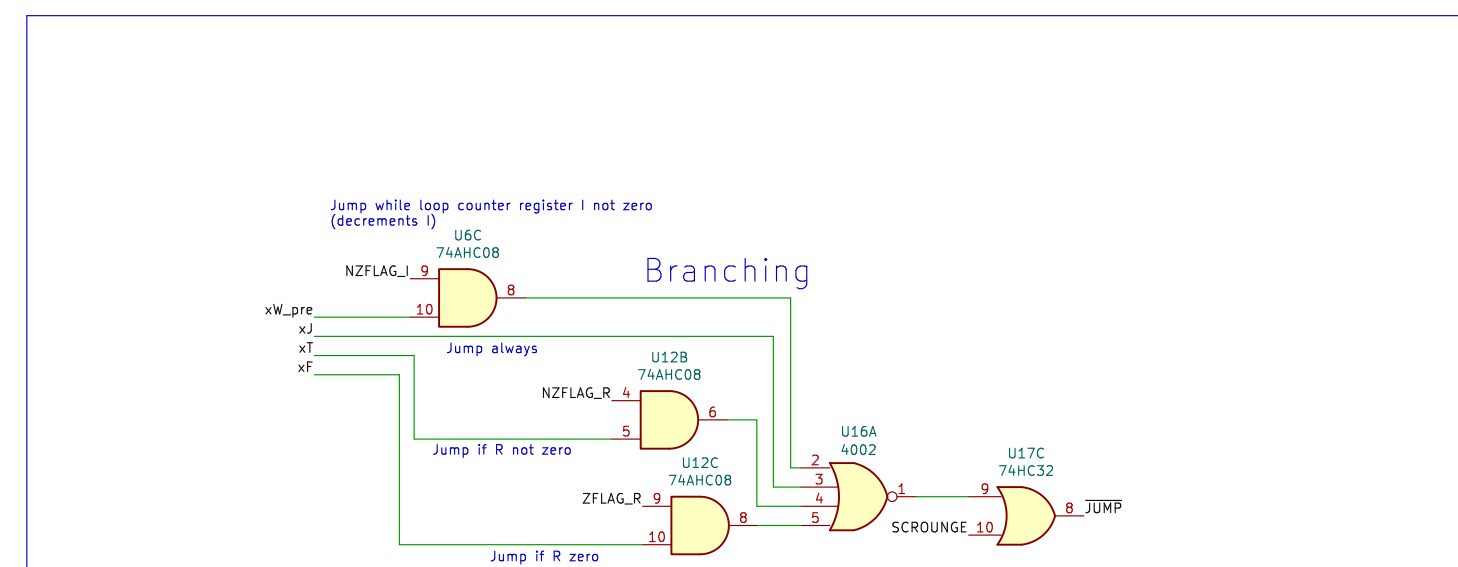


Sonne-8 Microcontroller Reference Schematics Rev. Myth/LOX



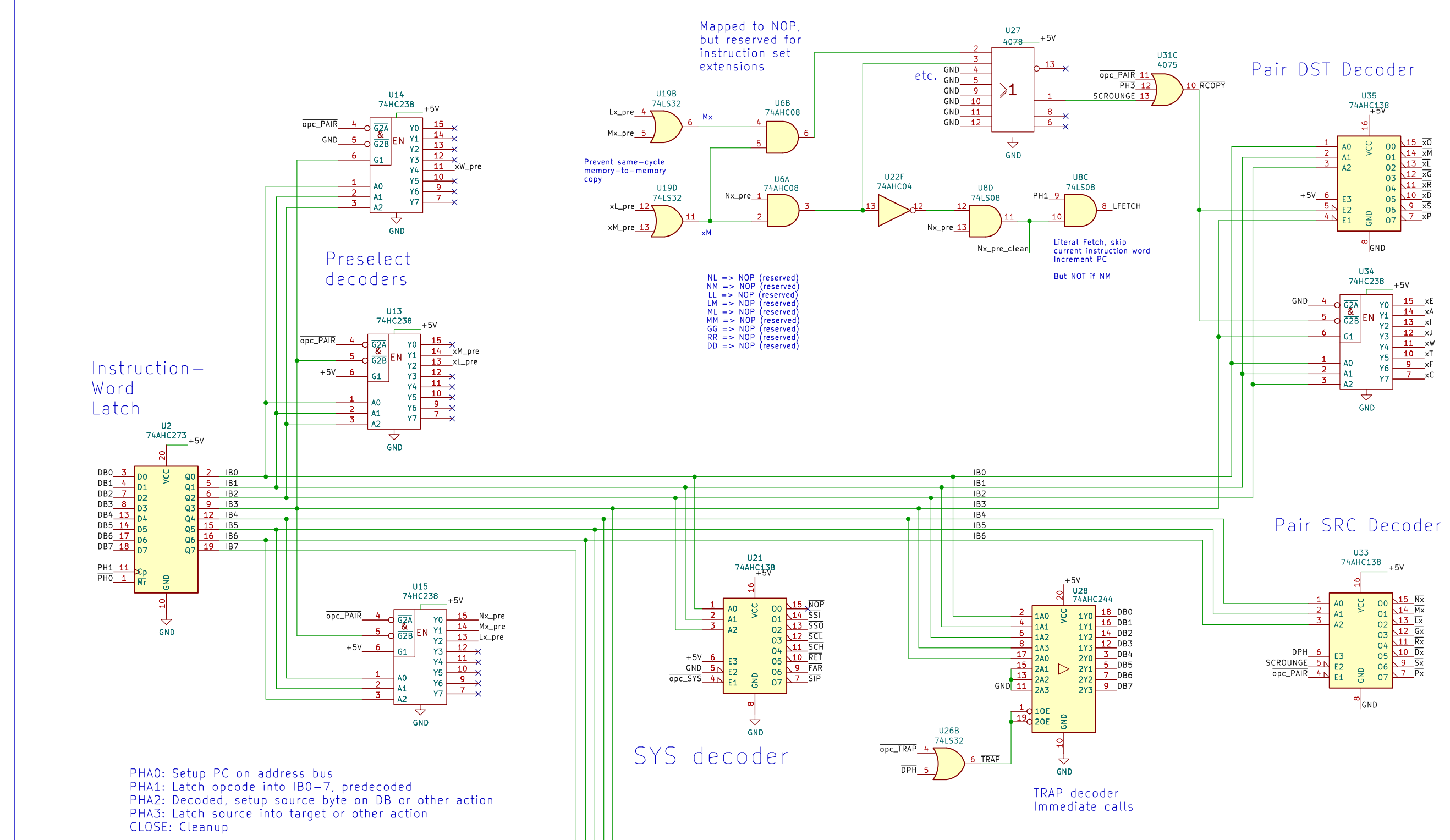
Caps



Instruction Decoder

Scrounger

Remap ("scrounger") G0, R0, R1 etc. and impracticable opcodes such as NM

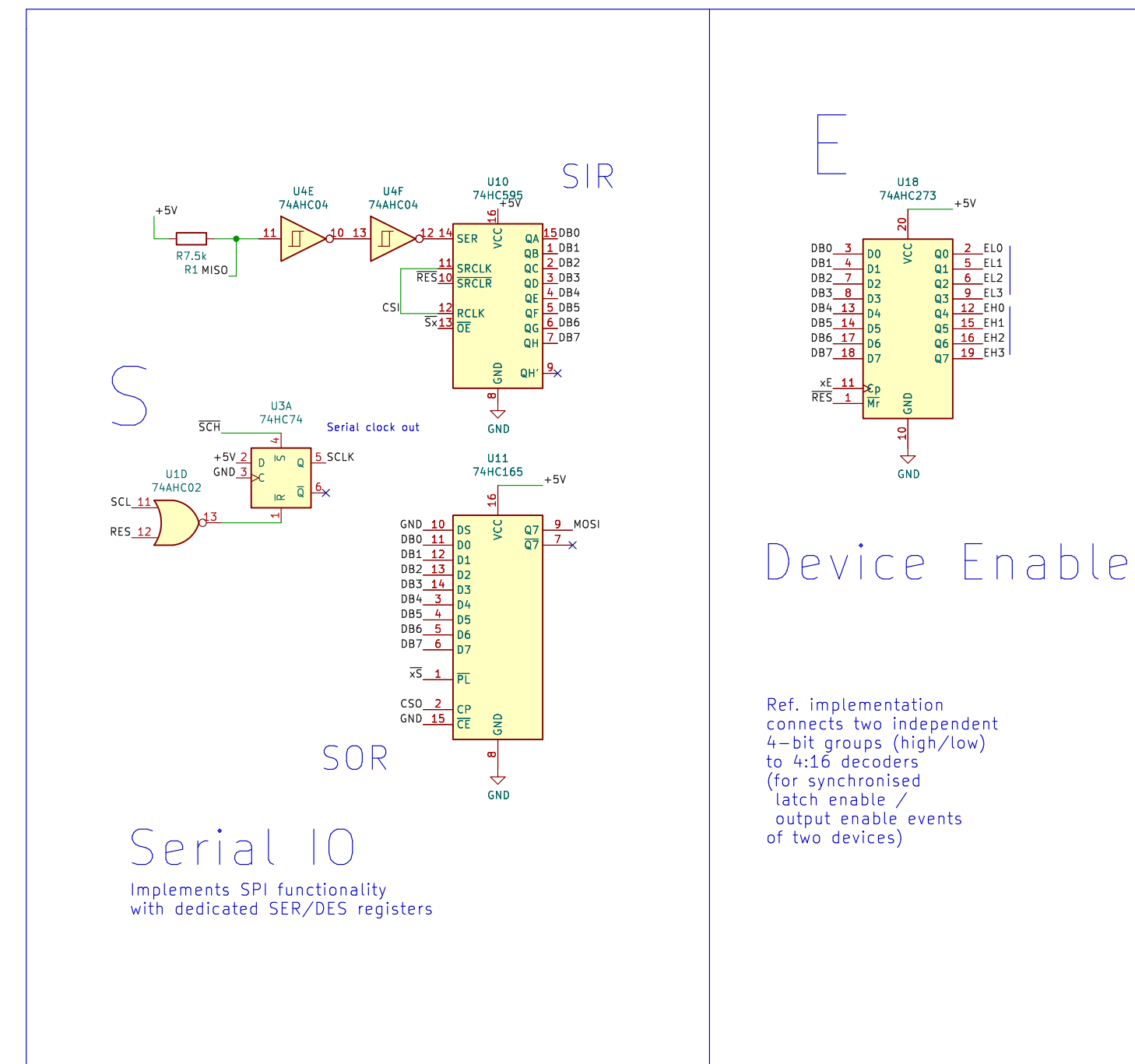
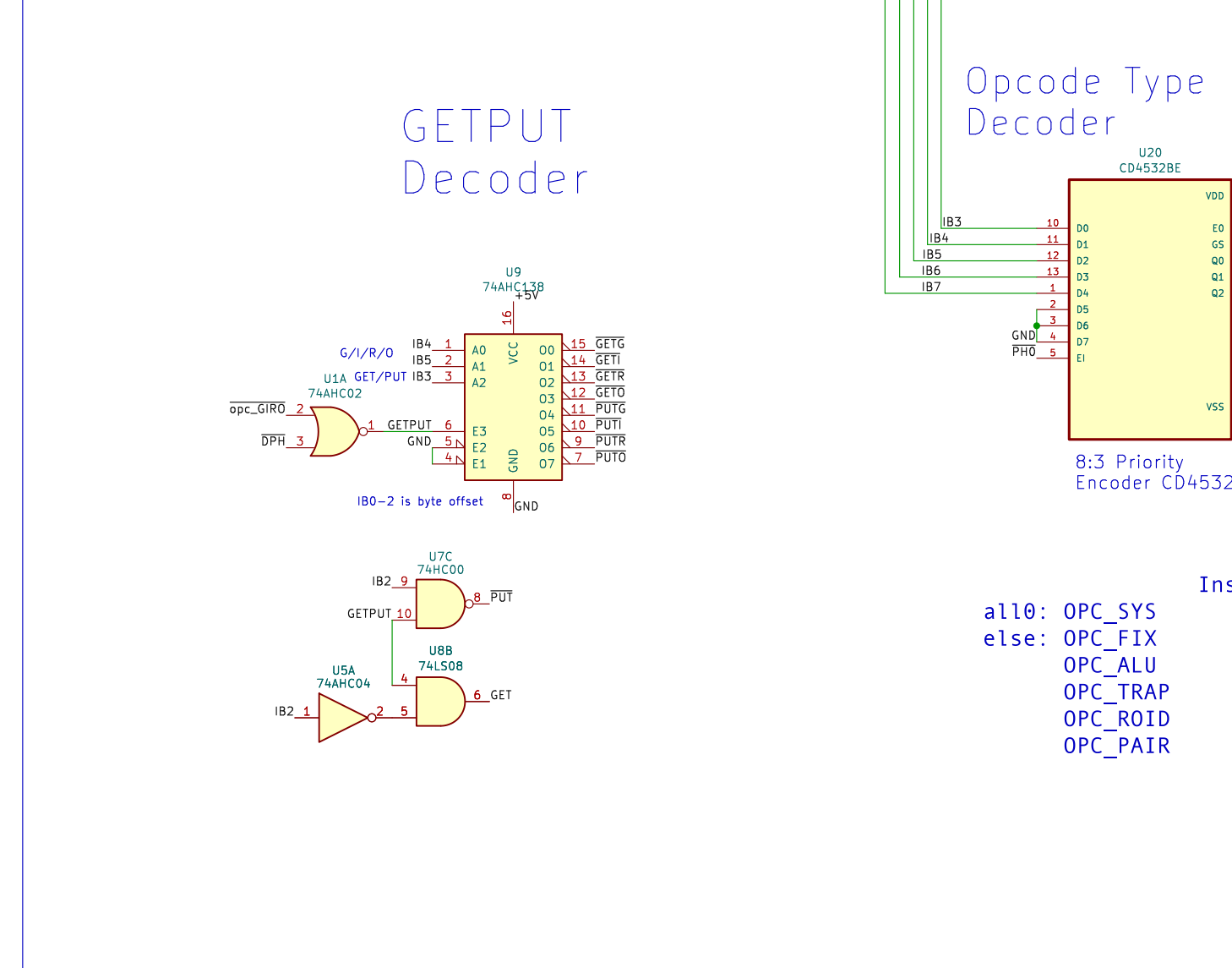


SYS decoder

Opcode Type Decoder

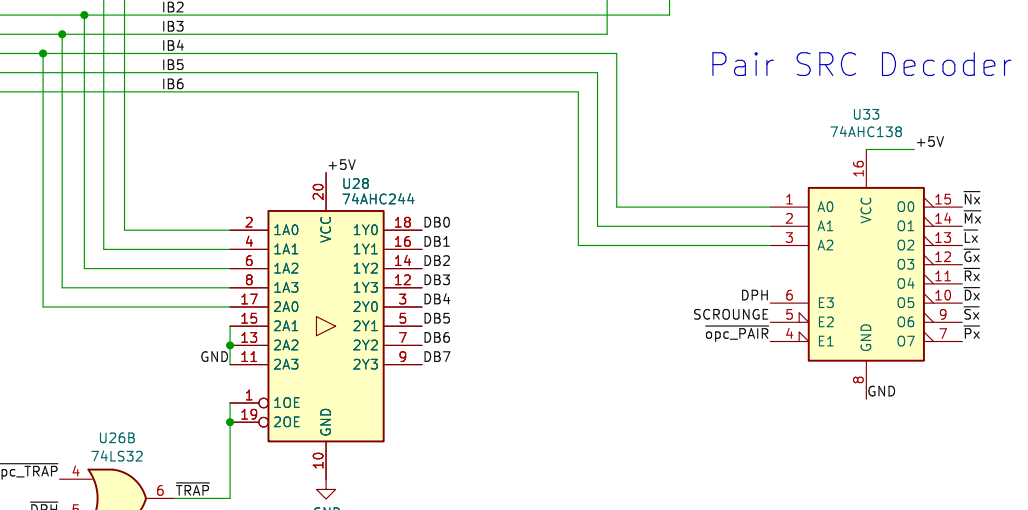
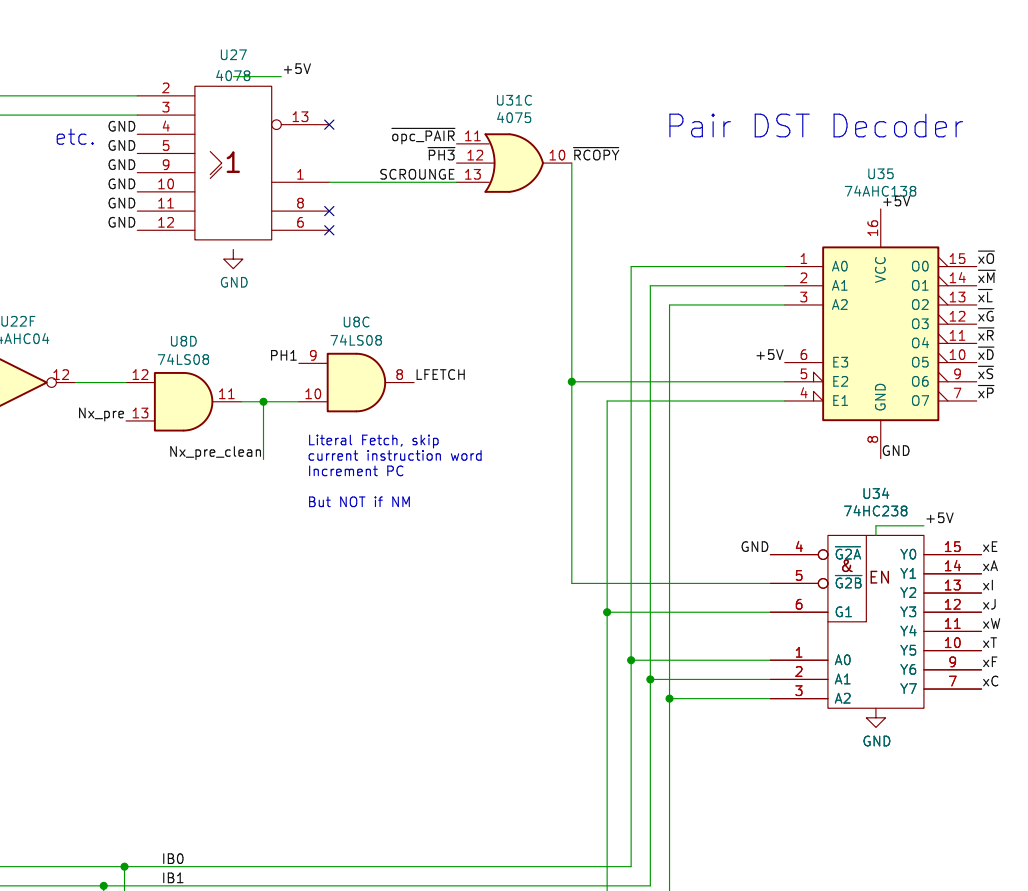
Instruction byte:
a10: OPC_SYS
else: OPC_FIX
OPC_AIU
OPC_TRAP
OPC_R0ID
OPC_PAIR

00000 xxx See table 0 SYS decoder
00001 xxx b2: extended sign bit b1-0 LSB
0001x xxx See table 0 ALU
001xx xxx b4: MSB b3-0: LSB (remaining bits set 1)
01xxx xxx db-2 OFFS b3: GET/PUT b4-5: REG(R0ID)
1xxxx xxx DEST SRC

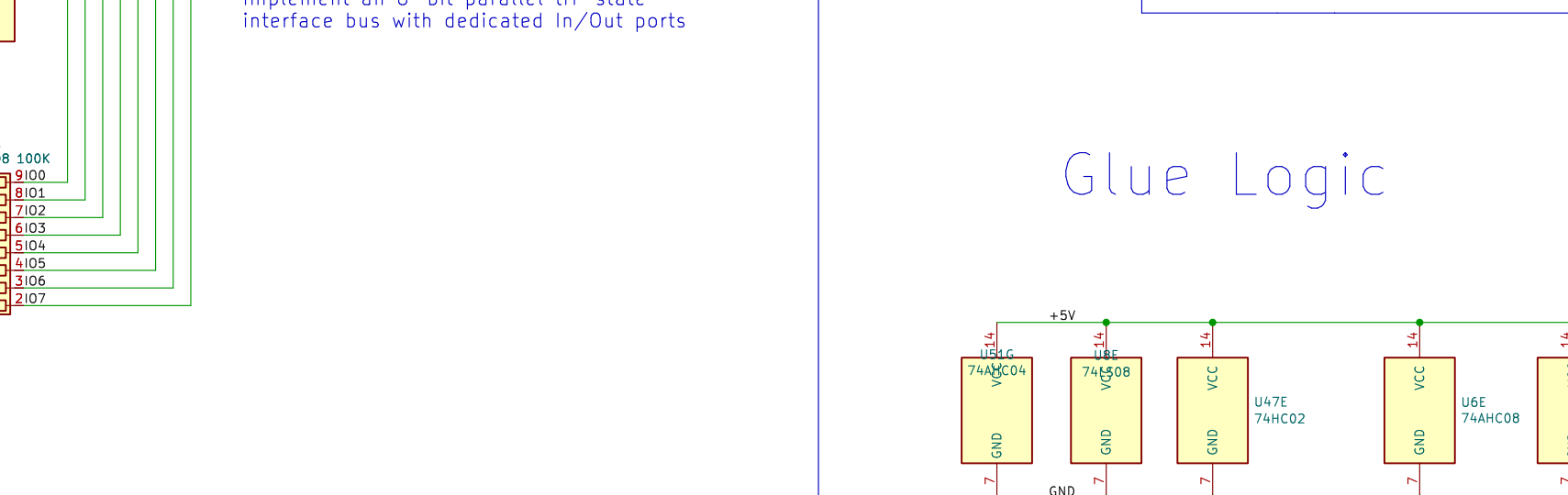
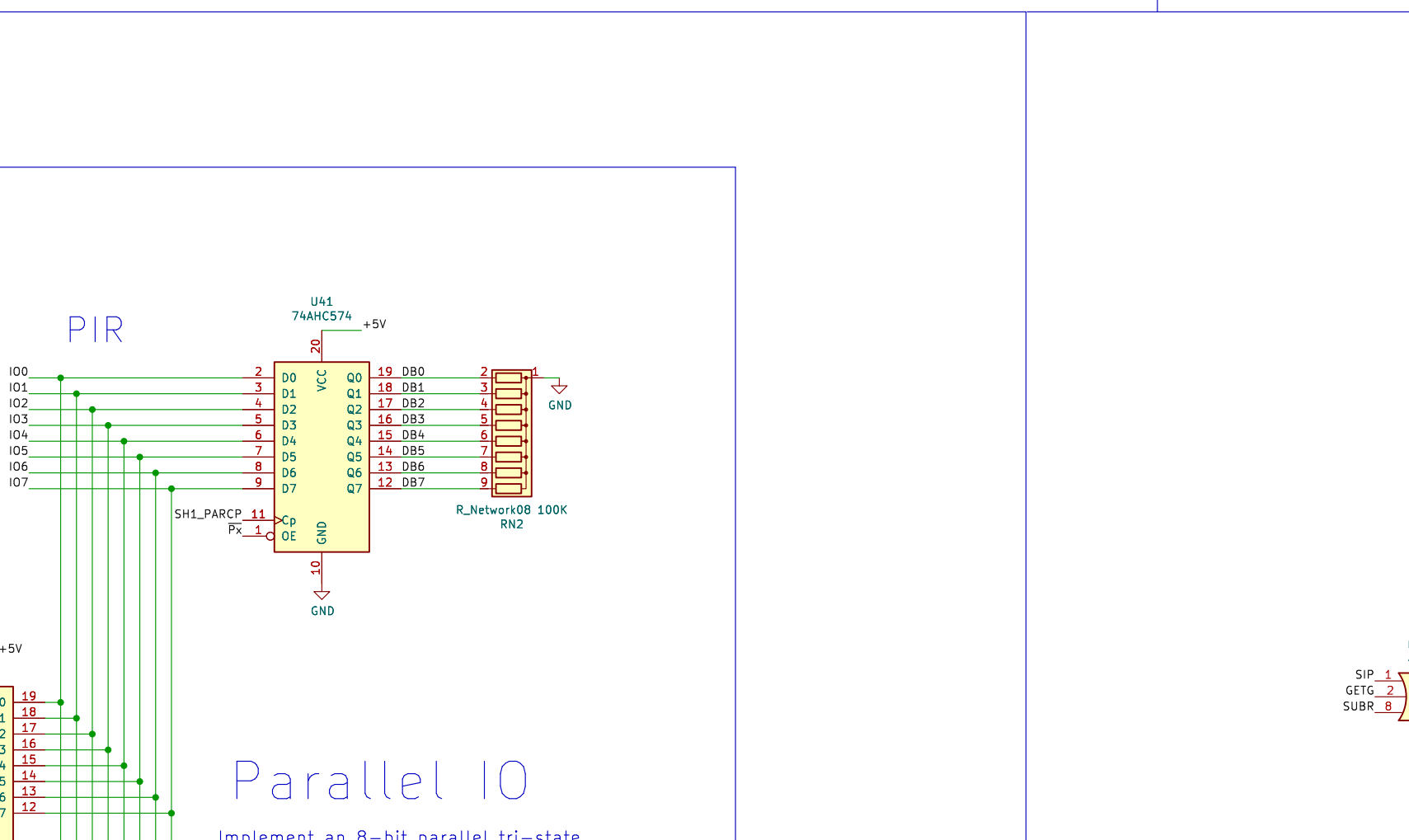
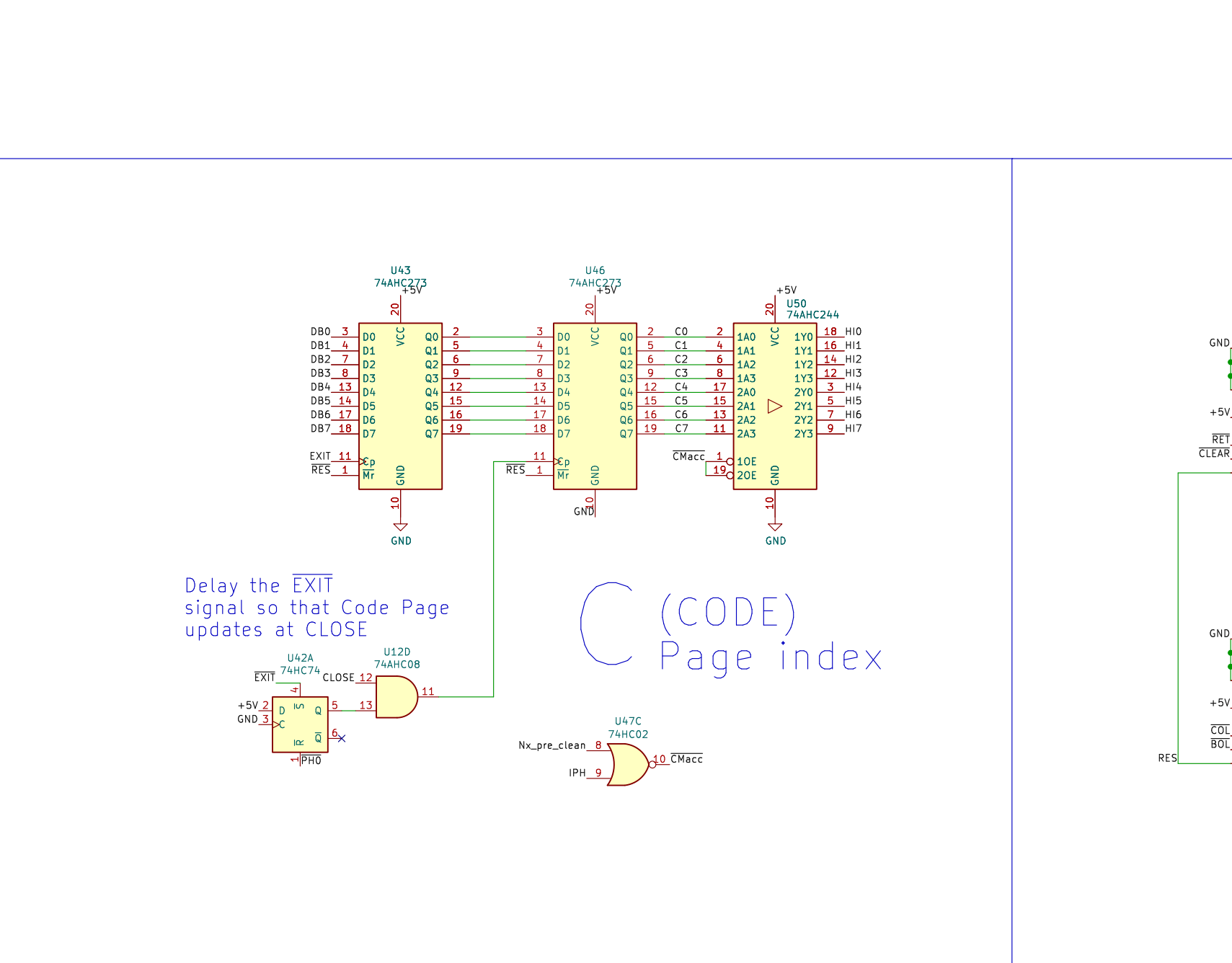
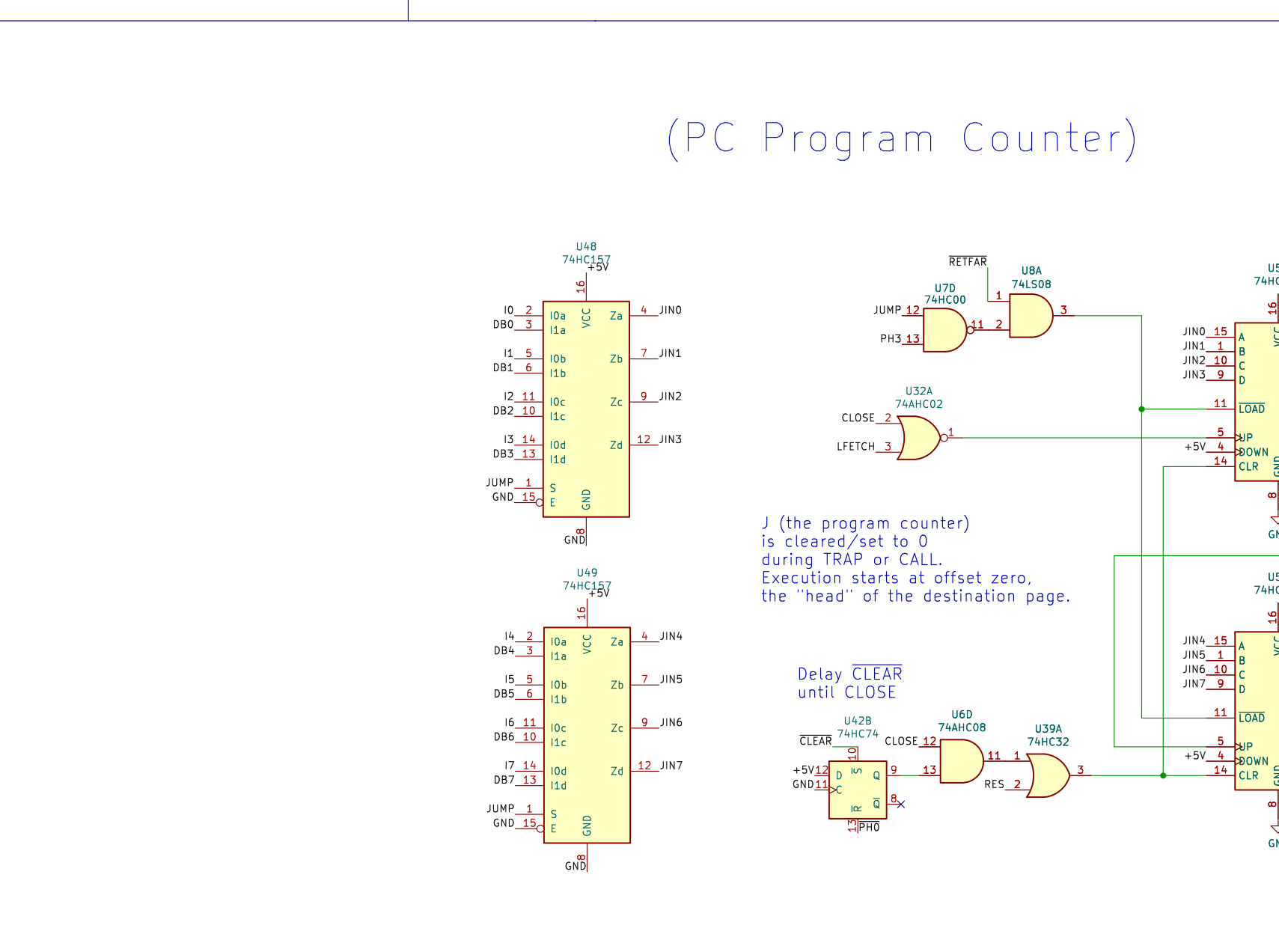
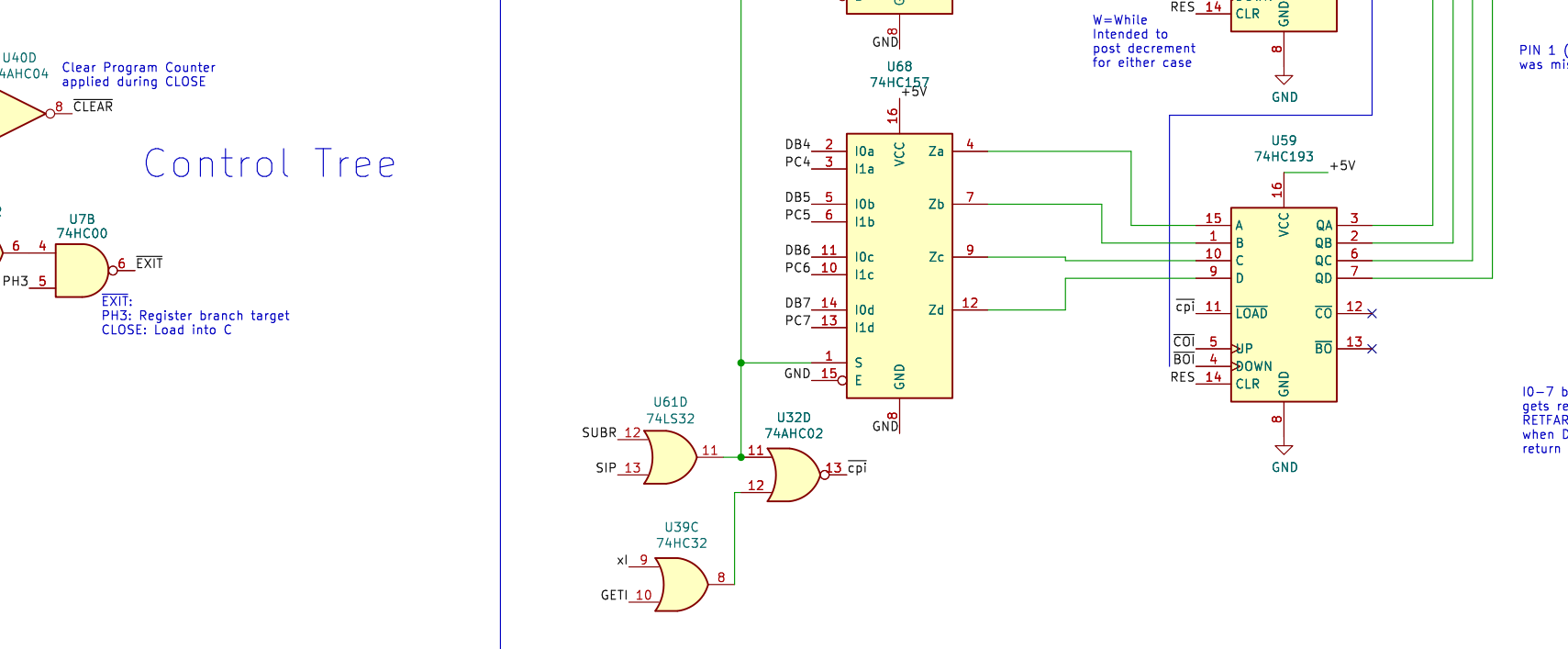


Device Enable

Ref. implementation connects two independent 5-bit decoders (high/low) to 4-16 decoders (for synchronised / latch enable / output enable events of two devices)

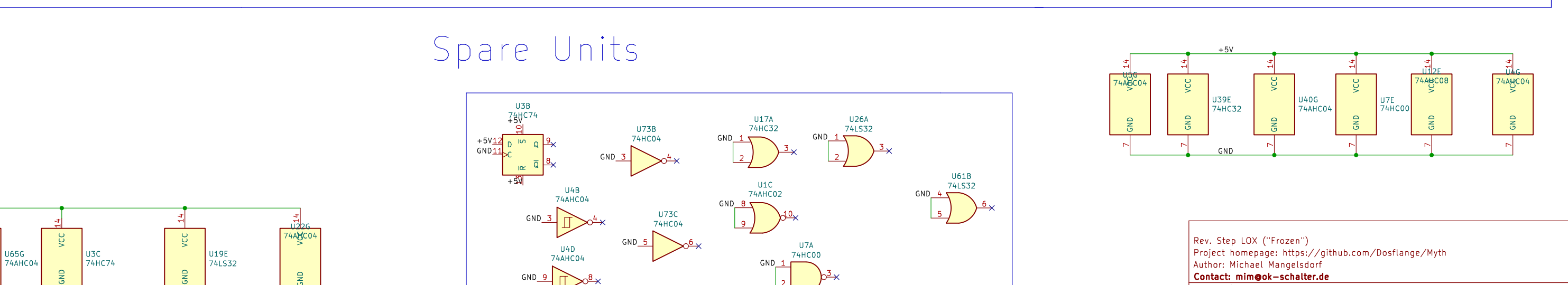
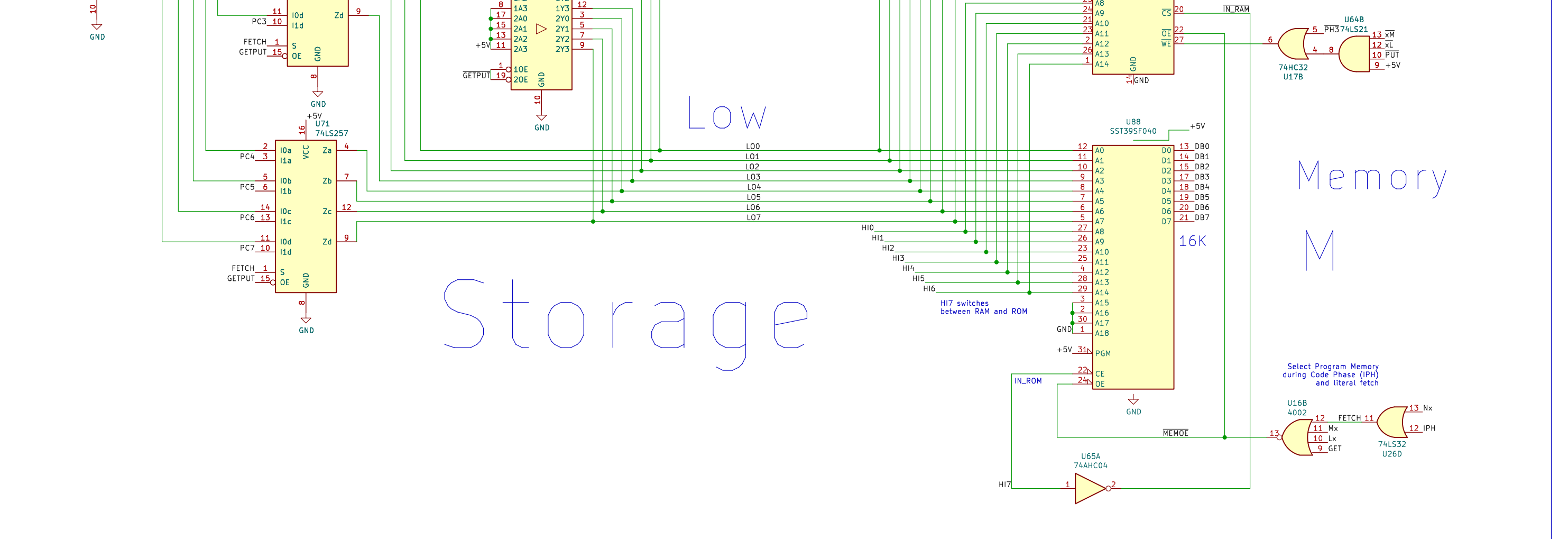
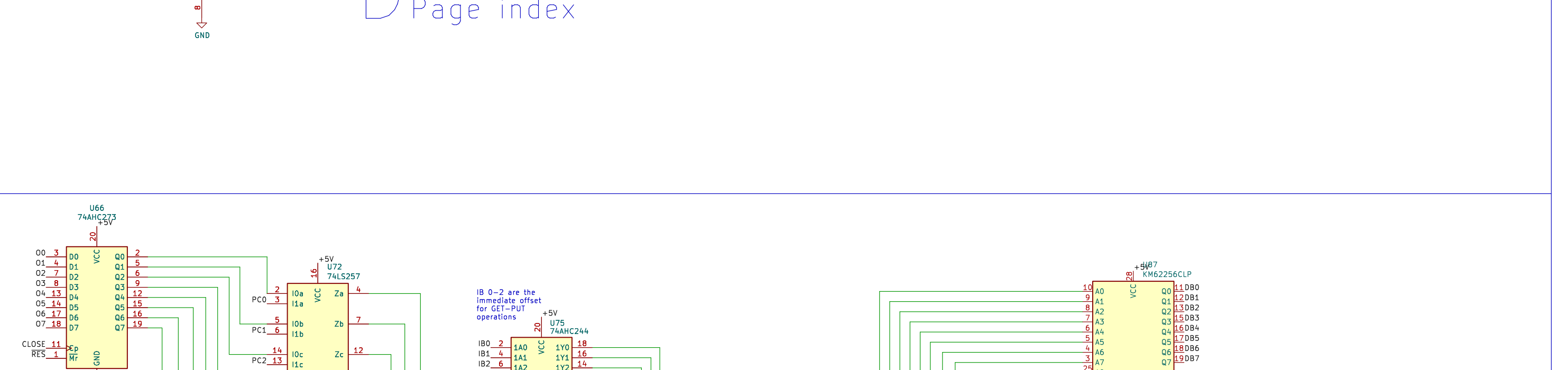
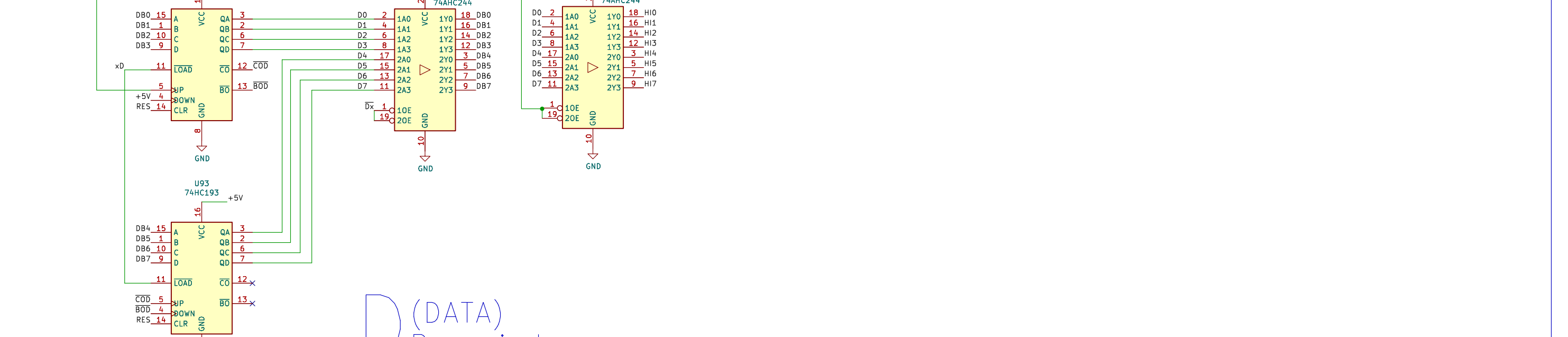
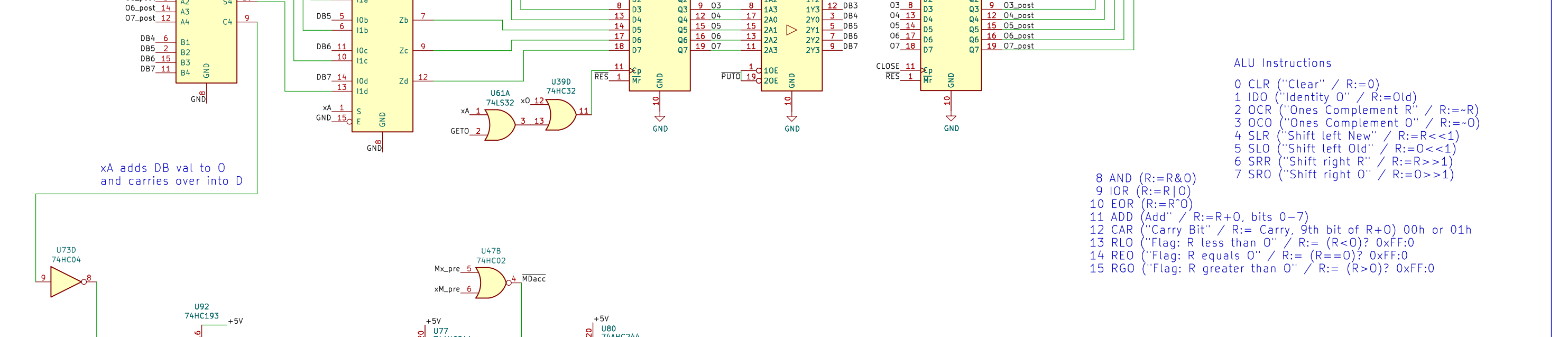
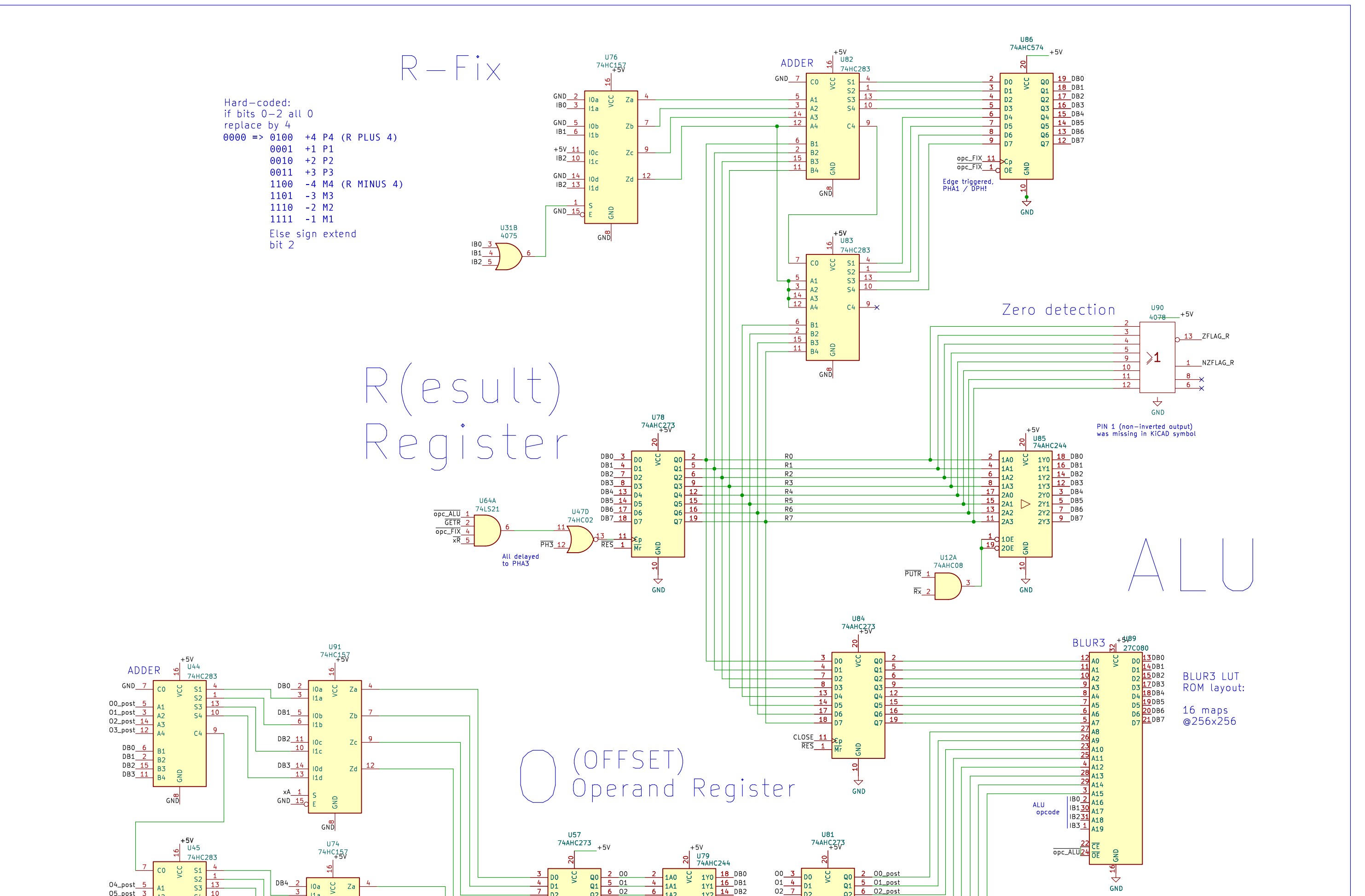
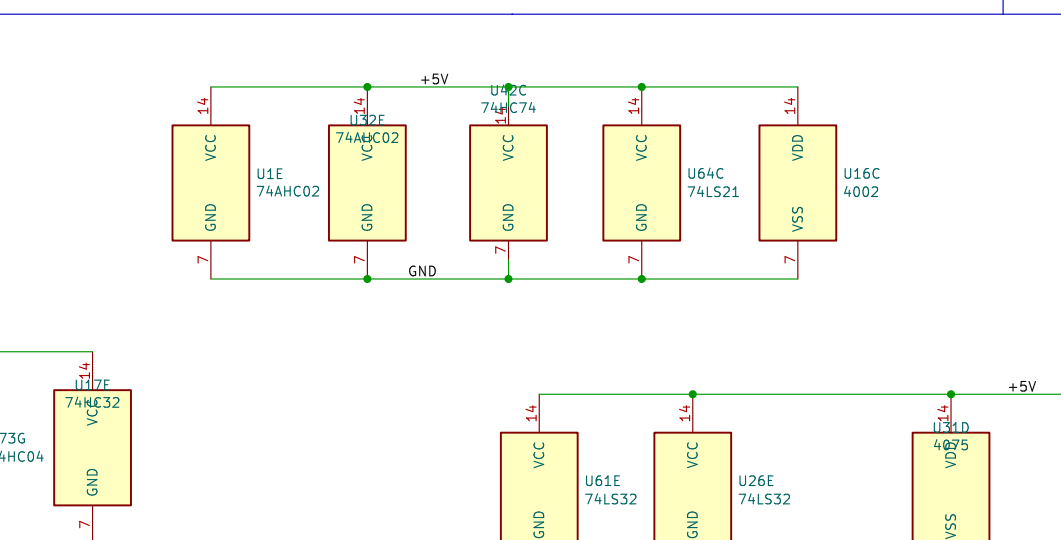
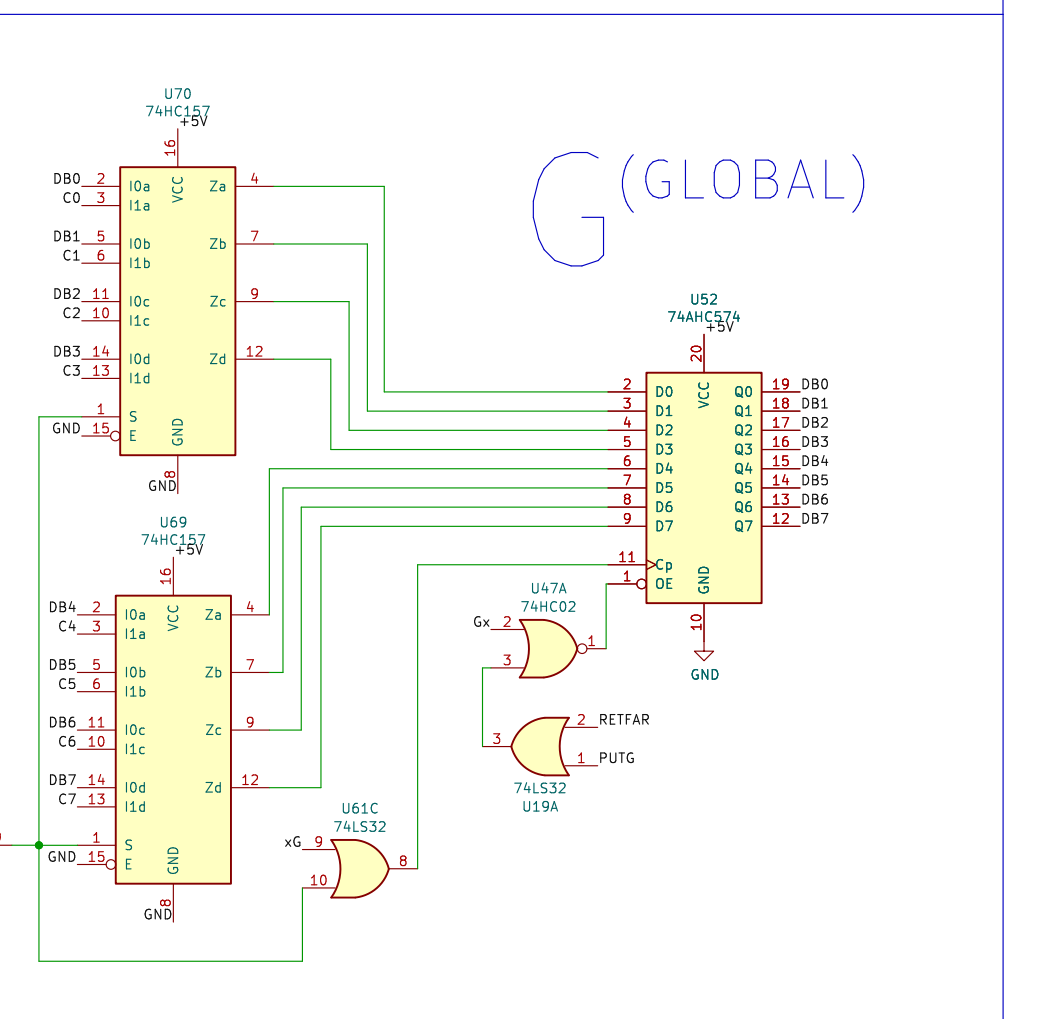
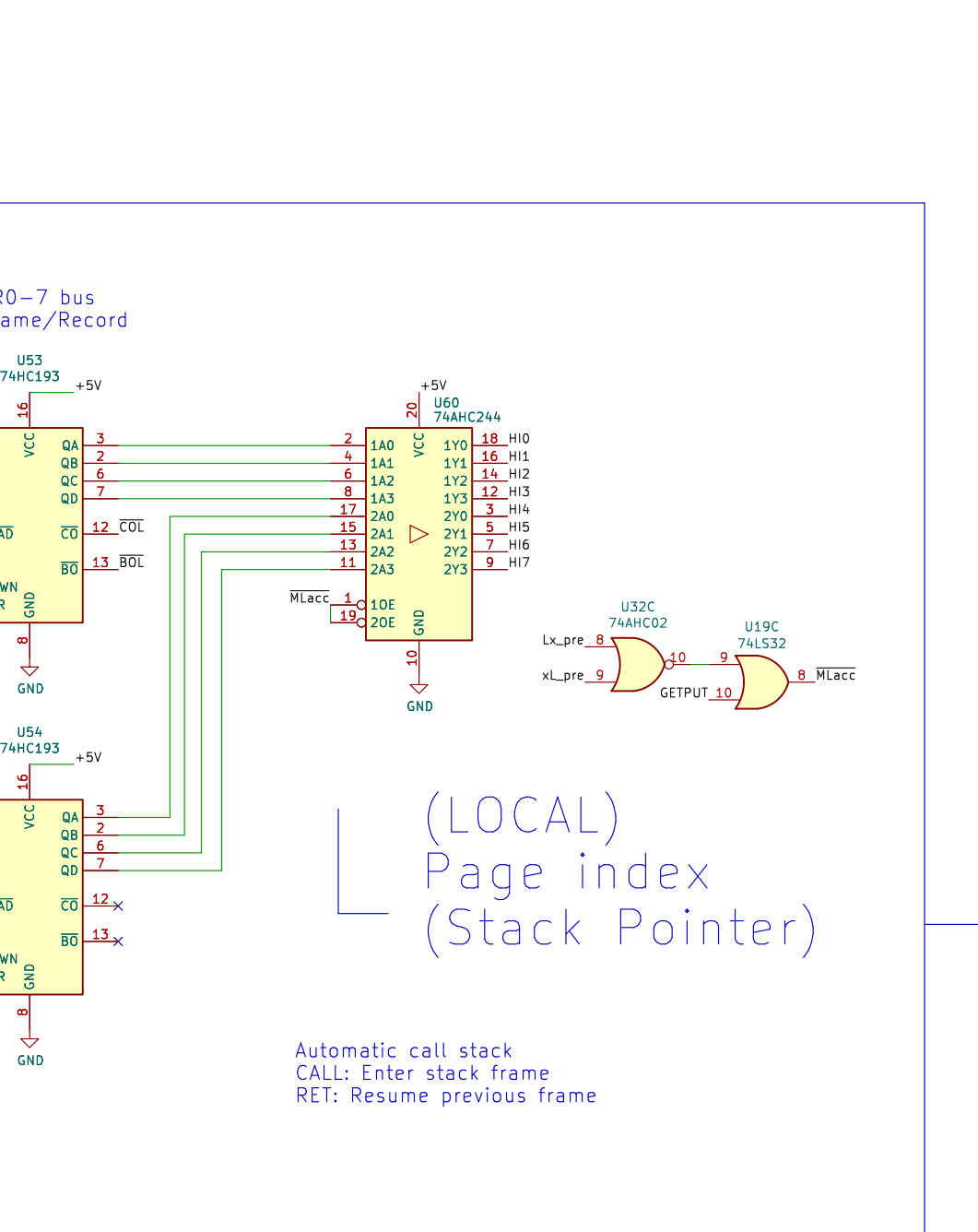
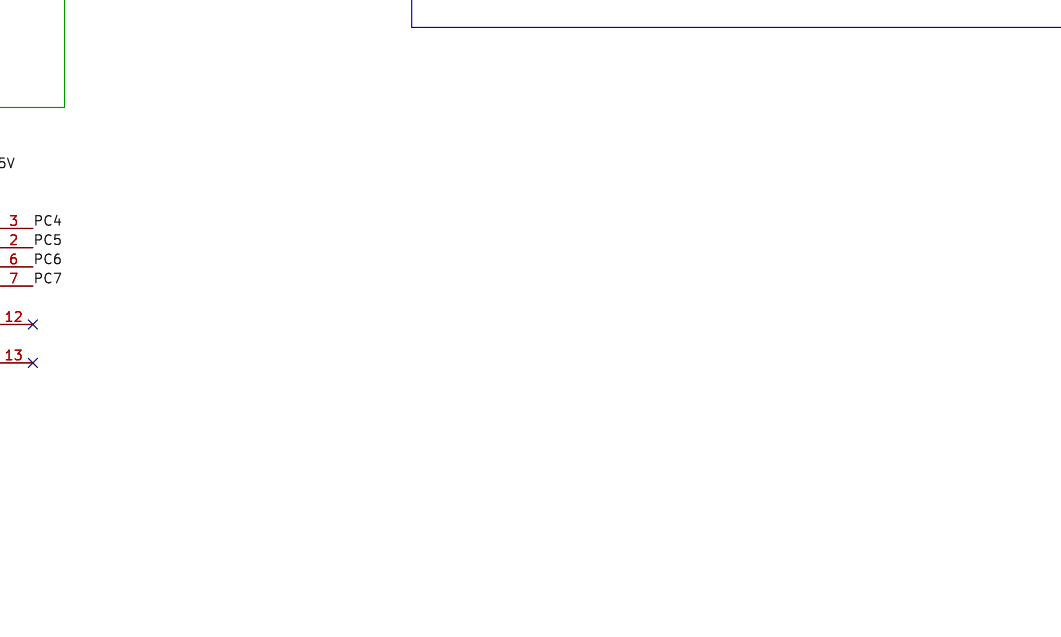
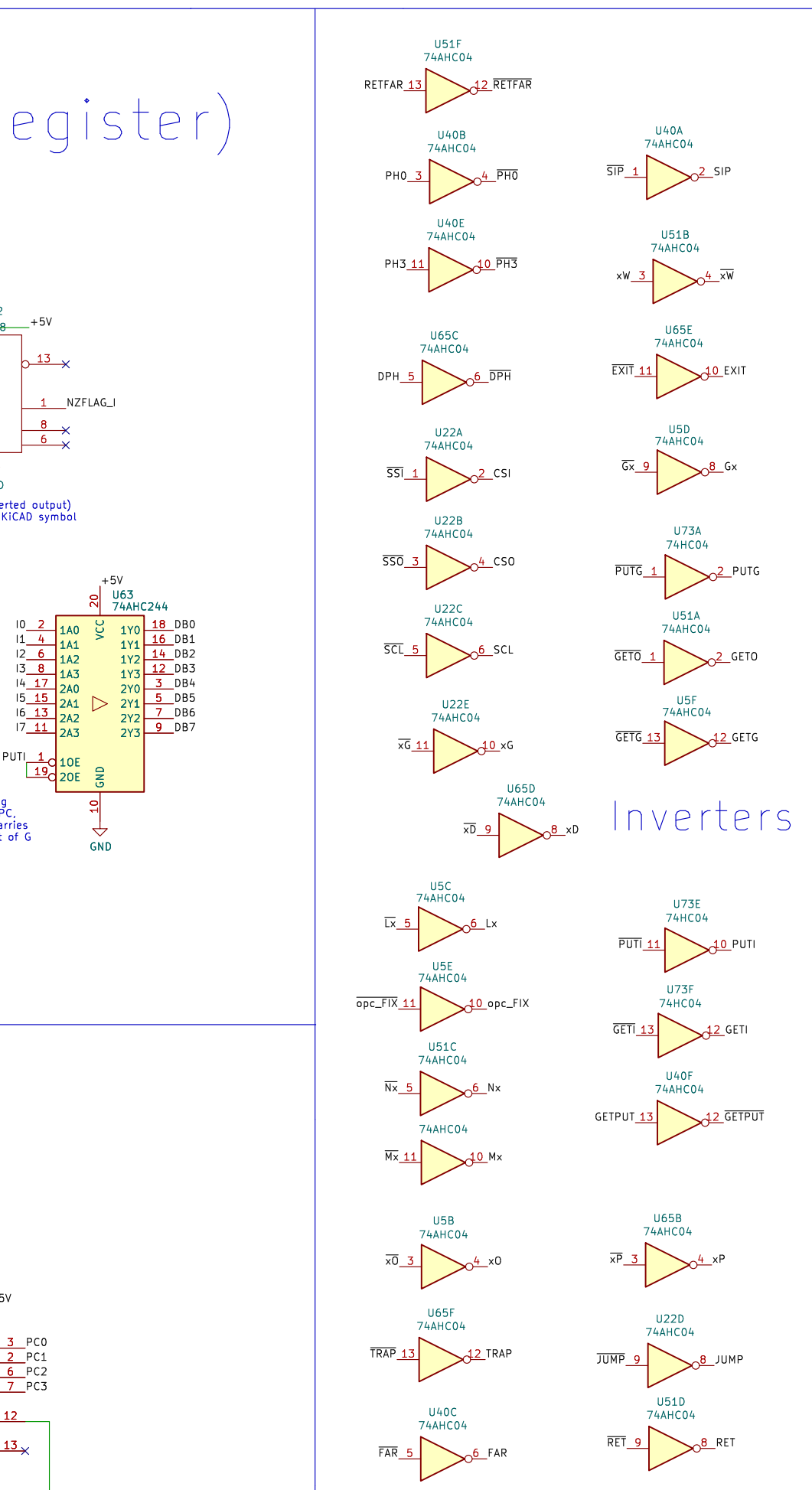
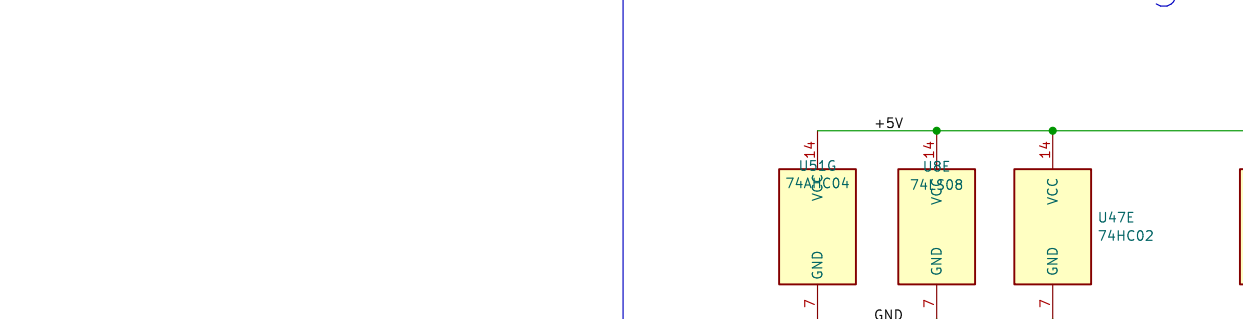


TRAP decoder immediate calls



Implement an 8-bit parallel tri-state interface bus with dedicated In/Out ports

Glue Logic



Spare Units

