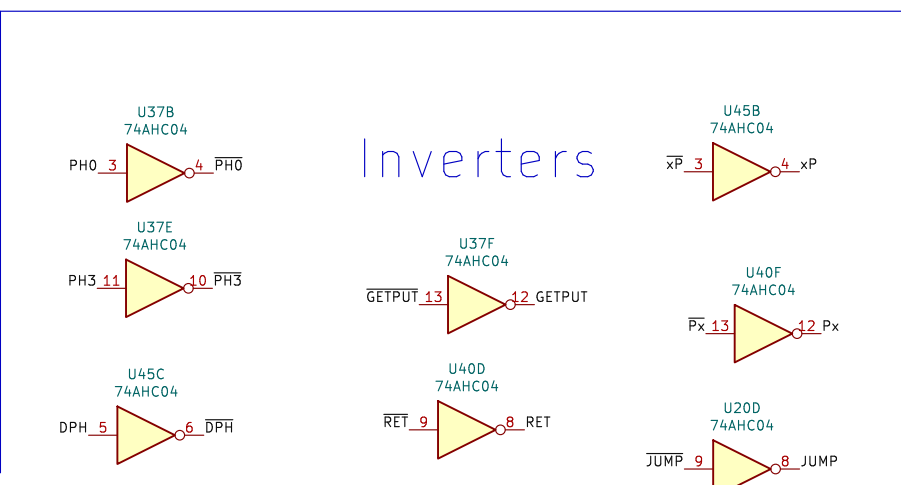
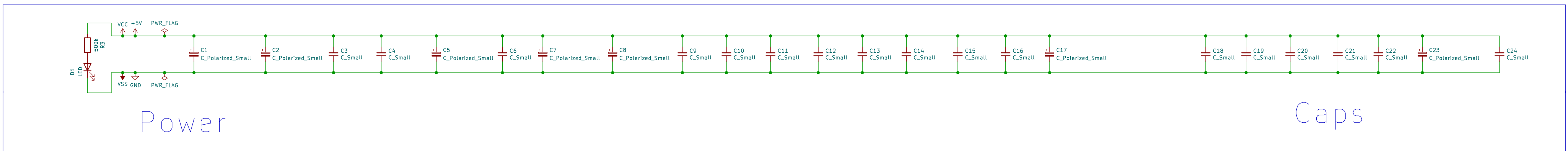
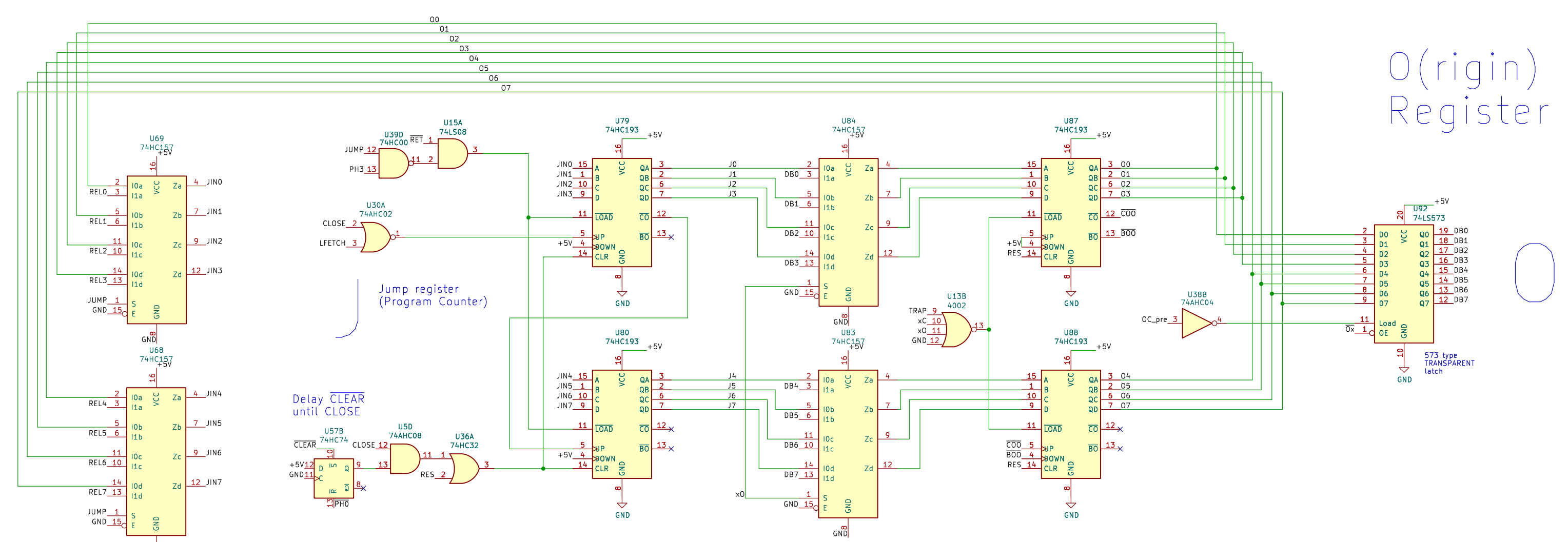


Sonne Microcontroller Reference Schematics rev. Myth



(Relative Jumps)



Instruction Decoder

Scrounger

Remap MM, RR, DD etc. and impracticable opcodes such as NM

Control Tree

Preselect decoders

Instruction-Word Latch

SYS decoder

Opcode Type Decoder

GETPUT Decoder

Instruction byte:
all0: OPC_SYS 00000 xxx
else OPC_ADJUST 00001 xxx
OPC_ALU 0001x xxx
OPC_TRAP 01xxx xxx
OPC_GETPUT 01xxx xxx
OPC_PAIR 1xxxx xxx

See table # SYS decoder
b2: extended sign bit b1-0 LSB
See table # ALU
b4-MSB b3-0: LSB (remaining bits set 1)
b5-4: OFFS b3-GL b2-GL b1-0: ABRV
DE5T SRC

A

R(result) Register

BLUR3 LUT ROM layout:
16 maps @256x256

0 IDA "Identity A" / F=A
1 IDB "Identity B" / F=B
2 OCA "Ones Complement A" / F=~A
3 OCB "Ones Complement B" / F=~B
4 SLA "Shift left A" / F=A<<1
5 SLB "Shift left B" / F=B<<1
6 SRA "Shift right A" / F=A>>1
7 SRA "Shift right B" / F=B>>1
8 AND (F=A&B)
9 OR (F=A|B)
10 XOR (F=A^B)
11 ADD "Add" / F=A+B, bits 0-7
12 CDB "Carry Bit" / F=Carry, 0th bit of A+B 0th or 0th
13 ALB "Flag: A less than B" / F=(A<B)? 0xF0
14 AEB "Flag: A equals B" / F=(A==B)? 0xF0
15 AGB "Flag: A greater than B" / F=(A>B)? 0xF0

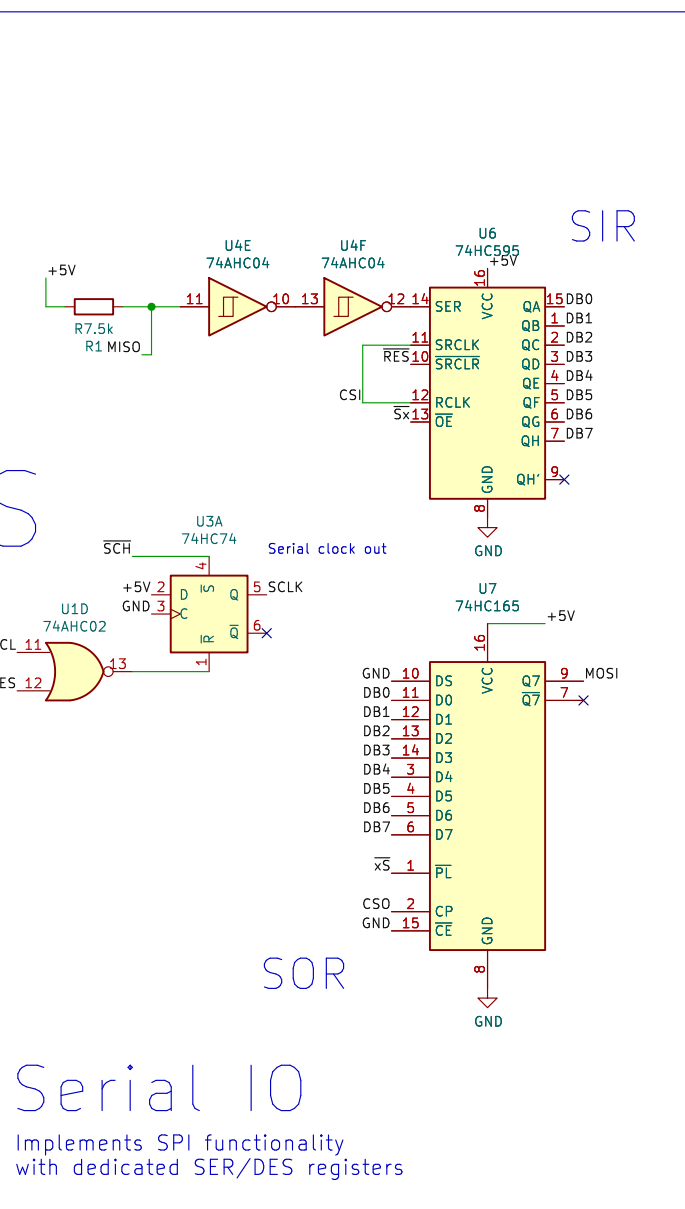
B

Storage

Memory M

High

(Gort = GLOBAL or LOCAL, including GETPUT)



Device Enable

Ref. implementation connects two independent 4-bit groups (high/low) to 4-bit encoders (for simultaneous latch enable / output enable of two separate devices)

SIR

E

PIR

P

POR

Parallel IO

Implement an 8-bit parallel tri-state interface bus with dedicated in/out ports

Glue Logic

I (INNER) Loop Register

L(ocal) page index Stack Pointer

FR0-7 Bus Frame/Record

Spare Units

C(ode) page index

D(ata) page index