Sonne-8 Microcontroller
Reference Schematics
Rev. Myth/LOX
"VLSI" Footprint
Clock Phases
Power
Caps
I (INNER Loop Register)
R-Fix
Instruction Decoder
Branching
Control Tree
Scrounger
Inverters
Pair DST Decoder
Preselect decoders
Instruction-Word Latch
Pair SRC Decoder
SYS decoder
TRAP decoder Immediate calls
(PC Program Counter)
R(esult) Register
ALU
Zero detection
O (OFFSET) Operand Register
ALU opcode
ALU Instructions
0 CLR ("Clear" / R:=0)
1 IDO ("Identity O" / R:=Old)
2 OCR ("Ones Complement R" / R:=~R)
3 OCO ("Ones Complement O" / R:=~O)
4 SLR ("Shift left New" / R:=R<<1)
5 SLO ("Shift left Old" / R:=O<<1)
6 SRR ("Shift right R" / R:=R>>1)
7 SRO ("Shift right O" / R:=O>>1)
8 AND (R:=R&O)
9 IOR (R:=R|O)
10 EOR (R:=R^O)
11 ADD (Add" / R:=R+O, bits 0-7)
12 CAR ("Carry Bit" / R:= Carry, 9th bit of R+O) 00h or 01h
13 RLO ("Flag: R less than O" / R:= (R<O)? 0xFF:0
14 REO ("Flag: R equals O" / R:= (R==O)? 0xFF:0
15 RGO ("Flag: R greater than O" / R:= (R>O)? 0xFF:0
D (DATA) Page index
GETPUT Decoder
Opcode Type Decoder
8:3 Priority Encoder CD4532
Instruction byte:
all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_FIX 00001 xxx b2:extended sign bit b1-0 LSB
OPC_ALU 0001x xxx See table @ ALU
OPC_TRAP 001xx xxx b4:MSB b3-0:LSB (remaining bits set 1)
OPC_ROID 01xxx xxx b0-2 OFFS b3:GET/PUT B4-5:REG(ROID)
OPC_PAIR 1xxxx xxx DEST SRC
PHA0: Setup PC on address bus
PHA1: Latch opcode into IB0-7, predecoded
PHA2: Decoded, setup source byte on DB or other action
PHA3: Latch source into target or other action
CLOSE: Cleanup
C (CODE) Page index
L (LOCAL) Page index (Stack Pointer)
Automatic call stack
CALL: Enter stack frame
RET: Resume previous frame
G (GLOBAL)
Low
Memory M
Storage
16K
S
SIR
SOR
Serial IO
Implements SPI functionality with dedicated SER/DES registers
E
Device Enable
ACTIVE HIGH ENABLE
ACTIVE LOW ENABLE
P
PIR
POR
Parallel IO
Implement an 8-bit parallel tri-state interface bus with dedicated In/Out ports
Glue Logic
Spare Units
Rev. Step LOX ("Frozen")
Project homepage: https://github.com/Dosflange/Myth
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Sheet: /
File: myth.kicad_sch
Title: Sonne-8 Micro-Controller
Size: A0
Date: 2024-09-04
Rev: Myth
KiCad E.D.A. 8.0.4
Id: 1/1