CprE 381 – Computer Organization and Assembly-Level Programming

Lab-01 Report

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Section / Lab Time 8 | 10:00 – 11:50 Wednesday

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-01 instructions for the context of the following questions.

a. [Part 1 (b)] Reference the circuit diagram at the end of this document (some parts simplified). There are 33 labeled areas in the diagram. For 15 of these labels, specify where (VHDL file and line number) these values are located – some will be found in more than one place. Also attempt to explain the functionality of each label as it occurs in the code.

b. [Part 1 (h)] In your report, provide a brief explanation of how the timing waveform corresponds to your understanding of the adder design.

c. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	0.25	0
Pencil/paper design	0	0
VHDL design	0.5	1
Assembly coding	0	0
Simulation	0.25	.1
Debugging	0	0
Report writing	0.5	0
Other:	0	0
Total	1.5	1.1

ii. If you could change one thing about the lab experience, what would it be? Why?

Make it clearer that the giga conversion was already applied to c in the equation E = mc^2, where c was supposed to be 9487 instead of 3 * 10^8. It would have saved me probably 30 minutes of being confused about syntax.

iii. What was the most interesting part of the lab?

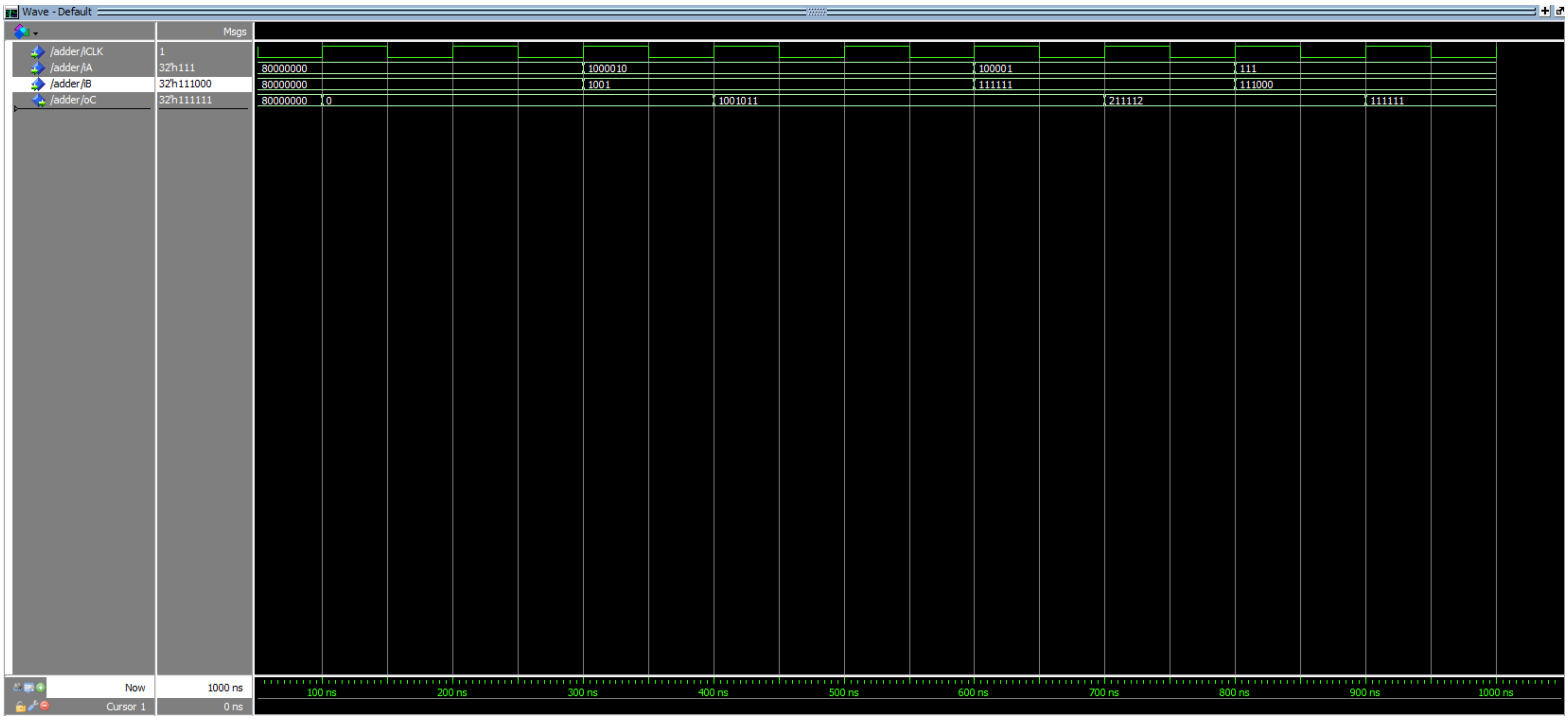
Learning the syntax of VHDL and seeing how it is composed compared to the other languages I have already learned.

Part 1 (b)

- cA is defined as a constant integer within quadratic.vhd. More specifically, it is defined to be five on line 49, and is designated to be an input to g_Mult1 called iA on line 68.
- iX is defined to be an integer input within quadratic.vhd on line 25. It is designated to be an input to the three multipliers: input to g_Mult1 iB on line 69, input to g_Mult2 iB on line 75, and input to g_Mult3 iB on line 84.
- cB is another constant within quadratic.vhd, except now it is wired to g_Mult2. It is defined to be the integer 23 on line 50, and is used as an input to g_Mult2's iA.
- cC within quadratic.vdh is defined to be an integer on line 51. It is defined to be two, and it is designated to be used as an input to g_Add1's iB on line 90.
- oC of g_Mult1 is defined to be connected to sVALUE_Ax on line 70 of Quadratic.vhd. oC is defined to be an integer output on line 31 of Multiplier.vhd.
- oC of g_Mult2 is defined to be connected to sVALUE_Bx on line 76 of Quadratic.vhd. oC is defined to be an integer output on line 31 of Multiplier.vhd.
- oC of g_Mult3 is defined to be connected to sVALUE_Axx on line 85 of Quadratic.vhd. oC is defined to be an integer output on line 31 of Multiplier.vhd.
- oC of g_Add1 is defined to be connected to sVALUE_Bxpc on line 91 of Quadratic.vhd. oC is defined to be an integer output on line 31 of Adder.vhd.
- oC of g_Add2 is defined to be connected to oY on line 100 of Quadratic.vhd. oC is defined to be an integer output on line 31 Adder.vhd.
- sVALUE_Ax is defined to be an integer signal within Quadratic.vhd on line 54. It is defined as the output oC of g_Mult1 on line 70 and the input iA of g_Mult3 on line 83.

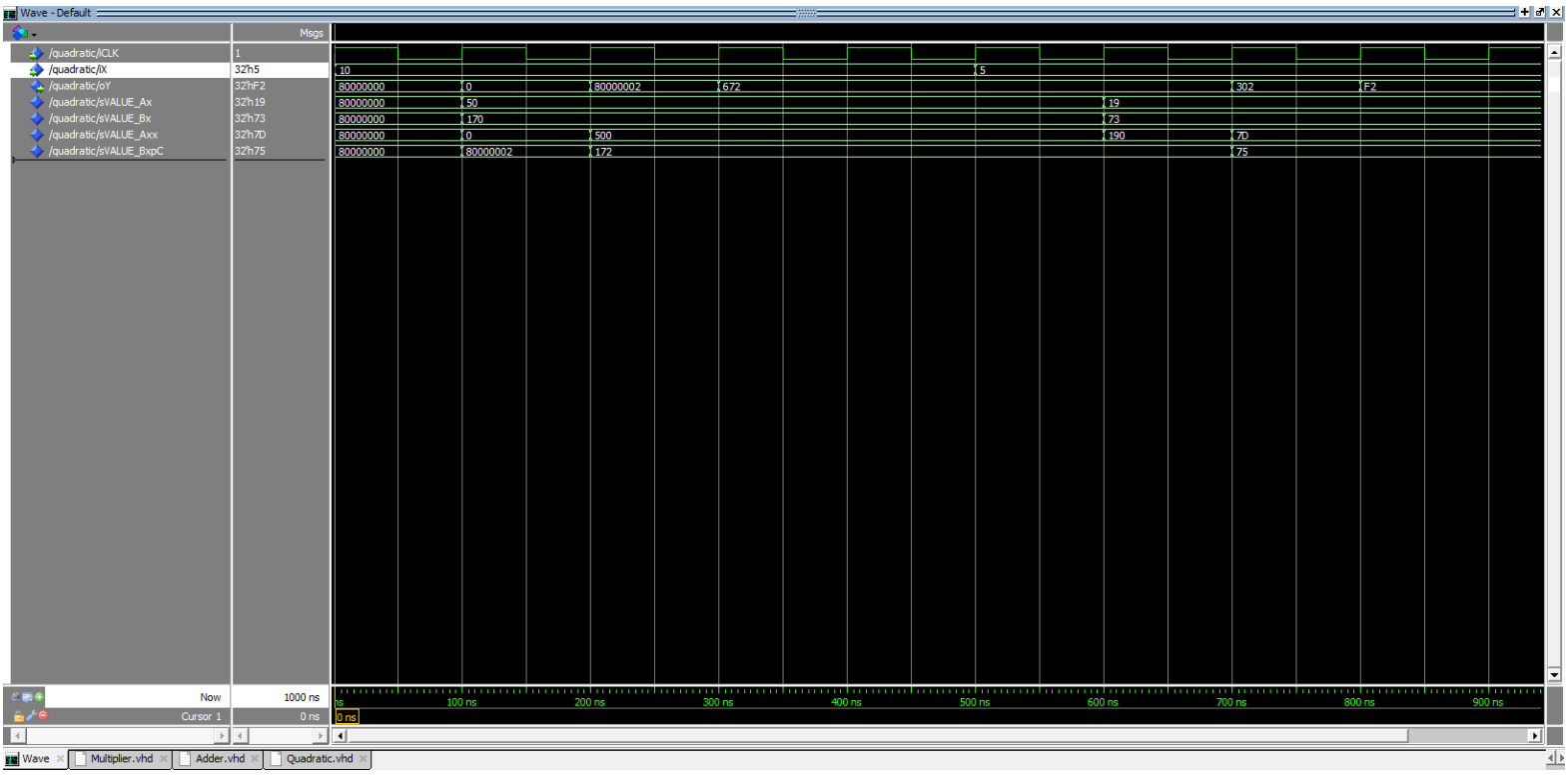
- sVALUE_Bx is defined to be an integer signal within Quadratic.vhd on line 54. It is defined as the output oC of g_Mult2 on line 76 and the input iA to g_Add1 on line 89.
- sVALUE_Axx is defined to be an integer signal within Quadratic.vhd on line 56. It is defined as the output oC of g_Mult3 on line 85 and the input iA of g_Add2 on line 98.
- sVALUE_Bxpc is defined to be an integer signal within Quadratic.vhd on line 58. It is defined to be the output oc of g_Add1 on line 91 and input iB of g_Add2 on line 99.
- oY is defined to be an output integer on line 26 of Quadratic.vhd. It is connected to the output of g_Add2 oC on line 100.
- iA within g_Mult1 is defined to be an input integer on line 31 of Multiplier.vhd. It is connected to cA within Quadratic.vhd on line 68.

Part 1 (h)

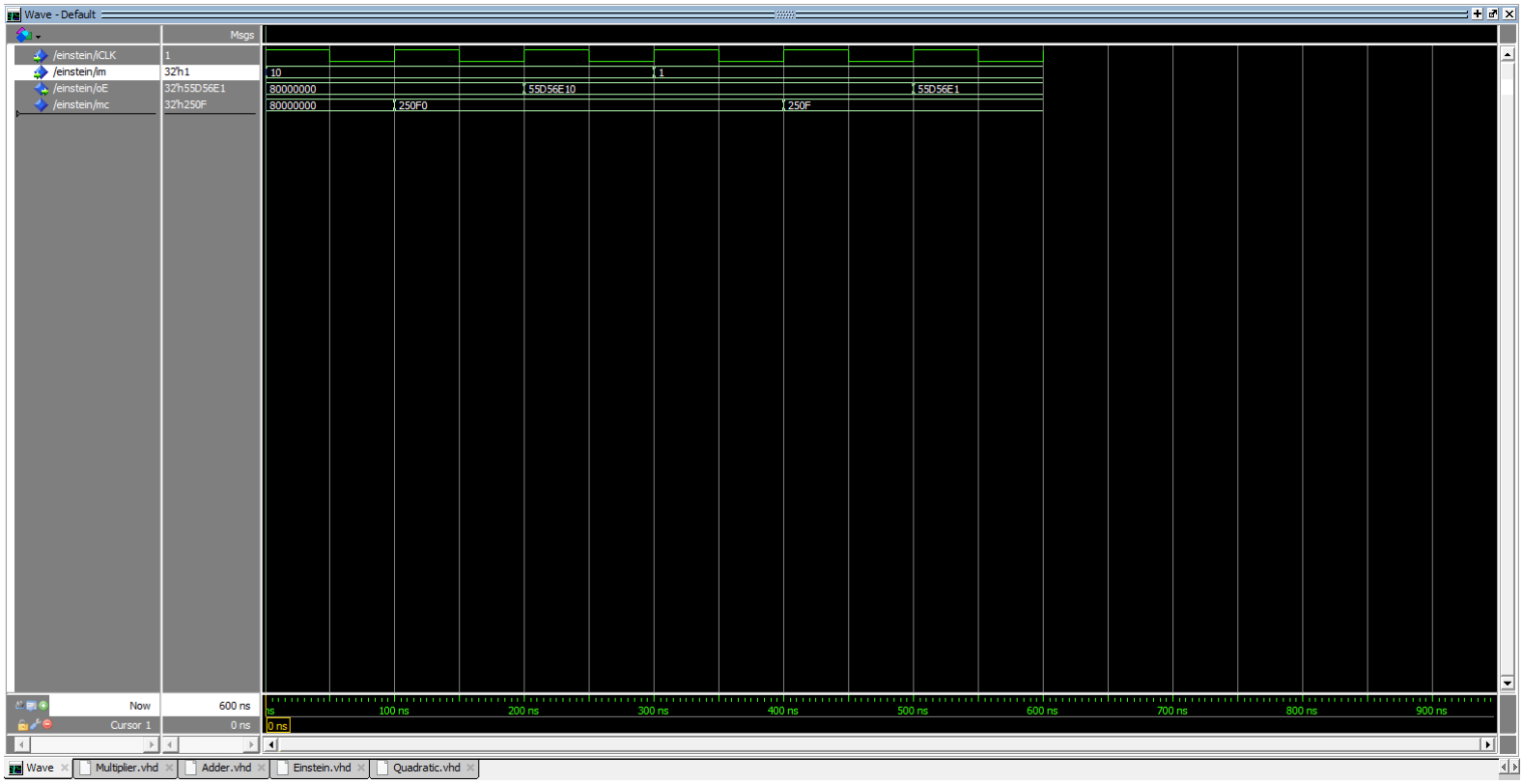


The timing waveform corresponds to the adder's functions as when there are values loaded into the adder when the clock hits a rising edge, it will calculate the sum of the two loaded values. The adder first processes that there have been new values forced. They are then being added by the adder when the "run for 100" task results in the next positive clock edge for the adder, which ends up being 300 ns later in this case.

Part 2



Part 3


Wave - Default
Msgs
/einstein/iCLK
/einstein/im
/einstein/oE
/einstein/mc
1
32'h1
32'h55D56E1
32'h250F
10
1
80000000
55D56E10
55D56E1
80000000
250F0
250F
Now
600 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Wave
Multiplier.vhd
Adder.vhd
Einstein.vhd
Quadratic.vhd