01_Description

ZYNQ-ICU

REV	DESCRIPTION	DATE
V1.0	Creat	16/03/22
V1.1	Modify	16/05/28
V1.2	Modify	

Change Logs

V1.0

1)Creat

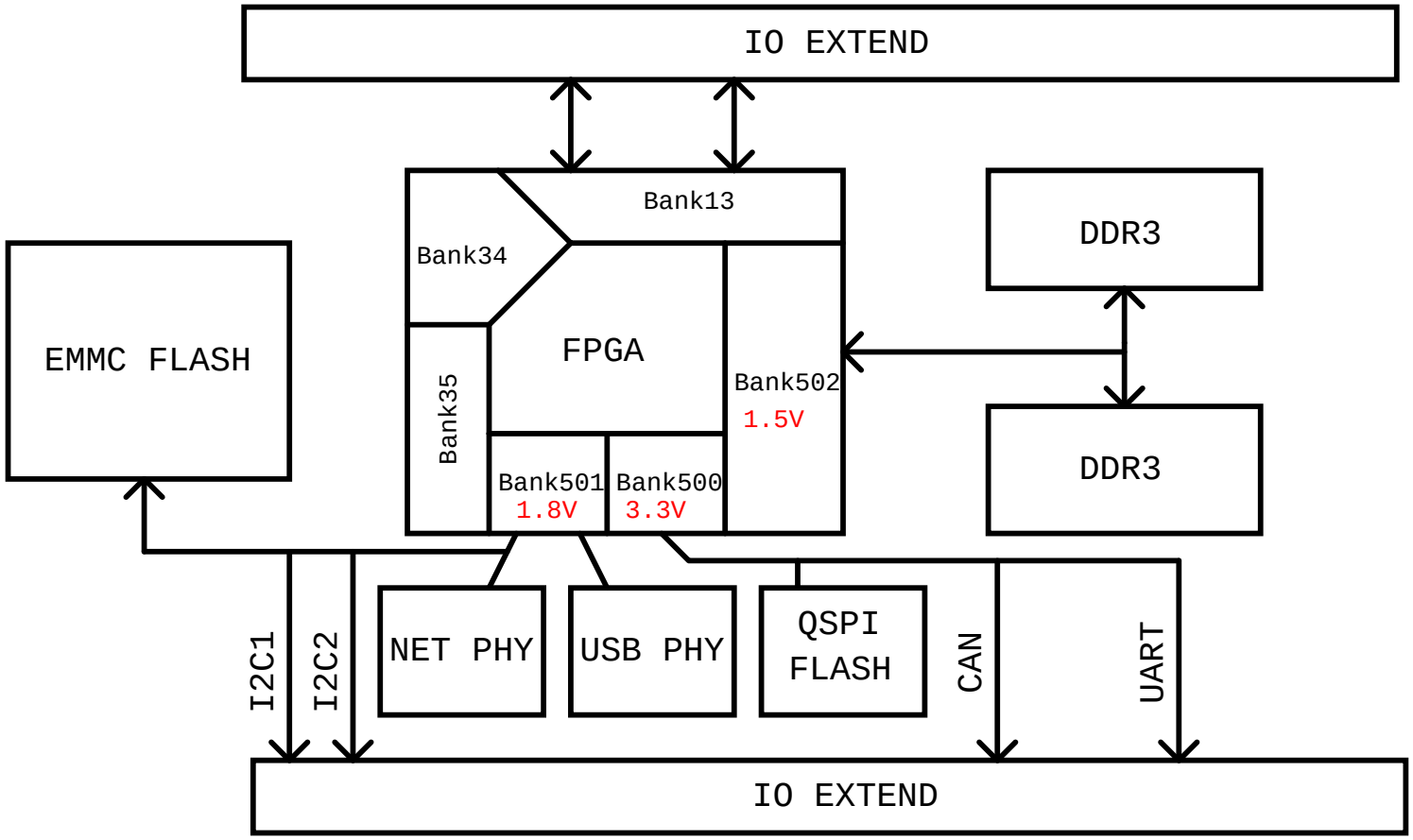
V1.1

1)Modified

V1.2

SMARTGIANT 思林杰科技	Project Name	SE2670
	Title	<Titl
Custormer	Drawn by	Leilei W
Version A	Checkd by	Wenbi
Sheet 1 of 1	Approved by	
Date: Monday, February 27, 2017	Doc Number	

02-Block Diagram



Customer	Drawn by	Leilei We
Version A	Checked by	Wenbin
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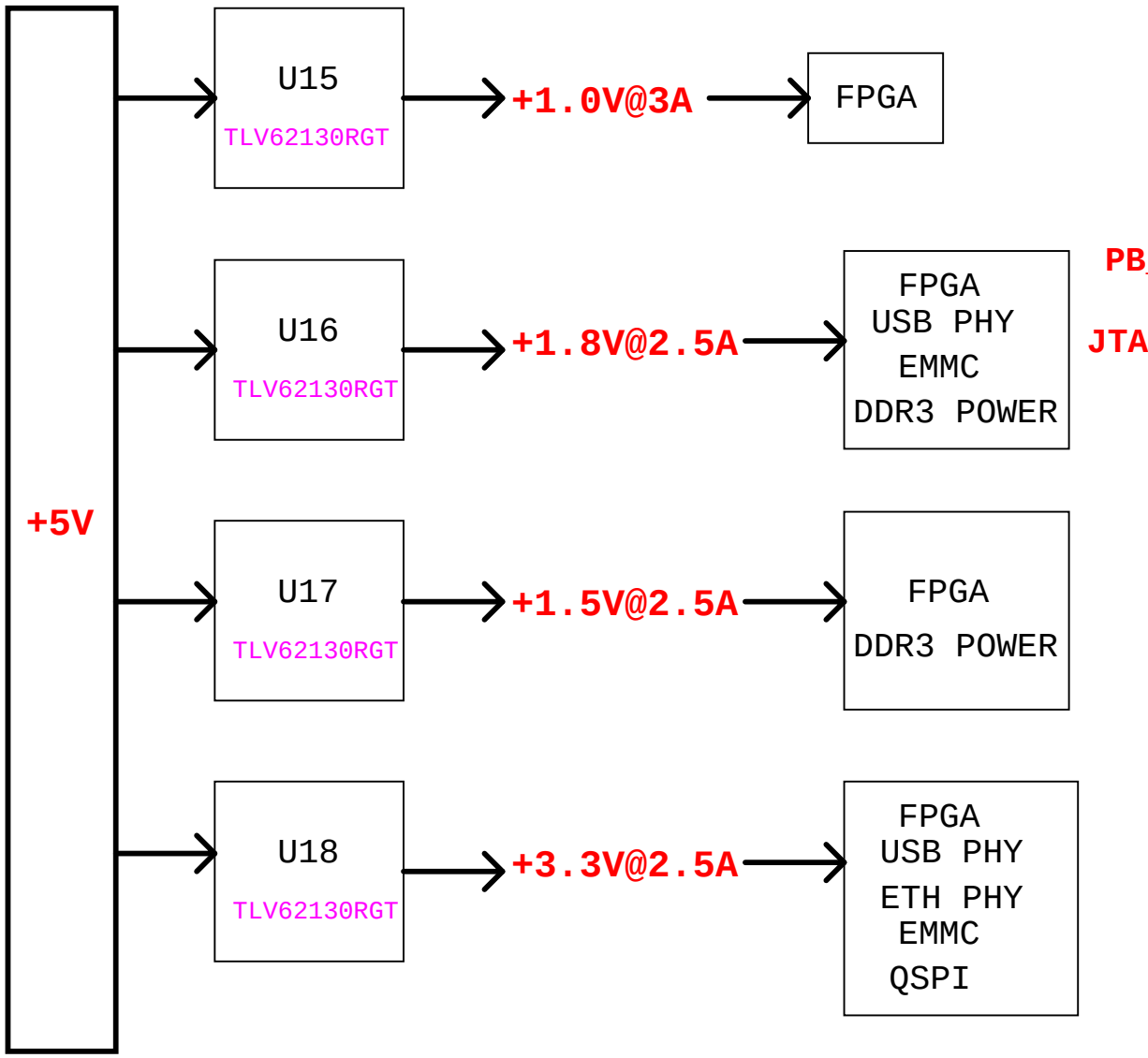
03-Power Distribution

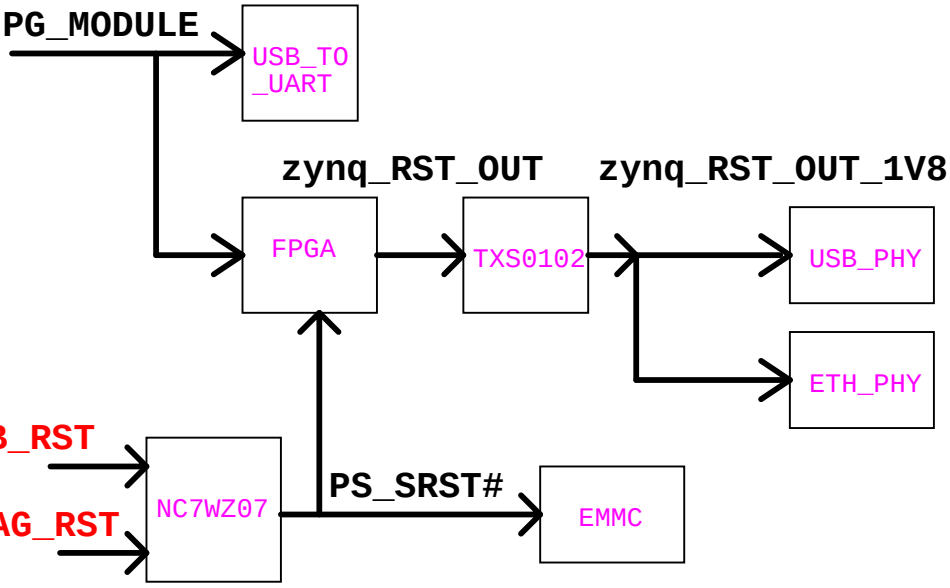
Power up sequence

+1.0V@3A → +1.8V@2.5A → +1.5V@2.5A → +3.3V@2.5A

Power Tree



Reset topology



SMARTGIANT 思林杰科技	Project Name
	Title
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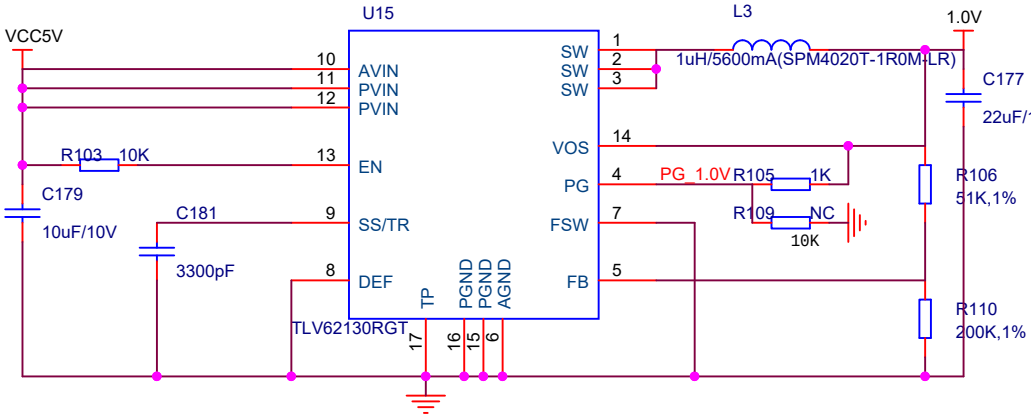
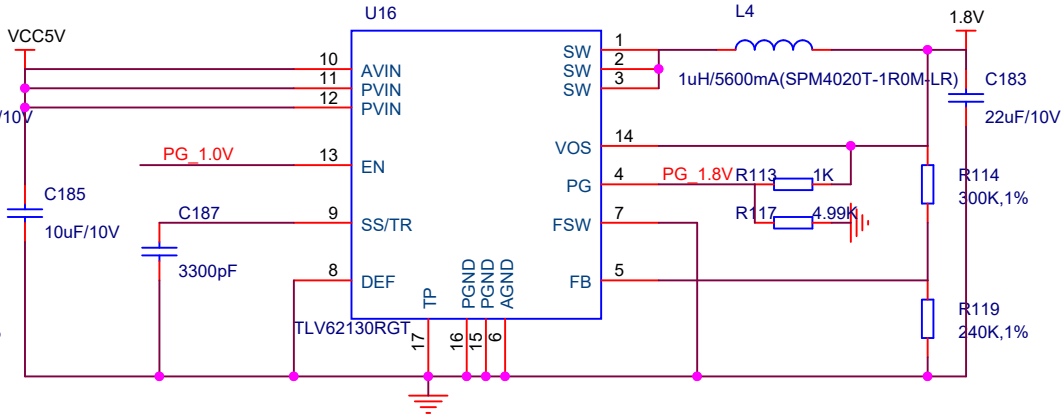
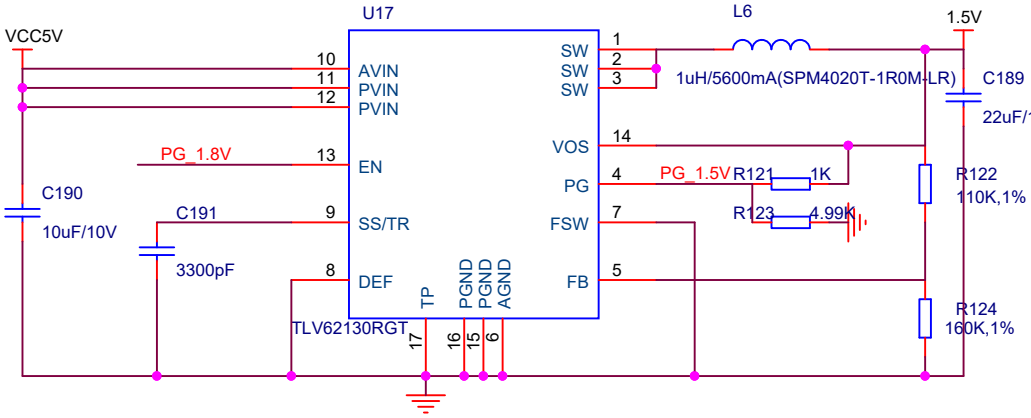
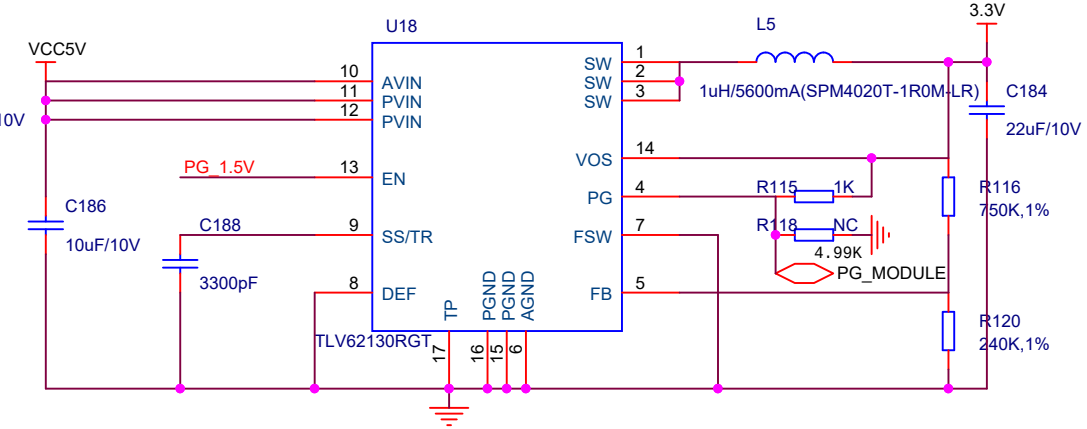
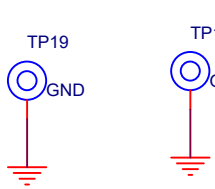
04-Power

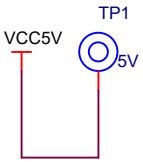


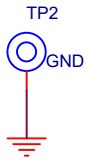


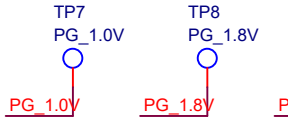


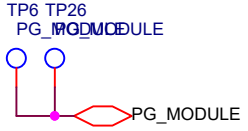


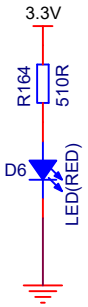












Css=Tss*2.5uA/1.25V

Vout=(Rup+Rdown)/Rdown*0.8V

Ifb>=2uA,Rdown<=400k

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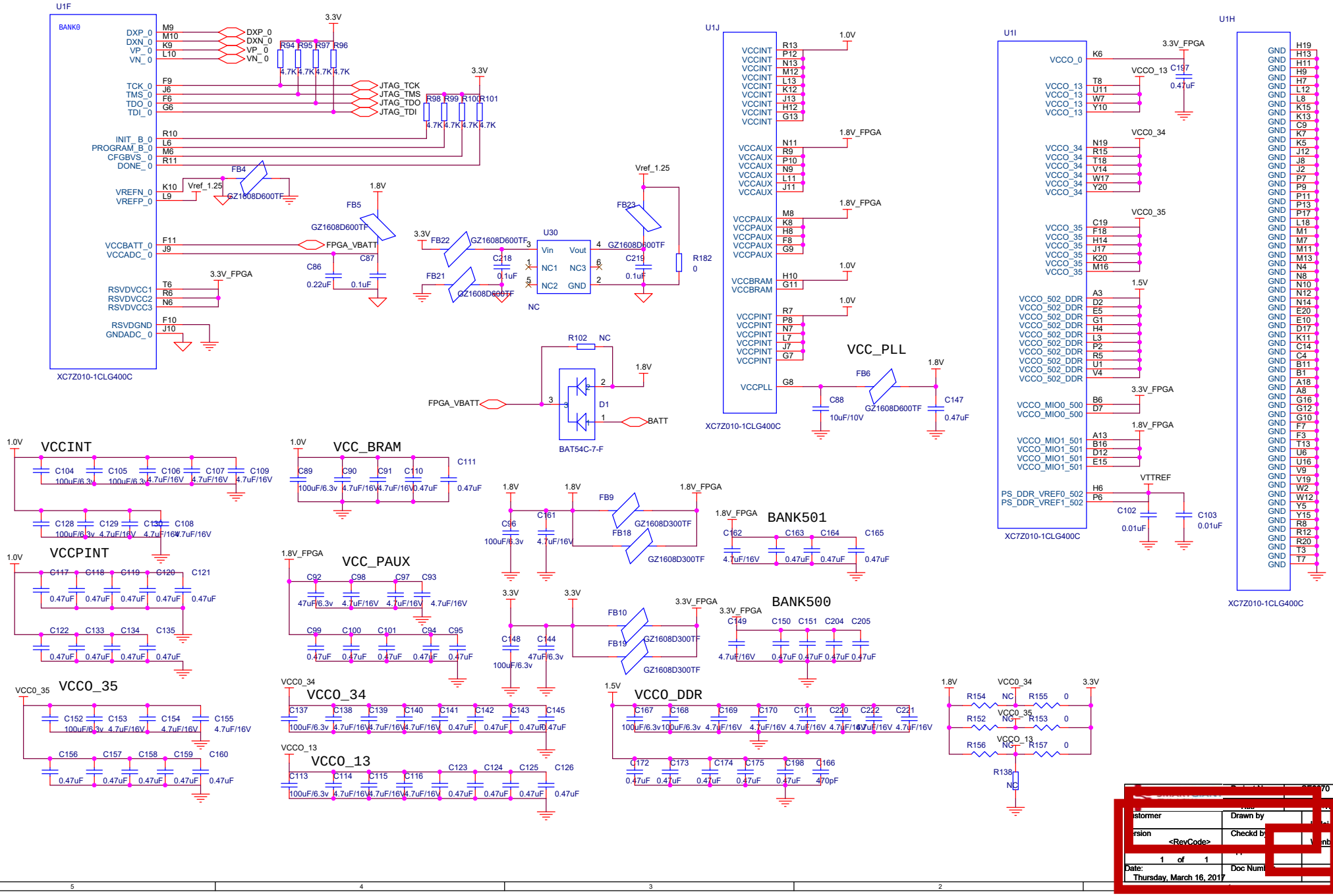
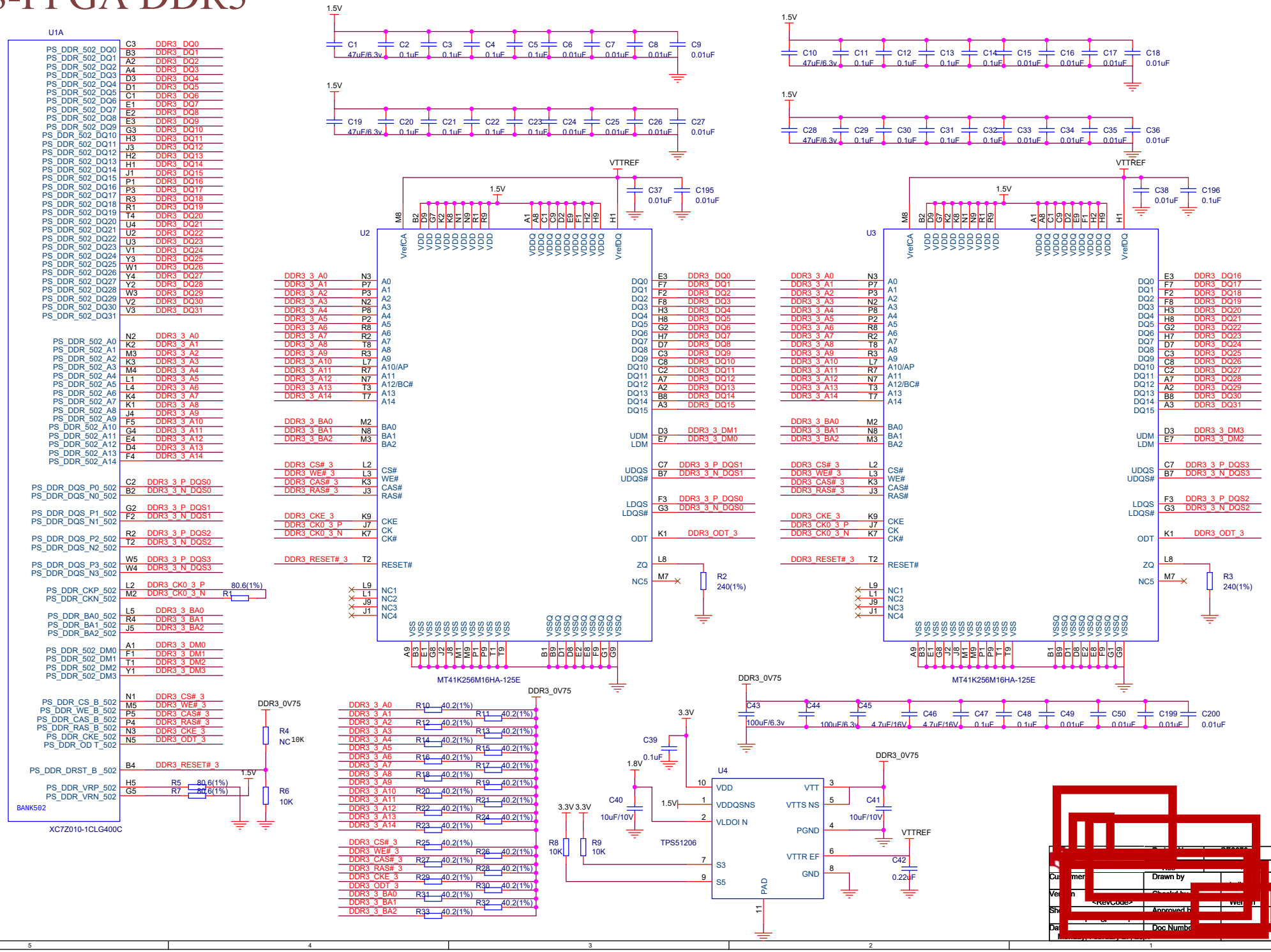
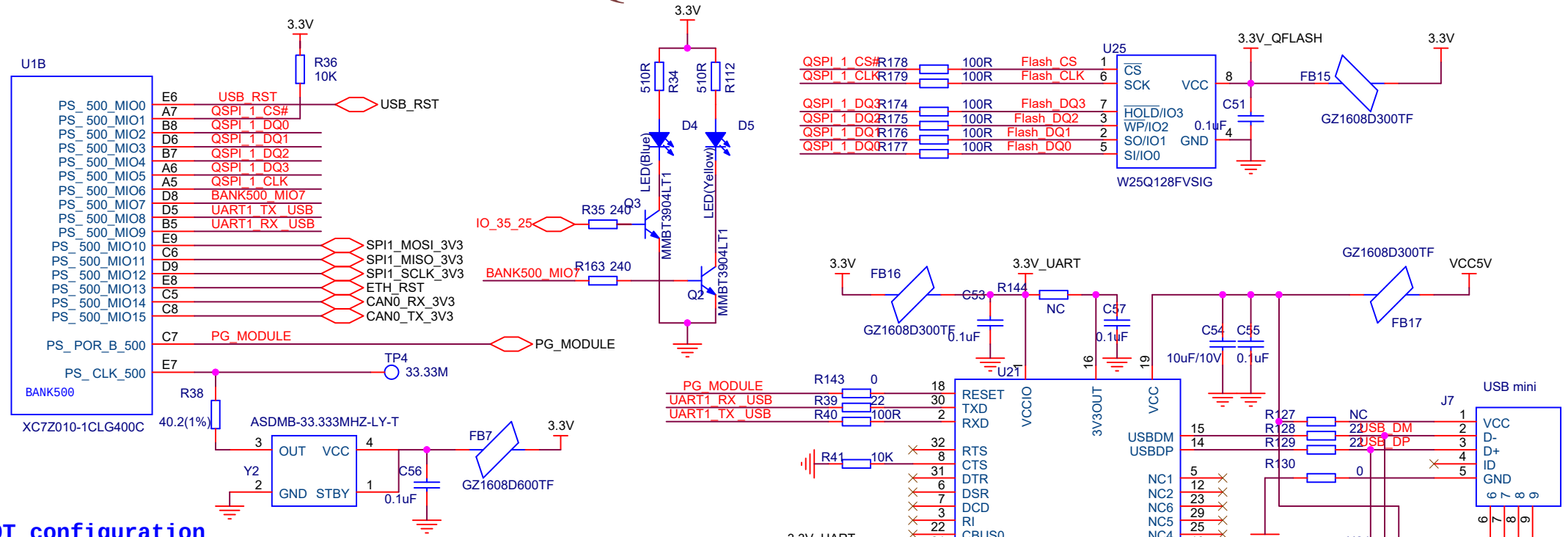
05-FPGA Power



08-FPGA DDR3

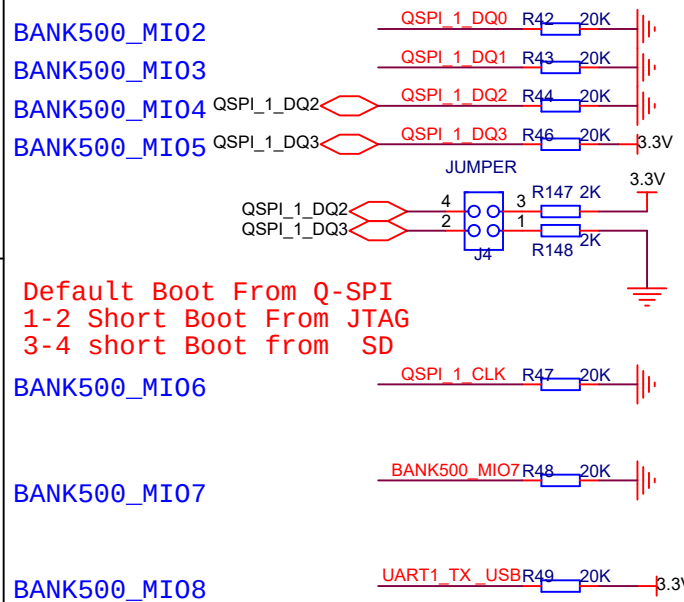

U1A
PS_DDR_502_DQ0
PS_DDR_502_DQ1
PS_DDR_502_DQ2
PS_DDR_502_DQ3
PS_DDR_502_DQ4
PS_DDR_502_DQ5
PS_DDR_502_DQ6
PS_DDR_502_DQ7
PS_DDR_502_DQ8
PS_DDR_502_DQ9
PS_DDR_502_DQ10
PS_DDR_502_DQ11
PS_DDR_502_DQ12
PS_DDR_502_DQ13
PS_DDR_502_DQ14
PS_DDR_502_DQ15
PS_DDR_502_DQ16
PS_DDR_502_DQ17
PS_DDR_502_DQ18
PS_DDR_502_DQ19
PS_DDR_502_DQ20
PS_DDR_502_DQ21
PS_DDR_502_DQ22
PS_DDR_502_DQ23
PS_DDR_502_DQ24
PS_DDR_502_DQ25
PS_DDR_502_DQ26
PS_DDR_502_DQ27
PS_DDR_502_DQ28
PS_DDR_502_DQ29
PS_DDR_502_DQ30
PS_DDR_502_DQ31
DDR3_DQ0
DDR3_DQ1
DDR3_DQ2
DDR3_DQ3
DDR3_DQ4
DDR3_DQ5
DDR3_DQ6
DDR3_DQ7
DDR3_DQ8
DDR3_DQ9
DDR3_DQ10
DDR3_DQ11
DDR3_DQ12
DDR3_DQ13
DDR3_DQ14
DDR3_DQ15
DDR3_DQ16
DDR3_DQ17
DDR3_DQ18
DDR3_DQ19
DDR3_DQ20
DDR3_DQ21
DDR3_DQ22
DDR3_DQ23
DDR3_DQ24
DDR3_DQ25
DDR3_DQ26
DDR3_DQ27
DDR3_DQ28
DDR3_DQ29
DDR3_DQ30
DDR3_DQ31
PS_DDR_502_A0
PS_DDR_502_A1
PS_DDR_502_A2
PS_DDR_502_A3
PS_DDR_502_A4
PS_DDR_502_A5
PS_DDR_502_A6
PS_DDR_502_A7
PS_DDR_502_A8
PS_DDR_502_A9
PS_DDR_502_A10
PS_DDR_502_A11
PS_DDR_502_A12
PS_DDR_502_A13
PS_DDR_502_A14
DDR3_A0
DDR3_A1
DDR3_A2
DDR3_A3
DDR3_A4
DDR3_A5
DDR3_A6
DDR3_A7
DDR3_A8
DDR3_A9
DDR3_A10
DDR3_A11
DDR3_A12
DDR3_A13
DDR3_A14
PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502
DDR3_P_DQS0
DDR3_N_DQS0
DDR3_P_DQS1
DDR3_N_DQS1
DDR3_P_DQS2
DDR3_N_DQS2
DDR3_P_DQS3
DDR3_N_DQS3
PS_DDR_CKP_502
PS_DDR_CKN_502
DDR3_CK0_3_P
DDR3_CK0_3_N
80.6(1%)
R1
PS_DDR_BA0_502
PS_DDR_BA1_502
PS_DDR_BA2_502
DDR3_BA0
DDR3_BA1
DDR3_BA2
PS_DDR_502_DM0
PS_DDR_502_DM1
PS_DDR_502_DM2
PS_DDR_502_DM3
DDR3_DM0
DDR3_DM1
DDR3_DM2
DDR3_DM3
PS_DDR_CS_B_502
PS_DDR_WE_B_502
PS_DDR_CAS_B_502
PS_DDR_RAS_B_502
PS_DDR_CKE_502
PS_DDR_OD T_502
DDR3_CS#_3
DDR3_WE#_3
DDR3_CAS#_3
DDR3_RAS#_3
DDR3_CKE_3
DDR3_ODT_3
PS_DDR_DRST_B_502
DDR3_RESET#_3
PS_DDR_VRP_502
PS_DDR_VRN_502
R5 80.6(1%)
R7 80.6(1%)
1.5V
DDR3_0V75
R4 NC 10K
R6 10K
BANK502
XC7Z010-1CLG400C
1.5V
C1 47uF/6.3v
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.01uF
C7 0.01uF
C8 0.01uF
C9 0.01uF
C19 47uF/6.3v
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.01uF
C25 0.01uF
C26 0.01uF
C27 0.01uF
VTTREF
C37 0.01uF
C195 0.01uF
U2
VrefCA
VrefDQ
VDD
VDDQ
VSS
VSSQ
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC#
A13
A14
BA0
BA1
BA2
CS#
WE#
CAS#
RAS#
CKE
CK
CK#
ODT
RESET#
ZQ
NC1
NC2
NC3
NC4
NC5
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
UDM
LDM
UDQS
UDQS#
LDQS
LDQS#
R2 240(1%)
MT41K256M16HA-125E
C10 47uF/6.3v
C11 0.1uF
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.01uF
C16 0.01uF
C17 0.01uF
C18 0.01uF
C28 47uF/6.3v
C29 0.1uF
C30 0.1uF
C31 0.1uF
C32 0.1uF
C33 0.01uF
C34 0.01uF
C35 0.01uF
C36 0.01uF
C38 0.01uF
C196 0.1uF
U3
R3 240(1%)
MT41K256M16HA-125E
DDR3_0V75
C43 100uF/6.3v
C44 100uF/6.3v
C45 4.7uF/16V
C46 4.7uF/16V
C47 0.1uF
C48 0.1uF
C49 0.01uF
C50 0.01uF
C199 0.01uF
C200 0.01uF
3.3V
C39 0.1uF
1.8V
C40 10uF/10V
3.3V 3.3V
R8 10K
R9 10K
U4
VDD
VDDQSNS
VLDOI N
S3
S5
PAD
VTT
VTTS NS
PGND
VTTR EF
GND
TPS51206
C41 10uF/10V
C42 0.22uF
DDR3_A0 R10 40.2(1%)
DDR3_A1 R11 40.2(1%)
DDR3_A2 R12 40.2(1%)
DDR3_A3 R13 40.2(1%)
DDR3_A4 R14 40.2(1%)
DDR3_A5 R15 40.2(1%)
DDR3_A6 R16 40.2(1%)
DDR3_A7 R17 40.2(1%)
DDR3_A8 R18 40.2(1%)
DDR3_A9 R19 40.2(1%)
DDR3_A10 R20 40.2(1%)
DDR3_A11 R21 40.2(1%)
DDR3_A12 R22 40.2(1%)
DDR3_A13 R24 40.2(1%)
DDR3_A14 R23 40.2(1%)
DDR3_CS#_3 R25 40.2(1%)
DDR3_WE#_3 R26 40.2(1%)
DDR3_CAS#_3 R27 40.2(1%)
DDR3_RAS#_3 R28 40.2(1%)
DDR3_CKE_3 R29 40.2(1%)
DDR3_ODT_3 R30 40.2(1%)
DDR3_BA0 R31 40.2(1%)
DDR3_BA1 R32 40.2(1%)
DDR3_BA2 R33 40.2(1%)
Drawn by
Approved
Doc Numbe

06-FFPGA BOOT&QSPI



BOOT configuration

BOOT from Q-flash; PLL enable;bank 500 3.3V;bank 501 1.8v



	MIO[5]	MIO[4]	MIO[3]	MIO[2]
JTAG	0	0	0	0
Q-SPI	1	0	0	0
SD	1	1	0	0

MIO[6] 0 PLL Enable

1 PLL Bypassed

MIO[7] 0 Bank500 2.5V,3.3V

1 Bank500 1.8V

MIO[8] 0 Bank501 2.5V,3.3V

1 Bank501 1.8V

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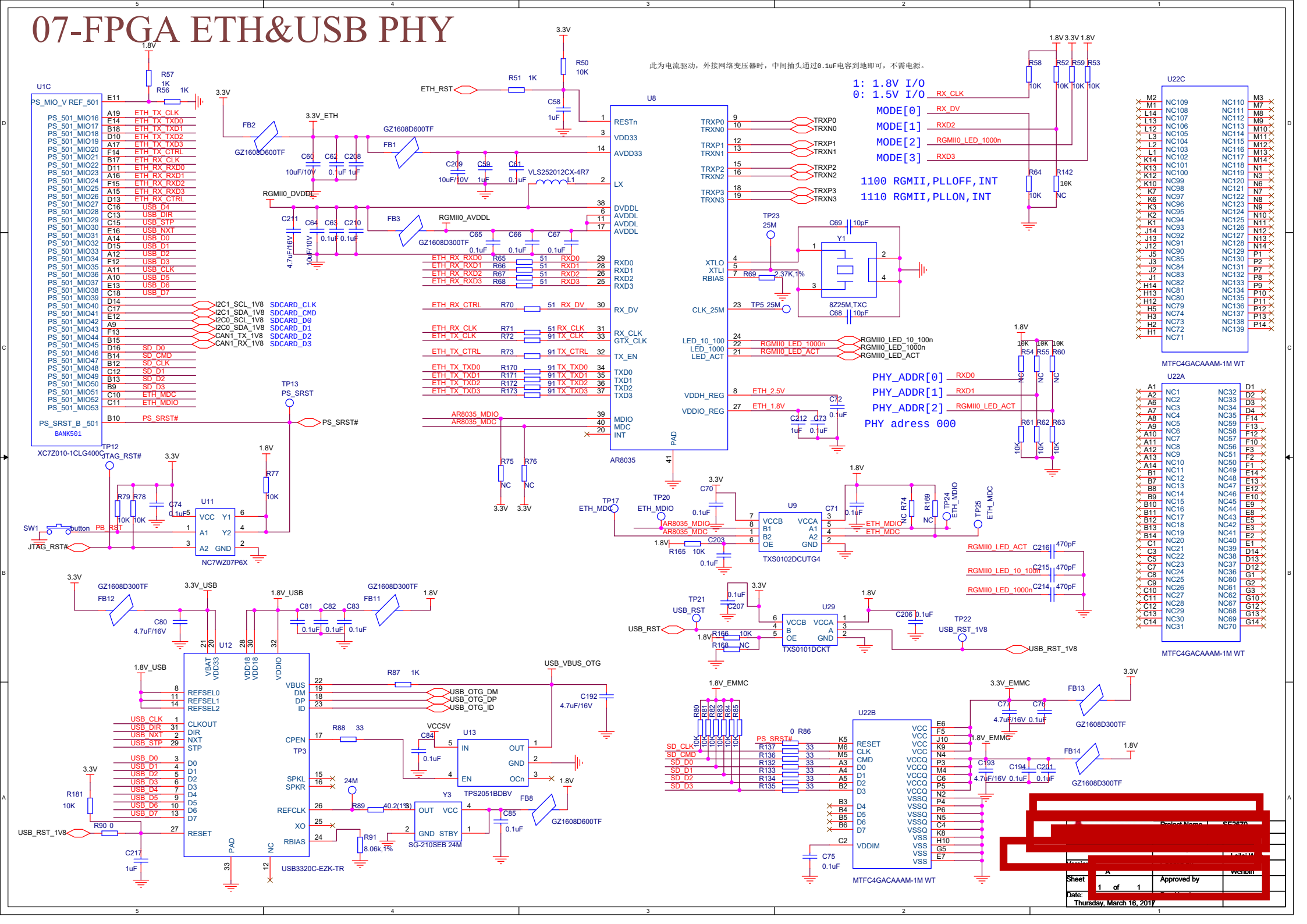
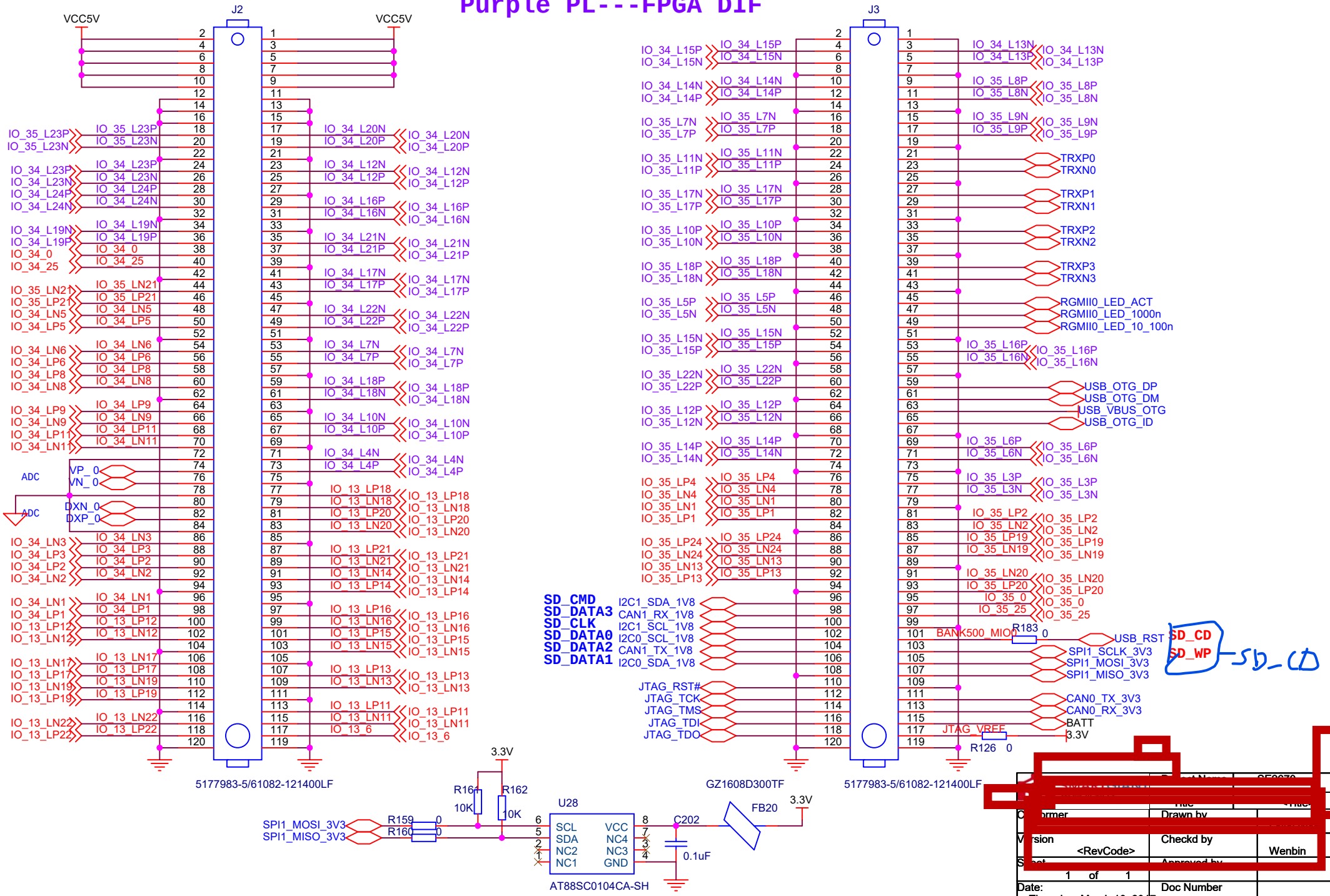
07-FPGA ETH&USB PHY



10-CONNECTOR

BLue PS---ARM
RED PL---FPGA SIG
Purple PL---FPGA DIF



	Drawn by	
Version <RevCode>	Checkd by	Wenbin
Sheet 1 of 1	Approved by	
Date: Thursday, March 16, 2017	Doc Number	

09-Conenctor